Processing System 7 v5.5

LogiCORE IP Product Guide

Vivado Design Suite

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XILINX
ALL PROGRAMMABLE™

Table of Contents

Appendix C: Additional Resources and Legal Notices

Introduction

The Xilinx LogiCORE™ IP Processing System 7 core is the software interface around the Zynq®-7000 platform Processing System. The Zynq-7000 family consists of an system-on-chip (SoC) style integrated processing system (PS) and a Programmable Logic (PL) unit, providing an extensible and flexible SoC solution on a single die.

The Processing System 7 core acts as a logic connection between the PS and the PL while assisting you to integrate custom and embedded IP cores with the processing system using the Vivado® Design Suite.

Features

- Enable/Disable I/O Peripherals (IOP)
- Enable/Disable AXI I/O ports
- Multiplexed I/O (MIO) Configuration
- Extended Multiple Use I/Os (EMIO)
- ACP Transaction checker (ATC)
- Interconnect logic for Vivado Design Suite IP – PS interface
- PL Clocks and Interrupts

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Zynq-7000
Supported User Interfaces	N/A
Resources	Not Applicable
Provided with Core	
Design Files	Verilog
Example Design	Not Provided
Test Bench	Not Provided
Constraints File	Not Provided
Simulation Model	Not Provided
Supported S/W Driver	N/A
Tested Design Flows(2)	
Design Entry	Vivado Design Suite
Simulation	For the list of supported simulators, see the Xilinx Design Tools: Release Notes Guide
Synthesis	Vivado Synthesis
Support	
Provided by Xilinx at the Xilinx Support web page	

Notes:

1. For a complete list of supported devices, see Vivado IP catalog.
2. For the supported versions of the tools, see the Xilinx Design Tools: Release Notes Guide.

Overview

The Zynq®-7000 family is based on the Xilinx All Programmable system-on-chip (AP SoC) architecture. These products integrate a feature-rich dual-core ARM® Cortex™-A9 MPCore™-based processing system (PS) and Xilinx programmable logic (PL) in a single device, built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, and high -k metal gate (HKMG) process technology. The ARM Cortex-A9 MPCore CPUs are the heart of the PS which also includes on-chip memory, external memory interfaces, and a rich set of I/O peripherals.

The Processing System 7 core is the software interface around the Zynq-7000 platform processing system. The Zynq-7000 family consists of an SoC style integrated PS and a PL unit, providing an extensible and flexible SoC solution on a single die. The Processing System 7 core acts as a logic connection between the PS and the PL while assisting you to integrate customized and embedded IP cores with the processing system using the Vivado® IP integrator.

For a detailed overview of the core, see Chapter 2, Product Specification.

Feature Summary

- Enable/Disable I/O Peripherals (IOP)
- Enable/Disable AXI I/O ports
- MIO Configuration
- Extended Multiple Use I/Os (EMIO)
- Accelerator coherency port (ACP) Transaction checker (ATC)
- Interconnect logic for Vivado Design Suite IP – PS interface
- PL Clocks and Interrupts
- PS internal clocking
- Generate PS configuration register

Unsupported Features

The Processing System 7 cores provide Vivado Integrated Design Environment (IDE)-based configuration of the PS instance and its I/O. Due to the flexibility of the PS, only the most common features, I/O configurations, and peripheral settings are configured by this core. Additional register settings might be necessary by your own register accesses.

Licensing and Ordering Information

This Xilinx LogiCORE™ IP module is provided at no additional cost with the Xilinx Vivado Design Suite under the terms of the Xilinx End User License.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE IP modules and tools, contact your local Xilinx sales representative.

Product Specification

Functional Description

The Processing System 7 wrapper instantiates the processing system section of the Zynq®-7000 All Programmable SoC for the programmable logic and external board logic. The wrapper includes unaltered connectivity and, for some signals, some logic functions. For a description of the architecture of the processing system, see the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

The Processing System 7 core stitches the interface signals with the rest of the embedded system in the programmable logic. The interfaces between the processing system and programmable logic mainly consists of three main groups: the extended multiplexed I/O (EMIO), programmable logic I/O, and the AXI I/O groups. The Zynq-7000 device configuration wizard configures the Processing System 7 core. The Processing System 7 performs the functions described in the following subsections.

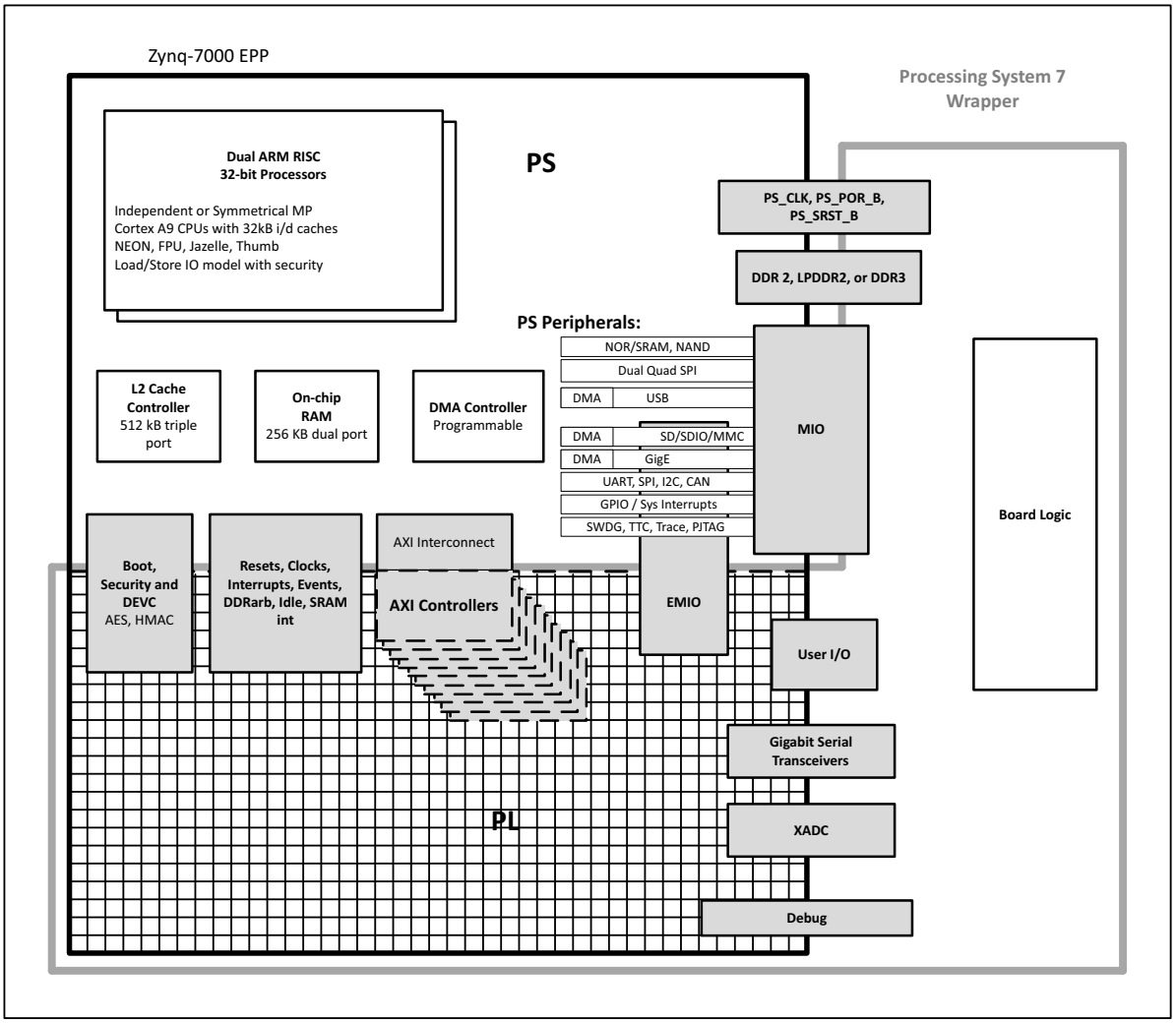

Figure 2-1: **Processing System 7 Wrapper**

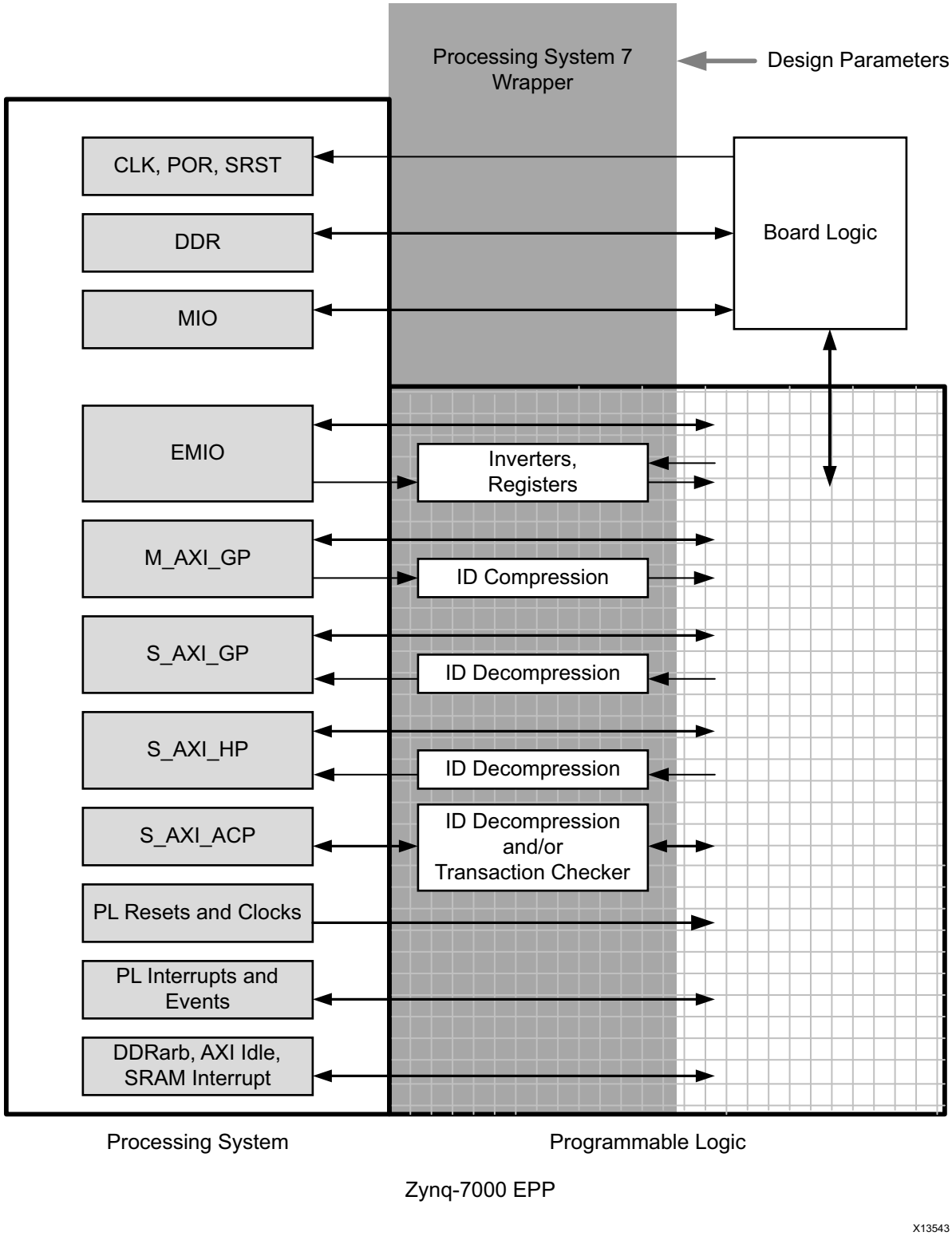

Figure 2-2: **Processing System 7 Wrapper Logic**

Connectivity

ddr, mio, por/clk/srst ports are unaltered.

- The width of general purpose I/O (GPIO) ports on EMIO are user selectable through the C_EMIO_GPIO_WIDTH parameter.
- ttc clocks and ttc waveo are made of individual signals instead of a [2:0] array.
- fclk are also made of individual signals instead of the array FCLKCLK (3:0).
- irqp2f are made of individual signals irq_p2f_dmac_abort, irq_p2f_dmac7, irq_p2f_dmac6, irq_p2f_dmac5, irq_p2f_dmac4, irq_p2f_dmac3, irq_p2f_dmac2, irq_p2f_dmac1, irq_p2f_dmac0, irq_p2f_smc, irq_p2f_qspi, irq_p2f_cti, irq_p2f_gpio, irq_p2f_usb0, irq_p2f_enet0, irq_p2f_enet_wake0, irq_p2f_sdio0, irq_p2f_i2c0, irq_p2f_spi0, irq_p2f_uart0, irq_p2f_can0, irq_p2f_usb1, irq_p2f_enet1, irq_p2f_enet_wake1, irq_p2f_sdio1, irq_p2f_i2c1, irq_p2f_spi1, irq_p2f_uart1, and irq_p2f_can1.
- spi or spi* sson are made of individual signals spi*_ss2_o, spi*_ss1_o, and spi*_ss_o.

AXI Interface IDs and Remap

ID compression and decompression is available for all the AXI interfaces to reduce the vector width of AXI ID signals in the programmable logic. ID compress/decompress logic for m_axi ports are dependent on the C_M_AXI_GP*_ENABLE_STATIC_REMAP parameter. If this parameter is 1, M_AXI THREAD ID widths are compressed to six bits; otherwise it is 12 bits. For the rest of the AXI slave, AXI interfaces ID width can be anything between 1 to the maximum ID width for a particular interface depending on user selection.

In general, enabling static remapping reduces resources, especially at a higher PL slave count versus a potential PL AXI maximum frequency impact. Remapping must be disabled when a PL master accesses PL slaves through the PS instead of through the PL directly.

ACP Transaction Checker

The accelerator coherency port (ACP) transaction checker (ATC) has the following limitation:

Write transactions with length = 3, size = 3, and write strobe ‡ 11111111 can cause the cache line in the CPUs to get corrupted.

The Processing System 7 core can be used to flag this limitation (cache lines being corrupted). If enabled, the Xilinx ACP adapter watches for transactions that could potentially corrupt the cache and generate an error response to the master that is requesting the write request. The write transaction is allowed to proceed to the ACP interface, so the possibility of cache corruption is *not* eliminated.

The master is notified of the possible problem in order to take the appropriate action. The ACP adapter can also generate an interrupt signal to the CPUs, which can be used by the software to detect such a situation.

The ACP Transaction checker detects if an ACP write transaction uses the correct type, size, and length qualifiers. It implements a command pipelined stage and stalls command flow if the check fails. The functions performed by ATC are:

- Checks if transaction is coherent.
- Checks transaction cache line address.
- Checks transaction burst type, size and length.
- Stores transaction information like ID, burst type, size, and length in FIFO.
- Throttles transaction and stalls commands if FIFO is full.
- Delays pipelined commands until all data for a transaction has flowed through.
- Generates AXI User Signal for ACP.

I/O Peripherals

I/O Peripherals (IOP) include Quad SPI flash memory, NOR/NAND Flash, UART, I2C, SPI, SDIO, GPIO, CAN, USB, and Ethernet. The interfaces for these IOPs can be routed to MIO ports and the EMIO interfaces as described in the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

MIO Ports

The Zynq-7000 All Programmable SoC design tools are used to configure the Zynq-7000 FPGA processing system MIO ports. There are up to 54 MIO ports available from the processing system. The wizard allows you to choose the peripheral ports to be connected to MIO ports.

Extended MIO Ports

Because there are only up to 54 MIO available ports, many peripheral I/O ports beyond these can still be routed to the programmable logic through the Extended MIO (EMIO) interface. Alternative routing for IOP interfaces through programmable logic enables you to take full advantage of the IOP available in the processing system. The EMIO for I2C, serial peripheral interface (SPI), Ethernet management data input/output (MDIO), PJTAG, SDIO, GPIO 3-state enable signals are inverted in the Processing System 7 core.

The Processing System 7 core allows you to select GPIO up to 64 bits. Processing System 7 has control logic to adjust user-selected width to flow into Processing System 7.

GigE MAC (Registering)

The Ethernet GMII `txd`, `tx_en`, `tx_er`, `col` and `crs` signals are registered on `tx_clk`, while the `rxd`, `rx_dv` and `rx_er` signals are registered on `rx_clk`.

Fabric Trace Monitor

The fabric trace monitor (FTM) signals such as `ftm trace data`, `valid` and `atid` signals are also registered on `ftmd_tracein_clk`.

Signal Inverters (3-State)

Only the 3-state (*_t_n) signals are inverted. However `sdio{0,1}_cmd_t` and `sdio{0,1}_data_t` are inverted only if `c_ps7_si_rev` is not a Commercial Temperature Range Engineering Sample (CES) 7020 silicon.

AXI I/O Interfaces

The AXI I/O interface group contains AXI interfaces between the processing system and the programmable logic. The AXI interfaces include two general purpose master ports, two general purpose slave ports along with four high performance ports and an accelerator coherency port (ACP). The ID widths of the slave ports are variable and Processing System 7 controls the ID width of these ports based on a user parameter. ACP transactions are monitored by the ACP transactions checker (ATC).

Logic for Vivado Design Suite IP - Processing System Interface

The Processing System 7 core allows you to add Vivado IP cores in the programmable logic to interface with the processing system. AXI interfaces can be used by an AXI3-compliant master or slave to be connected to the ARM® core. The Xilinx PL-based cores use AXI4 or AXI4-Lite and require conversion, typically through an AXI interconnect core. Custom direct memory access (DMA) functions can be implemented in the PL to oversee data movement irrespective of the processor intervention. The only modifications to the AXI interfaces are the applications of the ACP transaction checker and ID remap.

Programmable Logic Clocks and Interrupts

The interrupts from the processing system I/O peripherals (IOP) are routed to the PL and assert asynchronously to the `fclk` clocks.

The PL can asynchronously assert up to 20 interrupts to the PS.

- 16 interrupt signals are mapped to the interrupt controller as a peripheral interrupt where each interrupt signal is set to a priority level and mapped to one or both of the CPUs.
- The remaining four PL interrupt signals are inverted and routed to the `nFIQ` and `nIRQ` interrupt directly to the signals to the private peripheral interrupt (PPI) unit of the interrupt controller. There is an `nFIQ` and `nIRQ` interrupt for each of two CPUs.

The PS to PL, and PL to PS interrupts are listed in Table 2-1. For details on the interrupt signals, see the "Interrupts" chapter in the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Table 2-1: **Interrupt Signals**

Type	PL Signal Name	I/O	Destination
PL to PS Interrupts	irqf2p[7:0]	I	SPI: Numbers [68:61].
	irqf2p[15:8]	I	SPI: Numbers [91:84].
	irqf2p[19:16]	I	PPI: nFIQ, nIRQ (both CPUs).
PS to PL Interrupts	irqf2p[27:0]	O	PI Logic. The signals are received from the I/O peripherals and are forwarded to the interrupt controller. These signals are also provided as outputs to the PL.

The Processing System 7 core employs logic to handle PL interrupts, the number which varies from 1 to 16 depending on your selection. The number of interrupts connected to IRQ_F2P are calculated and the logic ensures the correct order of an interrupt assignment.

The Processing System 7 interrupts from IOPs are available to custom master interfaces in PL.

The ID assignment for interrupts can be upwards (start from 61 up to 91) or downwards (91 to 61). PS Configuration Wizard (PCW) has a parameter, PCW_IRQ_F2P_MODE, that can be set on the Tcl Console prompt. This parameter can take values as **DIRECT** and **REVERSE**. By default the ID assignment from PCW for interrupts is **DIRECT**. This means the IDs of the interrupt start at 61 and end at 91. For backward compatibility purposes, the value of **REVERSE** is provided for this parameter. Setting this parameter to **REVERSE** starts the interrupt ID assignment at 91 and ends at 61. For all newly created designs, the default value of PCW_IRQ_F2P_MODE is **DIRECT**. For all designs which are being upgraded from 2014.x and 2014.x Vivado design tools versions to the next Vivado design tools versions, PCW sets the value of this parameter as **REVERSE** to make sure the interrupt ID assignment remains the same after the upgrade.

For example, to set the PCW_IRQ_F2P_MODE to DIRECT, the following command can be used in the Vivado Tcl Console.

```
set_property config.PCW_IRQ_F2P_MODE DIRECT [get_bd_cells processing_system7_0],
```

where *processing_system7_0* is the instance name of the Zynq-7000 Processing System IP core.

Similarly, to set the PCW_IRQ_F2P_MODE to REVERSE, the following command can be used in the Vivado Tcl Console.

```
set_property config.PCW_IRQ_F2P_MODE REVERSE [get_bd_cells processing_system7_0],
```

where *processing_system7_0* is the instance name of the Zynq-7000 Processing System IP core. All values other than DIRECT & REVERSE have no impact on the function.

The Processing System 7 provides four clocks to the PL. Processing System 7 enables configuration of these clocks to be used in the PL. Processing System 7 inserts a BUFG for each of the PL clocks through parameters similar to C_FCLK_CLK0_BUF.

Standards

The Processing System 7 core is compatible with the AXI3 Interface. AXI interfaces can be used by an AXI3-compliant master or slave connected to the ARM® core.

See the "Interconnect" chapter in the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Performance

For information, see the "PL and Memory System Performance Overview" section in the "Programmable Logic Design Guide" chapter of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Maximum Frequencies

For information, see the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Latency

For information, see the "Power Management" chapter of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Throughput

For information, see the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Power

For information, see the "Power Management" chapter of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Resource Utilization

The Processing System 7 core is a hard IP so device utilization data is not available for this core.

Port Descriptions

The I/O signals for the design are listed in the following tables.

ENET0 I/O Signals

Table 2-2: **ENET0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P1	enet0_gmii_rx_clk	emioenet0gmiirxclk	I	Receive clock
P2	enet0_gmii_crs	emioenet0gmiicrs	I	Carrier sense from the physical-side interface (PHY)
P2	enet0_gmii_crs	emioenet0gmiicrs	I	Carrier sense from the PHY
P3	enet0_gmii_col	emioenet0gmiicol	I	Collision detect from the PHY
P4	enet0_gmii_rxd[7:0]	emioenet0gmiirxd[7:0]	I	Receive data from the PHY
P5	enet0_gmii_rx_er	emioenet0gmiirxer	I	Receive error signal from the PHY
P6	enet0_gmii_tx_clk	emioenet0gmiitxclk	I	Receive data valid signal from the PHY
P7	enet0_gmii_txd[7:0]	emioenet0gmiitxd[7:0]	O	Transmit clock
P8	enet0_gmii_tx_en	emioenet0gmiitxen	O	Transmit data to the PHY
P9	enet0_gmii_tx_er	emioenet0gmiitxer	O	Transmit enable to the PHY
P10	enet0_mdio_mdc	emioenet0mdiomdc	O	Management data clock to pin
P11	enet0_mdio_i	emioenet0mdioi	I	Management data input from MDIO pin
P12	enet0_mdio_o	emioenet0mdioo	O	Management data output to MDIO pin
P13	enet0_mdio_t	emioenet0mdiotn	O	Management data active-Low 3-state enable to MDIO pin, active-Low.
P14	enet0_ptp_sync_frame_tx	emioenet0ptpsyncframetx	O	Asserted High synchronous to `tx_clk` if precise timing protocol (PTP) sync frame is detected on transmit.

Table 2-2: **ENET0 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P15	enet0_ptp_delay_req_tx	emioenet0ptpdelayreqtx	O	Asserted High synchronous to `tx_clk` if PTP delay request frame is detected on transmit.
P16	enet0_ptp_pdelay_req_tx	emioenet0ptppdelayreqtx	O	Asserted High synchronous to `tx_clk` if PTP peer delay request frame is detected on transmit.
P17	enet0_ptp_pdelay_resp_tx	emioenet0ptppdelayresptx	O	Asserted High synchronous to `tx_clk` if PTP peer delay response frame is detected on transmit.
P18	enet0_sof_tx	emioenet0softx	O	Asserted High synchronous to `rx_clk` if PTP sync frame is detected on receive.
P19	enet0_ptp_sync_frame_rx	emioenet0ptpsyncframerx	O	Asserted High synchronous to `rx_clk` if PTP delay request frame is detected on receive.
P20	enet0_ptp_delay_req_rx	emioenet0ptpdelayreqrx	O	Asserted High synchronous to `rx_clk` if PTP peer delay request frame is detected on receive.
P21	enet0_ptp_pdelay_req_rx	emioenet0ptppdelayreqrx	O	Asserted High synchronous to `rx_clk` if PTP peer delay response frame is detected on receive.
P22	enet0_ext_intin	emioenet0extintin	I	Ethernet interrupt input

ENET1 I/O Signals

Table 2-3: **ENET1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P23	enet1_gmii_rx_clk	emioenet1gmiirxclk	I	Receive clock
P24	enet1_gmii_crs	emioenet1gmiicrs	I	Carrier sense from the PHY
P25	enet1_gmii_col	emioenet1gmiicol	I	Collision detect from the PHY
P26	enet1_gmii_rxd[7:0]	emioenet1gmiirxd[7:0]	I	Receive data from the PHY
P27	enet1_gmii_rx_er	emioenet1gmiirxer	I	Receive error signal from the PHY
P28	enet1_gmii_tx_clk	emioenet1gmiitxclk	I	Receive data valid signal from the PHY
P29	enet1_gmii_txd[7:0]	emioenet1gmiitxd[7:0]	O	Transmit clock
P30	enet1_gmii_txen	emioenet1gmiitxen	O	Transmit data to the PHY
P31	enet1_gmii_tx_er	emioenet1gmiitxer	O	Transmit enable to the PHY
P32	enet1_mdio_mdc	emioenet1mdiomdc	O	Management data clock to pin
P33	enet1_mdio_i	emioenet1mdioi	I	Management data input from MDIO pin
P34	enet1_mdio_o	emioenet1mdioo	O	Management data output to MDIO pin

Table 2-3: **ENET1 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P35	enet1_mdio_t	emioenet1mdiotn	O	Management data active-Low 3-state enable to MDIO pin, active-Low
P36	enet1_ptp_sync_frame_tx	emioenet1ptpsyncframetx	O	Asserted High synchronous to tx_clk if PTP sync frame is detected on transmit.
P37	enet1_ptp_delay_req_tx	emioenet1ptpdelayreqtx	O	Asserted High synchronous to tx_clk if PTP delay request frame is detected on transmit.
P38	enet1_ptp_pdelay_req_tx	emioenet1ptppdelayreqtx	O	Asserted High synchronous to tx_clk if PTP peer delay request frame is detected on transmit.
P39	enet1_ptp_pdelay_resp_tx	emioenet1ptppdelayresptx	O	Asserted High synchronous to tx_clk if PTP peer delay response frame is detected on transmit.
P40	enet1_sof_tx	emioenet1softx	O	Asserted High synchronous to rx_clk if PTP sync frame is detected on receive.
P41	enet1_ptp_sync_frame_rx	emioenet1ptpsyncframerx	O	Asserted High synchronous to rx_clk if PTP delay request frame is detected on receive.
P42	enet1_ptp_delay_reqrx	emioenet1ptpdelayreqrx	O	Asserted High synchronous to rx_clk if PTP peer delay request frame is detected on receive.
P43	enet1_ptp_pdelay_req_rx	emioenet1ptppdelayreqrx	O	Asserted High synchronous to rx_clk if PTP peer delay response frame is detected on receive.
P44	enet1_ext_intin	emioenet1extintin	I	Ethernet interrupt input.

TTC0 I/O Signals

Table 2-4: **TTC0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P45	ttc0_wave_o[2:0]	emiottc0waveo[2:0]	O	Waveform generated from ttc0
P46	ttc0_clk_i[2:0]	emiottc0clki[2:0]	I	Clock input for each timer

TTC1 I/O Signals

Table 2-5: **TTC1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P47	ttc1_wave_o[2:0]	emiottc1waveo[2:0]	O	Waveform generated ttc1
P48	ttc1_clk_i[2:0]	emiottc1clki[2:0]	I	Clock input for each timer

WDT I/O Signals

Table 2-6: **WDT I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P49	wdt_clk_i	emiowdtclki	I	Clock input
P50	wdt_rst_o	emiowdtrsto	O	Watchdog reset output

SPIO0 I/O Signals

Table 2-7: **SPIO0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P51	spi0_sclk_i	emiospi0sclki	I	SPI slave clock
P52	spi0_sclk_o	emiospi0sclko	O	SPI master clock output
P53	spi0_sclk_t	emiospi0sclktn	O	SPI clock 3-state enable
P54	spi0_miso_i	emiospi0mi	I	SPI master in slave out (MISO) signal master input
P55	spi0_miso_o	emiospi0mo	O	SPI master out slave in (MOSI) signal master output
P56	spi0_mosi_t	emiospi0motn	O	SPI MOSI signal 3-state enable
P57	spi0_mosi_i	emiospi0motn	I	SPI MOSI signal slave input
P58	spi0_miso_o	emiospi0so	O	SPI MISO signal slave output
P60	spi0_miso_t	emiospi0stn	O	SPI MISO signal 3-state enable
P61	spi0_ss_i	emiospi0ssin	I	SPI slave select input
P62	spi0_ss2_o spi0_ss1_o spi0_ss0_o	emiospi0sson[2:0]	O	SPI peripheral select outputs
P63	spi0_ss_t	emiospi0ssntn	O	SPI peripheral select 3-state enable

SPIO1 I/O Signals

Table 2-8: **SPIO1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P64	spi1_sclk_i	emiospi1sclki	I	SPI slave clock
P65	spi1_sclk_o	emiospi1sclko	O	SPI master clock output
P66	spi1_sclk_t	emiospi1sclktn	O	SPI clock 3-state enable
P67	spi1_miso_i	emiospi1mi	I	SPI MISO signal master input

Table 2-8: **SPIO1 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P68	spi1_miso_o	emiospi1mo	O	SPI MOSI signal master output
P69	spi1_mosi_t	emiospi1motn	O	SPI MOSI signal 3-state enable
P70	spi1_mosi_i	emiospi1motn	I	SPI MOSI signal slave input
P71	spi1_miso_o	emiospi1so	O	SPI MISO signal slave output
P72	spi1_miso_t	emiospi1stn	O	SPI MISO signal 3-state enable
P73	spi1_ss_i	emiospi1ssin	I	SPI slave select input
P74	spi1_ss2_o spi1_ss1_o spi1_ss0_o	emiospi1sson[2:0]	O	SPI peripheral select outputs
P75	spi1_ss_t	emiospi1ssntn	O	SPI peripheral select 3-state enable

I2C0 I/O Signals

Table 2-9: **I2C0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P76	i2c0_scl_i	emioi2c0scli	I	Actual state of the external scl clock signal
P77	i2c0_scl_o	emioi2c0sclo	O	Clock level to be placed on scl pin
P78	i2c0_scl_t	emioi2c0scltn	O	3-state enable for the scl output buffer
P79	i2c0_sda_i	emioi2c0sdai	I	Actual state of the external sda signal
P80	i2c0_sda_o	emioi2c0sdao	O	Data bit to be placed on external sda signal
P81	i2c0_sda_t	emioi2c0sdatn	O	3-state enable for the sda output buffer

I2C1 I/O Signals

Table 2-10: **I2C1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P82	i2c1_scl_i	emioi2c1scli	I	Actual state of the external scl clock signal
P83	i2c1_scl_o	emioi2c1sclo	O	Clock level to be placed on scl pin
P84	i2c1_scl_t	emioi2c1scltn	O	3-state enable for the scl output buffer
P85	i2c1_sda_i	emioi2c1sdai	I	Actual state of the external sda signal
P86	i2c1_sda_o	emioi2c1sdao	O	Data bit to be placed on external sda signal
P87	i2c1_sda_t	emioi2c1sdatn	O	3-state enable for the sda output buffer

CAN0 I/O Signals

Table 2-11: **CAN0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P88	can0_phy_tx	emiocan0phytx	O	Controller area network (CAN) bus transmit signal
P89	can0_phy_rx	emiocan0phyrx	I	CAN bus receive signal

CAN1 I/O Signals

Table 2-12: **CAN1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P90	can1_phy_tx	emiocan1phytx	O	CAN bus transmit signal
P91	can1_phy_rx	emiocan1phyrx	I	CAN bus receive signal

UART0 I/O Signals

Table 2-13: **UART0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P92	uart0_tx	emiouart0tx	O	UART transmitter serial output pin
P93	uart0_rx	emiouart0rx	I	UART receiver serial input pin
P94	uart0_ctsn	emiouart0ctsn	I	Clear-to-send flow control
P95	uart0_rtsn	emiouart0rtsn	O	Request-to-send flow control
P96	uart0_dsrn	emiouart0dsrn	I	Modem data set ready
P97	uart0_dcdn	emiouart0dcdn	I	Modem data carrier detect
P98	uart0_rin	emiouart0rin	I	Modem ring indicator
P99	uart0_dtrn	emiouart0dtrn	O	Modem data terminal ready

UART1 I/O Signals

Table 2-14: **UART1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P100	uart1_tx	emiouart1tx	O	UART transmitter serial output pin
P101	uart1_rx	emiouart1rx	I	UART receiver serial input pin
P102	uart1_ctsn	emiouart1ctsn	I	Clear-to-send flow control
P103	uart1_rtsn	emiouart1rtsn	O	Request-to-send flow control

Table 2-14: **UART1 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P104	uart1_dsrn	emiouart1dsrn	I	Modem data set ready
P105	uart1_dcdn	emiouart1dcdn	I	Modem data carrier detect
P106	uart1_rin	emiouart1rin	I	Modem ring indicator
P107	uart1_dtrn	emiouart1dtrn	O	Modem data terminal ready

SDIO0 I/O Signals

Table 2-15: **SDIO0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P108	sdio0_clk	emiosdio0clk	O	Clock output to SD/SDIO slave device
P109	sdio0_clk_fb	emiosdio0clkfb	I	Clock feedback input to SD/SDIO slave device
P110	sdio0_cmdo	emiosdio0cmdo	O	Command indicator input
P111	sdio0_cmdi	emiosdio0cmdi	I	Command indicator output
P112	sdio0_cmd_t	emiosdio0cmdtn	O	Command indicator 3-state enable
P113	sdio0_datai[3:0]	emiosdio0datai[3:0]	I	4-bit input data bus
P114	sdio0_data_o[3:0]	emiosdio0datao[3:0]	O	4-bit output data bus
P115	sdio0_data_tn[3:0]	emiosdio0datatn[3:0]	O	4-bit output data bus, 3-state enable
P116	sdio0_cdn	emiosdio0cdn	I	Card Detect
P117	sdio0_wp	emiosdio0wp	I	Write Protect
P118	sdio0_led	emiosdio0led	O	LED Output
P119	sdio0_buspow	emiosdio0buspow	O	Selects SDIO bus power
P120	sdio0_busvolt[2:0]	emiosdio0busvolt[2:0]	O	Selects SDIO bus voltage

SDIO1 I/O Signals

Table 2-16: **SDIO1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P121	sdio1_clk	emiosdio1clk	O	Clock output to SD/SDIO slave device
P122	sdio1_clk_fb	emiosdio1clkfb	I	Clock feedback input to SD/SDIO slave device
P123	sdio1_cmdo	emiosdio1cmdo	O	Command indicator input
P124	sdio1_cmdi	emiosdio1cmdi	I	Command indicator output
P125	sdio1_cmd_t	emiosdio1cmdtn	O	Command indicator 3-state enable

Table 2-16: **SDIO1 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P126	sdio1_datai[3:0]	emiosdio1datai[3:0]	I	4-bit input data bus
P127	sdio1_data_o[3:0]	emiosdio1datao[3:0]	O	4-bit output data bus
P128	sdio1_data_tn[3:0]	emiosdio1datatn[3:0]	O	4-bit output data bus 3-state enable
P129	sdio1_cdn	emiosdio1cdn	I	Card Detect
P130	sdio1_wp	emiosdio1wp	I	Write Protect
P131	sdio1_led	emiosdio1led	O	LED Output
P132	sdio1_buspow	emiosdio1buspow	O	Selects SDIO bus power
P133	sdio1_busvolt[2:0]	emiosdio1busvolt[2:0]	O	Selects SDIO bus voltage

GPIO I/O Signals

Table 2-17: **GPIO I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P134	gpio_i[(c_emio_gpio_width-1):0]	emiogpioi[63:0]	I	GPIO port inputs
P135	gpio_o[c_emio_gpio_width-1:0]	emiogpioo[63:0]	O	GPIO port outputs
P136	gpio_t[(c_emio_gpio_width-1):0]	emiogpiotn[63:0]	O	3-state enable signals for GPIO port

TRACE I/O Signals

Table 2-18: **TRACE I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P137	trace_clk	emiotraceclk	I	Trace clock input
P138	trace_ctl	emiotracectl	O	Trace control output
P139	trace_data[31:0]	emiotracedata[31:0]	O	Trace data output

PJTAG I/O Signals

Table 2-19: **PJTAG I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P140	pjtag_tck	emiopjtagtck	I	JTAG clock input
P141	pjtag_tms	emiopjtagtms	I	JTAG mode select
P142	pjtag_td_i	emiopjtagtdi	I	JTAG data input
P143	pjtag_td_t	emiopjtagtdtn	O	3-state enable for trace data out (TDO)
P144	pjtag_td_o	emiopjtagtdo	O	JTAG data output

USB0 I/O Signals

Table 2-20: **USB0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P145	usb0_port_indctl	emiousb0portindctl[1:0]	O	USB port indicator
P146	usb0_vbus_pwrfault	emiousb0vbuspwrfault	I	USB power fault
P147	usb0_vbus_pwrselect	emiousb0vbuspwrselect	O	USB power select

USB1 I/O Signals

Table 2-21: **USB1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P148	usb1_port_indctl	emiousb1portindctl[1:0]	O	USB port indicator
P149	usb1_vbus_pwrfault	emiousb1vbuspwrfault	I	USB power fault
P150	usb1_vbus_pwrselect	emiousb1vbuspwrselect	O	USB power select

SRAM I/O Signal

Table 2-22: **SRAM I/O Signal**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P151	sram_intin	emiosramintin	I	SRAM interrupt

PL Clock and Reset Signals

Table 2-23: **PL Clock and Reset Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P152 P153 P154 P155	fclk_clk3 fclk_clk2 fclk_clk1 fclk_clk0	fclkclk[3:0]	O	Clocks to be used as frequency source in PL
P156 P157 P158 P159	fclk_clktrig3_n fclk_clktrig2_n fclk_clktrig1_n fclk_clktrig0_n	fclkclktrign[3:0]	I	Signal to enable or halt clock pulse asynchronous to clock
P160 P161 P162 P163	fclk_reset3_n fclk_reset2_n fclk_reset1_n fclk_reset0_n	fclkresetn[3:0]	O	General reset signal from PS to PL

PL Idle Signals

Table 2-24: **PL Idle Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P164	fpga_idle_n	fpgaidlen	I	Input to indicate PL AXI idle
P165	event_eventi	eventeventi	I	eventi input for A9 MPCore™ multicore processor wake up from wait for event (WFE). Any transition on the eventi input from the PL causes a one-cycle pulse input to the A9 MPCore.

EVENT I/O Signals

Table 2-25: **EVENT I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P166	event_evento	eventevento	O	evento output of the A9 MPCore- Active when SEV is executed. A one-cycle pulse output from the A9 MPCore on EVENTO causes the PL evento signal to toggle.
P167	event_standbywfe[1:0]	eventstandbywfe[1:0]	O	Indicates A9[1:0]
P168	event_standbywfi[1:0]	eventstandbywfi[1:0]	O	Indicates A9[1:0] is in Standby wait for interrupt (WFI) state.

DDR ARB I/O Signal

Table 2-26: **DDR ARB I/O Signal**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P169	ddr_arb[3:0]	ddrarb[3:0]	I	Input to double data rate (DDR) bypass

PL TRACE I/O Signals

Table 2-27: **PL TRACE I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P170	ftmd_tracein_data[31:0]	ftmdtraceindata[31:0]	I	Trace input data
P171	ftmd_tracein_valid	ftmdtraceinvalid	I	Trace input valid. Data is clocked into the `ftm` when valid is 1.
P172	ftmd_tracein_clk	ftmdtraceinclock	I	Trace input clock
P173	ftmd_tracein_atid[31:0]	ftmdtraceinatid[3:0]	I	Trace ID

Cross Trigger I/O Signals

Table 2-28: **Cross Trigger I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P174	ftmt_f2p_trig[3:0]	ftmtf2ptrig[3:0]	I	PL Trigger
P175	ftmt_f2p_trigack[3:0]	ftmtf2ptrigack[3:0]	O	PL Trigger Acknowledge
P176	ftmt_f2p_debug[31:0]	ftmtf2pdebug[31:0]	I	Debug inputs from PL
P177	ftmt_p2f_trig[3:0]	ftmtp2ftrig[3:0]	O	PS Trigger
P178	ftmt_p2f_trigack[3:0]	ftmtp2ftrigack[3:0]	I	PS Trigger Acknowledge
P179	ftmt_p2f_debug[31:0]	ftmtp2fdebug[31:0]	O	Debug outputs to PL

DMA0 I/O Signals

Table 2-29: **DMA0 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P180	dma0_daready	dma0daready	I	Peripheral ready
P181	dma0_datype[1:0]	dma0datype[1:0]	O	DMA request/ack type
P182	dma0_davalid	dma0davalid	O	DMA data valid
P183	dma0_drlast	dma0drlast	I	Last data of DMA transfer
P184	dma0_drready	dma0drready	O	DMA ready
P185	dma0_drtype[1:0]	dma0drtype[1:0]	O	Peripheral request/ack type
P186	dma0_drvalid	dma0drvalid	I	Peripheral data valid
P188	dma0_aclk	dma0aclk	I	Clock for DMA request transfers

DMA1 I/O Signals

Table 2-30: **DMA1 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P189	dma1_daready	dma1daready	I	Indicates if the peripheral can accept the information that the direct memory access controller (DMAC) provides on datype_<x>[1:0].
P190	dma1_datype[1:0]	dma1datype[1:0]	O	Indicates the type of acknowledgement, or request that the DMAC signals: • b00: DMAC has completed the single DMA transfer. • b01: DMAC has completed the burst DMA transfer. • b10: DMAC requesting the peripheral to perform a flush request. • b11: Reserved
P191	dma1_davalid	dma1davalid	O	Indicates when the DMAC provides valid control information: • 0: No control information is available. • 1: datype_<x>[1:0] contains valid information for the peripheral.
P192	dma1_drlast	dma1drlast	I	Indicates that the peripheral is sending the last data transfer for the current DMA transfer: • 0: Last data request is not in progress. • 1: Last data request is in progress. ***Note:*** The DMAC only uses this signal when drtype_<x>[1:0] is b00 or b01.
P193	dma1_drready	dma1drready	O	Indicates if the DMAC can accept the information that the peripheral provides on drtype_<x>[1:0]. • 0: DMAC not ready • 1: DMAC ready
P194	dma1_drtype[1:0]	dma1drtype[1:0]	O	Indicates the type of acknowledgement, or request, that the peripheral signals. • b00: Single level request • b01: Burst level request • b10: Acknowledging a flush request that the DMAC requested • b11: Reserved

Table 2-30: **DMA1 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P195	dma1_drvalid	dma1drvalid	I	Indicates when the peripheral provides valid control information. • 0: No control information is available • 1: drtype_<x>[1:0] and drlast_<x> contain valid information for the DMAC.
P197	dma1_aclk	dma1aclk	I	Clock for DMA request transfers

DMA2 I/O Signals

Table 2-31: **DMA2 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P198	dma2_daready	dma2daready	I	Indicates if the peripheral can accept the information that the DMAC provides on datype_<x>[1:0].
P199	dma2_datype[1:0]	dma2datype[1:0]	O	Indicates the type of acknowledgement, or request that the DMAC signals: • b00: DMAC has completed the single DMA transfer. • b01: DMAC has completed the burst DMA transfer. • b10: DMAC requesting the peripheral to perform a flush request. • b11: Reserved
P200	dma2_davalid	dma2davalid	O	Indicates when the DMAC provides valid control information: • 0: No control information is available. • 1: datype_<x>[1:0] contains valid information for the peripheral.
P201	dma2_drlast	dma2drlast	I	Indicates that the peripheral is sending the last data transfer for the current DMA transfer: • 0: Last data request is not in progress • 1: Last data request is in progress ***Note:*** The DMAC only uses this signal when drtype_<x>[1:0] is b00 or b01.
P202	dma2_drready	dma2drready	O	Indicates if the DMAC can accept the information that the peripheral provides on drtype_<x>[1:0]. • 0: DMAC not ready • 1: DMAC ready

Table 2-31: **DMA2 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P203	dma2_drtype[1:0]	dma2drtype[1:0]	O	Indicates the type of acknowledgement, or request that the peripheral signals. • b00: Single level request • b01: Burst level request • b10: Acknowledging a flush request that the DMAC requested • b11: Reserved
P204	dma2_drvalid	dma2drvalid	I	Indicates when the peripheral provides valid control information. • 0: No control information is available. • 1: drtype_<x>[1:0] and drlast_<x> contain valid information for the DMAC.
P206	dma2_aclk	dma2aclk	I	Clock for DMA request transfers

DMA3 I/O Signals

Table 2-32: **DMA3 I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P207	dma3_daready	dma3daready	I	Indicates if the peripheral can accept the information that the DMAC provides on datype_<x>[1:0].
P208	dma3_datype[1:0]	dma3datype[1:0]	O	Indicates the type of acknowledgement, or request, that the DMAC signals: • b00: DMAC has completed the single DMA transfer. • b01: DMAC has completed the burst DMA transfer. • b10: DMAC requesting the peripheral to perform a flush request. • b11: Reserved
P209	dma3_davalid	dma3davalid	O	Indicates when the DMAC provides valid control information: • 0: No control information is available. • 1: datype_<x>[1:0] contains valid information for the peripheral.

Table 2-32: **DMA3 I/O Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P210	dma3_drlast	dma3drlast	I	Indicates that the peripheral is sending the last data transfer for the current DMA transfer: • 0: Last data request is not in progress. • 1: Last data request is in progress. ***Note:*** The DMAC only uses this signal when drtype_<x>[1:0] is b00 or b01.
P211	dma3_drready	dma3drready	O	Indicates if the DMAC can accept the information that the peripheral provides on drtype_<x>[1:0]. • 0: DMAC not ready • 1: DMAC ready
P212	dma3_drtype[1:0]	dma3drtype[1:0]	O	Indicates the type of acknowledgement, or request, that the peripheral signals. • b00: Single level request • b01: Burst level request • b10: Acknowledging a flush request that the DMAC requested • b11: Reserved
P213	dma3_drvalid	dma3drvalid	I	Indicates when the peripheral provides valid control information. • 0: No control information is available. • 1: drtype_<x>[1:0] and drlast_<x> contain valid information for the DMAC.
P215	dma3_aclk	dma3aclk	I	Clock for DMA request transfers

Interrupts Signals

Table 2-33: **Interrupts Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P216	irq_f2p [7:0]	irqf2p[7:0]	I	Application Processor Unit (APU) Peripherals interrupts 68 to 61
P217	irq_f2p [15:8]	irqf2p[15:8]	I	APU Peripherals interrupts 91 to 84
P218	core0_nirq	irqf2p[16]	I	APU CPU 0 nIRQ
P219	core1_nirq	irqf2p [17]	I	APU CPU 1 nIRQ
P220	core0_nfiq	irqf2p [18]	I	APU CPU 0 nFIQ
P221	core1_nfiq	irqf2p [19]	I	APU CPU 1 nFIQ
P222	irq_p2f_dmac_abort	irqp2f[28]	O	DMAC0 Abort Interrupt

Table 2-33: **Interrupts Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P223	irq_p2f_dmac7 irq_p2f_dmac6 irq_p2f_dmac5 irq_p2f_dmac4 irq_p2f_dmac3 irq_p2f_dmac2 irq_p2f_dmac1 irq_p2f_dmac0	irqp2f[27:20]	O	Eight Interrupts for DMAC0
P224	irq_p2f_smc	irqp2f[19]	O	Static memory controller (SMC) interrupt
P225	irq_p2f_qspi	irqp2f[18]	O	Quad-SPI interrupt
P226	irq_p2f_cti	irqp2f[17]	O	Cross Trigger Interrupt
P227	irq_p2f_gpio	irqp2f[16]	O	GPIO interrupt
P228	irq_p2f_usb0	irqp2f[15]	O	USB port #0 interrupt
P229	irq_p2f_enet0	irqp2f[14]	O	gigabit ethernet media (GEM) port #0 interrupt
P230	irq_p2f_enet_wake0	irqp2f[13]	O	GEM port #0 wake interrupt
P231	irq_p2f_sdio0	irqp2f[12]	O	SDIO port #0 interrupt
P232	irq_p2f_i2c0	irqp2f[11	O	I2C port #0 interrupt
P233	irq_p2f_spi0	irqp2f[10]	O	SPI port #0 interrupt
P234	irq_p2f_uart0	irqp2f[9]	O	UART port #0 interrupt
P235	irq_p2f_can0	irqp2f[8]	O	CAN port #0 interrupt
P236	irq_p2f_usb1	irqp2f[7]	O	USB port #1 interrupt
P237	irq_p2f_enet1	irqp2f[6]	O	GEM port #1 interrupt
P238	irq_p2f_enet_wake1	irqp2f[5]	O	GEM port #1 wake interrupt
P239	irq_p2f_sdio1	irqp2f[4]	O	SDIO port #1 interrupt
P240	irq_p2f_i2c1	irqp2f[3]	O	I2C port #1 interrupt
P241	irq_p2f_spi1	irqp2f[2]	O	SPI port #1 interrupt
P242	irq_p2f_uart1	irqp2f[1]	O	UART port #1 interrupt
P243	irq_p2f_can1	irqp2f[0]	O	CAN port #1 interrupt

M_AXI_GP0 Signals

Table 2-34: **PS Master, PL Slave – General Purpose Port – M_AXI_GP0 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P244	m_axi_gp0_aclk	maxigp0aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P246	m_axi_gp0_awid[c_m_axi_gp0_thread_id_width-1:0]	maxigp0awid[11:0]	O	Write ID.
P247	m_axi_gp0_awaddr[31:0]	maxigp0awaddr[31:0]	O	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P248	m_axi_gp0_awlen[3:0]	maxigp0awlen[3:0]	O	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P249	m_axi_gp0_awsize[2:0]	maxigp0awsize[1:0]	O	Burst size. m_axi_gp0_awsize[2] is not used.
P250	m_axi_gp0_awburst[1:0]	maxigp0awburst[1:0]	O	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P251	m_axi_gp0_awlock[1:0]	maxigp0awlock[1:0]	O	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P252	m_axi_gp0_awcache[3:0]	maxigp0awcache[3:0]	O	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P253	m_axi_gp0_awprot[2:0]	maxigp0awprot[2:0]	O	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.

Table 2-34: **PS Master, PL Slave – General Purpose Port – M_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P254	m_axi_gp0_awvalid	maxigp0awvalid	O	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.
P255	m_axi_gp0_awready	maxigp0awready	I	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P256	m_axi_gp0_wid[c_m_axi_gp0_thread_id_width-1:0]	maxigp0wid[11:0]	O	Write ID tag. This signal is the ID tag of the write data transfer. The Width ID (WID) value must match the AXI Width ID (AWID) value of the write transaction.
P257	m_axi_gp0_wdata[31:0]	maxigp0wdata[31:0]	O	Write data.
P260	m_axi_gp0_wstrb[3:0]	maxigp0wstrb[3:0]	O	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds to WDATA[(8 × *n*) + 7:(8 × *n*)].
P261	m_axi_gp0_wlast	maxigp0wlast	O	Write last. This signal indicates the last transfer in a write burst.
P262	m_axi_gp0_wvalid	maxigp0wvalid	O	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.
P263	m_axi_gp0_wready	maxigp0wready	I	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P264	m_axi_gp0_bid[c_m_axi_gp0_thread_id_width-1:0]	maxigp0bid[11:0]	I	Response ID. The identification tag of the write response. The Bus ID (BID) value must match the AWID value of the write transaction to which the slave is responding.

Table 2-34: **PS Master, PL Slave – General Purpose Port – M_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P265	m_axi_gp0_bresp[1:0]	maxigp0bresp[1:0]	I	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P266	m_axi_gp0_bvalid	maxigp0bvalid	I	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P267	m_axi_gp0_bready	maxigp0bready	O	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P268	m_axi_gp0_arid[c_m_axi_gp0_thread_id_width-1:0]	maxigp0arid[11:0]	O	Read address ID. This signal is the identification tag for the read address group of signals.
P269	m_axi_gp0_araddr[31:0]	maxigp0araddr[31:0]	O	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P270	m_axi_gp0_arlen[3:0]	maxigp0arlen[3:0]	O	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
P271	m_axi_gp0_arsize[2:0]	maxigp0arsize[1:0]	O	Burst size. This signal indicates the size of each transfer in the burst. m_axi_gp0_arsize[2] is not used.
P272	m_axi_gp0_arburst[1:0]	maxigp0arburst[1:0]	O	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P273	m_axi_gp0_arlock[1:0]	maxigp0arlock[1:0]	O	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P274	m_axi_gp0_arcache[3:0]	maxigp0arcache[3:0]	O	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.

Table 2-34: **PS Master, PL Slave – General Purpose Port – M_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P275	m_axi_gp0_arprot[2:0]	maxigp0arprot[2:0]	O	Protection type. This signal provides protection unit information for the transaction.
P276	m_axi_gp0_arvalid	maxigp0arvalid	O	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal arready is High. • 1: Address and control information valid • 0: Address and control information not valid
P277	m_axi_gp0_arready	maxigp0arready	I	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P278	m_axi_gp0_rid[c_m_axi_gp0_thread_id_width-1:0]	maxigp0rid[11:0]	I	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the AXI Read ID (ARID) value of the read transaction to which it is responding.
P279	m_axi_gp0_rdata[31:0]	maxigp0rdata[31:0]	I	Read data.
P280	m_axi_gp0_rresp[1:0]	maxigp0rresp[1:0]	I	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P281	m_axi_gp0_rlast	maxigp0rlast	I	Read last. This signal indicates the last transfer in a read burst.
P282	m_axi_gp0_rvalid	maxigp0rvalid	I	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P283	m_axi_gp0_rready	maxigp0rready	O	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready

Table 2-34: **PS Master, PL Slave – General Purpose Port – M_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P284	m_axi_gp0_awqos[3:0]	maxigp0awqos[3:0]	O	Wr Quality Of Service (QOS) bits. 4'hf is highest priority, 4'h0 is lowest priority.
P285	m_axi_gp0_arqos[3:0]	maxigp0arqos[3:0]	O	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.

M_AXI_GP1 Signals

Table 2-35: **PS Master, PL Slave – General Purpose Port – M_AXI_GP1 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P286	m_axi_gp1_aclk	maxigp1aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P288	m_axi_gp1_awid[c_m_axi_gp1_thread_id_width-1:0]	maxigp1awid[11:0]	O	Write ID.
P289	m_axi_gp1_awaddr[31:0]	maxigp1awaddr[31:0]	O	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P290	m_axi_gp1_awlen[3:0]	maxigp1awlen[3:0]	O	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P291	m_axi_gp1_awsize[2:0]	maxigp1awsize[1:0]	O	Burst size. m_axi_gp1_awsize[2] is not used.
P292	m_axi_gp1_awburst[1:0]	maxigp1awburst[1:0]	O	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P293	m_axi_gp1_awlock[1:0]	maxigp1awlock[1:0]	O	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P294	m_axi_gp1_awcache[3:0]	maxigp1awcache[3:0]	O	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.

Table 2-35: **PS Master, PL Slave – General Purpose Port – M_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P295	m_axi_gp1_awprot[2:0]	maxigp1awprot[2:0]	O	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P296	m_axi_gp1_awvalid	maxigp1awvalid	O	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.
P297	m_axi_gp1_awready	maxigp1awready	I	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P298	m_axi_gp1_wid[c_m_axi_gp1_thread_id_width-1:0]	maxigp1wid[11:0]	O	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P299	m_axi_gp1_wdata[31:0]	maxigp1wdata[31:0]	O	Write data.
P300	m_axi_gp1_wstrb[3:0]	maxigp1wstrb[3:0]	O	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds to WDATA[(8 × *n*) + 7:(8 × *n*)].
P301	m_axi_gp1_wlast	maxigp1wlast	O	Write last. This signal indicates the last transfer in a write burst.
P302	m_axi_gp1_wvalid	maxigp1wvalid	O	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.
P303	m_axi_gp1_wready	maxigp1wready	I	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready

Table 2-35: **PS Master, PL Slave – General Purpose Port – M_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P304	m_axi_gp1_bid[c_m_axi_gp1_thread_id_width-1:0]	maxigp1bid[11:0]	I	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P305	m_axi_gp1_bresp[1:0]	maxigp1bresp[1:0]	I	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P306	m_axi_gp1_bvalid	maxigp1bvalid	I	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P307	m_axi_gp1_bready	maxigp1bready	O	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P308	m_axi_gp1_arid[c_m_axi_gp1_thread_id_width-1:0]	maxigp1arid[11:0]	O	Read address ID. This signal is the identification tag for the read address group of signals.
P309	m_axi_gp1_araddr[31:0]	maxigp1araddr[31:0]	O	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P310	m_axi_gp1_arlen[3:0]	maxigp1arlen[3:0]	O	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
P311	m_axi_gp1_arsize[2:0]	maxigp1arsize[1:0]	O	Burst size. This signal indicates the size of each transfer in the burst. m_axi_gp1_arsize[2] is not used.
P312	m_axi_gp1_arburst[1:0]	maxigp1arburst[1:0]	O	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P313	m_axi_gp1_arlock[1:0]	maxigp1arlock[1:0]	O	Lock type. This signal provides additional information about the atomic characteristics of the transfer.

Table 2-35: **PS Master, PL Slave – General Purpose Port – M_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P314	m_axi_gp1_arcache[3:0]	maxigp1arcache[3:0]	O	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P315	m_axi_gp1_arprot[2:0]	maxigp1arprot[2:0]	O	Protection type. This signal provides protection unit information for the transaction.
P316	m_axi_gp1_arvalid	maxigp1arvalid	O	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal arready is High. • 1: Address and control information valid • 0: Address and control information not valid
P317	m_axi_gp1_arready	maxigp1arready	I	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P318	m_axi_gp1_rid[c_m_axi_gp1_thread_id_width-1:0]	maxigp1rid[11:0]	I	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P319	m_axi_gp1_rdata[31:0]	maxigp1rdata[31:0]	I	Read data.
P320	m_axi_gp1_rresp[1:0]	maxigp1rresp[1:0]	I	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P321	m_axi_gp1_rlast	maxigp1rlast	I	Read last. This signal indicates the last transfer in a read burst.
P322	m_axi_gp1_rvalid	maxigp1rvalid	I	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available

Table 2-35: **PS Master, PL Slave – General Purpose Port – M_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P323	m_axi_gp1_rready	maxigp1rready	O	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P324	m_axi_gp1_awqos[3:0]	maxigp1awqos[3:0]	O	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P325	m_axi_gp1_arqos[3:0]	maxigp1arqos[3:0]	O	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.

S_AXI_GP0 Signals

Table 2-36: **PS Slave, PL Master – General Purpose Port – S_AXI_GP0 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P326	s_axi_gp0_aclk	saxigp0aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P328	s_axi_gp0_awid[c_s_axi_gp0_id_width-1:0]	saxigp0awid[5:0]	I	Write ID.
P329	s_axi_gp0_awaddr[31:0]	saxigp0awaddr[31:0]	I	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P330	s_axi_gp0_awlen[3:0]	saxigp0awlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P331	s_axi_gp0_awsize[2:0]	saxigp0awsize[1:0]	I	Burst size. s_axi_gp0_awsize[2] is not used.
P332	s_axi_gp0_awburst[1:0]	saxigp0awburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P333	s_axi_gp0_awlock[1:0]	saxigp0awlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.

Table 2-36: **PS Slave, PL Master – General Purpose Port – S_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P334	s_axi_gp0_awcache[3:0]	saxigp0awcache[3:0]	I	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P335	s_axi_gp0_awprot[2:0]	saxigp0awprot[2:0]	I	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P336	s_axi_gp0_awvalid	saxigp0awvalid	I	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.
P337	s_axi_gp0_awready	saxigp0awready	O	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P338	s_axi_gp0_wid[c_s_axi_gp0_id_width-1:0]	saxigp0wid[5:0]	I	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P339	s_axi_gp0_wdata[31:0]	saxigp0wdata[31:0]	I	Write data.
P340	s_axi_gp0_wstrb[3:0]	saxigp0wstrb[3:0]	I	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore `wstrb[n]` corresponds to WDATA[(8 × *n*) + 7:(8 × *n*)].
P341	s_axi_gp0_wlast	saxigp0wlast	I	Write last. This signal indicates the last transfer in a write burst.
P342	s_axi_gp0_wvalid	saxigp0wvalid	I	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.

Table 2-36: **PS Slave, PL Master – General Purpose Port – S_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P343	s_axi_gp0_wready	saxigp0wready	O	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P344	s_axi_gp0_bid[c_s_axi_gp0_id_width-1:0]	saxigp0bid[5:0]	O	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P345	s_axi_gp0_bresp[1:0]	saxigp0bresp[1:0]	O	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P346	s_axi_gp0_bvalid	saxigp0bvalid	O	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P347	s_axi_gp0_bready	saxigp0bready	I	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P348	s_axi_gp0_arid[c_s_axi_gp0_id_width-1:0]	saxigp0arid[5:0]	I	Read address ID. This signal is the identification tag for the read address group of signals.
P349	s_axi_gp0_araddr[31:0]	saxigp0araddr[31:0]	I	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P350	s_axi_gp0_arlen[3:0]	saxigp0arlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
P351	s_axi_gp0_arsize[2:0]	saxigp0arsize[1:0]	I	Burst size. This signal indicates the size of each transfer in the burst. `s_axi_gp0_arsize[2]` is not used.

Table 2-36: **PS Slave, PL Master – General Purpose Port – S_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P352	s_axi_gp0_arburst[1:0]	saxigp0arburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P353	s_axi_gp0_arlock[1:0]	saxigp0arlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P354	s_axi_gp0_arcache[3:0]	saxigp0arcache[3:0]	I	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P355	s_axi_gp0_arprot[2:0]	saxigp0arprot[2:0]	I	Protection type. This signal provides protection unit information for the transaction.
P356	s_axi_gp0_arvalid	saxigp0arvalid	I	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal `arready` is High. • 1: Address and control information valid • 0: Address and control information not valid
P357	s_axi_gp0_arready	saxigp0arready	O	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P358	s_axi_gp0_rid[c_s_axi_gp0_id_width-1:0]	saxigp0rid[5:0]	O	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P359	s_axi_gp0_rdata[31:0]	saxigp0rdata[31:0]	O	Read data.
P360	s_axi_gp0_rresp[1:0]	saxigp0rresp[1:0]	O	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P361	s_axi_gp0_rlast	saxigp0rlast	O	Read last. This signal indicates the last transfer in a read burst.

Table 2-36: **PS Slave, PL Master – General Purpose Port – S_AXI_GP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P362	s_axi_gp0_rvalid	saxigp0rvalid	O	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P363	s_axi_gp0_rready	saxigp0rready	I	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P364	s_axi_gp0_awqos[3:0]	saxigp0awqos[3:0]	I	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P365	s_axi_gp0_arqos[3:0]	saxigp0arqos[3:0]	I	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.

S_AXI_GP1 Signals

Table 2-37: **PS Slave, PL Master – General Purpose Port – S_AXI_GP1 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P366	s_axi_gp1_aclk	saxigp1aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P368	s_axi_gp1_awid[c_s_axi_gp1_id_width-1:0]	saxigp1awid[5:0]	I	Write ID.
P369	s_axi_gp1_awaddr[31:0]	saxigp1awaddr[31:0]	I	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P370	s_axi_gp1_awlen[3:0]	saxigp1awlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P371	s_axi_gp1_awsize[2:0]	saxigp1awsize[1:0]	I	Burst size. s_axi_gp1_awsize[2] is not used.

Table 2-37: **PS Slave, PL Master – General Purpose Port – S_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P372	s_axi_gp1_awburst[1:0]	saxigp1awburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P373	s_axi_gp1_awlock[1:0]	saxigp1awlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P374	s_axi_gp1_awcache[3:0]	saxigp1awcache[3:0]	I	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P375	s_axi_gp1_awprot[2:0]	saxigp1awprot[2:0]	I	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P376	s_axi_gp1_awvalid	saxigp1awvalid	I	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.
P377	s_axi_gp1_awready	saxigp1awready	O	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P378	s_axi_gp1_wid[c_s_axi_gp1_id_width-1:0]	saxigp1wid[5:0]	I	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P379	s_axi_gp1_wdata[31:0]	saxigp1wdata[31:0]	I	Write data.
P380	s_axi_gp1_wstrb[3:0]	saxigp1wstrb[3:0]	I	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds toWDATA[(8 × *n*) + 7:(8 × *n*)].
P381	s_axi_gp1_wlast	saxigp1wlast	I	Write last. This signal indicates the last transfer in a write burst.

Table 2-37: **PS Slave, PL Master – General Purpose Port – S_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P382	s_axi_gp1_wvalid	saxigp1wvalid	I	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.
P383	s_axi_gp1_wready	saxigp1wready	O	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P384	s_axi_gp1_bid[c_s_axi_gp1_id_width-1:0]	saxigp1bid[5:0]	O	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P385	s_axi_gp1_bresp[1:0]	saxigp1bresp[1:0]	O	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P386	s_axi_gp1_bvalid	saxigp1bvalid	O	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P387	s_axi_gp1_bready	saxigp1bready	I	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P388	s_axi_gp1_arid[c_s_axi_gp1_id_width-1:0]	saxigp1arid[5:0]	I	Read address ID. This signal is the identification tag for the read address group of signals.
P389	s_axi_gp1_araddr[31:0]	saxigp1araddr[31:0]	I	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P390	s_axi_gp1_arlen[3:0]	saxigp1arlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.

Table 2-37: **PS Slave, PL Master – General Purpose Port – S_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P391	s_axi_gp1_arsize[2:0]	saxigp1arsize[1:0]	I	Burst size. This signal indicates the size of each transfer in the burst. s_axi_gp1_arsize[2] is not used.
P392	s_axi_gp1_arburst[1:0]	saxigp1arburst[1:0]	I	Burst type. The burst type coupled with the size information detail show the address for each transfer within the burst is calculated.
P393	s_axi_gp1_arlock[1:0]	saxigp1arlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P394	s_axi_gp1_arcache[3:0]	saxigp1arcache[3:0]	I	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P395	s_axi_gp1_arprot[2:0]	saxigp1arprot[2:0]	I	Protection type. This signal provides protection unit information for the transaction.
P396	s_axi_gp1_arvalid	saxigp1arvalid	I	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal arready is High. • 1: Address and control information valid • 0: Address and control information not valid
P397	s_axi_gp1_arready	saxigp1arready	O	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P398	s_axi_gp1_rid[c_s_axi_gp1_id_width-1:0]	saxigp1rid[5:0]	O	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P399	s_axi_gp1_rdata[31:0]	saxigp1rdata[31:0]	O	Read data.
P400	s_axi_gp1_rresp[1:0]	saxigp1rresp[1:0]	O	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.

Table 2-37: **PS Slave, PL Master – General Purpose Port – S_AXI_GP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P401	s_axi_gp1_rlast	saxigp1rlast	O	Read last. This signal indicates the last transfer in a read burst.
P402	s_axi_gp1_rvalid	saxigp1rvalid	O	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P403	s_axi_gp1_rready	saxigp1rready	I	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P404	s_axi_gp1_awqos[3:0]	saxigp1awqos[3:0]	I	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P405	s_axi_gp1_arqos[3:0]	saxigp1arqos[3:0]	I	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.

S_AXI_ACP Signals

Table 2-38: **PS Slave, PL Master – Accelerator Coherence Port – S_AXI_ACP Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P406	s_axi_acp_aclk	saxiacpaclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P408	s_axi_acp_awid[c_s_axi_acp_id_width-1:0]	saxiacpawid[2:0]	I	Write ID.
P409	s_axi_acp_awaddr[31:0]	saxiacpawaddr[31:0]	I	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P410	s_axi_acp_awlen[3:0]	saxiacpawlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P411	s_axi_acp_awsize[2:0]	saxiacpawsize[1:0]	I	Burst size. s_axi_acp_awsize[2] is not used.

Table 2-38: **PS Slave, PL Master – Accelerator Coherence Port – S_AXI_ACP Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P412	s_axi_acp_awburst[1:0]	saxiacpawburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P413	s_axi_acp_awlock[1:0]	saxiacpawlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P414	s_axi_acp_awcache[3:0]	saxiacpawcache[3:0]	I	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P415	s_axi_acp_awprot[2:0]	saxiacpawprot[2:0]	I	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P416	s_axi_acp_awvalid	saxiacpawvalid	I	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal `awready` goes High.
P417	s_axi_acp_awready	saxiacpawready	O	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P418	s_axi_acp_wid[c_s_axi_acp_id_width-1:0]	saxiacpwid[2:0]	I	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P419	s_axi_acp_wdata[63:0]	saxiacpwdata[63:0]	I	Write data.
P420	s_axi_acp_wstrb[7:0]	saxiacpwstrb[7:0]	I	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds toWDATA[(8 × *n*) + 7:(8 × *n*)].
P421	s_axi_acp_wlast	saxiacpwlast	I	Write last. This signal indicates the last transfer in a write burst.

Table 2-38: **PS Slave, PL Master – Accelerator Coherence Port – S_AXI_ACP Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P422	s_axi_acp_wvalid	saxiacpwvalid	I	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.
P423	s_axi_acp_wready	saxiacpwready	O	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P424	s_axi_acp_bid[c_s_axi_acp_id_width-1:0]	saxiacpbid[2:0]	O	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P425	s_axi_acp_bresp[1:0]	saxiacpbresp[1:0]	O	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P426	s_axi_acp_bvalid	saxiacpbvalid	O	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P427	s_axi_acp_bready	saxiacpbready	I	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P428	s_axi_acp_arid[c_s_axi_acp_id_width-1:0]	saxiacparid[2:0]	I	Read address ID. This signal is the identification tag for the read address group of signals.
P429	s_axi_acp_araddr[31:0]	saxiacparaddr[31:0]	I	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P430	s_axi_acp_arlen[3:0]	saxiacparlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.

Table 2-38: **PS Slave, PL Master – Accelerator Coherence Port – S_AXI_ACP Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P431	s_axi_acp_arsize[2:0]	saxiacparsize[1:0]	I	Burst size. This signal indicates the size of each transfer in the burst. s_axi_acp_arsize[2] is not used.
P432	s_axi_acp_arburst[1:0]	saxiacparburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P433	s_axi_acp_arlock[1:0]	saxiacparlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P434	s_axi_acp_arcache[3:0]	saxiacparcache[3:0]	I	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P435	s_axi_acp_arprot[2:0]	saxiacparprot[2:0]	I	Protection type. This signal provides protection unit information for the transaction.
P436	s_axi_acp_arvalid	saxiacparvalid	I	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal arready is High. • 1: Address and control information valid • 0: Address and control information not valid
P437	s_axi_acp_arready	saxiacparready	O	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P438	s_axi_acp_rid[c_s_axi_acp_id_width-1:0]	saxiacprid[2:0]	O	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P439	s_axi_acp_rdata[63:0]	saxiacprdata[63:0]	O	Read data.
P440	s_axi_acp_rresp[1:0]	saxiacprresp[1:0]	O	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.

Table 2-38: **PS Slave, PL Master – Accelerator Coherence Port – S_AXI_ACP Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P441	s_axi_acp_rlast	saxiacprlast	O	Read last. This signal indicates the last transfer in a read burst.
P442	s_axi_acp_rvalid	saxiacprvalid	O	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P443	s_axi_acp_rready	saxiacprready	I	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P444	s_axi_acp_awqos[3:0]	saxiacpawqos[3:0]	I	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P445	s_axi_acp_arqos[3:0]	saxiacparqos[3:0]	I	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P446	s_axi_acp_awuser[4:0]	saxiacparuser[4:0]	I	User pins to inform the snoop control unit (SCU) about the cacheable nature of the transaction-sharable inner cache policy.
P447	s_axi_acp_aruser[4:0]	saxiacparuser[4:0]	I	User pins to inform the SCU about the cacheable nature of the transaction-sharable inner cache policy.

S_AXI_HP0 Signals

Table 2-39: **PS Slave, PL Master – High Performance Port – S_AXI_HP0 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P447	s_axi_hp0_aclk	saxihp0aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P449	s_axi_hp0_awid[c_s_axi_hp0_id_width-1:0]	saxihp0awid[5:0]	I	Write ID.
P450	s_axi_hp0_awaddr[31:0]	saxihp0awaddr[31:0]	I	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.

Table 2-39: **PS Slave, PL Master – High Performance Port – S_AXI_HP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P451	s_axi_hp0_awlen[3:0]	saxihp0awlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P452	s_axi_hp0_awsize[2:0]	saxihp0awsize[1:0]	I	Burst size. s_axi_hp0_awsize[2] is not used.
P453	s_axi_hp0_awburst[1:0]	saxihp0awburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P454	s_axi_hp0_awlock[1:0]	saxihp0awlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P455	s_axi_hp0_awcache[3:0]	saxihp0awcache[3:0]	I	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P456	s_axi_hp0_awprot[2:0]	saxihp0awprot[2:0]	I	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P457	s_axi_hp0_awvalid	saxihp0awvalid	I	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.
P458	s_axi_hp0_awready	saxihp0awready	O	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.

Table 2-39: **PS Slave, PL Master – High Performance Port – S_AXI_HP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P459	s_axi_hp0_wid[c_s_axi_hp0_id_width-1:0]	saxihp0wid[5:0]	I	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P460	s_axi_hp0_wdata[c_s_axi_hp0_data_width-1:0]	saxihp0wdata[63:0]	I	Write data.
P461	s_axi_hp0_wstrb[(c_s_axi_hp0_data_width/8)-1:0]	saxihp0wstrb[7:0]	I	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds toWDATA[(8 × *n*) + 7:(8 × *n*)].
P462	s_axi_hp0_wlast	saxihp0wlast	I	Write last. This signal indicates the last transfer in a write burst.
P463	s_axi_hp0_wvalid	saxihp0wvalid	I	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.
P464	s_axi_hp0_wready	saxihp0wready	O	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P465	s_axi_hp0_bid[c_s_axi_hp0_id_width-1:0]	saxihp0bid[5:0]	O	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P466	s_axi_hp0_bresp[1:0]	saxihp0bresp[1:0]	O	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P467	s_axi_hp0_bvalid	saxihp0bvalid	O	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P468	s_axi_hp0_bready	saxihp0bready	I	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready

Table 2-39: **PS Slave, PL Master – High Performance Port – S_AXI_HP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P469	s_axi_hp0_arid[c_s_axi_hp0_id_width-1:0]	saxihp0arid[5:0]	I	Read address ID. This signal is the identification tag for the read address group of signals.
P470	s_axi_hp0_araddr[31:0]	saxihp0araddr[31:0]	I	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P471	s_axi_hp0_arlen[3:0]	saxihp0arlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
P472	s_axi_hp0_arsize[2:0]	saxihp0arsize[1:0]	I	Burst size. This signal indicates the size of each transfer in the burst. s_axi_hp0_arsize[2] is not used.
P473	s_axi_hp0_arburst[1:0]	saxihp0arburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P474	s_axi_hp0_arlock[1:0]	saxihp0arlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P475	s_axi_hp0_arcache[3:0]	saxihp0arcache[3:0]	I	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P476	s_axi_hp0_arprot[2:0]	saxihp0arprot[2:0]	I	Protection type. This signal provides protection unit information for the transaction.
P477	s_axi_hp0_arvalid	saxihp0arvalid	I	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal arready is High. • 1: Address and control information valid • 0: Address and control information not valid

Table 2-39: **PS Slave, PL Master – High Performance Port – S_AXI_HP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P478	s_axi_hp0_arready	saxihp0arready	O	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P479	s_axi_hp0_rid[c_s_axi_hp0_id_width-1:0]	saxihp0rid[5:0]	O	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P480	s_axi_hp0_rdata[c_s_axi_hp0_data_width-1:0]	saxihp0rdata[63:0]	O	Read data.
P481	s_axi_hp0_rresp[1:0]	saxihp0rresp[1:0]	O	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P482	s_axi_hp0_rlast	saxihp0rlast	O	Read last. This signal indicates the last transfer in a read burst.
P483	s_axi_hp0_rvalid	saxihp0rvalid	O	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P484	s_axi_hp0_rready	saxihp0rready	I	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P485	s_axi_hp0_awqos[3:0]	saxihp0awqos[3:0]	I	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P486	s_axi_hp0_arqos[3:0]	saxihp0arqos[3:0]	I	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P487	s_axi_hp0_wcount[7:0]	saxihp0wcount[7:0]	O	Write Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P488	s_axi_hp0_wrissuecap1en	saxihp0wrissuecap1en	I	Write Issuing capability of AXI FIFO Interface (AFI). 1-selects wrIssuing Cap advanced peripheral bus (APB) register 1.
P489	s_axi_hp0_wacount[7:0]	saxihp0wacount[7:0]	O	

Table 2-39: **PS Slave, PL Master – High Performance Port – S_AXI_HP0 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P490	s_axi_hp0_rcount[7:0]	saxihp0rcount[7:0]	O	Read Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P491	s_axi_hp0_racount[7:0]	saxihp0racount[7:0]	O	
P492	s_axi_hp0_rdissuecap1en	saxihp0rdissuecap1en	I	Read Issuing capability of AXI FIFO Interface (AFI). 1-selects rd Issuing Cap APB register 1.

S_AXI_HP1 Signals

Table 2-40: **PS Slave, PL Master – High Performance Port – S_AXI_HP1 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P493	s_axi_hp1_aclk	saxihp1aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P495	s_axi_hp1_awid[c_s_axi_hp1_id_width-1:0]	saxihp1awid[5:0]	I	Write ID.
P496	s_axi_hp1_awaddr[31:0]	saxihp1awaddr[31:0]	I	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P497	s_axi_hp1_awlen[3:0]	saxihp1awlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P498	s_axi_hp1_awsize[2:0]	saxihp1awsize[1:0]	I	Burst size. s_axi_hp1_awsize[2] is not used.
P499	s_axi_hp1_awburst[1:0]	saxihp1awburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P500	s_axi_hp1_awlock[1:0]	saxihp1awlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.

Table 2-40: **PS Slave, PL Master – High Performance Port – S_AXI_HP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P491	s_axi_hp1_awcache[3:0]	saxihp1awcache[3:0]	I	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P492	s_axi_hp1_awprot[2:0]	saxihp1awprot[2:0]	I	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P493	s_axi_hp1_awvalid	saxihp1awvalid	I	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.
P494	s_axi_hp1_awready	saxihp1awready	O	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P495	s_axi_hp1_wid[c_s_axi_hp1_id_width-1:0]	saxihp1wid[5:0]	I	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P496	s_axi_hp1_wdata[c_s_axi_hp1_data_width-1:0]	saxihp1wdata[63:0]	I	Write data.
P497	s_axi_hp1_wstrb[(c_s_axi_hp1_data_width/8)-1:0]	saxihp1wstrb[7:0]	I	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds toWDATA[(8 × *n*) + 7:(8 × *n*)].
P498	s_axi_hp1_wlast	saxihp1wlast	I	Write last. This signal indicates the last transfer in a write burst.
P499	s_axi_hp1_wvalid	saxihp1wvalid	I	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.

Table 2-40: **PS Slave, PL Master – High Performance Port – S_AXI_HP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P500	s_axi_hp1_wready	saxihp1wready	O	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P501	s_axi_hp1_bid[c_s_axi_hp1_id_width-1:0]	saxihp1bid[5:0]	O	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P502	s_axi_hp1_bresp[1:0]	saxihp1bresp[1:0]	O	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P503	s_axi_hp1_bvalid	saxihp1bvalid	O	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P504	s_axi_hp1_bready	saxihp1bready	I	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P505	s_axi_hp1_arid[c_s_axi_hp1_id_width-1:0]	saxihp1arid[5:0]	I	Read address ID. This signal is the identification tag for the read address group of signals.
P506	s_axi_hp1_araddr[31:0]	saxihp1araddr[31:0]	I	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P507	s_axi_hp1_arlen[3:0]	saxihp1arlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
P508	s_axi_hp1_arsize[2:0]	saxihp1arsize[1:0]	I	Burst size. This signal indicates the size of each transfer in the burst. s_axi_hp1_arsize[2] is not used.

Table 2-40: **PS Slave, PL Master – High Performance Port – S_AXI_HP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P509	s_axi_hp1_arburst[1:0]	saxihp1arburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P510	s_axi_hp1_arlock[1:0]	saxihp1arlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P511	s_axi_hp1_arcache[3:0]	saxihp1arcache[3:0]	I	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P512	s_axi_hp1_arprot[2:0]	saxihp1arprot[2:0]	I	Protection type. This signal provides protection unit information for the transaction.
P513	s_axi_hp1_arvalid	saxihp1arvalid	I	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal aready is High. • 1: Address and control information valid • 0: Address and control information not valid
P514	s_axi_hp1_arready	saxihp1arready	O	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P515	s_axi_hp1_rid[c_s_axi_hp1_id_width-1:0]	saxihp1rid[5:0]	O	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P516	s_axi_hp1_rdata[c_s_axi_hp1_data_width-1:0]	saxihp1rdata[63:0]	O	Read data
P517	s_axi_hp1_rresp[1:0]	saxihp1rresp[1:0]	O	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P518	s_axi_hp1_rlast	saxihp1rlast	O	Read last. This signal indicates the last transfer in a read burst.

Table 2-40: **PS Slave, PL Master – High Performance Port – S_AXI_HP1 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P519	s_axi_hp1_rvalid	saxihp1rvalid	O	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P520	s_axi_hp1_rready	saxihp1rready	I	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P521	s_axi_hp1_awqos[3:0]	saxihp1awqos[3:0]	I	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P522	s_axi_hp1_arqos[3:0]	saxihp1arqos[3:0]	I	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P523	s_axi_hp1_wcount[7:0]	saxihp1wcount[7:0]	O	Write Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P524	s_axi_hp1_wrissuecap1en	saxihp1wrissuecap1en	I	Write Issuing capability of AFI. 1-selects wrIssuing Cap APB register 1.
P525	s_axi_hp1_wacount[7:0]	saxihp1wacount[7:0]	O	
P526	s_axi_hp1_rcount[7:0]	saxihp1rcount[7:0]	O	Read Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P527	s_axi_hp1_racount[7:0]	saxihp1racount[7:0]	O	
P528	s_axi_hp1_rdissuecap1en	saxihp1rdissuecap1en	I	Read Issuing capability of AFI. 1-selects rd Issuing Cap APB register 1.

S_AXI_HP2 Signals

Table 2-41: **PS Slave, PL Master – High Performance Port – S_AXI_HP2 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P529	s_axi_hp2_aclk	saxihp2aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P531	s_axi_hp2_awid[c_s_axi_hp2_id_width-1:0]	saxihp2awid[5:0]	I	Write ID.

Table 2-41: **PS Slave, PL Master – High Performance Port – S_AXI_HP2 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P532	s_axi_hp2_awaddr[31:0]	saxihp2awaddr[31:0]	I	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P533	s_axi_hp2_awlen[3:0]	saxihp2awlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P534	s_axi_hp2_awsize[2:0]	saxihp2awsize[1:0]	I	Burst size. s_axi_hp2_awsize[2] is not used.
P535	s_axi_hp2_awburst[1:0]	saxihp2awburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P536	s_axi_hp2_awlock[1:0]	saxihp2awlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P537	s_axi_hp2_awcache[3:0]	saxihp2awcache[3:0]	I	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P538	s_axi_hp2_awprot[2:0]	saxihp2awprot[2:0]	I	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P539	s_axi_hp2_awvalid	saxihp2awvalid	I	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.

Table 2-41: **PS Slave, PL Master – High Performance Port – S_AXI_HP2 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P540	s_axi_hp2_awready	saxihp2awready	O	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P541	s_axi_hp2_wid[c_s_axi_hp2_id_width-1:0]	saxihp2wid[5:0]	I	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P542	s_axi_hp2_wdata[c_s_axi_hp2_data_width-1:0]	saxihp2wdata[63:0]	I	Write data.
P543	s_axi_hp2_wstrb[(c_s_axi_hp2_data_width/8)-1:0]	saxihp2wstrb[7:0]	I	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds to WDATA[(8 × *n*) + 7:(8 × *n*)],
P544	s_axi_hp2_wlast	saxihp2wlast	I	Write last. This signal indicates the last transfer in a write burst.
P545	s_axi_hp2_wvalid	saxihp2wvalid	I	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.
P546	s_axi_hp2_wready	saxihp2wready	O	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P547	s_axi_hp2_bid[c_s_axi_hp2_id_width-1:0]	saxihp2bid[5:0]	O	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P548	s_axi_hp2_bresp[1:0]	saxihp2bresp[1:0]	O	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P549	s_axi_hp2_bvalid	saxihp2bvalid	O	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available

Table 2-41: **PS Slave, PL Master – High Performance Port – S_AXI_HP2 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P550	s_axi_hp2_bready	saxihp2bready	I	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P551	s_axi_hp2_arid[c_s_axi_hp2_id_width-1:0]	saxihp2arid[5:0]	I	Read address ID. This signal is the identification tag for the read address group of signals.
P552	s_axi_hp2_araddr[31:0]	saxihp2araddr[31:0]	I	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P553	s_axi_hp2_arlen[3:0]	saxihp2arlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.
P554	s_axi_hp2_arsize[2:0]	saxihp2arsize[1:0]	I	Burst size. This signal indicates the size of each transfer in the burst. s_axi_hp2_arsize[2] is not used.
P555	s_axi_hp2_arburst[1:0]	saxihp2arburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P556	s_axi_hp2_arlock[1:0]	saxihp2arlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P557	s_axi_hp2_arcache[3:0]	saxihp2arcache[3:0]	I	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P558	s_axi_hp2_arprot[2:0]	saxihp2arprot[2:0]	I	Protection type. This signal provides protection unit information for the transaction.

Table 2-41: **PS Slave, PL Master – High Performance Port – S_AXI_HP2 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P559	s_axi_hp2_arvalid	saxihp2arvalid	I	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal `arready` is High. • 1: Address and control information valid • 0: Address and control information not valid
P560	s_axi_hp2_arready	saxihp2arready	O	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P561	s_axi_hp2_rid[c_s_axi_hp2_id_width-1:0]	saxihp2rid[5:0]	O	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P562	s_axi_hp2_rdata[c_s_axi_hp2_data_width-1:0]	saxihp2rdata[63:0]	O	Read data.
P563	s_axi_hp2_rresp[1:0]	saxihp2rresp[1:0]	O	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P564	s_axi_hp2_rlast	saxihp2rlast	O	Read last. This signal indicates the last transfer in a read burst.
P565	s_axi_hp2_rvalid	saxihp2rvalid	O	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P566	s_axi_hp2_rready	saxihp2rready	I	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P567	s_axi_hp2_awqos[3:0]	saxihp2awqos[3:0]	I	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P568	s_axi_hp2_arqos[3:0]	saxihp2arqos[3:0]	I	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.

Table 2-41: **PS Slave, PL Master – High Performance Port – S_AXI_HP2 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P569	s_axi_hp2_wcount[7:0]	saxihp2wcount[7:0]	O	Write Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P570	s_axi_hp2_wrissuecap1en	saxihp2wrissuecap1en	I	Write Issuing capability of AFI. 1-selects wrIssuing Cap APB register 1.
P571	s_axi_hp2_wacount[7:0]	saxihp2wacount[7:0]	O	
P572	s_axi_hp2_rcount[7:0]	saxihp2rcount[7:0]	O	Read Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P573	s_axi_hp2_racount[7:0]	saxihp2racount[7:0]	O	
P574	s_axi_hp2_rdissuecap1en	saxihp2rdissuecap1en	I	Read Issuing capability of AFI. 1-selects rd Issuing Cap APB register 1.

S_AXI_HP3 Signals

Table 2-42: **PS Slave, PL Master – High Performance Port – S_AXI_HP3 Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P575	s_axi_hp3_aclk	saxihp3aclk	I	Global clock signal. All signals are sampled on the rising edge of the global clock.
P577	s_axi_hp3_awid[c_s_axi_hp3_id_width-1:0]	saxihp3awid[5:0]	I	Write ID.
P578	s_axi_hp3_awaddr[31:0]	saxihp3awaddr[31:0]	I	Write address. The write address bus gives the address of the first transfer in a write burst transaction. The associated control signals are used to determine the addresses of the remaining transfers in the burst.
P579	s_axi_hp3_awlen[3:0]	saxihp3awlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address. This signal indicates the size of each transfer in the burst. Byte lane strobes indicate exactly which byte lanes to update.
P580	s_axi_hp3_awsize[2:0]	saxihp3awsize[1:0]	I	Burst size. s_axi_hp3_awsize[2] is not used.
P581	s_axi_hp3_awburst[1:0]	saxihp3awburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.

Table 2-42: **PS Slave, PL Master – High Performance Port – S_AXI_HP3 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P582	s_axi_hp3_awlock[1:0]	saxihp3awlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P583	s_axi_hp3_awcache[3:0]	saxihp3awcache[3:0]	I	Cache type. This signal indicates the bufferable cacheable write-through write back and allocates attributes of the transaction.
P584	s_axi_hp3_awprot[2:0]	saxihp3awprot[2:0]	I	Protection type. This signal indicates the normal privileged or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
P585	s_axi_hp3_awvalid	saxihp3awvalid	I	Write address valid. This signal indicates that valid write address and control information are available: • 1: Address and control information available • 0: Address and control information not available The address and control information remain stable until the address acknowledge signal awready goes High.
P586	s_axi_hp3_awready	saxihp3awready	O	Write address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready.
P587	s_axi_hp3_wid[c_s_axi_hp3_id_width-1:0]	saxihp3wid[5:0]	I	Write ID tag. This signal is the ID tag of the write data transfer. The WID value must match the AWID value of the write transaction.
P588	s_axi_hp3_wdata[c_s_axi_hp3_data_width-1:0]	saxihp3wdata[63:0]	I	Write data.
P589	s_axi_hp3_wstrb[(c_s_axi_hp3_data_width/8)-1:0]	saxihp3wstrb[7:0]	I	Write strobes. This signal indicates which byte lanes to update in memory. There is one write strobe for each eight bits of the write data bus. Therefore wstrb[n] corresponds to WDATA[(8 × *n*) + 7:(8 × *n*)].
P590	s_axi_hp3_wlast	saxihp3wlast	I	Write last. This signal indicates the last transfer in a write burst.

Table 2-42: **PS Slave, PL Master – High Performance Port – S_AXI_HP3 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P591	s_axi_hp3_wvalid	saxihp3wvalid	I	Write valid. This signal indicates that valid write data and strobes are available. • 1: Write data and strobes available • 0: Write data and strobes not available.
P592	s_axi_hp3_wready	saxihp3wready	O	Write ready. This signal indicates that the slave can accept the write data. • 1: Slave ready • 0: Slave not ready
P593	s_axi_hp3_bid[c_s_axi_hp3_id_width-1:0]	saxihp3bid[5:0]	O	Response ID. The identification tag of the write response. The BID value must match the AWID value of the write transaction to which the slave is responding.
P594	s_axi_hp3_bresp[1:0]	saxihp3bresp[1:0]	O	Write response. This signal indicates the status of the write transaction. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.
P595	s_axi_hp3_bvalid	saxihp3bvalid	O	Write response valid. This signal indicates that a valid write response is available. • 1: Write response available • 0: Write response not available
P596	s_axi_hp3_bready	saxihp3bready	I	Response ready. This signal indicates that the master can accept the response information. • 1: Master ready • 0: Master not ready
P597	s_axi_hp3_arid[c_s_axi_hp3_id_width-1:0]	saxihp3arid[5:0]	I	Read address ID. This signal is the identification tag for the read address group of signals.
P598	s_axi_hp3_araddr[31:0]	saxihp3araddr[31:0]	I	Read address. The read address bus gives the initial address of a read burst transaction. Only the start address of the burst is provided and the control signals that are issued alongside the address detail how the address is calculated for the remaining transfers in the burst.
P599	s_axi_hp3_arlen[3:0]	saxihp3arlen[3:0]	I	Burst length. The burst length gives the exact number of transfers in a burst. This information determines the number of data transfers associated with the address.

Table 2-42: **PS Slave, PL Master – High Performance Port – S_AXI_HP3 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P600	s_axi_hp3_arsize[2:0]	saxihp3arsize[1:0]	I	Burst size. This signal indicates the size of each transfer in the burst. s_axi_hp3_arsize[2] is not used.
P601	s_axi_hp3_arburst[1:0]	saxihp3arburst[1:0]	I	Burst type. The burst type coupled with the size information details how the address for each transfer within the burst is calculated.
P602	s_axi_hp3_arlock[1:0]	saxihp3arlock[1:0]	I	Lock type. This signal provides additional information about the atomic characteristics of the transfer.
P603	s_axi_hp3_arcache[3:0]	saxihp3arcache[3:0]	I	Cache type. This signal provides additional information about the cacheable characteristics of the transfer.
P604	s_axi_hp3_arprot[2:0]	saxihp3arprot[2:0]	I	Protection type. This signal provides protection unit information for the transaction.
P605	s_axi_hp3_arvalid	saxihp3arvalid	I	Read address valid. This signal indicates when High that the read address and control information is valid and remains stable until the address acknowledge signal arready is High. • 1: Address and control information valid • 0: Address and control information not valid
P606	s_axi_hp3_arready	saxihp3arready	O	Read address ready. This signal indicates that the slave is ready to accept an address and associated control signals. • 1: Slave ready • 0: Slave not ready
P607	s_axi_hp3_rid[c_s_axi_hp3_id_width-1:0]	saxihp3rid[5:0]	O	Read ID tag. This signal is the ID tag of the read data group of signals. The RID value is generated by the slave and must match the ARID value of the read transaction to which it is responding.
P608	s_axi_hp3_rdata[c_s_axi_hp3_data_width-1:0]	saxihp3rdata[63:0]	O	Read data.
P609	s_axi_hp3_rresp[1:0]	saxihp3rresp[1:0]	O	Read response. This signal indicates the status of the read transfer. The allowable responses are OKAY, EXOKAY, SLVERR, and DECERR.

Table 2-42: **PS Slave, PL Master – High Performance Port – S_AXI_HP3 Signals *(Cont'd)***

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P610	s_axi_hp3_rlast	saxihp3rlast	O	Read last. This signal indicates the last transfer in a read burst.
P611	s_axi_hp3_rvalid	saxihp3rvalid	O	Read valid. This signal indicates that the required read data is available and the read transfer can complete. • 1: Read data available • 0: Read data not available
P612	s_axi_hp3_rready	saxihp3rready	I	Read ready. This signal indicates that the master can accept the read data and response information. • 1: Master read • 0: Master not ready
P613	s_axi_hp3_awqos[3:0]	saxihp3awqos[3:0]	I	Wr QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P614	s_axi_hp3_arqos[3:0]	saxihp3arqos[3:0]	I	Rd QOS bits. 4'hf is highest priority, 4'h0 is lowest priority.
P615	s_axi_hp3_wcount[7:0]	saxihp3wcount[7:0]	O	Write Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P616	s_axi_hp3_wrissuecap1en	saxihp3wrissuecap1en	I	Write Issuing capability of AFI. 1-selects wrIssuing Cap APB register 1
P617	s_axi_hp3_wacount[7:0]	saxihp3wacount[7:0]	O	
P618	s_axi_hp3_rcount[7:0]	saxihp3rcount[7:0]	O	Read Data FIFO fill level. • 7'b000_0001=1 Qword... • 7'b100_0000=64 Qwords
P619	s_axi_hp3_racount[7:0]	saxihp3racount[7:0]	O	
P670	s_axi_hp3_rdissuecap1en	saxihp3rdissuecap1en	I	Read Issuing capability of AFI. 1-selects rd Issuing Cap APB register 1.

PS Clock and Reset Signals

Table 2-43: **PS Clock and Reset Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P671	ps_clk	psclk	I	ps_clk is the PS reference clock input.
P672	ps_por_b	psporb	I	ps_por_b is used to hold the PS in reset until all PS power supplies are at required voltage levels.
P673	ps_srst_b	pssrstb	I	ps_srst_b is used to force a PS system reset.

Multiplexed I/O Signals

Table 2-44: **Multiplexed I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P674	mio[53:0]	mio[53:0]	I/O	Input/Output ports of the PS

DDR I/O Signals

Table 2-45: **DDR I/O Signals**

Port	Processing System 7 I/O Name	Zynq-7000 PS7 I/O Name	I/O	Description
P675	ddr_addr[14:0]	ddra[14:0]	O	Address
P676	ddr_bankaddr[2:0]	ddrba[2:0]	O	Bank Address
P677	ddr_cas_n	ddrcasb	O	Column address select
P678	ddr_cke	ddrcke	O	Clock enable
P679	ddr_clk_n	ddrckn	O	Differential clock
P680	ddr_clk	ddrckp	O	Differential clock
P681	ddr_cs_n	ddrcsb	O	Chip select
P682	ddr_dm[3:0]	ddrdm[3:0]	O	Data mask
P683	ddr_dq[31:0]	ddrdq[31:0]	I/O	Data
P684	ddr_dqs_n[3:0]	ddrdqsn[3:0]	I/O	Differential data strobe
P685	ddr_dqs[3:0]	ddrdqsp[3:0]	I/O	Differential data strobe
P686	ddr_drstb	ddrdrstb	O	Reset
P687	ddr_odt	ddrodt	O	Output dynamic termination
P688	ddr_ras_n	ddrrasb	O	Row address select
P689	ddr_vrn	ddrvrn	I/O	Used to calibrate input termination
P690	ddr_vrp	ddrvrp	I/O	Used to calibrate input termination
P691	ddr_web	ddrweb		

Parameters

The Processing System 7 core can be parameterized for individual applications. Parameters related to enabling of interfaces or functions reflect the state of the Zynq-7000 device configuration. The Zynq-7000 device configuration custom Vivado IDE is available in the Vivado IP integrator and should be used to update the parameters mentioned in Table 2-46.

These parameter are updated in the IP integrator. Ports related to specific peripherals are either valid or invalid. Invalid ports are not visible. The IP integrator database uses these parameters to initialize associated PS registers in the `ps7_init.tcl` or First Stage Boot Loader (FSBL). The FSBL enables you to configure the design as needed, including the PS and PL. By default, the JTAG interface is enabled to give you access to the PS and PL for test and debug purposes.

Table 2-46: **Processing System 7 Design Parameters**

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
G1	C_Processing System 7_SI_REV	Revision of Zynq-7000 architecture	PRODUCTION , 1.0, 2.0, 3.0	PRODUCTION	String
G2	C_USE_TRACE	Trace Ports are valid when this parameter value is 1.	0, 1	0	Integer
G3	C_USE_CROSS_ TRIGGER	Ports used to integrate PL triggers into SoC cross triggering system are valid when this parameter value is 1.	0, 1	0	Integer
G4	C_USE_CR_FABRIC	PS to PL clock, PL reset port is valid when this parameter value is 1.	0, 1	1	Integer
G5	C_USE_AXI_FABRIC_IDLE	PL idle Port is valid when this parameter value is 1.	0, 1	1	Integer
G6	C_USE_DDR_BYPASS	DDR arbitration bypass signal for four DDR ports are valid when this parameter value is 1.	0, 1	0	Integer
G7	C_USE_FABRIC_INTERRUPT	PL interrupts ports are valid when this parameter value is 1.	0, 1	0	Integer
G8	C_USE_PROC_EVENT_BUS	Processor event bus are valid when this parameter value is 1.	0, 1	0	Integer

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
G9	C_EN_QSPI	Quad-SPI interrupt pin to PL is valid when this parameter value is 1 along with G7 = 1.	0, 1	0	Integer
G10	C_EN_SMC	SMC interrupt pin to PL is valid when this parameter value is 1 along with G7 = 1.	0, 1	0	Integer
G11	C_EN_EMIO_SRAM_INT	PL interrupt pin to SRAM is valid when this parameter value is 1.	0, 1	0	Integer
G12	C_INCLUDE_ACP_TRANS_CHECK	Include ATC (ACP transaction checker)	0, 1	0	Integer
CAN0 Parameters					
G13	C_EN_CAN0	CAN0 interface is enabled when this parameter is 1.	0, 1	0	Integer
G14	C_EN_EMIO_CAN0	EMIO CAN0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G15	C_CAN0_BASEADDR	Base address of CAN0 control registers	Constant	0xE0008000	std_logic_vector
G16	C_CAN0_HIGHADDR	High address of CAN0 control registers	Constant	0xE0008FFF	std_logic_vector
CAN1 Parameters					
G17	C_EN_CAN1	CAN1 interface is enabled when this parameter is 1.	0, 1	0	Integer
G18	C_EN_EMIO_CAN1	EMIO CAN1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G19	C_CAN1_BASEADDR	Base address of CAN1 control registers	Constant	0xE0009000	std_logic_vector
G20	C_CAN1_HIGHADDR	High address of CAN1 control registers	Constant	0xE0009FFF	std_logic_vector
ENET0 Parameters					
G21	C_EN_ENET0	ENET0 interface is enabled when this parameter is 1.	0, 1	0	Integer
G22	C_EN_EMIO_ENET0	EMIO ENET0 ports are valid when this parameter value is 1.	0, 1	0	Integer

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
G23	C_ENET0_BASEADDR	Base address of ENET0 control registers	Constant	0xE000B000	std_logic_ vector
G24	C_ENET0_ HIGHADDR	High address of ENET0 control registers	Constant	0xE000BFFF	std_logic_ vector
ENET1 Parameters					
G25	C_EN_ENET1	ENET1 interface is enabled when this parameter is 1.	0, 1	0	Integer
G26	C_EN_EMIO_ENET1	EMIO ENET1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G27	C_ENET1_BASEADDR	Base address of ENET1 control registers	Constant	0xE000C000	std_logic_ vector
G28	C_ENET1_HIGHADDR	High address of ENET1 control registers	Constant	0xE000CFFF	std_logic_ vector

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
GPIO Parameters					
G29	C_EN_GPIO	GPIO0 interface is enabled when this parameter is 1.	0, 1	0	Integer
G30	C_EN_EMIO_GPIO	EMIO GPIO ports are valid when this parameter value is 1.	0, 1	0	Integer
G31	C_EMIO_GPIO_WIDTH	The width of GPIO ports	1:64	64	Integer
G32	C_GPIO_BASEADDR	Base address of GPIO control registers	Constant	0xE000A000	std_logic_ vector
G33	C_GPIO_HIGHADDR	High address of GPIO control registers	Constant	0xE000AFFF	std_logic_ vector
I2C0 Parameters					
G34	C_EN_I2C0	I2C0 interface is enabled when this parameter is 1.	0, 1	0	Integer
G35	C_EN_EMIO_I2C0	EMIO I2C0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G36	C_I2C0_BASEADDR	Base address of I2C0 control registers	Constant	0xE0004000	std_logic_ vector
G37	C_I2C0_HIGHADDR	High address of I2C0 control registers	Constant	0xE0004FFF	std_logic_ vector
I2C1 Parameters					
G38	C_EN_I2C1	I2C1 interface is enabled when this parameter is 1.	0, 1	0	Integer
G39	C_EN_EMIO_I2C1	EMIO I2C1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G40	C_I2C1_BASEADDR	Base address of I2C1 control registers	Constant	0xE0005000	std_logic_ vector
G41	C_I2C1_HIGHADDR	High address of I2C1 control registers	Constant	0xE0005FFF	std_logic_ vector

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
PJTAG Parameters					
G42	C_EN_PJTAG	PJTAG interface is enabled when this parameter is 1.	0, 1	0	Integer
G43	C_EN_EMIO_PJTAG	EMIO PJTAG ports are enabled when this parameter is 1.	0, 1	0	Integer
SDIO0 Parameters					
G44	C_EN_SDIO0	SDIO0 interface is enabled when this parameter is 1.	0, 1	0	Integer
G45	C_EN_EMIO_SDIO0	EMIO SDIO 0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G46	C_SDIO0_BASEADDR	Base address of SDIO0 control registers	Constant	0xE0100000	std_logic_ vector
G47	C_SDIO0_HIGHADDR	High address of SDIO0 control registers	Constant	0xE0100FFF	std_logic_ vector
SDIO1 Parameters					
G48	C_EN_SDIO1	SDIO1 interface is enabled when this parameter is 1.	0, 1	0	Integer
G49	C_EN_EMIO_SDIO1	EMIO SDIO1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G50	C_SDIO1_BASEADDR	Base address of SDIO1 control registers	Constant	0xE0101000	std_logic_ vector
G51	C_SDIO1_HIGHADDR	High address of SDIO1 control registers	Constant	0xE0101FFF	std_logic_ vector
SPI0 Parameters					
G52	C_EN_SPI0	SPI0 interface is enabled when this parameter is 1.	0, 1	0	Integer
G53	C_EN_EMIO_SPI0	EMIO SPIO0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G54	C_SPI0_BASEADDR	Base address of SPI0 control registers	Constant	0xE0006000	std_logic_ vector
G55	C_SPI0_HIGHADDR	High address of SPI0 control registers	Constant	0xE0006FFF	std_logic_vec tor

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
SPI1 Parameters					
G56	C_EN_SPI1	SPI1 interface is enabled when this parameter is 1.	0, 1	0	Integer
G57	C_EN_EMIO_SPI1	EMIO SPI1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G58	C_SPI1_BASEADDR	Base address of SPI1 control registers	Constant	0xE0007000	std_logic_ vector
G59	C_SPI1_HIGHADDR	High address of SPI1 control registers	Constant	0xE0007FFF	std_logic_ vector
UART0 Parameters					
G60	C_EN_UART0	UART0 interface is enabled when this parameter is 1.	0, 1	0	Integer
G61	C_EN_EMIO_UART0	EMIO UART0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G62	C_UART0_BASEADDR	Base address of UATRT0 control registers	Constant	0xE0000000	std_logic_ vector
G63	C_UART0_HIGHADDR	High address of UART0 control registers	Constant	0xE0000FFF	std_logic_ vector
G64	C_EN_MODEM_UART0	Enable MODEM UART0	0, 1	0	Integer
G65	C_EN_EMIO_MODEM_ UART0	Enable EMIO MODEM UART0	0, 1	0	Integer
UART1 Parameters					
G66	C_EN_UART1	UART1 interface is enabled when this parameter is 1.	0, 1	0	Integer
G67	C_EN_EMIO_UART1	EMIO UART1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G68	C_UART1_BASEADDR	Base address of UART1 control registers	Constant	0xE0001000	std_logic_ vector
G69	C_UART1_HIGHADDR	High address of UART1 control registers	Constant	0xE0001000	std_logic_ vector
G70	C_EN_MODEM_UART1	Enable MODEM UART1	0, 1	0	Integer
G71	C_EN_EMIO_MODEM_ UART1	Enable EMIO MODEM UART1	0, 1	0	Integer

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
TTC0 Parameters					
G72	C_EN_TTC0	TTC0 interface is enabled when this parameter value is 1.	0, 1	0	Integer
G73	C_EN_EMIO_TTC0	EMIO TTC0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G74	C_TTC0_BASEADDR	Base address of TTC0 registers	Constant	0xE0104000	std_logic_ vector
G75	C_TTC0_HIGHADDR	High address of TTC0 control registers	Constant	0xE0104FFF	std_logic_ vector
TTC1 Parameters					
G76	C_EN_TTC1	TTC1 interface is enabled when this parameter value is 1.	0, 1	0	Integer
G77	C_EN_EMIO_TTC1	EMIO TTC1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G78	C_TTC1_BASEADDR	Base address of TTC1 registers	Constant	0xE0105000	std_logic_ vector
G79	C_TTC1_HIGHADDR	High address of TTC1 control registers	Constant	0xE0105FFF	std_logic_ vector
WDT Parameters					
G80	C_EN_WDT	Watchdog timer WDT interface is enabled when this parameter value is 1.	0, 1	0	Integer
G81	C_EN_EMIO_WDT	EMIO WDT ports are valid when this parameter value is 1.	0, 1	0	Integer
G82	C_EN_TRACE	Enable Trace	0, 1	0	Integer
G83	C_EN_EMIO_TRACE	Enable EMIO Trace	0, 1	0	Integer
USB0 Parameters					
G84	C_EN_USB0	USB0 interface is enabled when this parameter value is 1.	0, 1	0	Integer
G85	C_USB0_BASEADDR	Base address of USB0 control registers	Constant	0xE0102000	std_logic_ vector
G86	C_USB0_HIGHADDR	High address of USB0 control registers	Constant	0xE0102FFF	std_logic_ vector

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
USB1 Parameters					
G87	C_EN_USB1	USB1 interface is enabled when this parameter value is 1.	0, 1	0	Integer
G88	C_USB1_BASEADDR	Base address of USB1 control registers	Constant	0xE0103000	std_logic_ vector
G89	C_USB1_HIGHADDR	High address of USB1 control registers	Constant	0xE0103FFF	std_logic_ vector
AXI I/O Parameters					
G90	C_USE_M_AXI_GP0	M_AXI_GP0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G91	C_USE_M_AXI_GP1	PS M_AXI_GP1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G92	C_USE_S_AXI_GP0	PS S_AXI_GP0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G93	C_USE_S_AXI_GP1	PS S_AXI_GP1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G94	C_USE_S_AXI_ACP	PS S_AXI_ACP ports are valid when this parameter value is 1.	0, 1	0	Integer
G95	C_USE_S_AXI_HP0	PS S_AXI_HP0 ports are valid when this parameter value is 1.	0, 1	0	Integer
G96	C_USE_S_AXI_HP1	PS S_AXI_HP1 ports are valid when this parameter value is 1.	0, 1	0	Integer
G97	C_USE_S_AXI_HP2	PS S_AXI_HP2 ports are valid when this parameter value is 1.	0, 1	0	Integer
G98	C_USE_S_AXI_HP3	PS S_AXI_HP3 ports are valid when this parameter value is 1.	0, 1	0	Integer
G99	C_S_AXI_GP0_ENABLE_ LOWOCM_DDR	S_AXI_GP0 address range to access Low On Chip Memory (OCM) is valid when this parameter value is 1.	0, 1	0	Integer

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
G100	C_S_AXI_GP1_ENABLE_LOWOCM_DDR	S_AXI_GP1 address range to access Low OCM is valid when this parameter value is 1.	0, 1	0	Integer
G101	C_S_AXI_ACP_ENABLE_HIGHOCM	S_AXI_ACP address range to access High OCM is valid when this parameter value is 1.	0, 1	0	Integer
G102	C_S_AXI_HP0_ENABLE_HIGHOCM	S_AXI_HP0 address range to access High OCM is valid when this parameter value is 1.	0, 1	0	Integer
G103	C_S_AXI_HP1_ENABLE_HIGHOCM	S_AXI_HP1 address range to access High OCM is valid when this parameter value is 1.	0, 1	0	Integer
G104	C_S_AXI_HP2_ENABLE_HIGHOCM	S_AXI_HP2 address range to access High OCM is valid when this parameter value is 1.	0, 1	0	Integer
G105	C_S_AXI_HP3_ENABLE_HIGHOCM	S_AXI_HP3 address range to access High OCM is valid when this parameter value is 1.	0, 1	0	Integer
DMA Parameters					
G106	C_USE_DMA0	DMA channel 0 ports on PS-PL interface are valid if this parameter value is 1.	0, 1	0	Integer
G107	C_USE_DMA1	Use DMA channel 1 ports on PS-PL interface are valid if this parameter value is 1.	0, 1	0	Integer
G108	C_USE_DMA2	Use DMA channel 2 ports on PS-PL interface are valid if this parameter value is 1.	0, 1	0	Integer
G109	C_USE_DMA3	Use DMA channel 3 ports on PS-PL interface are valid if this parameter value is 1.	0, 1	0	Integer

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
DDR Parameters					
G110	C_EN_DDR	DDR ports are valid when this parameter value is 1.	0, 1	0	Integer
G111	C_DDR_RAM_BASEADDR	DDR base address	Constant	0x00000000	std_logic_ vector
G112	C_DDR_RAM_HIGHADDR	DDR High address	Range from 0x00000000 to maximum of 0x3FFFFFFF	0x3FFFFFFF	std_logic_ vector
PL Interrupt Parameters					
G113	C_NUM_F2P_INTR_INPUTS	Number of PLs to processing system interrupts	1:16	2	Integer
FCLK Parameters					
G114	C_FCLK_CLK0_FREQ	Frequency of FCLK_CLK0 in hertz	-	0	Integer
G115	C_FCLK_CLK1_FREQ	Frequency of FCLK_CLK1 in hertz	-	0	Integer
G116	C_FCLK_CLK2_FREQ	Frequency of FCLK_CLK2 in hertz	-	0	Integer
G117	C_FCLK_CLK3_FREQ	Frequency of FCLK_CLK3 in hertz	-	0	Integer
G118	C_FCLK_CLK0_BUF	Use buffered FCLK_CLK0 clock when this parameter value ID is TRUE	TRUE, FALSE	TRUE	STRING
G119	C_FCLK_CLK1_BUF	Use buffered FCLK_CLK1 clock when this parameter value ID is TRUE	TRUE, FALSE	TRUE	STRING
G120	C_FCLK_CLK2_BUF	Use buffered FCLK_CLK2 clock when this parameter value ID is TRUE	TRUE, FALSE	TRUE	STRING
G121	C_FCLK_CLK3_BUF	Use buffered FCLK_CLK3 clock when this parameter value ID is TRUE	TRUE, FALSE	TRUE	STRING

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
M_AXI_GP0 Parameters					
G122	C_M_AXI_GP0_PROTOCOL	AXI compliant protocol for M_AXI_GP0	-	AXI3	String
G123	C_M_AXI_GP0_ID_WIDTH	AXI transaction ID Width	12	12	Integer
G124	C_M_AXI_GP0_ADDR_WIDTH	Address Width	Constant	32	Integer
G125	C_M_AXI_GP0_DATA_WIDTH	Data Width	Constant	32	Integer
G126	C_M_AXI_GP0_SUPPORTS_NARROW_BURST	Enable narrow burst support	0, 1	0	Integer
G127	C_M_AXI_GP0_SUPPORTS_REORDERING	Enable AXI transaction reordering	0, 1	0	Integer
G128	C_M_AXI_GP0_SUPPORTS_THREADS	Enable AXI thread ID support	0, 1	1	Integer
G129	C_M_AXI_GP0_THREAD_ID_WIDTH	AXI transaction thread ID Width	Constant	12	Integer
M_AXI_GP1 Parameters					
G130	C_M_AXI_GP1_PROTOCOL	AXI compliant protocol for M_AXI_GP1	-	AXI3	String
G131	C_M_AXI_GP1_ID_WIDTH	AXI transaction ID Width	12	12	Integer
G132	C_M_AXI_GP1_ADDR_WIDTH	Address Width	Constant	32	Integer
G133	C_M_AXI_GP1_DATA_WIDTH	Data Width	Constant	32	Integer
G134	C_M_AXI_GP0_SUPPORTS_NARROW_BURST	Enable narrow burst support	0, 1	0	Integer
G135	C_M_AXI_GP1_SUPPORTS_REORDERING	Enable AXI transaction reordering	0, 1	0	Integer
G136	C_M_AXI_GP1_SUPPORTS_THREADS	Enable AXI thread ID support	0, 1	1	Integer
G137	C_M_AXI_GP1_THREAD_ID_WIDTH	AXI transaction thread ID Width	Constant	12	Integer

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
S_AXI_GP0 Parameters					
G138	C_S_AXI_GP0_PROTOCOL	AXI compliant protocol for S_AXI_GP0	-	AXI3	String
G139	C_S_AXI_GP0_ID_WIDTH	AXI transaction ID Width	1:6	6	Integer
G140	C_S_AXI_GP0_ADDR_WIDTH	Address Width	Constant	32	Integer
G141	C_S_AXI_GP0_DATA_WIDTH	Data Width	Constant	32	Integer
G142	C_S_AXI_GP0_BASEADDR	S_AXI_GP0 base address	Constant	0xE0000000	std_logic_vector
G143	C_S_AXI_GP0_HIGHADDR	S_AXI_GP0 High address	Constant	0xFFFFFFFF	std_logic_vector
G144	C_S_AXI_GP0_LOWOCM_DDR_BASEADDR	S_AXI_GP0 base address for Low OCM and DDR address range	Range from 0x00000000 to 0x3FFFFFFF	0x00000000	std_logic_vector
G145	C_S_AXI_GP0_LOWOCM_DDR_HIGHADDR	S_AXI_GP0 High address for Low OCM and DDR address range	Range from 0x00000000 to 0x3FFFFFFF	0x3FFFFFFF	std_logic_vector
S_AXI_GP1 Parameters					
G146	C_S_AXI_GP1_PROTOCOL	AXI compliant protocol for S_AXI_GP1	-	AXI3	String
G147	C_S_AXI_GP1_ID_WIDTH	AXI transaction ID Width	1:6	6	Integer
G148	C_S_AXI_GP1_ADDR_WIDTH	Address Width	Constant	32	Integer
G149	C_S_AXI_GP1_DATA_WIDTH	Data Width	Constant	32	Integer
G150	C_S_AXI_GP1_BASEADDR	S_AXI_GP1base address	Constant	0xE0000000	std_logic_vector
G151	C_S_AXI_GP1_HIGHADDR	S_AXI_GP1 High address	Constant	0xFFFFFFFF	std_logic_vector
G152	C_S_AXI_GP1_LOWOCM_DDR_BASEADDR	S_AXI_GP1 base address for Low OCM and DDR address range	Range from 0x00000000 to 0x3FFFFFFF	0x00000000	std_logic_vector
G153	C_S_AXI_GP1_LOWOCM_DDR_HIGHADDR	S_AXI_GP1 High address for Low OCM and DDR address range	Range from 0x00000000 to 0x3FFFFFFF	0x3FFFFFFF	std_logic_vector

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
S_AXI_ACP Parameters					
G154	C_S_AXI_ACP_PROTOCOL	AXI compliant protocol for S_AXI_ACP	-	AXI3	String
G155	C_S_AXI_ACP_ID_WIDTH	AXI transaction ID Width	1:3	3	Integer
G156	C_S_AXI_ACP_ADDR_WIDTH	Address Width	Constant	32	Integer
G157	C_S_AXI_ACP_DATA_WIDTH	Data Width	Constant	64	Integer
G158	C_S_AXI_ACP_SUPPORTS_USER_SIGNALS	Enable ACP user signal support	0, 1	1	Integer
G159	C_S_AXI_ACP_ARUSER_WIDTH	Enable read address channel user signals	Constant	5	Integer
G160	C_S_AXI_ACP_AWUSER_WIDTH	Enable write address channel user signals	Constant	5	Integer
G161	C_S_AXI_ACP_BASEADDR	S_AXI_ACP base address	Range from 0x00000000 to 0x3FFFFFFF	0x00000000	std_logic_vector
G162	C_S_AXI_ACP_HIGHADDR	S_AXI_ACP High address	Range from 0x00000000 to 0x3FFFFFFF	0x3FFFFFFF	std_logic_vector
G163	C_S_AXI_ACP_HIGHOCM_BASEADDR	S_AXI_ACP base address for High OCM and DDR address range	Constant	0xFFFC0000	std_logic_vector
G164	C_S_AXI_ACP_HIGHOCM_HIGHADDR	S_AXI_ACP High address for High OCM and DDR address range	Constant	0xFFFFFFFF	std_logic_vector
S_AXI_HP0 Parameters					
G165	C_S_AXI_HP0_PROTOCOL	AXI compliant protocol for S_AXI_HP0	-	AXI3	String
G166	C_S_AXI_HP0_ID_WIDTH	AXI transaction ID Width	1:6	6	Integer
G167	C_S_AXI_HP0_ADDR_WIDTH	Address Width	Constant	32	Integer
G168	C_S_AXI_HP0_DATA_WIDTH	Data Width	32, 64	64	Integer
G169	C_S_AXI_HP0_BASEADDR	S_AXI_HP0 base address	Range from 0x00000000 to 0x3FFFFFFF	0x00000000	std_logic_vector

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
G170	C_S_AXI_HP0_HIGHADDR	S_AXI_HP0 High address	Range from 0x00000000 to 0x3FFFFFFF	0x3FFFFFFF	std_logic_vector
G171	C_S_AXI_HP0_HIGHOCM_BASEADDR	S_AXI_HP0 High address for High OCM and DDR address range	Constant	0xFFFC0000	std_logic_vector
G172	C_S_AXI_HP0_HIGHOCM_HIGHADDR	S_AXI_HP0 High address for High OCM and DDR address range	Constant	0xFFFFFFFF	std_logic_vector
S_AXI_HP1 Parameters					
G173	C_S_AXI_HP1_PROTOCOL	AXI compliant protocol for S_AXI_HP1	-	AXI3	String
G174	C_S_AXI_HP1_ID_WIDTH	AXI transaction ID Width	1:6	6	Integer
G175	C_S_AXI_HP1_ADDR_WIDTH	Address Width	Constant	32	Integer
G176	C_S_AXI_HP1_DATA_WIDTH	Data Width	32, 64	64	Integer
G177	C_S_AXI_HP1_BASEADDR	S_AXI_HP1 base address	Range from 0x00000000 to 0x3FFFFFFF	0x00000000	std_logic_vector
G178	C_S_AXI_HP1_HIGHADDR	S_AXI_HP1 High address	Range from 0x00000000 to 0x3FFFFFFF	0x3FFFFFFF	std_logic_vector
G179	C_S_AXI_HP1_HIGHOCM_BASEADDR	S_AXI_HP1 base address for High OCM and DDR address range	Constant	0xFFFC0000	std_logic_vector
G180	C_S_AXI_HP1_HIGHOCM_HIGHADDR	S_AXI_HP1 High address for High OCM and DDR address range	Constant	0xFFFFFFFF	std_logic_vector
S_AXI_HP2 Parameters					
G181	C_S_AXI_HP2_PROTOCOL	AXI compliant protocol for S_AXI_HP2	-	AXI3	String
G182	C_S_AXI_HP2_ID_WIDTH	AXI transaction ID Width	1:6	6	Integer
G183	C_S_AXI_HP2_ADDR_WIDTH	Address Width	Constant	32	Integer
G184	C_S_AXI_HP2_DATA_WIDTH	Data Width	32, 64	64	Integer

Table 2-46: **Processing System 7 Design Parameters *(Cont'd)***

Generic	Parameter Name	Feature / Description	Allowable Values	Default Value	VHDL Type
G185	C_S_AXI_HP2_BASEADDR	S_AXI_HP2 base address	Range from 0x00000000 to 0x3FFFFFFF	0x00000000	std_logic_vector
G186	C_S_AXI_HP2_HIGHADDR	S_AXI_HP2 High address	Range from 0x00000000 to 0x3FFFFFFF	0x3FFFFFFF	std_logic_vector
G187	C_S_AXI_HP2_HIGHOCM_BASEADDR	S_AXI_HP2 base address for High OCM and DDR address range	Constant	0xFFFC0000	std_logic_vector
G188	C_S_AXI_HP2_HIGHOCM_HIGHADDR	S_AXI_HP2 High address for High OCM and DDR address range	Constant	0xFFFFFFFF	std_logic_vector
S_AXI_HP3 Parameters					
G189	C_S_AXI_HP3_PROTOCOL	AXI compliant protocol for S_AXI_HP3	-	AXI3	String
G190	C_S_AXI_HP3_ID_WIDTH	AXI transaction ID Width	1:6	6	Integer
G191	C_S_AXI_HP3_ADDR_WIDTH	Address Width	Constant	32	Integer
G192	C_S_AXI_HP3_DATA_WIDTH	Data width	32, 64	64	Integer
G193	C_S_AXI_HP3_BASEADDR	S_AXI_HP3 base address	Range from 0x00000000 to 0x3FFFFFFF	0x00000000	std_logic_vector
G194	C_S_AXI_HP3_HIGHADDR	S_AXI_HP3 High address	Range from 0x00000000 to 0x3FFFFFFF	0x3FFFFFFF	std_logic_vector
G195	C_S_AXI_HP3_HIGHOCM_BASEADDR	S_AXI_HP3 base address for High OCM and DDR address range	Constant	0xFFFC0000	std_logic_vector
G196	C_S_AXI_HP3_HIGHOCM_HIGHADDR	S_AXI_HP3 high address for High OCM and DDR address range	Constant	0xFFFFFFFF	std_logic_vector
G197	C_M_AXI_GP0_ENABLE_STATIC_REMAP	Enable compress/decompress AXI transaction ID feature	0, 1	0	Integer
G198	C_M_AXI_GP1_ENABLE_STATIC_REMAP	Enable compress/decompress AXI transaction ID feature	0, 1	0	Integer

Register Space

The Processing System 7 core provides access from PL masters to PS internal peripherals, and memory through GP, HP and ACP interfaces. The Vivado IP integrator address editor provides various address segments with a fixed address for each slave interface. The availability of the address segments is controlled through the following addressing parameters:

- **Allow access to High OCM**: Allows address mapping to PS internal OCM at High Address.
- **Detailed IOP address space**: Provides individual address spaces for PS internal peripherals.
- **Allow access to PS/SLCR registers**: Allows address mapping to PS and SLCR register space. (SLCR stands for System Level Control Registers.)
- **Allow access to DAP ROM**: Allows address mapping to debug access port (DAP) ROM.
- **Detailed PS/SLCR address space**: Provides individual address spaces for PS/SLCR registers.

The PS address space accessible from the PL consists of DDR, OCM, SMC memories, SLCR registers, PS I/O peripheral registers, and PS system registers. For more information, see the "System Addresses" chapter of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Designing with the Core

This chapter includes guidelines and additional information to facilitate designing with the core.

General Design Guidelines

There are three interfaces through which the Processing System 7 core can access the PL side peripherals and vice versa. For more details, see the individual sections of AXI_HP, AXI_GP, and AXI_ACP interfaces in the "Interconnect" chapter of the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

For example, the Processing System 7 DDR can be accessed from the MicroBlaze™ processor master through S_AXI_HP*, S_AXI_GP*, and S_AXI_ACP interfaces.

Clocking

There are three major phase-locked loops (PLLs) through which the design gets the clock with different frequencies. They are:

- **ARM PLL**: The ARM® Cortex™-A9 CPU gets the clock from the ARM PLL. The current implementation generates the frequency ranges from 50 to 667 MHz.
- **DDR PLL**: The ARM DDR peripheral gets the clock from DDR PLL. The current implementation generates the frequency ranges from 200 to 534 MHz.
- **I/O PLL**: The ARM I/O peripheral operates under I/O PLL. The current implementation generates the frequency ranges from 10 to 200 MHz.

PL side peripherals can be operated through a fabric clock (FCLK_CLK0...3). They generate the frequency ranges from 0.1 to 250 MHz

Resets

There are many applicable resets:

- Power on reset
- External system reset
- System software and peripheral resets given by writing to the SLCR registers
- WDT reset
- Debug reset (through JTAG)

For more details about the individual resets, see the *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585) [Ref 1].

Design Flow Steps

This chapter describes customizing and generating the core, constraining the core, and the simulation, synthesis and implementation steps that are specific to this IP core. More detailed information about the standard Vivado® design flows and the IP integrator can be found in the following Vivado Design Suite user guides:

- *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 2]
- *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3]
- *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4]
- *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 5]

Customizing and Generating the Core

This section includes information about using Xilinx tools to customize and generate the core in the Vivado Design Suite.

If you are customizing and generating the core in the Vivado IP integrator, see the *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994) [Ref 2] for detailed information. IP integrator might auto-compute certain configuration values when validating or generating the design. To check whether the values do change, see the description of the parameter in this chapter. To view the parameter value, run the `validate_bd_design` command in the Tcl Console.

You can customize the IP for use in your design by specifying values for the various parameters associated with the IP core in the IP integrator using the following steps:

1. Select the IP from the Vivado IP catalog.
2. Double-click the selected IP, or select the **Customize IP** command from the toolbar or right-click menu.

For details, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3] and the *Vivado Design Suite User Guide: Getting Started* (UG910) [Ref 4].

Note: Figures in this chapter are illustrations of the Vivado Integrated Design Environment (IDE). The layout depicted here might vary from the current version.

The **Zynq Block Design** page with a block diagram appears in the window (Figure 4-1). Review the contents of the block diagram. The green colored blocks in the diagram are configurable.

TIP: *To open the corresponding configuration page, you can click a green block, or select the page in the Page Navigator at the left side.*

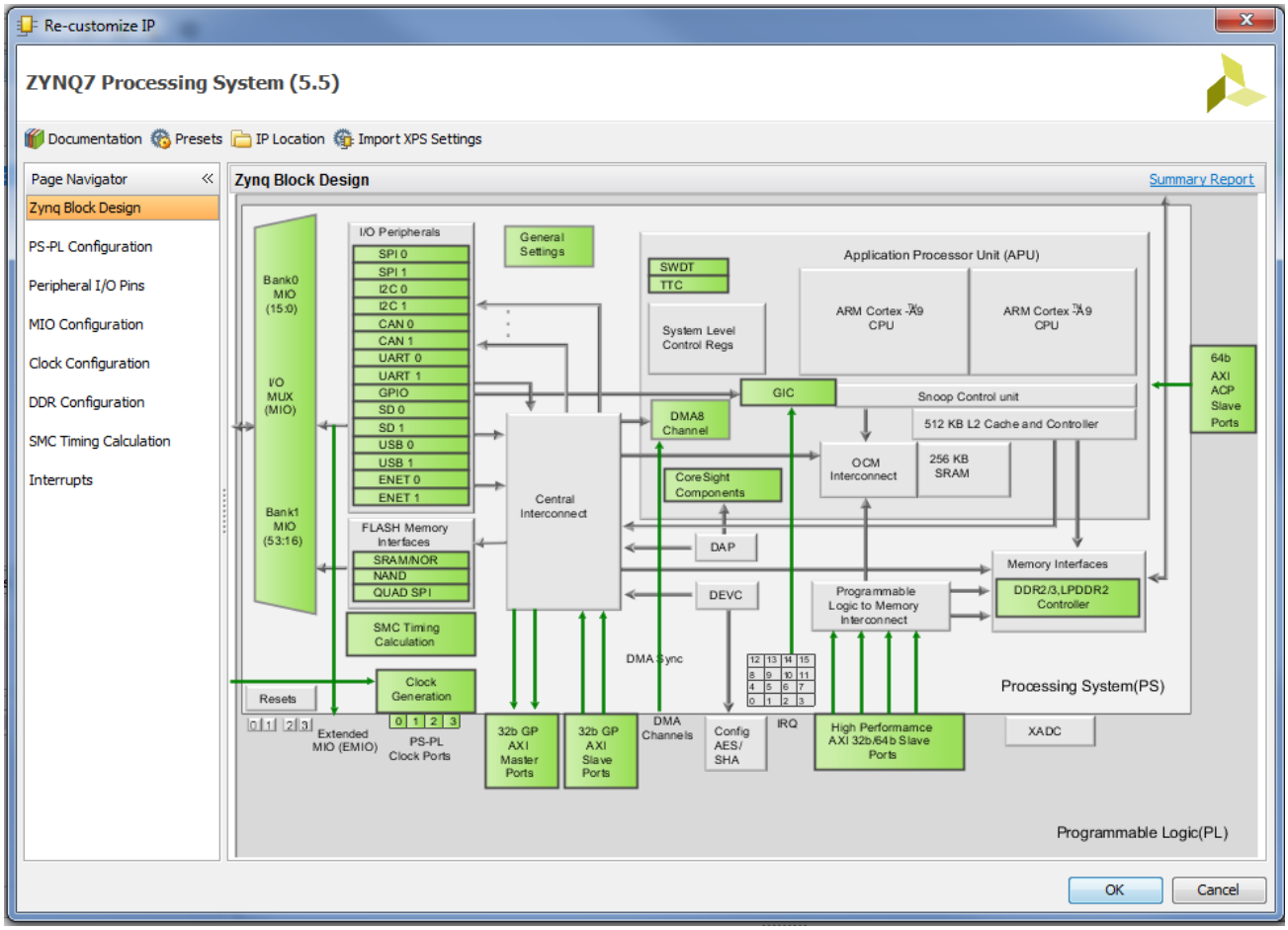

Figure 4-1: **Zynq Block Design Page**

The **PS-PL Configuration** page enabled you to configure PS-PL interfaces including AXI, HP, and ACP bus interfaces.

The **Peripheral IO Pins** page enables you to configure MIO/EMIO configuration for different I/O peripherals. This page maps all peripherals I/O signals to MIO pins in tree table view.

The **MIO Configuration** page enables you to configure MIO/EMIO pin configuration for different I/O peripherals.

The **Clock Configuration** page enables you to configure Processing System 7 peripheral clocks, fabric clocks, DDR and CPU clocks.

The **DDR Configuration** page enables you to set user DDR controller configurations.

The SMC timing calculation is performed using the **SMC Timing Calculation** page.

The **Interrupts** page enables you to configure the PS-PL interrupt ports.

User Parameters

See Parameters in Chapter 2.

Output Generation

For details about common core output files, see "Generating IP Output Products" in the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3].

The Vivado design tool exports the Hardware Platform Specification for your design to the Software Development Kit (SDK). The following five files are exported to SDK:

- The `system.xml` file opens by default when SDK launches. The address map of your system read from this file is shown by default in the SDK window.

  Note: The `system.xml` file contains information regarding addressing in the design which is available only through the IP integrator flow for automatic generation of `system.xml`. Hence `system.xml` generation is not possible in non-IP integrator flows.

- The `ps7_init.tcl`, `ps7_init.c` and `ps7_init.h` files contain the initialization code for the Zynq-7000 processing system and initialization settings for DDR, clocks, plls, and MIOs. SDK uses these settings when initializing the processing system so that applications can be run on top of the processing system.
  - `ps7_init.tcl`: This Processor System 7 initialization Tcl file is used for the device initialization Xilinx Microprocessor Debugger (XMD) flow.
  - `ps7_init.c`: Generated by the PS Configuration Wizard (PCW), this header file for the first stage boot loader (FSBL) contains proc of a `ps7_init()` and the return values. The FSBL uses only this file, and it calls the `ps7_init()` functions, and checks return values.
  - `ps7_init.h`: Generated by the PCW, this file implements the `ps7_init()`. This file also contains some testing code. This testing code enhances the testing performed by the PCW.
- The `ps7_init.html` file stores a summary report of Processor System 7 register configuration. Figure 4-2 shows a sample report.

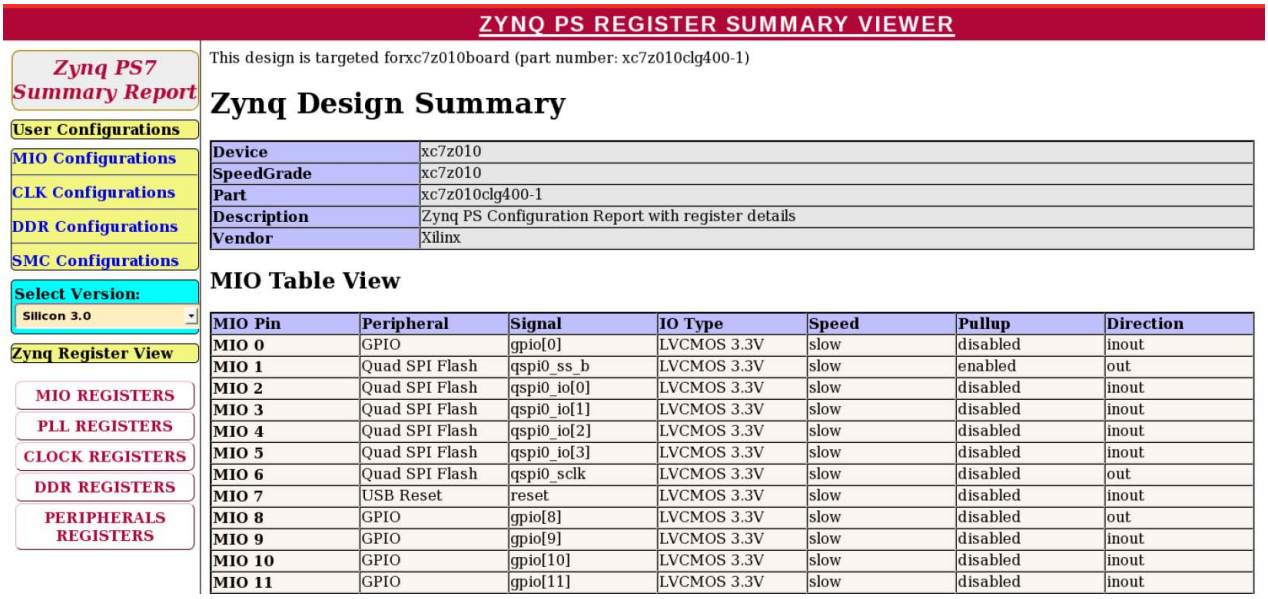

Figure 4-2: **Zynq Design Summary Report**

How the PS Configuration Wizard Tool Generates Output Code

The PS Configuration Wizard tool generates a table of words, which is interpreted by a small engine, looping through the table and performing the actions. The following is an example table:

```
unsigned long ps7_mio_init_data_3_0[] = {
   EMIT_MASKWRITE(0XF8000100, 0x00000001U ,
0x00000000U),
   EMIT_MASKPOLL(0XF800010C, 0x00000001U),
   EMIT_MASKWRITE(0XF8000100, 0x00000010U ,0x00000000U),
};
```

All the `EMIT_*` are #defines, which adds 1 to 4 words to the `ps7_init_data` array.

The supporting `.c` and `.h` files (described previously) are also produced by the PCW.

The Processing System 7 core overwrites all files when regenerated.

Constraining the Core

This section is not applicable to this core because PS is a hard IP.

The Processing System 7 core generates fabric clocks based on your selections.

```
create_clock -name clk_fpga_0 -period "20" [get_pins "PS7_i/FCLKCLK[0]"]
set_input_jitter clk_fpga_0 0.6
```

The clocks are asynchronous, so you should constrain them appropriately

Required Constraints

This section is not applicable to this core because PS is a hard IP.

Device, Package, and Speed Grade Selections

This section is not applicable to this core because PS is a hard IP.

Clock Frequencies

This section is not applicable to this core because PS is a hard IP.

Clock Management

This section is not applicable to this core because PS is a hard IP.

Clock Placement

This section is not applicable to this core because PS is a hard IP.

Banking

This section is not applicable to this core because PS is a hard IP.

Transceiver Placement

This section is not applicable to this core because PS is a hard IP.

I/O Standard and Placement

This section is not applicable to this core because PS is a hard IP.

Simulation

For comprehensive information about Vivado simulation components, as well as information about using supported third-party tools, see the *Vivado Design Suite User Guide: Logic Simulation* (UG900) [Ref 5].

See also the *Zynq-7000 All Programmable SoC Verification IP Data Sheet* (DS940) [Ref 6].

IMPORTANT: *For cores targeting 7 series or Zynq-7000 devices, UNIFAST libraries are not supported. Xilinx IP is tested and qualified with UNISIM libraries only.*

Synthesis and Implementation

For details about synthesis and implementation, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 3].

Migrating and Upgrading

This appendix contains information about migrating a design from the ISE® Design Suite to the Vivado® Design Suite, and for upgrading to a more recent version of the IP core. For customers upgrading in the Vivado Design Suite, important details (where applicable) about any port changes and other impact to user logic are included.

Migrating to the Vivado Design Suite

For information on migrating to the Vivado Design Suite, see *ISE to Vivado Design Suite Migration Methodology Guide* (UG911) [Ref 7].

Upgrading in the Vivado Design Suite

This section provides information about any changes to the user logic or port designations that take place when you upgrade to a more current version of this IP core in the Vivado Design Suite. There are no changes from the previous release.

Debugging

This appendix includes details about resources available on the Xilinx Support website and debugging tools.

Finding Help on Xilinx.com

To help in the design and debug process when using the Processing System 7, the Xilinx Support web page contains key resources such as product documentation, release notes, answer records, information about known issues, and links for obtaining further product support.

Documentation

This product guide is the main document associated with the Processing System 7. This guide, along with documentation related to all products that aid in the design process, can be found on the Xilinx Support web page or by using the Xilinx Documentation Navigator.

Download the Xilinx Documentation Navigator from the Downloads page. For more information about this tool and the features available, open the online help after installation.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Answer Records

Answer Records include information about commonly encountered problems, helpful information on how to resolve these problems, and any known issues with a Xilinx product. Answer Records are created and maintained daily ensuring that users have access to the most accurate information available.

Answer Records for this core can also be located by using the Search Support box on the main Xilinx support web page. To maximize your search results, use proper keywords such as

- Product name
- Tool message(s)
- Summary of the issue encountered

A filter search is available after results are returned to further target the results.

Master Answer Record for the Processing System 7

AR: 54446

Technical Support

Xilinx provides technical support at the Xilinx Support web page for this LogiCORE™ IP product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support if you do any of the following:

- Implement the solution in devices that are not defined in the documentation.
- Customize the solution beyond that allowed in the product documentation.
- Change any section of the design labeled DO NOT MODIFY.

To contact Xilinx Technical Support, navigate to the Xilinx Support web page.

Vivado Design Suite Debug Feature

There are many tools available to address debugging for the Processing System 7 design issues. The Vivado® Design Suite debug feature inserts logic analyzer and virtual I/O cores directly into your design. The debug feature also allows you to set trigger conditions to capture application and integrated block port signals in hardware. Captured signals can then be analyzed. This feature in the Vivado IDE is used for logic debugging and validation of a design running in Xilinx devices.

The Vivado logic analyzer is used to interact with the logic debug LogiCORE IP cores, including:

- ILA 2.0 (and later versions)
- VIO 2.0 (and later versions)

See *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 8].

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

References

These documents provide supplemental material useful with this product guide:

1. *Zynq-7000 All Programmable SoC Technical Reference Manual* (UG585)
2. *Vivado Design Suite User Guide: Designing IP Subsystems using IP Integrator* (UG994)
3. *Vivado Design Suite User Guide: Designing with IP* (UG896)
4. *Vivado Design Suite User Guide: Getting Started* (UG910)
5. *Vivado Design Suite User Guide: Logic Simulation* (UG900)
6. *Zynq-7000 All Programmable SoC Verification IP Data Sheet* (DS940)
7. *ISE to Vivado Design Suite Migration Guide* (UG911)
8. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
9. *AMBA AXI4-Stream Protocol Specification*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/10/2017	5.5	• Added reference and link to the *Zynq-7000 All Programmable SoC Verification IP Data Sheet* (DS940).
09/30/2015	5.5	• Updated Figure 4-1, Zynq Block Design Page. • Added a note about ID assignment for interrupts to the Programmable Logic Clocks and Interrupts section in the Product Specification chapter. • Added a note about the system.xml file in the Output Generation section of the Design Flow Steps chapter. • Added an example showing how to set PCW_IRQ_F2P_MODE to DIRECT and REVERSE in a Tcl Console.
10/02/2013	5.3	Initial Xilinx release as a product guide. Replaces the *LogiCORE IP Processing System 7 Data Sheet* (DS871). • Removed the DMA reset signals: DMA0_RSTN, DMA1_RSTN, DMA2_RSTN, and DMA3_RSTN • Removed the AXI reset signals: M_AXI_GP0_ARESETN, M_AXI_GP1_ARESETN, S_AXI_GP0_ARESETN, S_AXI_GP1_ARESETN, S_AXI_ACP_ARESETN, S_AXI_HP0_ARESETN, S_AXI_HP1_ARESETN, S_AXI_HP2_ARESETN, S_AXI_HP3_ARESETN

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