Information Technology University, Lahore, Pakistan

BS Computer and Software Engineering

Computer Organization and Assembly Language

Quiz 7, Spring 2025

Thursday, May 15, 2025

Name: _____ Roll Number: _____

Maximum Time Allowed: 10 minutes Maximum Marks: 10

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1. A direct-mapped cache has [1+3+1]
   - Size: 16 KB
   - Block size: 64 bytes
   - Address: 32-bit, byte-addressable

   (a) How many cache blocks are there? _____

   (b) For the address `0x0001A3F4`, calculate:

   - Offset bits _____
   - Index bits _____
   - Tag bits _____

   (c) What is the block number and cache index for the address of part (b)? _____

2. You have a 2-way set-associative cache: [1+3+1]
   - Total size: 2 KB
   - Block size: 64 bytes
   - 32-bit, byte-addressable memory
   - LRU replacement

   A program accesses these addresses: `0x00000000, 0x00000040, 0x00001000, 0x00000000, 0x00001000, 0x00002000`

   (a) How many sets are in the cache? _____

   (b) Which one of the above accesses result in cache hits? Show your work. _____ _____

   _____ _____ _____ _____

   (c) After the final access, what is the content (tags) of the set that was accessed last? _____