Department of Computer and Software Engineering – ITU

SE201L: Digital Logic Design Lab

Course Instructor: Ms Aqsa Khalid	**Dated: 20 – 11 – 2024**
Lab Engineer: Muhammad Kashif	**Semester: Fall 2024**
Batch: BSSE 23 A	

LAB 11 Sequential Circuits: 4-bit Universal Shift Register with Parallel Load and Left/Right Shift Operations

Name	Roll Number	Lab Marks
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Checked on: _____

Signature: _____

Sequential Circuits: 4-bit Universal Shift Register with Parallel Load and Left/Right Shift Operations

11.1. Introduction

This lab exercise aims to develop an understanding of the working of a universal shift register and its different modes of operation. In one task, pseudo-random number sequence is generated by use of shift register and XOR gate and in another a Johnson counter is designed and tested using a shift register.

11.2. Objectives

This lab will enable the students to achieve the following:

- Understand the shift operation and the construction and working of a shift register
- Demonstrate parallel load, shift left and shift right operations in a universal shift register
- Generate pseudo-random numbers using shift registers
- Design and test the operation of a Johnson counter using shift register

11.3. Conduct of Lab

1. All tasks of this lab have to be performed using the logic trainer in Embedded Lab.
2. Bring printout of this lab manual when you come to perform the lab.
3. You can work and get evaluated in groups of two. However, manual submission has to be separate.
4. If there is difficulty in understanding any aspect of the lab, please seek help from the lab engineer or the TA.
5. If a lab task contains an instruction to show the work to lab engineer, make sure that the lab engineer evaluates and marks on your manual for that task. If your manual is unmarked for this task, it can result in mark deduction.
6. All tasks must be evaluated within the lab time. Submit the lab manual before leaving the lab.

11.4. Theory and Background

11.4.1. Register

A register is a group of flip-flops that can store binary information. One flip-flop can store one bit. An n-bit register has n flip-flops and stores n-bits of binary information.

11.4.1.1. Shift register

In addition to flip-flops, a register also has logic gates that determine how the data in the register is to be processed. A register with combinational logic gates that has the ability to shift its data from right to left or left to right is called a shift register. Depending on the combinational logic circuit used in the shift register, it may have operations of parallel load, serial input, clear, right shift and left shift etc.

11.5. Lab Tasks

11.5.1. Task 1: Universal shift register [Marks: 4]

1. A universal shift register is a special type of shift register that is capable of performing the following four operations:
    - Load parallel input
    - Shift right with serial input from left
    - Shift left with serial input from right
    - Hold output

2. To select one of the four modes, there are two select inputs S1 and S0. 74194 is a 4-bit bidirectional universal shift register. Its pin configuration is as below:

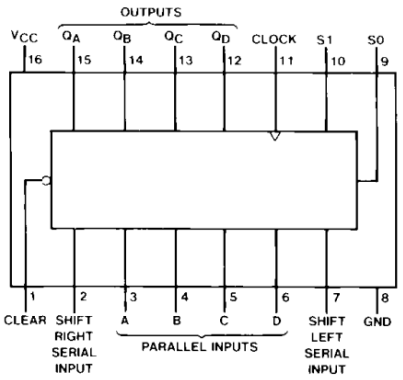

Figure 11.1: Pin configuration of 74194

S0-S1: Mode selection inputs
Clear (Active-Low): Stores 0 in all bits of the register asynchronously
Shift right serial input (SI_R): Serial input when right shift mode is selected
A, B, C, D: Parallel outputs
Shift left serial input (SIL): Serial input when left shift mode is selected
A, B, C, D: Parallel inputs; these will be loaded into the shift register when parallel input mode selected
Q_A-Q_D: Parallel outputs
Clock: Positive-edge of the clock triggers the register

3. Connect this circuit on breadboard according to the following figure, where all keys are to be connected to switches and OA – OD are to be connected to the state monitor LEDs of your logic trainer.

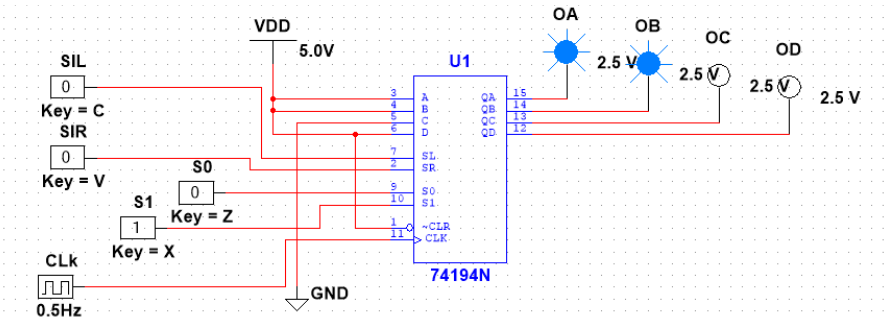

Figure 11.2: Multisim circuit to test the operation of 74194 shift register

4. At every clock pulse, change inputs according to Table 11.1. Apply inputs in the same order as given in this table. Keep the clock frequency very low so that you get time to observe current outputs of the register and also to change inputs in between consecutive clock pulses. Enter your observed outputs under columns Q_A, Q_B, Q_C and Q_D. [4]

Table 11.1: Operation of shift register IC 74194

S1	S0	SI_R	SI_L	A	B	C	D	Clock	Q_A	Q_B	Q_C	Q_D	Mode of operation
1	1	X	X	1	1	0	1	↑					Parallel load
0	1	1	X	X	X	X	X	↑					Right-shift
0	1	1	X	X	X	X	X	↑					
0	1	0	X	X	X	X	X	↑					
0	1	0	X	X	X	X	X	↑					
1	0	X	1	X	X	X	X	↑					Left-shift
1	0	X	1	X	X	X	X	↑					
1	0	X	0	X	X	X	X	↑					
1	0	X	0	X	X	X	X	↑					
0	0	X	X	X	X	X	X	↑					Output-hold

5. Give answer to question 1 of Analysis.

11.5.2. Task 2: Linear-feedback shift register (LFSR) [Marks: 7]

1. Figure 11.3 shows a circuit designed to work as a 4-bit Fibonacci linear-feedback shift register (LFSR). LFSR can generate a pseudo-random sequence of binary numbers.

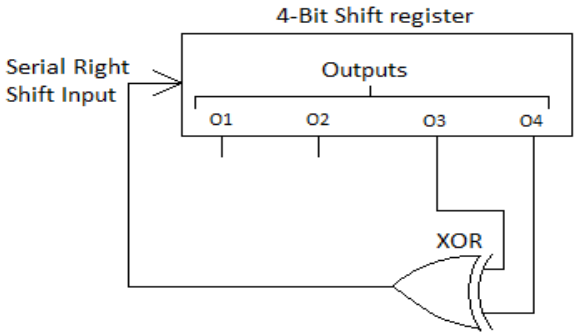

Figure 11.3: Linear Feedback Shift Register (LFSR)

2. Build this circuit on breadboard using the universal shift register IC 74194 and XOR gate IC 7486. [3]
3. When running the circuit, initially select parallel load mode of the shift register and load 0001 in the register.
4. Then, select the right-shift mode of the shift register. Note down the 4-bit output after each positive edge of the clock in Table 11.2 and show working hardware to the lab engineer to obtain credit. [4]

Table 11.2: Random numbers generated using LSFR

Clock edge	4-bit output	Clock edge	4-bit output
1	0001	**17**	1001
2	1000	**18**	0100
3	0100	**19**	1010
4	1010	**20**	0101
5	0101	**21**	1110
6	1110	**22**	0111
7	0111	**23**	0011
8	0011	**24**	0001
9	0001	**25**	1000
10	1000	**26**	0100
11	0100	**27**	1010
12	1010	**28**	0101
13	0101	**29**	1110
14	1110	**30**	0111
15	0111	**31**	0011
16	0011	**32**	0001

5. Give answer to question 2 of Analysis.

11.5.3. Task 3: Johnson counter using shift register [Marks: 9]

1. A Johnson counter is a special type of ring counter. A 3-bit Johnson counter outputs the following 3-bit sequence (Table 11.3) in 6 clock cycles and then repeats.

Table 11.3: 3-bit Johnson counter

Clock edge	O2	O1	O0
1	0	0	0
2	1	0	0
3	1	1	0
4	1	1	1
5	0	1	1
6	0	0	1
7 (Repeat)	0	0	0

2. Design a 4-bit Johnson counter using a shift register and additional combinational logic circuitry. Draw the logic diagram of your design in the following box: [3]

3. Build circuit on breadboard according to your proposed design diagram. [2]
4. Power up the circuit and note down the output of your shift register at each clock edge starting with 0000 in Table 11.4. Also, show working hardware to the lab engineer to obtain credit. [4]

7. Table 11.4: 4-bit Johnson counter

Clock edge	O3	O2	O1	O0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	1
4	0	1	1	1
5	1	1	1	1
6	1	1	1	0
7	1	1	0	0
8	1	0	0	0
9	0	0	0	0
10	0	0	0	1

8. Give answer to question 3 of Analysis.

11.5.4. Analysis [Marks: 5]

1. Does the output of your table indicate correct working according to the stated mode of operation in the last column? [1]

9. This circuit generates a sequence of random numbers and repeats the sequence after a certain number of clock cycles. State below your observations; specifically state the number of clock cycles after which the sequence repeats itself. [2]

10. Looking at Table 11.3 and Table 11.4, can you suggest a formula for the number of clock cycles after which an n-bit Johnson counter repeats itself? Please state below along with reasoning. [2]

Assessment Rubric

Method:
Lab report evaluation and instructor observation during lab sessions.

Performance	CLO	Able to complete the tasks over 80% (4-5)	Able to complete the tasks 50 – 80% (2-3)	Tasks completion below 50% (0-1)	Marks
1. Teamwork	1	Actively engages and cooperates with other group members in an effective manner	Cooperates with other group members in a reasonable manner	Distracts or discourages other group members from conducting the experiments	
2. Laboratory safety and disciplinary rules	1	Observes lab safety rules; handles the development board and other components with care and adheres to the lab disciplinary guidelines aptly	Observes safety rules and disciplinary guidelines with minor deviations	Disregards lab safety and disciplinary rules	
3. Realization of experiment	2	Conceptually understands the topic under study and develops the experimental setup accordingly	Needs guidance to understand the purpose of the experiment and to develop the required setup	Incapable of understanding the purpose of the experiment and consequently fails to develop the required setup	
4. Conducting experiment	2	Sets up hardware/software properly according to the requirement of experiment and examines the output carefully	Makes minor errors in hardware/software setup and observation of output	Unable to set up experimental setup, and perform the procedure of experiment	
5. Data collection	2	Completes data collection from the experiment setup by giving proper inputs and observing the outputs, complies with the instructions regarding data entry in manual	Completes data collection with minor errors and enters data in lab report with slight deviations from provided guidelines	Fails at collecting data by giving proper inputs and observing output states of experiment setup, unable to fill the lab report properly	
6. Data analysis	2	Analyzes the data obtained from experiment thoroughly and accurately verifies it with theoretical understanding, accounts for any discrepancy in data from theory with sound explanation, where asked	Analyzes data with minor error and correlates it with theoretical values reasonably. Attempts to account for any discrepancy in data from theory	Unable to establish the relationship between practical and theoretical values and lacks the theoretical understanding to explain any discrepancy in data	
7. Computer use	2	Successfully uses lab PC and internet to look for relevant datasheets, carry out calculations, or verify results using simulation	Requires assistance in looking for IC datasheets and carrying out calculation and simulation tasks	Does not know how to use computer to look up datasheets or carry out calculation and simulation tasks	
				Total (out of 35)	