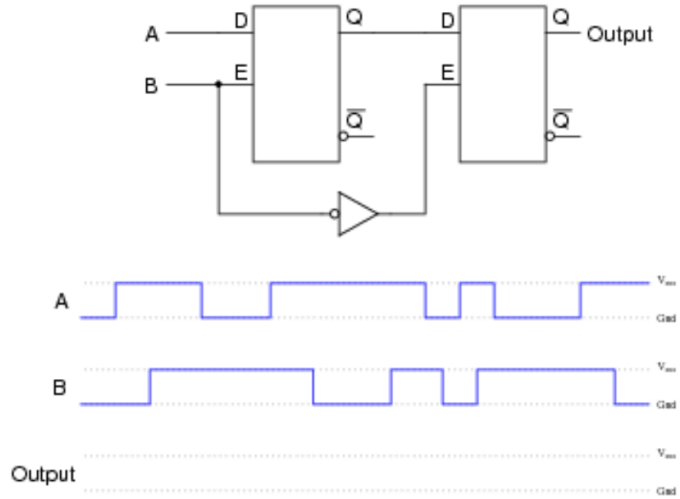
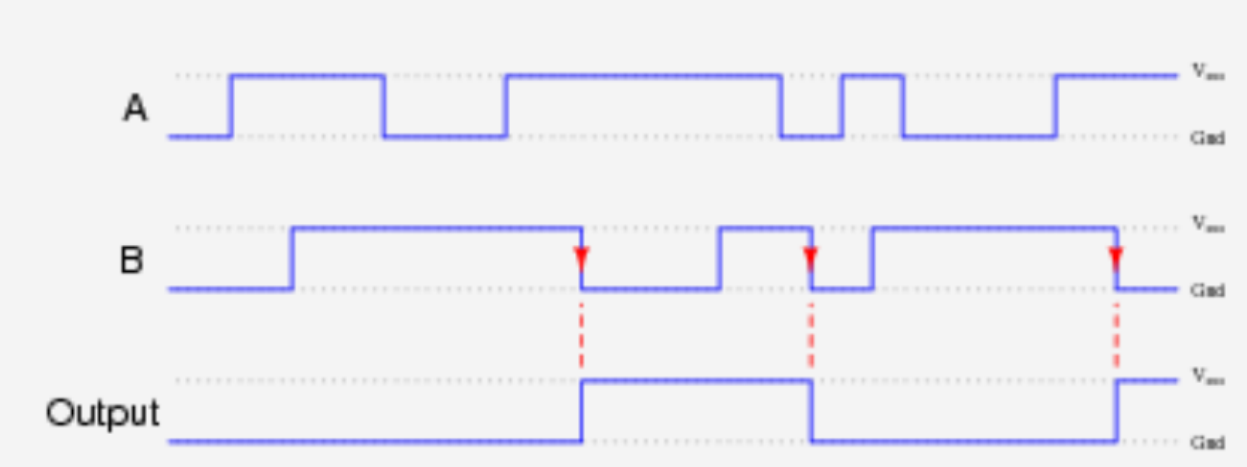
Q:

Determine the final output states over time for the following circuit, built from D-type gated latches:



At what specific times in the pulse diagram does the final output assume the input's state? How does this behavior differ from the normal response of a D-type latch?

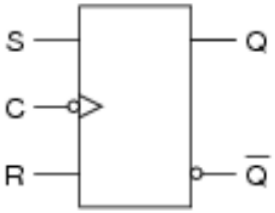
Sol:

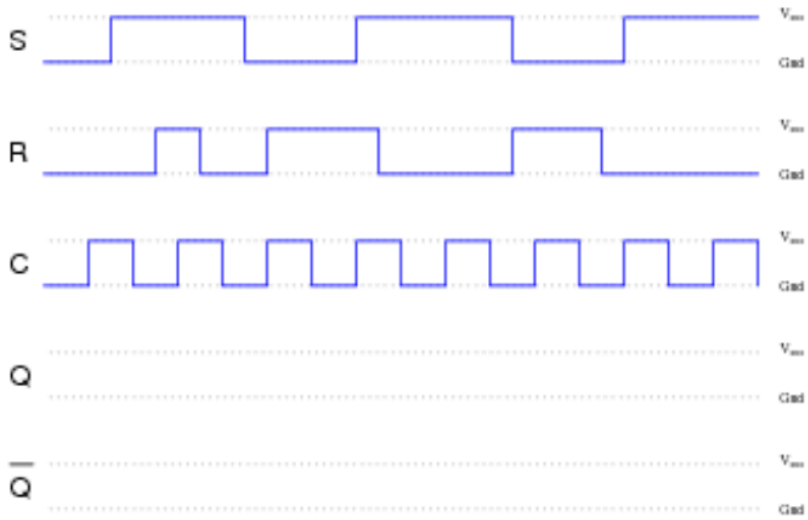


The final output assumes the same logic state as the input only when the enable input signal (B) *transitions* from “high” to “low”.

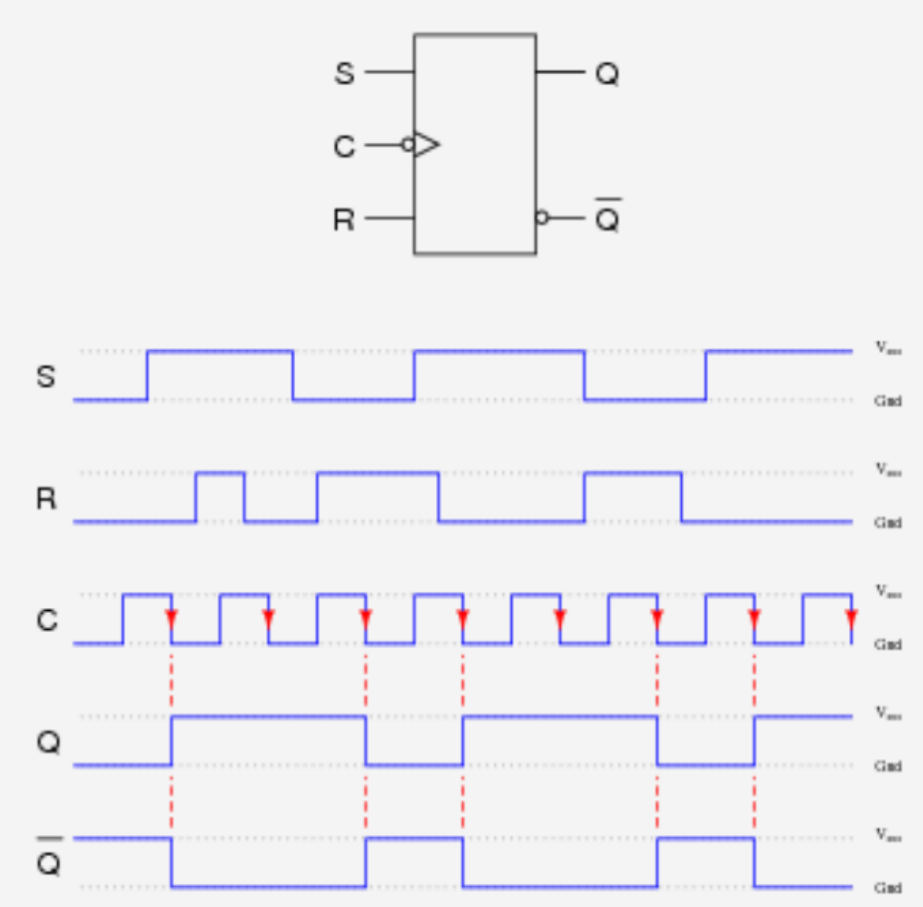
Q:

Determine the output states for this S-R flip-flop, given the pulse inputs shown:





Ans:

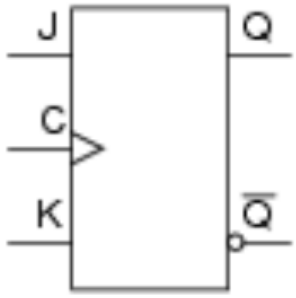


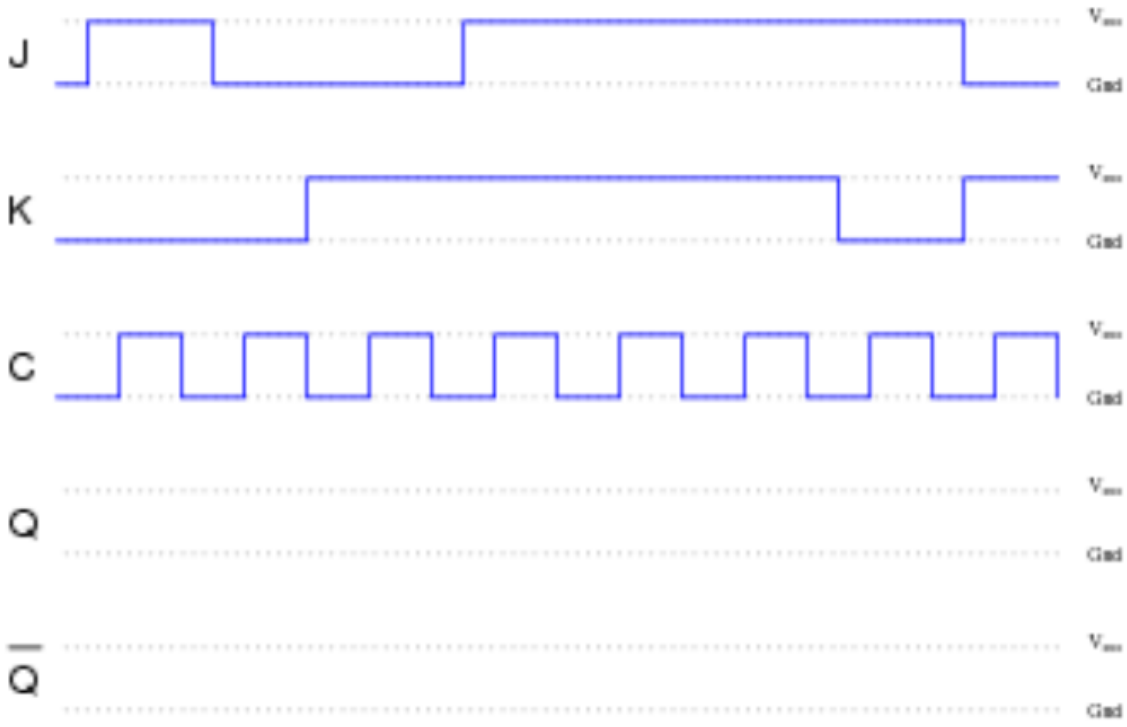
negative-edge-triggered SR flip-flop shows the output of the flip-flop when the clock pulse transitions from 1 to 0:

- **S = 1, R = 0**: Set
- **S = 0, R = 0**: Hold
- **S = 0, R = 1**: Reset
- **S = 1, R = 1**: Not allowed

Q:

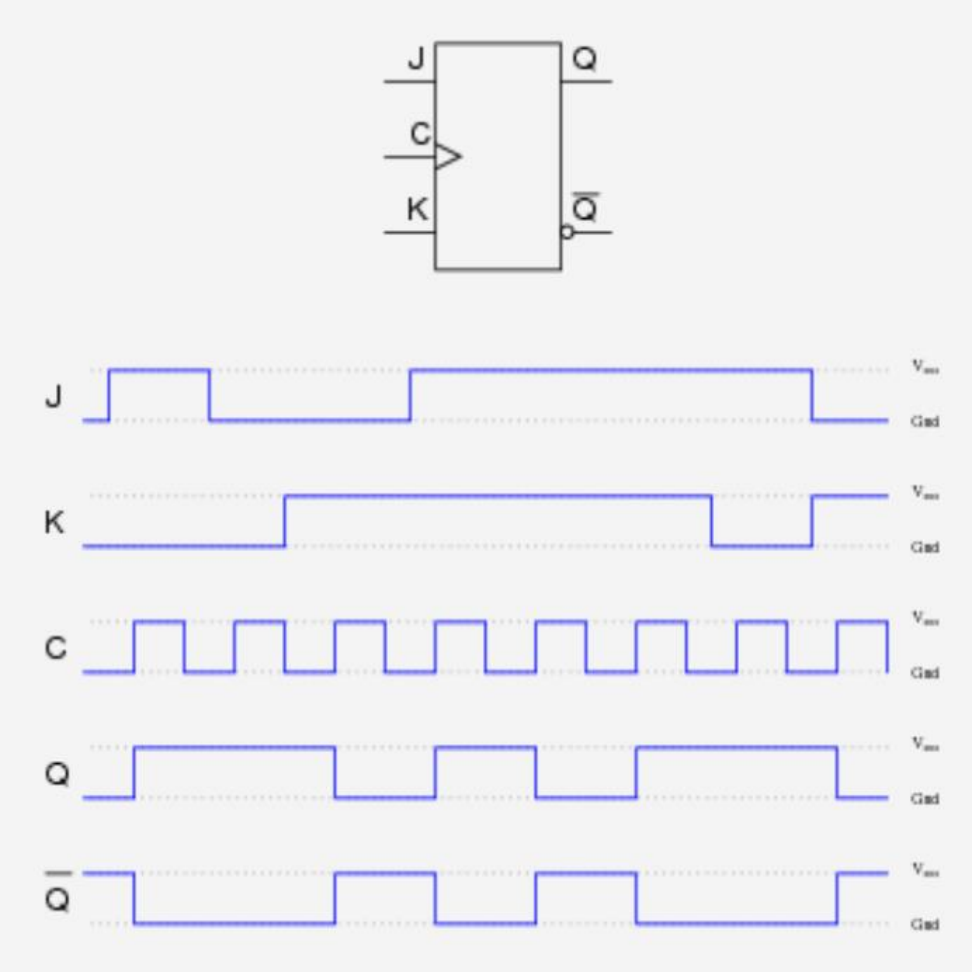
Determine the output states for this J-K flip-flop, given the pulse inputs shown:





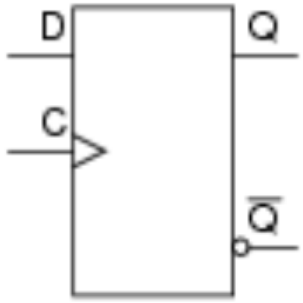
Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

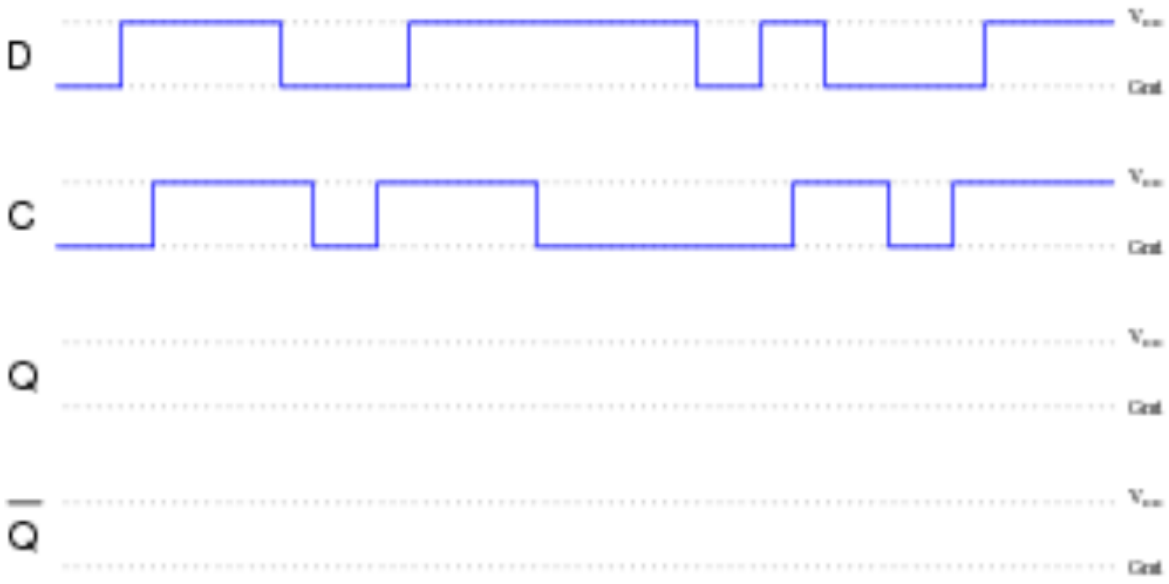
Ans:



Q:

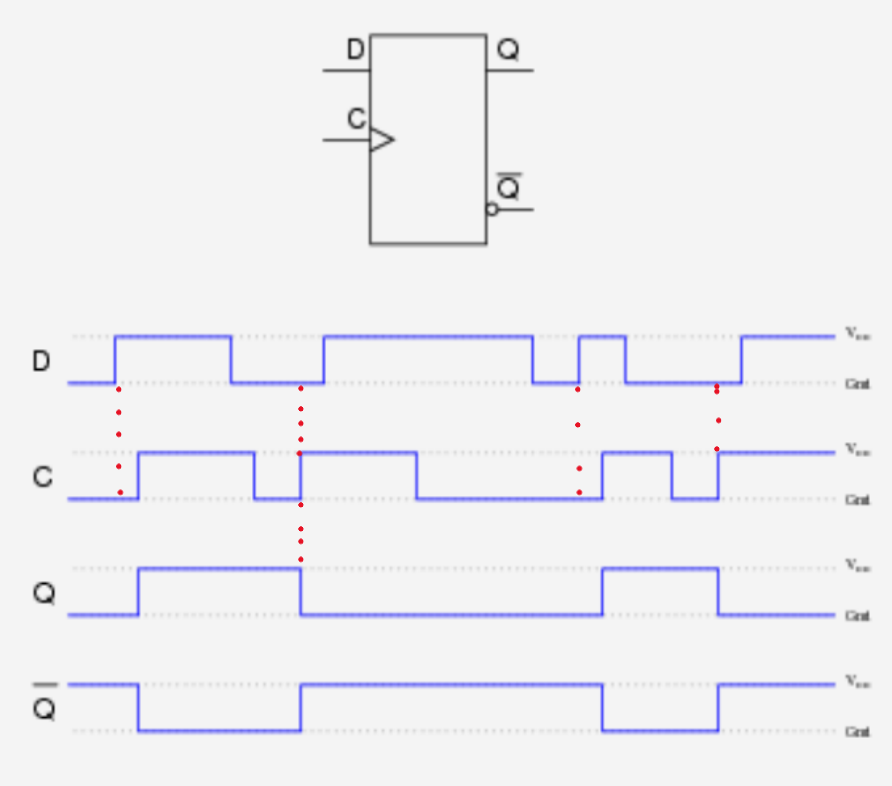
Determine the output states for this D flip-flop, given the pulse inputs shown:





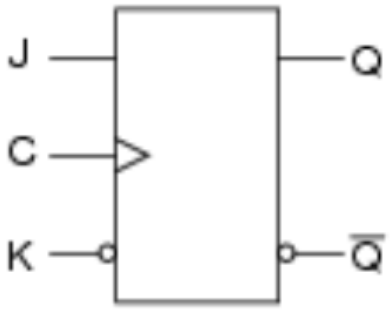
Sol:

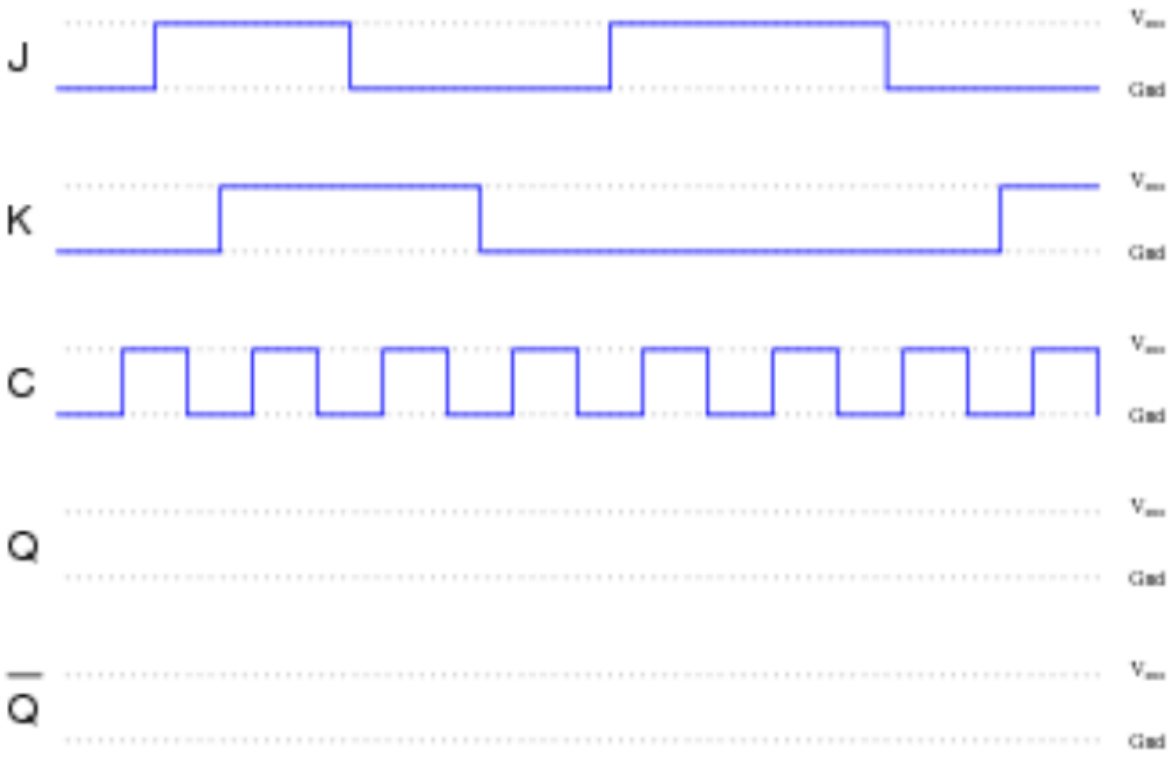
C	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1



Q:

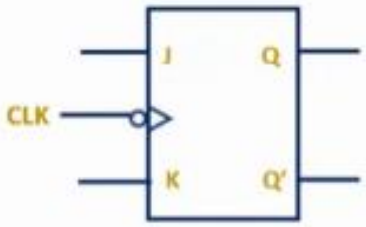
Determine the output states for this J-K flip-flop, given the pulse inputs shown:





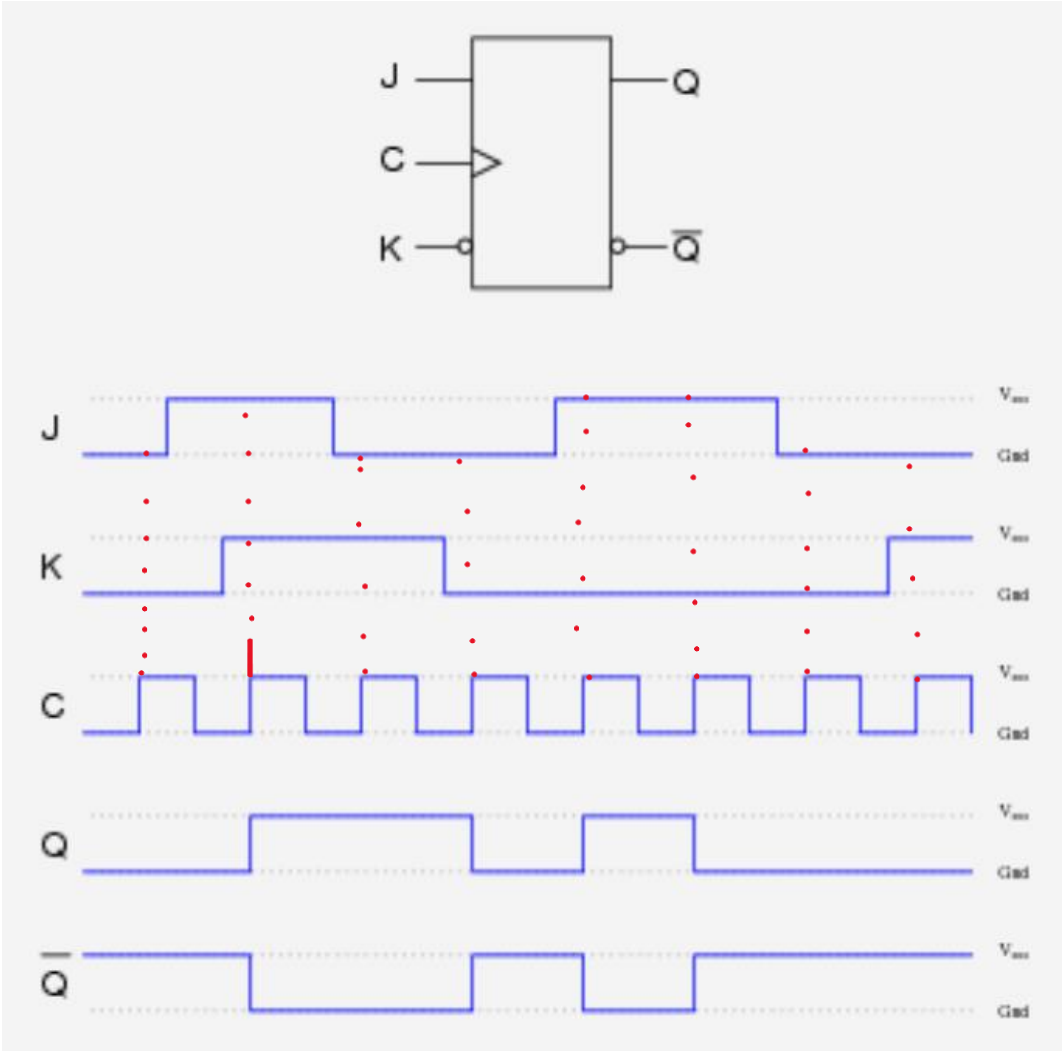
Sol:

Symbol



Truth Table

CLK	J	K	Q n+1
↓	0	0 1	Q n
↓	0	1 0	0
↓	1	0 1	1
↓	1	1 0	Q n'



Reference:

https://www.allaboutcircuits.com/worksheets/flip-flop-circuits/#