FoE Practice Test (Fall 2024)
SE201T – Digital Logic Design

Name: Solution
Time allowed: 1 hour

Roll No.: _____
Maximum Marks: 20

Instructions

a. **This test exam will assess your CLOs as per OBE.**
b. It is a **CLOSED BOOK/NOTES** exam.
c. Part I has **TWO (2) questions/problems with a,b part** for which you are required to provide the solution in the given space.
d. If you are found cheating or helping others cheat, your test will be cancelled and disciplinary action will be taken.

CLOs

1. Apply the concept of different number systems and representations, to perform number system conversions and arithmetic operations.
2. Apply the concepts of Boolean algebra and logic simplification to realize simplified designs of combinational and sequential circuits.
3. Demonstrate the design of sequential circuits from their respective finite state machine representations.

Part I				Total (20)
Q1a – CLO1 (5)	Q1b – CLO2 (5)	Q2a – CLO2 (5)	Q2 – CLO2 (5)	

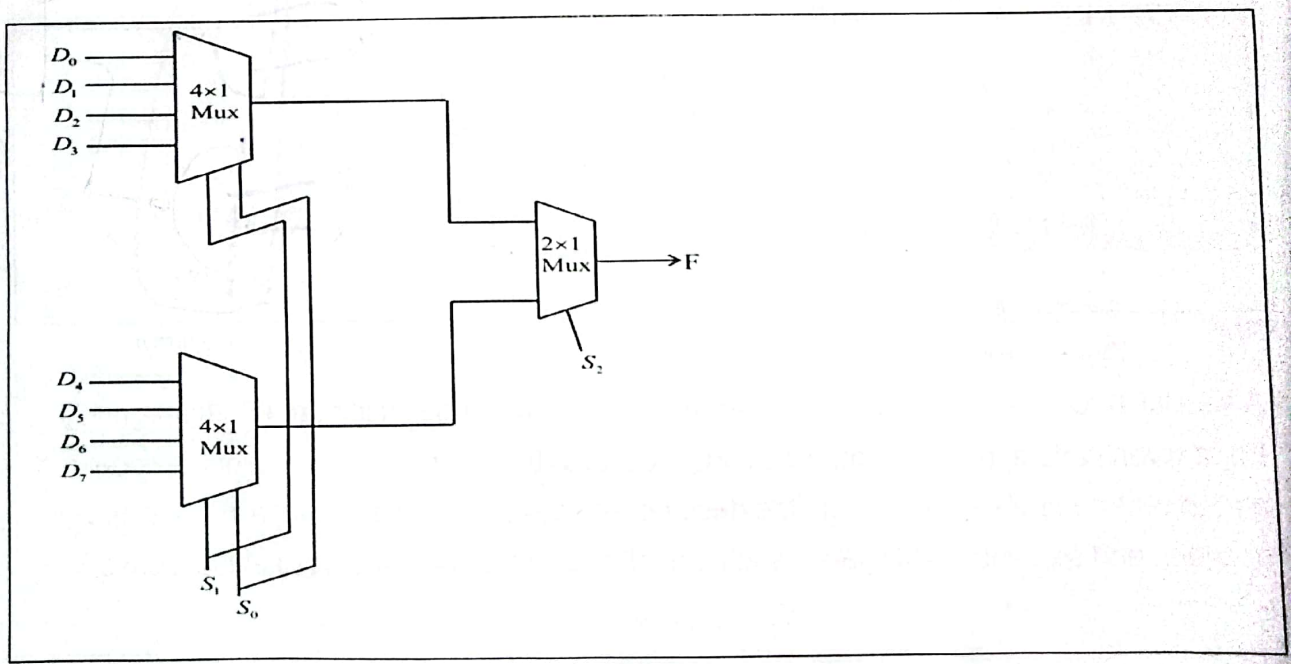
Instructor: Ms. Aqsa Khalid
Teaching Assistant: Ms. Areesha Sami

Signature: _____

PART I

Q1) a- **(5 marks)**

Design an optimized solution for 8-to-1 line multiplexer using 4-to-1 and 2-to-1 line multiplexer.



Q1) b- **(5 marks)**

A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise.

(a) Design a 3 input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.

(b) How many nand gates (2 inputs) are needed to implement this function f. Show derivation with law names also at each step.

Sol:→ (a)

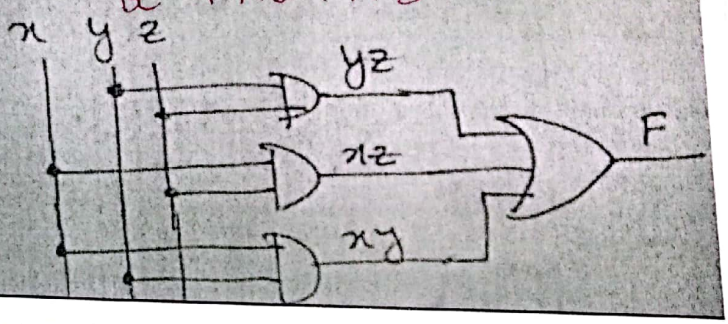
x	y	z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

K map for F

x \ yz	00	01	11	10
0	0	0	1	0
1	0	1	1	1

ABC
XYZ

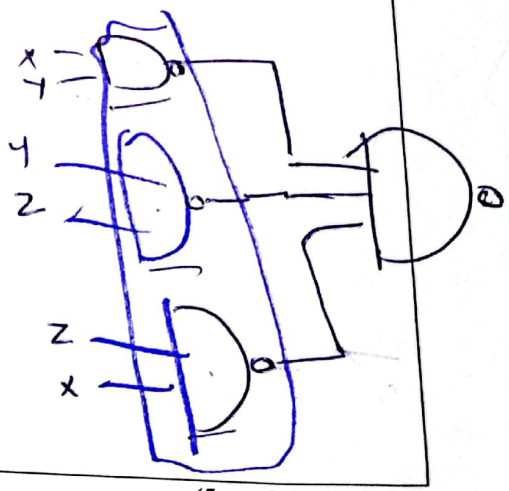
$F = yz + xz + xy$
$BC + AC + AB$



(b) $F = \{(yz + zx + xy)'\}'$

$= \{(yz)' \cdot (zx)' \cdot (xy)'\}'$

we have 3 no. of 2 input NAND gate.



Q2) a- **(5 marks)**

A special 4–to–6-line decoder is to be designed. The input codes used are 000 through 101. For a given code applied, the output *Di*, with *i* equal to the decimal equivalent of the code, is 1 and all other outputs are 0. Design the decoder with a 2–to–4-line decoder, a 1–to–2-line decoder, and six 2-input AND gates, such that all decoder outputs are used at least once.

$2^4 = 16$

4 — 16

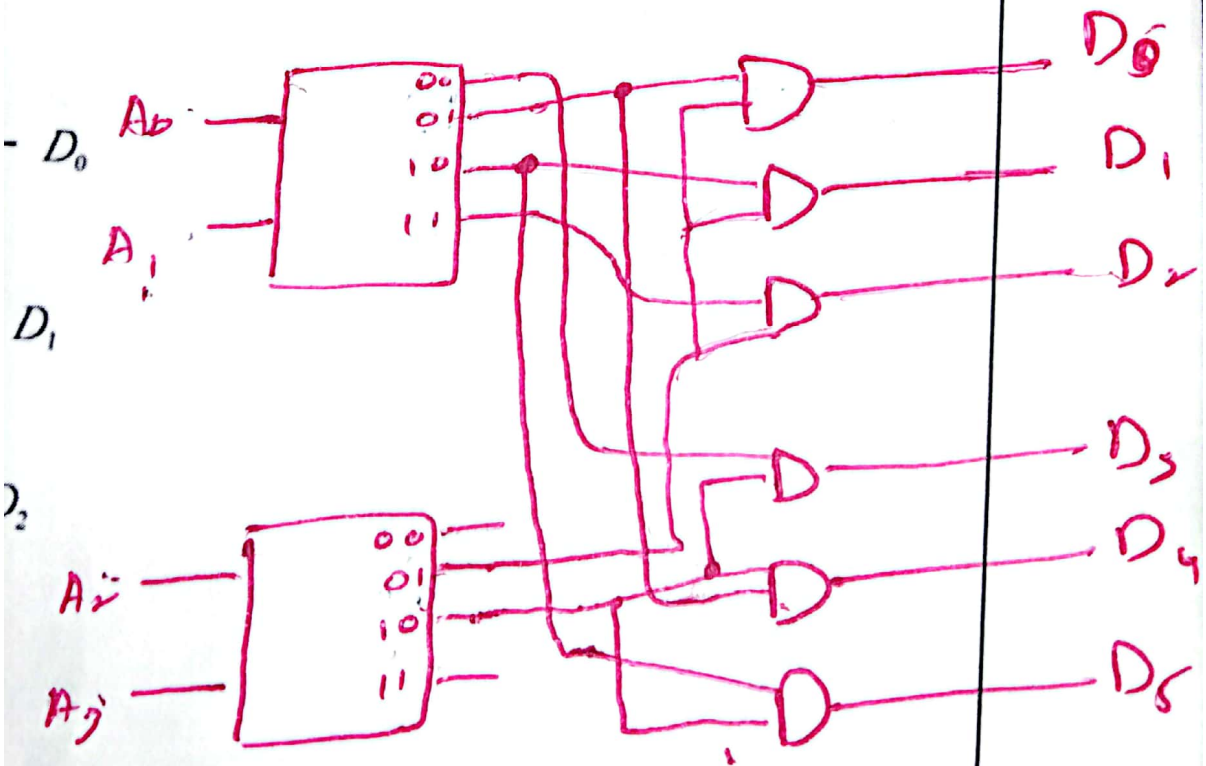
4 to 6

-2 line decoder and 2

tion of 2-to-4 line

A_3	A_2	A_1	A_0	D_6	D_4	D_3	D_2	D_1	D_0
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	0	0	1	0
0	0	1	1	0	0	0	1	0	0
0	1	0	0	0	0	1	0	0	0
0	1	0	1	0	1	0	0	0	0
0	1	1	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0

ecoder,



Q2) b-

A combinational circuit is defined by the following three Boolean functions:

$$F_1 = \overline{X + Z} + XYZ$$

$$F_2 = \overline{X + Z} + \bar{X}YZ$$

$$F_3 = X\bar{Y}Z + \overline{X + Z}$$

Design the circuit with a decoder and external OR gates.

$F1 = \overline{X+Z} + XYZ$

$F2 = \overline{X+Z} + \bar{X}YZ$

$F3 = X\bar{Y}Z + \overline{X+Z}$

First we express the functions in minterm canonical form by expanding the second term with the missing literal.

i.e $F1 = \overline{X+Z} + XYZ$

$= (\bar{X}.\bar{Z}) + (XYZ)$

$= (\bar{X}.\bar{Z})(Y+\bar{Y}) + (XYZ) \quad (\because Y+\bar{Y}=1)$

$= \bar{X}Y\bar{Z} + \bar{X}\bar{Y}\bar{Z} + XYZ$

$\therefore F1 = \sum m(0,2,7)$

Step 2 of 4

$F2 = \overline{X+Z} + \bar{X}YZ$

$= (\bar{X}.\bar{Z}) + \bar{X}YZ$

$= (\bar{X}.\bar{Z}).(Y+\bar{Y}) + (\bar{X}YZ) \quad (\because Y+\bar{Y}=1)$

$= \bar{X}Y\bar{Z} + \bar{X}\bar{Y}\bar{Z} + \bar{X}YZ$

$F2 = \sum m(0,2,3)$

Step 3 of 4

$F3 = X\bar{Y}Z + \overline{X+Z}$

$= (X\bar{Y}Z) + (\bar{X}.\bar{Z})$

$= (X\bar{Y}Z) + (\bar{X}.\bar{Z})(Y+\bar{Y}) \quad (\because Y+\bar{Y}=1)$

$= X\bar{Y}Z + \bar{X}Y\bar{Z} + \bar{X}\bar{Y}\bar{Z}$

$F3 = \sum m(0,2,5)$

Step 4 of 4

The circuit is designed by using one 3 – to –8 decoder.