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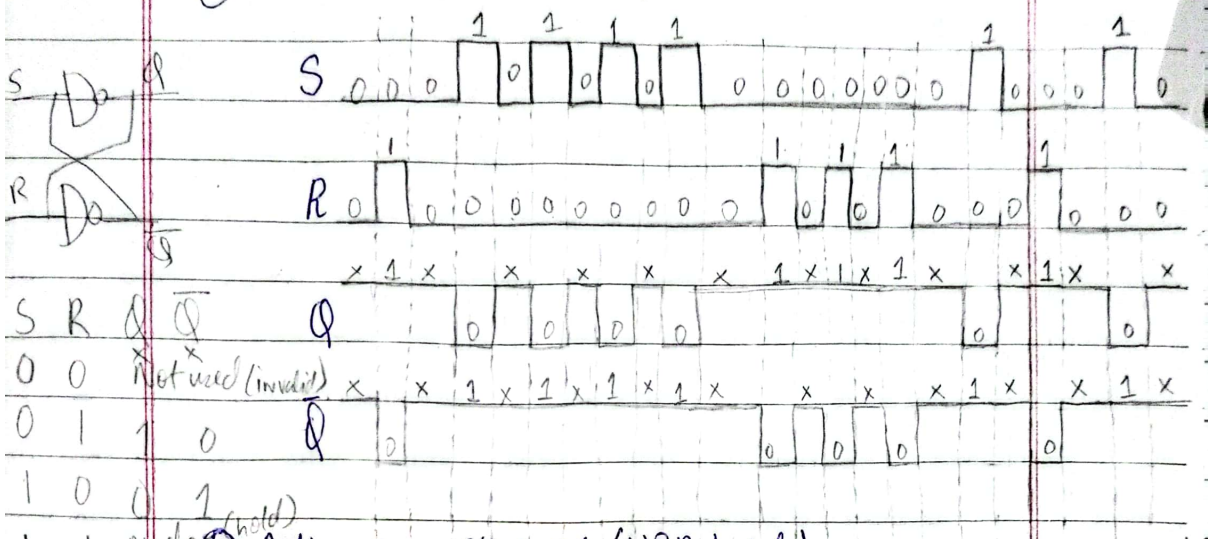
Reg#
BSSE23057

Date: Day:

Assignment #3
Digital Logic Design
DLD

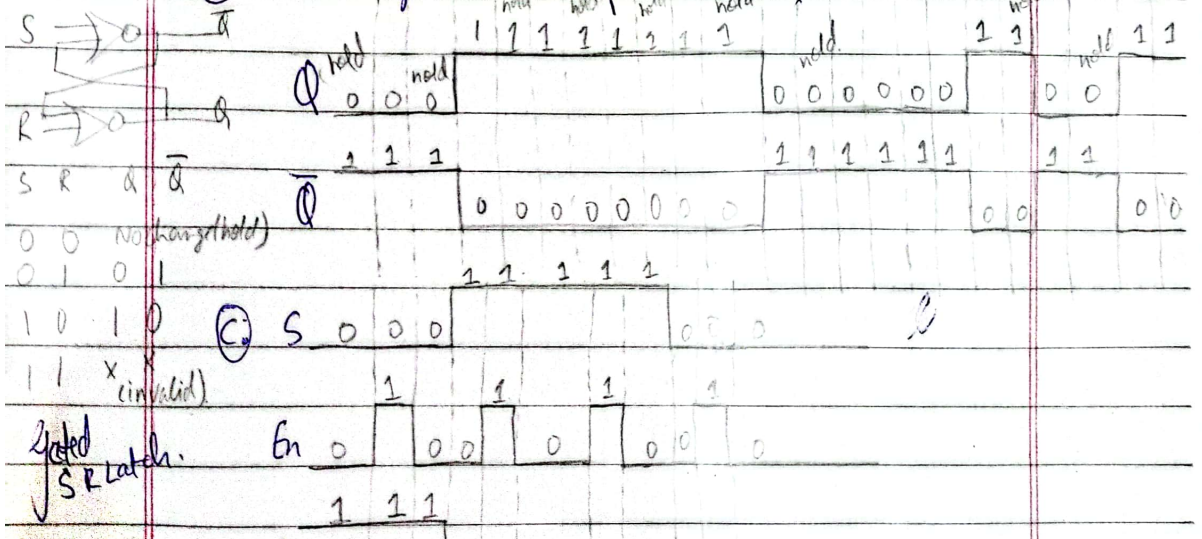
Q1 Latches

(a) Active Low SR Latch. (NAND latch)



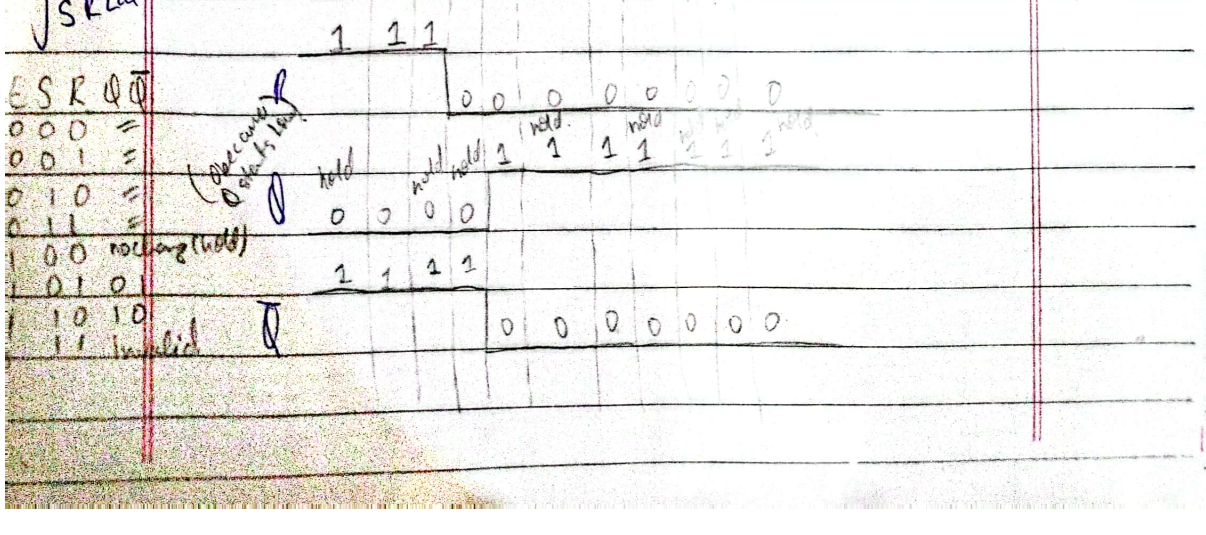
S	R	Q	$\overline{Q}$
0	0	x	x (Not used (invalid))
0	1	1	0
1	0	0	1
1	1	No change (hold)	

(b) Active High SR Latch. (NOR Latch)



S	R	Q	$\overline{Q}$
0	0	No change (hold)	
0	1	0	1
1	0	1	0
1	1	x (invalid)	

(c) Gated SR Latch.



E	S	R	Q	$\overline{Q}$	
0	0	0	=	=	
0	0	1	=	=	
0	1	0	=	=	
0	1	1	=	=	
1	0	0	No change (hold)		
1	0	1	0	1	
1	1	0	1	0	
1	1	1	Invalid		

P	Clk	Q	Q'
1	↑	1	0
0	↑	0	1
1	↓	1	0
0	↓	0	1

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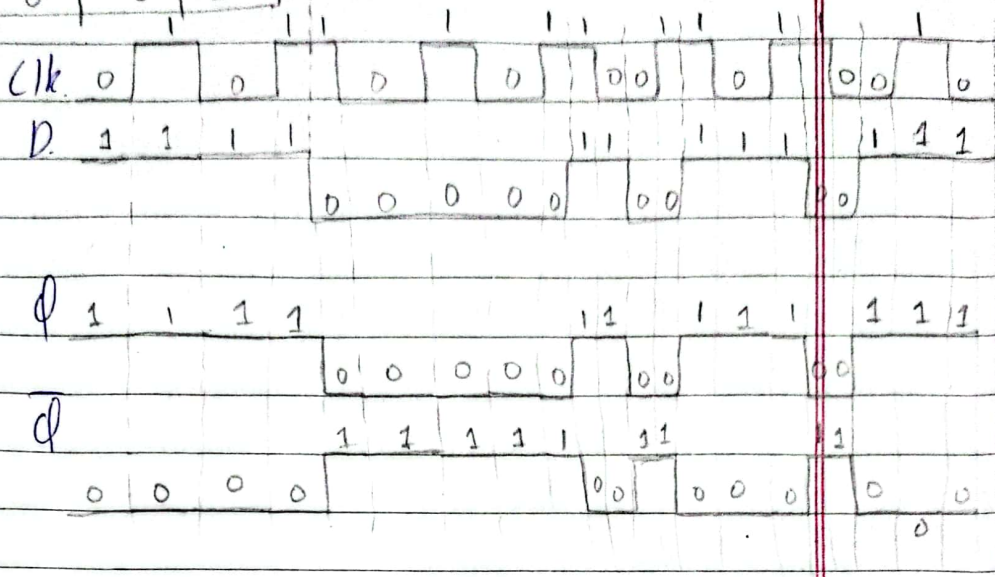
Q2 a.

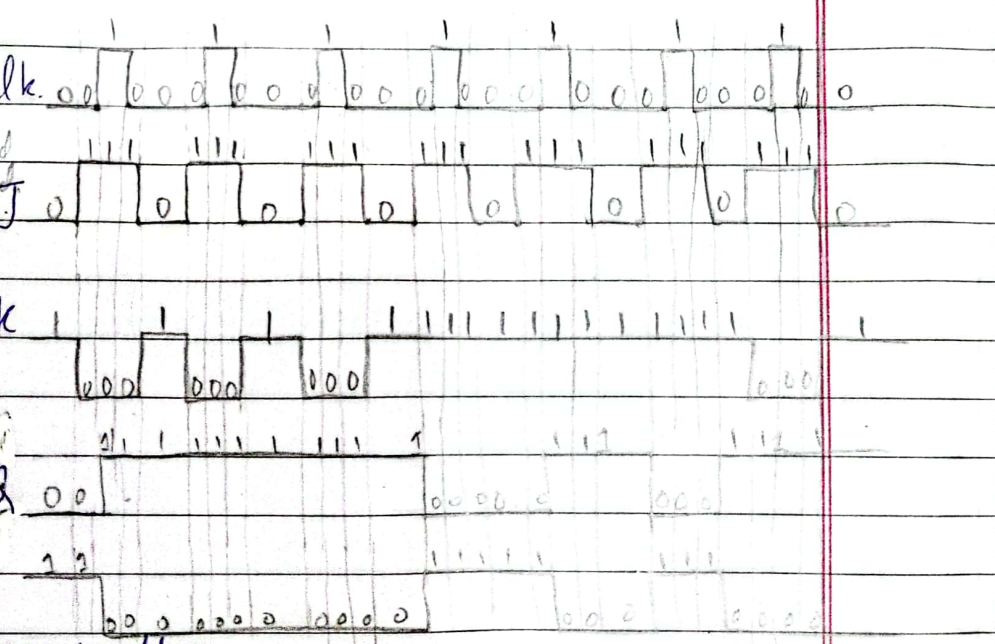


Note.
*Complete one rising T & H duration at last.

b.

Clk	J	K	Q	$\bar{Q}$
0	0	0	No change	
0	0	1	No change	
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	a	
1	1	1	0	1

T flip flop



c. PN flip flop.

– Tabulate the characteristic table,

P	N	Q_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

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- Derive the characteristic table.

PN \ Q_n	0	1
00		
01		1
11	1	1
10	1	

PNQ: 11 D, 100 → P Q'

PNQ: 011, 111 → NQ

$$Q_{n+1} = P\bar{Q}_n + NQ$$

- Tabulate the excitation Table.

Q_n	Q_{n+1}	P	N
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Show how the PN flip flop can be converted to a D flip flop.

P N
Excitation Table

Q_n	Q_{n+1}	P	N
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D
characteristics table.

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

D	Q_n	Q_{n+1}	P	N
0	0	0	0	X
0	1	0	X	0
1	0	1	1	X
1	1	1	X	1

Mapping P on k map.

D \ Q_n	0	1	P = D
0		X	1 0
1		X	1 1
			D.

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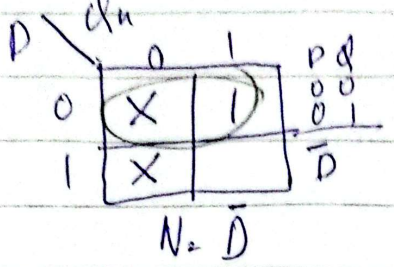
Q2 part a

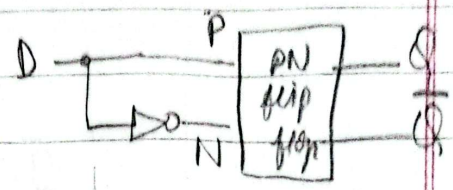
Mapping N on K map.



$P \cdot \bar{D}$

$N = \bar{D}$

D from PN



Q2 part b.