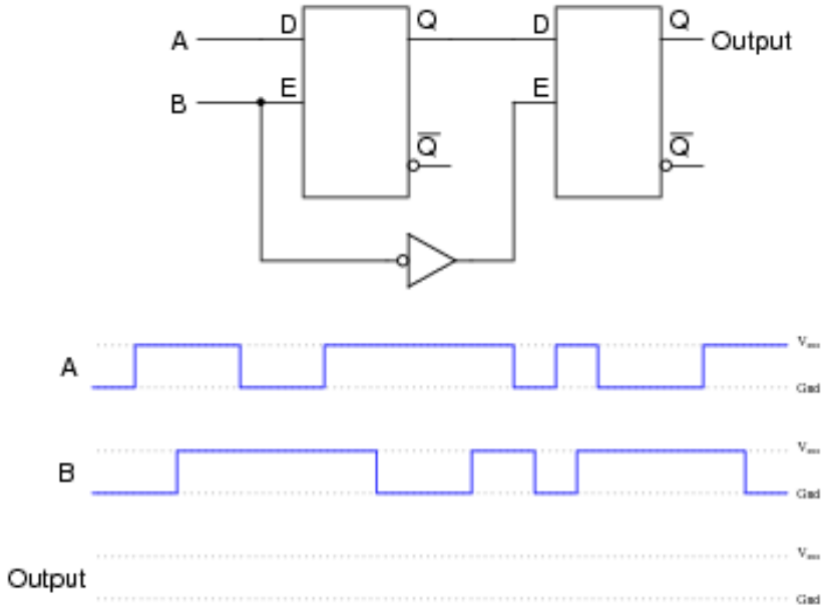
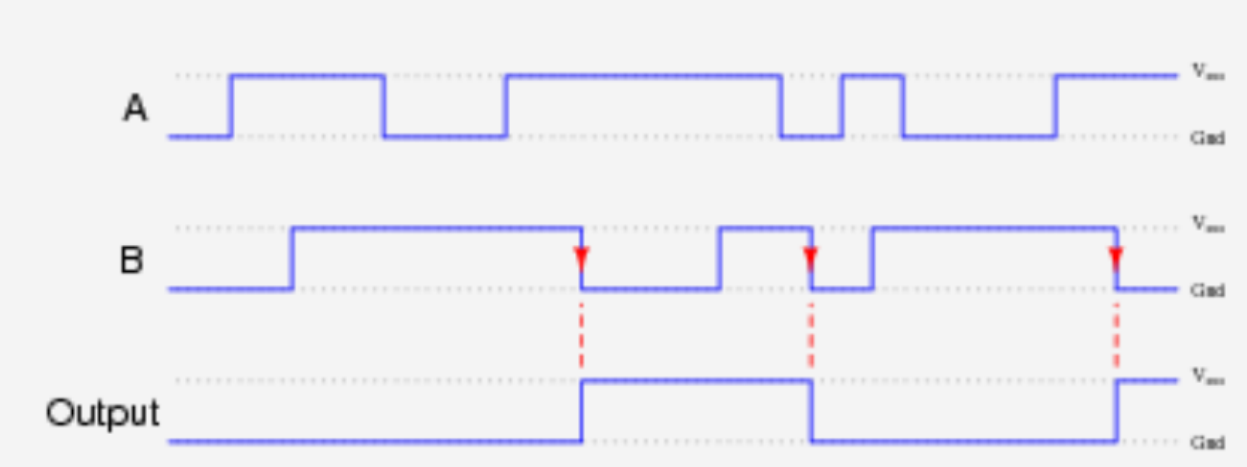
Q:

Determine the final output states over time for the following circuit, built from D-type gated latches:



At what specific times in the pulse diagram does the final output assume the input's state? How does this behavior differ from the normal response of a D-type latch?

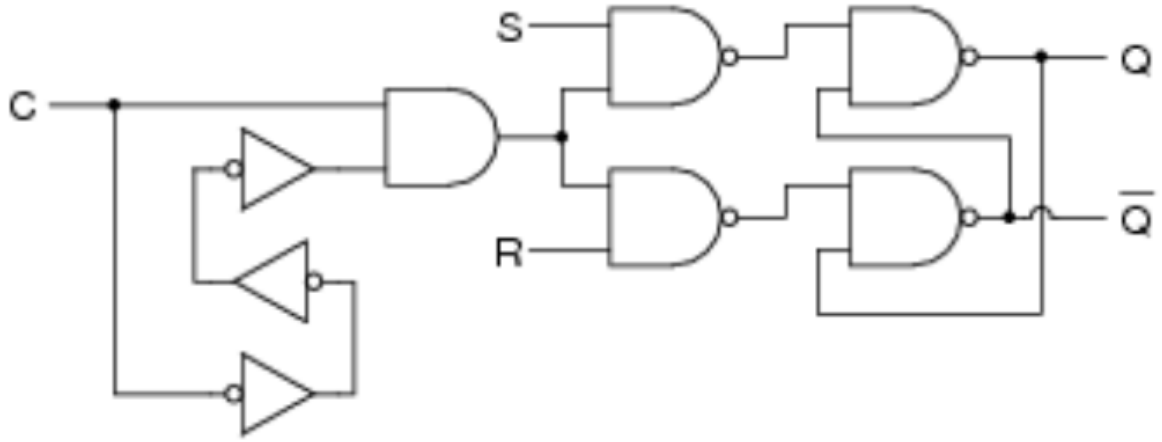
Sol:



The final output assumes the same logic state as the input only when the enable input signal (B) *transitions* from “high” to “low”.

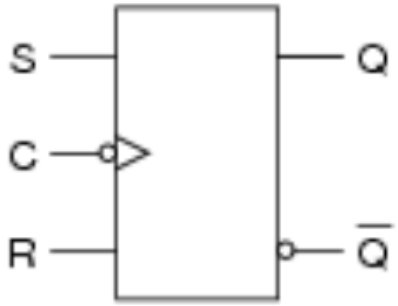
Q.

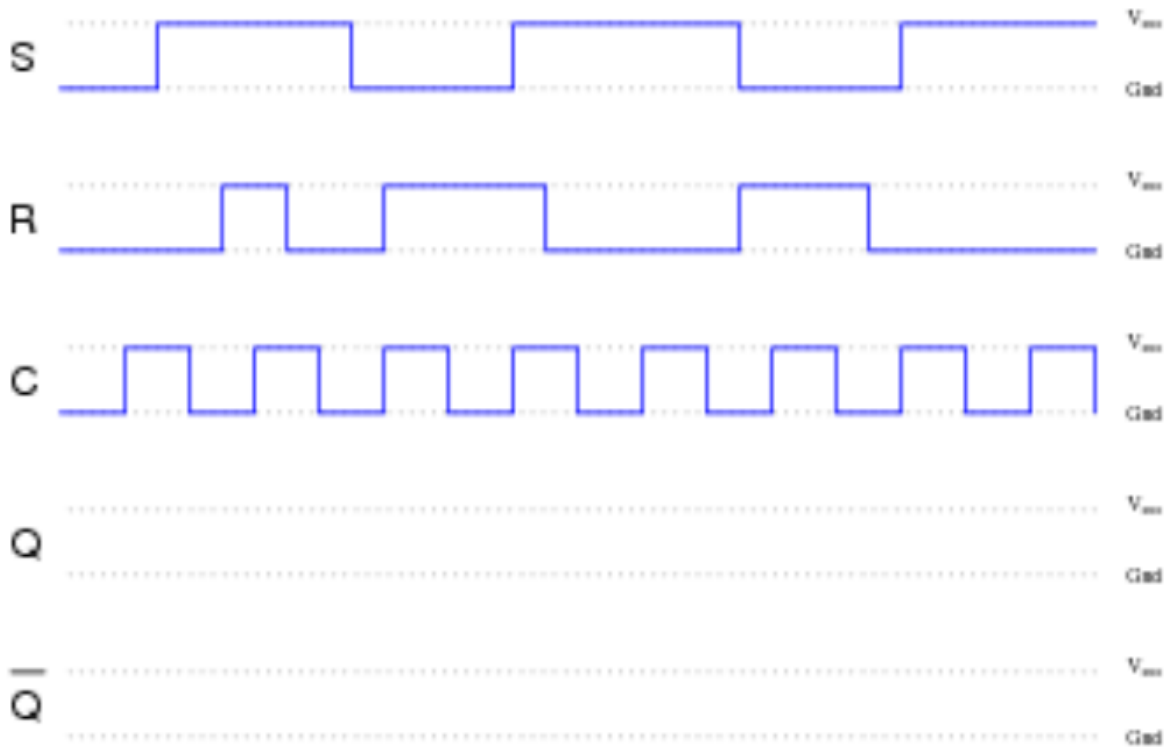
Explain how the addition of a propagation-delay-based one-shot circuit to the enable input of an S-R latch changes its behavior:



Q:

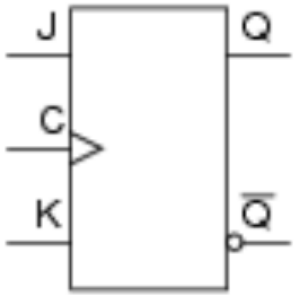
Determine the output states for this S-R flip-flop, given the pulse inputs shown:

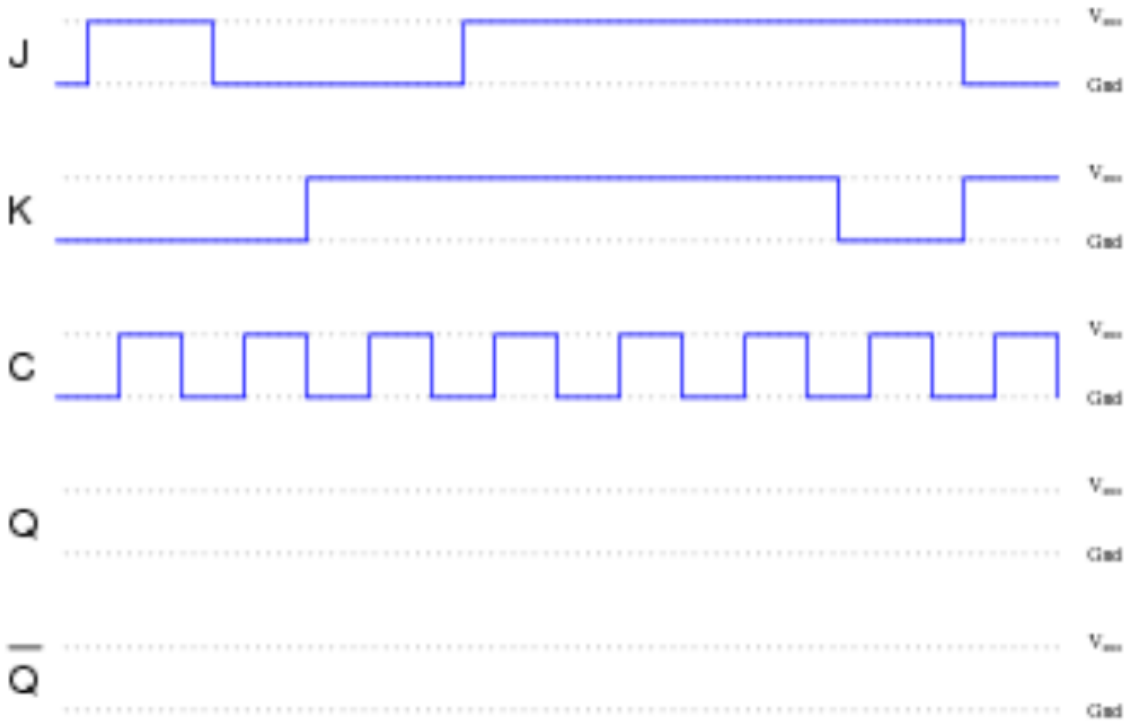




Q:

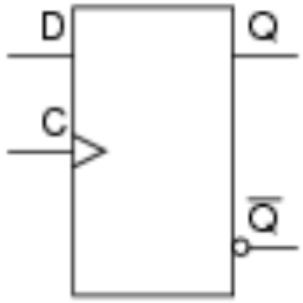
Determine the output states for this J-K flip-flop, given the pulse inputs shown:

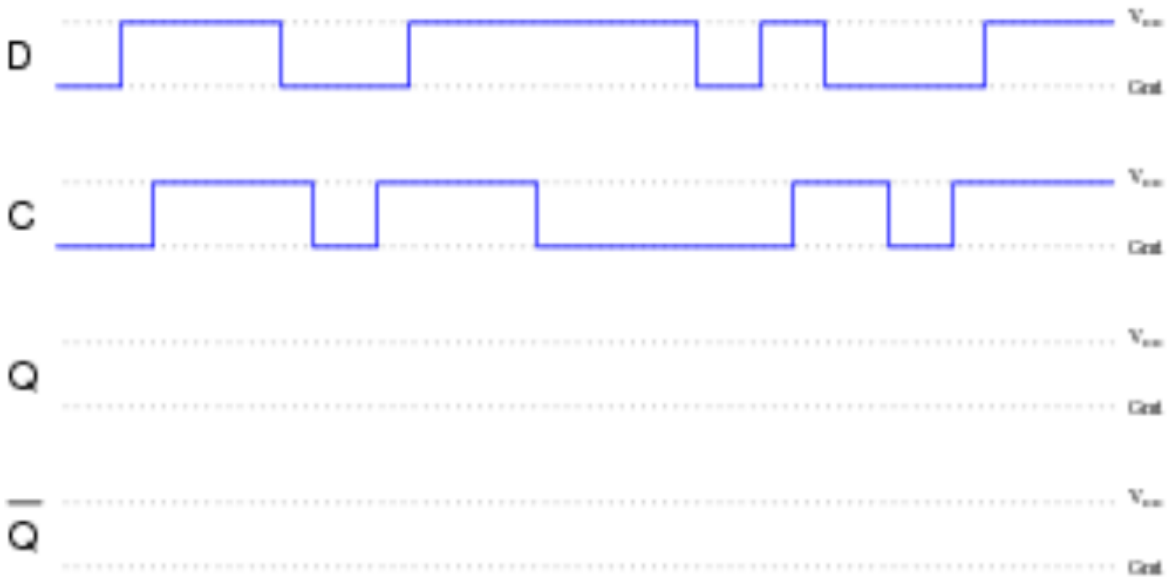




Q:

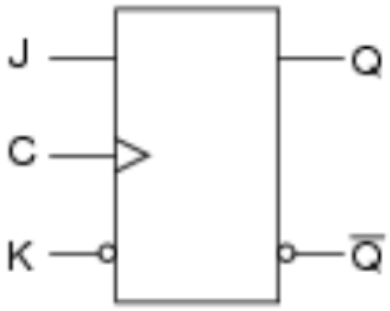
Determine the output states for this D flip-flop, given the pulse inputs shown:

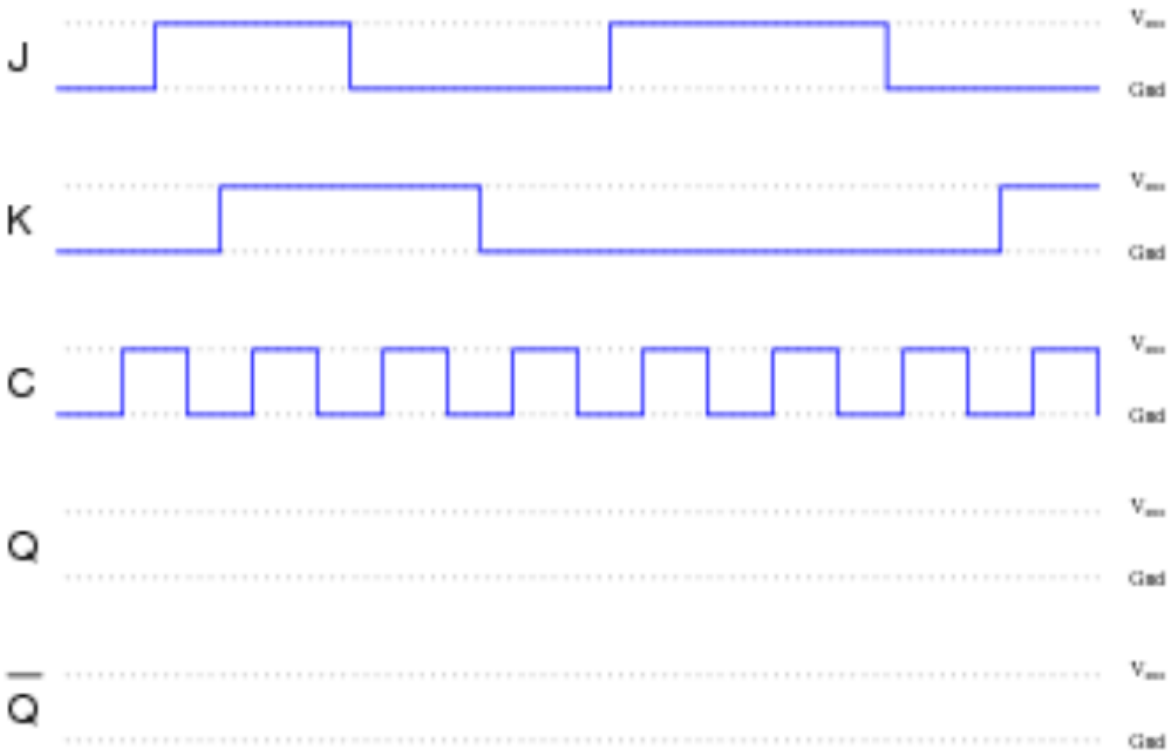




Q:

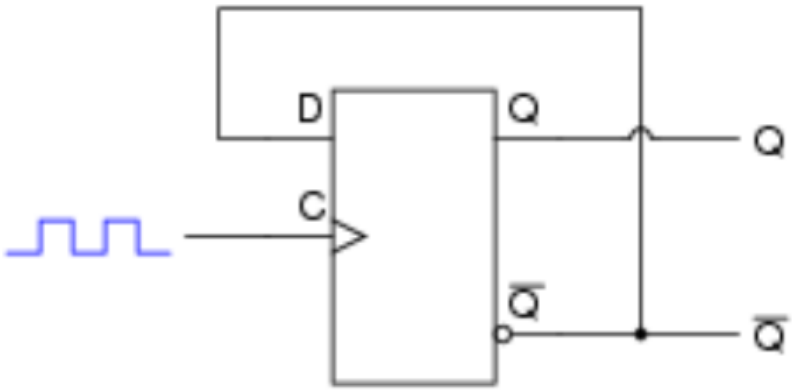
Determine the output states for this J-K flip-flop, given the pulse inputs shown:





Q:

Although the *toggle* function of the J-K flip-flop is one of its most popular uses, this is not the only type of flip-flop capable of performing a toggle function. Behold the surprisingly versatile D-type flip-flop configured to do the same thing:



Explain how this circuit performs the "toggle" function more commonly associated with J-K flip-flops.