## Information Technology University, Lahore, Pakistan

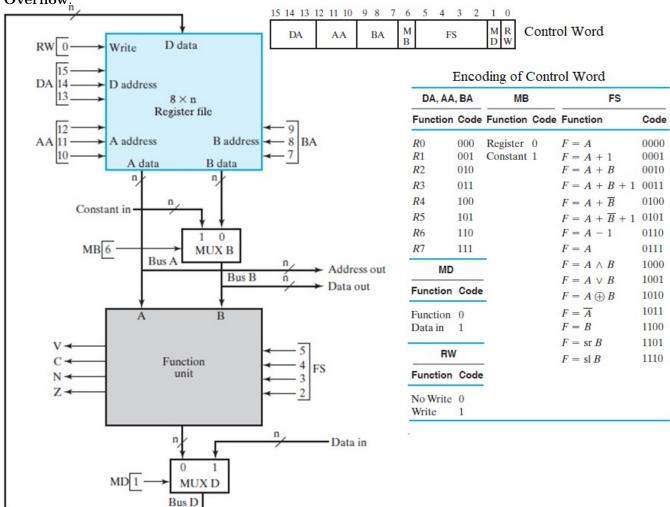
BS Computer Engineering

## Digital Logic Design

Quiz# 1, Spring 2025 Tuesday January 28, 2025

Name:	Roll Number:
Maximum Time Allowed: 20 minutes	Maximum Marks: 10

Assume that Register file (shown below) comprises of eight 4-bit registers, R0, R1, ...., R7. One of the registers is selected as the destination register based on 3-bit control input **DA** (bits 13, 14, 15). None of the registers is selected as destination if bit0 (the RW bit) is 0. Bits 10, 11, 12 are used to select first source register and bits 7, 8, 9 are used to select second source register. The control word and its complete encoding scheme is also shown. **Z**, **N**, **C** and **V** are the single bit flip-flops for **Zero**, **Negative**, **Carry** and **Overflow**.



Block diagram of a simple Arithmetic and Logic Unit with Register file.

Initial values of the registers are shown in the first row in the table below.

- 1. Write down the 16-bit control words (in hexadecimal) for the given sequence of operations in the table.
- 2. Write down the register values (only the updated ones).
- 3. Show the status of flags  $\mathbf{Z}$ ,  $\mathbf{S}$ ,  $\mathbf{C}$  and  $\mathbf{N}$  for each operation in the given table (show only the updated ones).

Perform the following register transfer operations and fill-in the table accordingly:

- 1.  $R3 \leftarrow R1 + R2$
- 2.  $R4 \leftarrow R2 R1$
- 3.  $R5 \leftarrow R5 1$
- 4.  $R0 \leftarrow 0$
- 5. R6  $\leftarrow$  R1 AND R3
- 6.  $R7 \leftarrow R1/2$
- 7.  $R3 \leftarrow M[6]$

Operation	Control Word	R0	R1	R2	R3	R4	R5	R6	R7	Z	$\mathbf{S}$	$\mathbf{C}$	V
Initially	-	10	5	2	-4	4	3	1	-8	0	0	0	0
1													
2													
3													
4													
5													
6													
7													
8													
9													