

20. Using structural modeling, write code for a Verilog module that uses only the nand gate primitive to implement the NAND-only circuit derived in step 4. [2]

```
module my_func (A,B,C,D,F);  
  
    input A, B, C, D;  
  
    output F;  
  
    wire NOT_A, NOT_B, NOT_C;  
  
    wire NOT_A_NAND_NOT_B, NOT_C_NAND_D, ABD, nand1, nand2;  
  
    nand(NOT_A, A, A);  
  
    nand(NOT_B, B, B);  
  
    nand(NOT_C, C, C);  
  
    nand(NOT_A_NAND_NOT_B, NOT_A, NOT_B);  
  
    nand(NOT_C_NAND_D, NOT_C, D);  
  
    nand(ABD, A, B, D);  
  
    nand(nand1, NOT_A_NAND_NOT_B, NOT_A_NAND_NOT_B);  
  
    nand(nand2, NOT_C_NAND_D, NOT_C_NAND_D);  
  
    nand(F, nand1, nand2, ABD);  
  
endmodule
```

21. Write code for a test bench module that tests the above module for all combinations of A, B, C and D. [1]

```
module test_my_func;  
  
    reg A, B, C, D;  
  
    wire F;  
  
    my_func func_1 (.A(A), .B(B), .C(C), .D(D), .F(F));  
  
    initial begin  
  
        A = 0; B = 0; C = 0; D = 0; #100;  
        A = 0; B = 0; C = 0; D = 1; #100;  
        A = 0; B = 0; C = 1; D = 0; #100;  
        A = 0; B = 0; C = 1; D = 1; #100;  
        A = 0; B = 1; C = 0; D = 0; #100;  
        A = 0; B = 1; C = 0; D = 1; #100;  
        A = 0; B = 1; C = 1; D = 0; #100;  
        A = 0; B = 1; C = 1; D = 1; #100;  
  
    end  
  
endmodule
```

A = 1; B = 0; C = 0; D = 0; #100;

A = 1; B = 0; C = 0; D = 1; #100;

A = 1; B = 0; C = 1; D = 0; #100;

A = 1; B = 0; C = 1; D = 1; #100;

A = 1; B = 1; C = 0; D = 0; #100;

A = 1; B = 1; C = 0; D = 1; #100;

A = 1; B = 1; C = 1; D = 0; #100;

A = 1; B = 1; C = 1; D = 1; #100;

end

endmodule

22. Fill in the truth table of G in Table 4.2 according to the timing waveforms obtained after running the simulation. Verify that the truth table corresponds to the minterms of G. Show simulation results to the lab engineer to obtain credit.[2]

23. Take clear screenshots of code of all modules of this task and the simulation timing waveforms and paste them in your WORD file such that all fit on no more than two pages. Make sure that screenshots are legible.



