	Assignment #4. Such	Apriz 23058
Dates	Assignment # 4. Seets Digital Logic Design	
	Dystal Logic Design	o de estado en estado en la compansión de la compansión de la compansión de la compansión de la compansión de La compansión de la compa
Q1	DA - 3 bits to select the regreter.	R4
Andread Control of the State of	AA - 3 bits to select me negrote for Bus A	K.1
	BA -3 bits to select the register for Bus BonMUX	
	MB - I bit to select b/w register data on court.	"YY
1996 Adalahan Santanan Santan	FS - 4 sits to control me ALU operation	ridip
	MO - 1 bit to select B/W ALU output	ontpu
	RW-1 bit to brothe sogists witing.	wirte
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(a)	R4 < R1 + R3 DA AA BA MB FS MD RW	
	100 001 011 0 0010 0 1	
	Binary = (1000010110001001)2	
	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	
	Hanadleimal 2 (8589)16	
(b)	R3 < Data in	
(-)	DA AA BA MB FS MP RW	
	011 000 000 0 0000 1 1	
	Binary 2 (011 000 000 0000 011)2	
	0110 0000 0000 0011	
	22 20	
	6 0 0 3	
	Henadecimal = (6003)11	

Date:_					Day:	purpolarizate (no significate) no com significación de proposate (no significación de constitución de constitu	
(c)	R1 = SIRU DA AA	BA 1	MB FS	MD	RW		
	001 000 Binary 2 0					and the second second second second second second	
	3 (a	010 0010	2011100	_)*			
			And a substitute of control of co	001			
	2'	2' 2		2°			
	2	2	3	7			
	Henadecima	0 =	122391	14			
	p v vacoopy a		(				
(d)	R3 €0					/	
	DA AA				RW		
	Binary = (01100000000101001)2						
	Binary 2	0110000	0001010	0 ( ) 2		A CONTRACTOR OF THE CONTRACTOR	
	0110	0000	0010	1001			
	222		2'	23	2°		
	22'			8+1	,		
	6	0	2	9			
		1/10	2 9/11	•			
	Henaderimal = (6029)16						
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