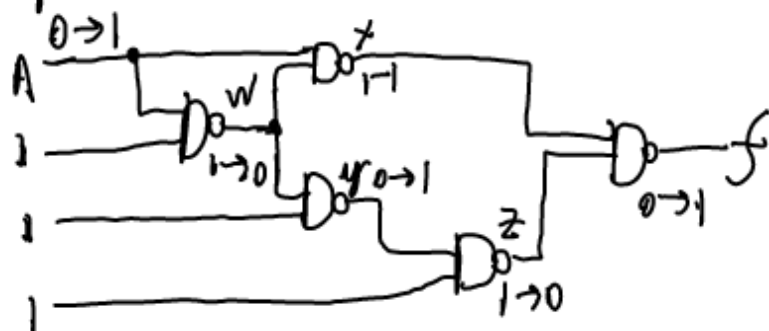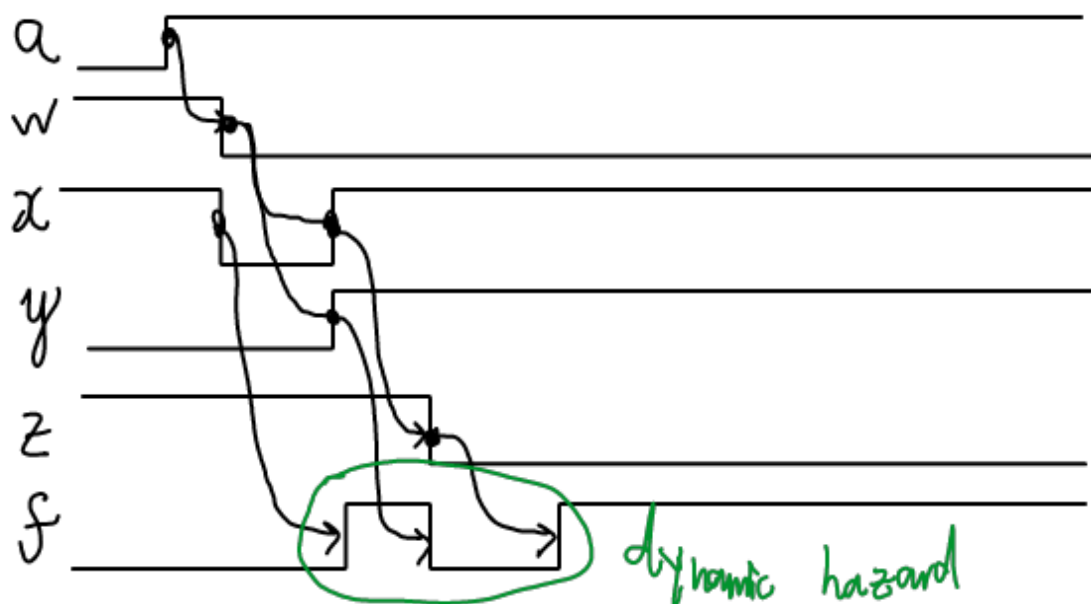# Dynamic hazards in multi-level circuits

* All NANDS have a delay of 1 ns.

dynamic hazard

Races

* Occurs in asynchronous circuits when ≥ 2 state variables need to change at the same time. due to change in an input.

⟹ Due to delays in circuits, the variables might not change at the same time.

⟹ could cause a problem → you might reach an unexpected state.

Races can be <u>critical</u> or <u>non-critical</u>.

exists and is a problem
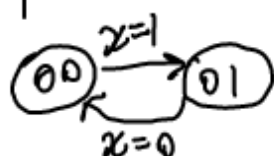
(i.e., you might end up in wrong state)

exists but is not a problem.

(i.e., you endup in correct state regardless of delays)

Consider the following transition table.

Curr state $y_1 y_0$	next state (y_1, y_0)	
	$x=0$	$x=1$
00	⟨00⟩	11
01	00	⟨01⟩
11	00	01
10	00	11

Assume 00 and $x=0$
Change x from $0 \to 1$

⟨00⟩ → 11 → ⟨01⟩

⟨00⟩ → ⟨01⟩

⟨00⟩ → 10 → 11 → ⟨01⟩

<u>non-critical</u>

Consider

$y_1 y_0$	next $y_1 y_0$	
	$x=0$	$x=1$
00	⟨00⟩	11
01	00	11
11	00	⟨11⟩
10	00	⟨10⟩
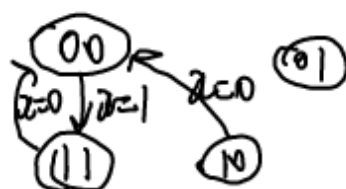
⟨00⟩ → ⟨11⟩

⟨00⟩ → ⟨10⟩ *** <u>critical race</u>

00 → 01 → ⟨11⟩

Races don't exist in <u>flowtables</u>

Therefore races are a consequence of <u>state assignment.</u>
So, if you want to avoid races, avoid assigning state
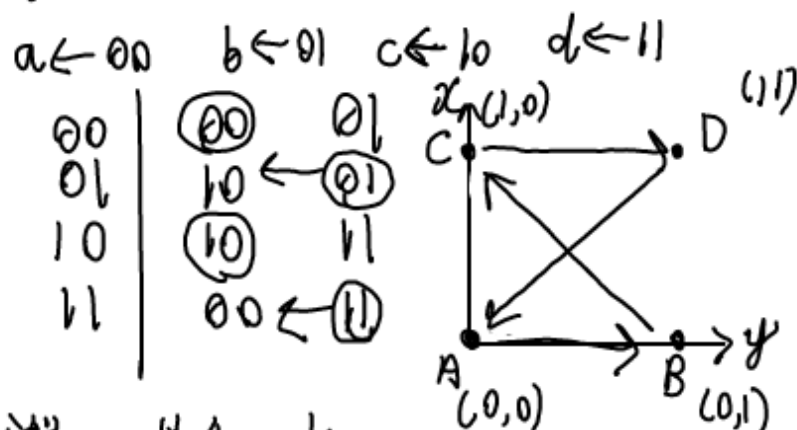values whice require multiple bits to change.
  ⟹ This will avoid all races.

<u>Race free State Assignment</u>

* Preemptive — do state assignment, which avoids <u>all</u> races.

Curr state	Next state X=0	X=1
a	ⓐ	b
b	c	ⓑ
c	ⓒ	d
d	a	ⓓ

Consider

$a \leftarrow 00 \quad b \leftarrow 01 \quad c \leftarrow 10 \quad d \leftarrow 11$

00	⓪⓪	01
01	10	⓪1
10	⑩	11
11	00	⑪

"untwist" so that only on variable changes to switch states.

00	⓪⓪	01
01	11	⓪1
11	⑪	10
10	00	⑩

* Can't always "untwist" the diagram without adding states *
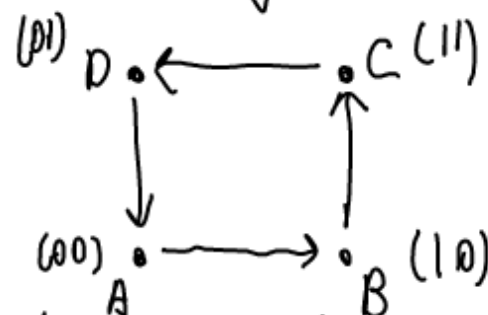
	$X_1X_2=00$	01	10	11
A	Ⓐ	Ⓐ	C	B
B	A	Ⓑ	D	Ⓑ
C	Ⓒ	B	Ⓒ	D
D	C	A	Ⓓ	Ⓓ
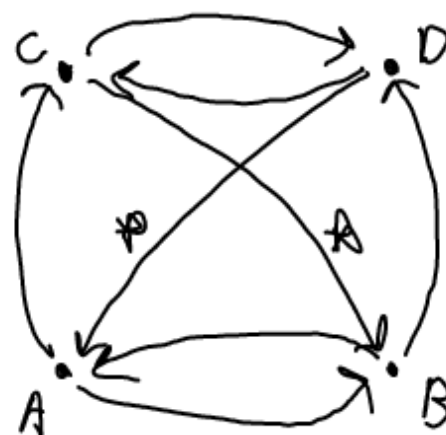
* no way to untwist this situation *

⟹ Always a race if you only use 2-bits.

Method 1: Use one-hot encoding

Consider transition from state $i \rightarrow$ state j

$$00..010--0 \rightarrow 00..010----0$$

$\uparrow$ i $\uparrow$ j

$\Rightarrow$ Exactly 2-bits change in any state to state transition.

$$00..010--010-- \Leftarrow \text{new temporary state}$$

         i j

0001	A	Ⓐ	Ⓐ	E	F
0010	B	F	Ⓑ	G	Ⓑ
0100	C	Ⓒ	H	Ⓒ	I
1000	D	I	J	Ⓓ	Ⓓ
0101	E			C	
0011	F	A			B
1010	G			D	
0110	H		B		
1100	I	C			D
1001	J		A		