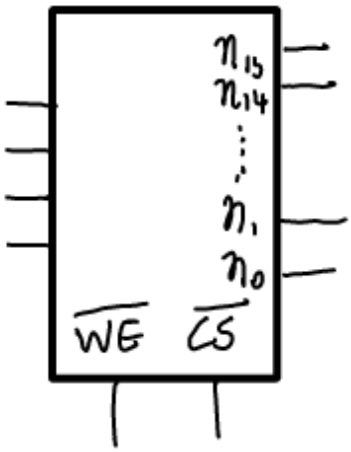

addr pins = $\log_2$ # pins

$\overline{CS}$ - chip select (active low)

$\overline{WE}$ - write enable (active low)

- Internal View
  - see handout
- The decoder selects a word line (makes it '1')
  - that selects a row of cells

4.1) Large Memory Chips

e.g. 2M words x 8 bits

2^{21} words x 8 bits/word
$= 2^{24}$ bit cells
$= 16$ M bits
$= 4096 \times 4096$ bits

- a 21×2097152 decoder would be slow
- instead arrange cells in a symmetric array (4096×4096) with 512 words / row
- see digram on handout.
- the row addr and column addr. share address pins (time multiplexed)
  - first row addr is given, then the col addr
  - latches save these addresses and are controlled by the Row Address Strobe ($\overline{RAS}$) and Col Address Strobe ($\overline{CAS}$)

- with Async DRAM, the controller is external to the memory chip
- see Async DRAM timing diagram

share same 12 pins

4096 rows $\Rightarrow \log_2(4096)$ row addr bits $= 12$ (A_{20-9})
512 cols $\Rightarrow \log_2(512)$ col addr bits $= 9$ (A_{8-0})

4.2) Fast Page Mode (FPM)

- a latch is added to the sense/write circuit, the whole row is latched
  - (consecutive) words within some row can be read without re-selecting the row
- most DRAM's were asynchronous until mid-90's.

4.3) Synchronous DRAM (SDRAM)

- has internal controller timed to memory bus
- programmed for burst of 1, 2, 4, 8 words
- see timing diagram for 2-word burst
  - only initial col is needed

4.4) Double Data Rate (DDR) SDRAM

- data is transferred on the rising & falling clock edges

5) Memory Metries

- latency: # cycles from $\overline{RAS}$ until first word is produced (5 cycles in diagrams)
- bandwidth: volume of data per unit time
  e.g. word size = 8 bytes, clock speed = 200 MHz, burst size = 2.

Async DRAM:

2 words × 8 bytes/word × 200 MHz/12 = 267 MB/s

Async FPM DRAM:

2 words × 8 bytes/word × 200 MHz/9 = 356 MB/s

SDRAM:

2 words × 8 bytes/word × 200 MHz/7 ≈ 457 MB/s

DDR SDRAM:

2 words × 8 bytes/word × 200 MHz/6 ≈ 533 MB/s

e.g. PC3-12800

- 800 MHz Clock

⇒ 1600 MT/s × 8 bytes/transfer = 12800 MB/s

6) Memory Modules

- DMM: dual inline memory module
- several mem. chips are combined on a PCB (printed circuit board)