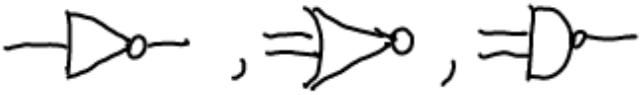
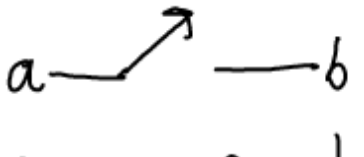
CMOS → Pull up & pull down

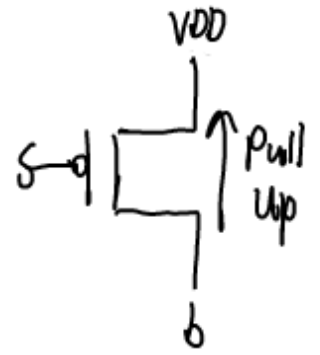
→ implementation of 

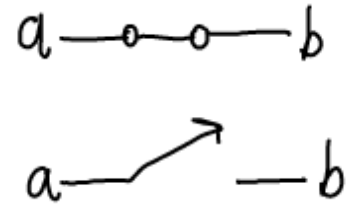
Transistors

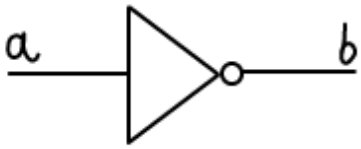
NMOS



PMOS

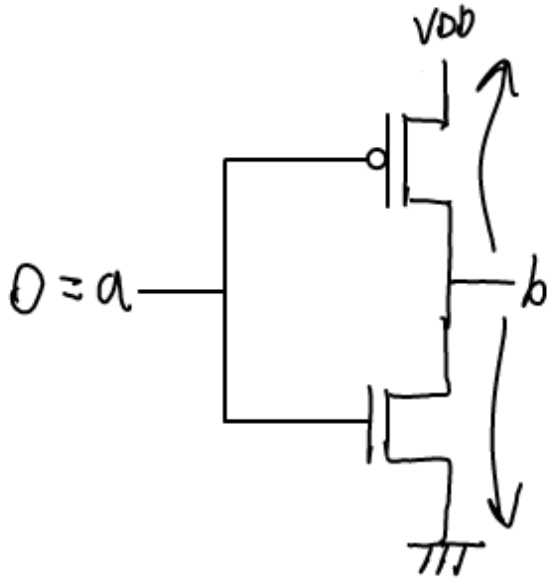




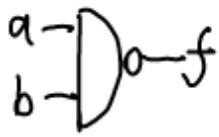


$b = \bar{a}$

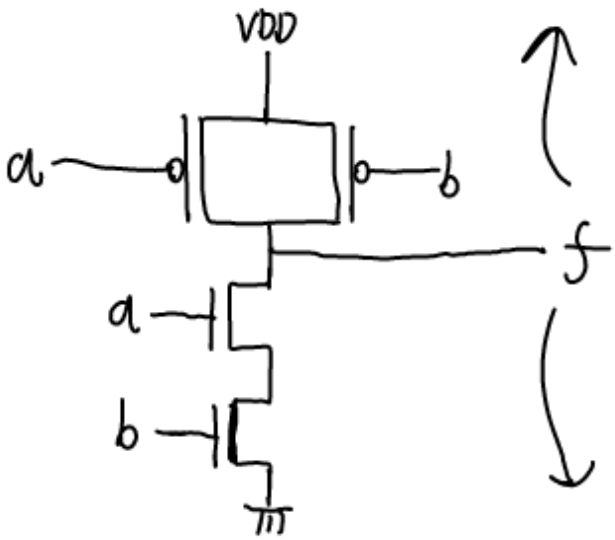
a	b
0	VDD
1	0 (G-D)



NAND



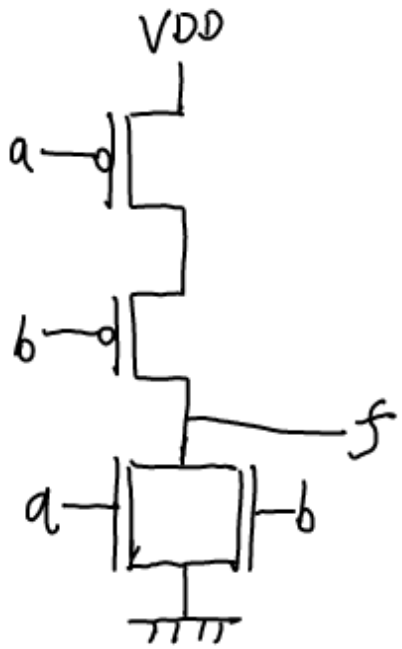
a	b	f
0	0	1
0	1	1
1	0	1
1	1	0



CMOS is always dual (Pull up / Pull down)
- ensures to never have a short circuit from VDD to GND

NOR

a	b	f
0	0	1
0	1	0
1	0	0
1	1	0

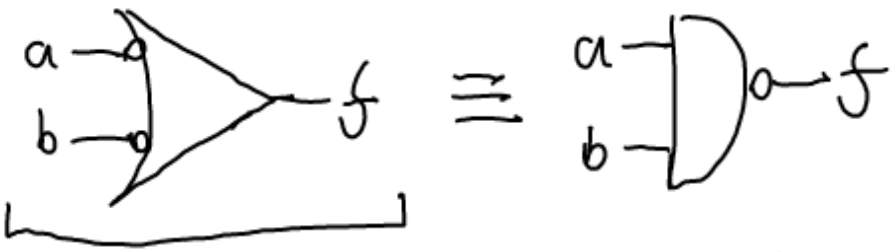


NOT = 2
NOR = 4
NAND = 4
AND = NAND + NOT = 6
OR = NOR + NOT = 6

# of transistors

Cost: should consider transistor count.
How to convert to NAND only or NOR only.

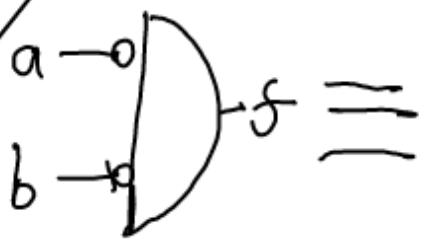
Key idea

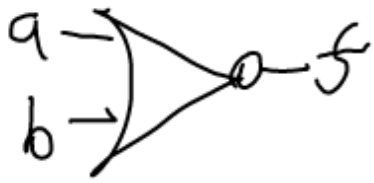


a	b	f
0	0	1
0	1	1
1	0	1
1	1	0

$f = (\bar{a} + \bar{b})$

$= \overline{(ab)}$





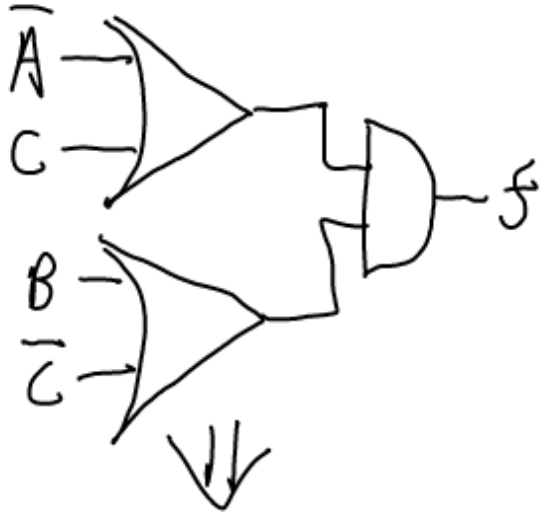
a	b	f
0	0	1
0	1	0
1	0	0
1	1	0

$f = (\bar{a}\,\bar{b})$

$= \overline{(a+b)}$

POS

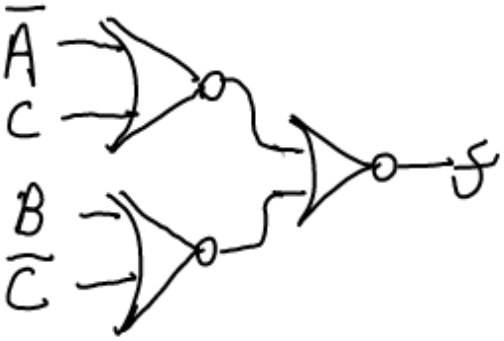
$f = (\bar{A}+C)(\bar{C}+B)$



$f = \left[[(\bar{A}+C)(\bar{C}+B)]' \right]'$

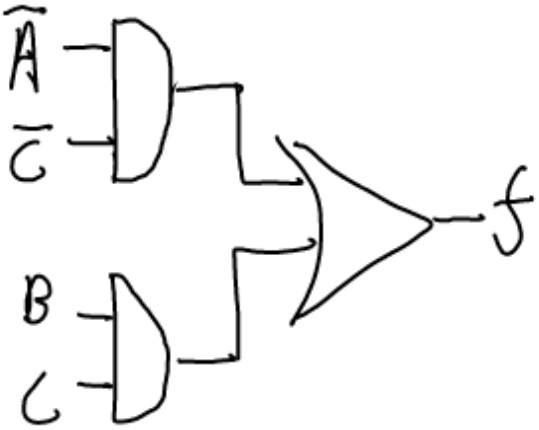
$= \left[\bar{X}+\bar{Y} \right]'$

$= \left[\overline{(\bar{A}+C)} + \overline{(\bar{C}+B)} \right]'$



SOP NAND

$f = \bar{A}\bar{C} + BC$



$f = \left((\bar{A}\bar{C} + BC)' \right)'$

$= \left(\overline{(\bar{A}\bar{C})(BC)} \right)'$