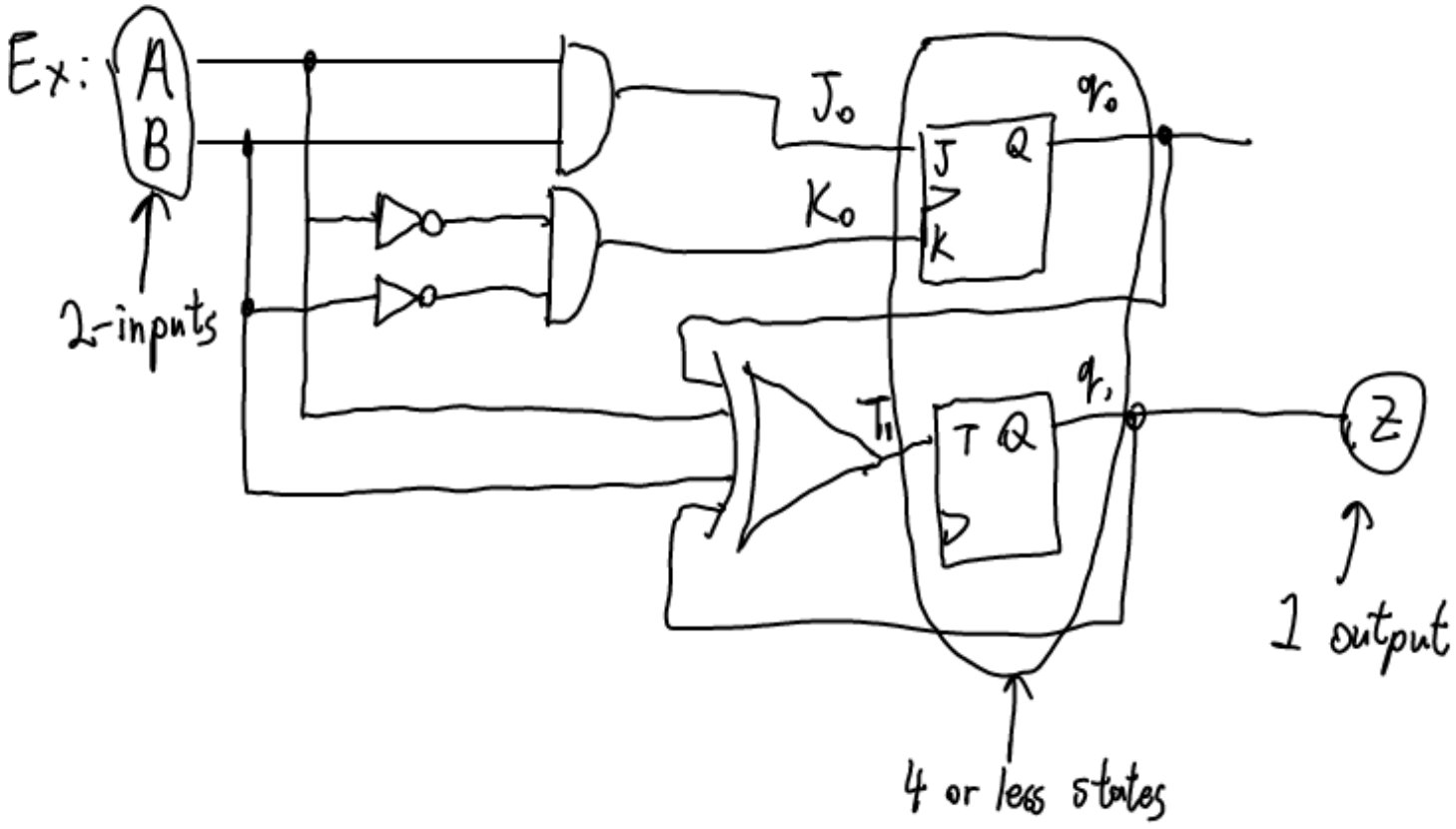
Clocked Sequential Circuit Analysis

* Reverse of design - given a circuit, derive the state diagram.

Procedure: 1) Identify flip flops that hold the state info.
2) Identify outputs
3) Write down logic-eqns for outputs && FF inputs.
(FF input eqns help me figure out the next state)
* get state diagram & state table *



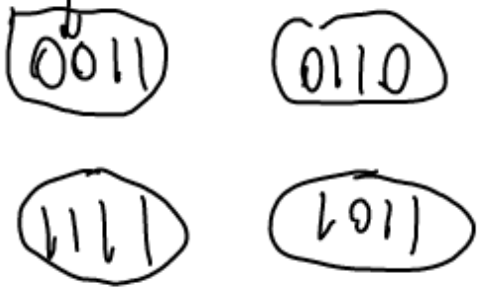
eqns: $Z = q_1$

$T_1 = A \oplus B \oplus q_0 \oplus q_1$

$J_0 = A \cdot B$

$K_0 = \overline{A} \cdot \overline{B}$

$q_1 q_0$



Need the transitions *

Curr. state $q_1 q_0$	T_1 (AB: 00 01 10 11)	$J_0 K_0$ (AB: 00 01 10 11)	next state (q_0, q_1) (AB: 00 01 10 11)
0 0	0 1 1 0	01 00 00 10	00 10 10 01
0 1	1 0 0 1	01 00 00 10	00 10 10 01
1 0	1 0 0 1	01 00 00 10	10 01 01 11
1 1	0 1 1 0	01 00 00 10	10 01 01 11

T	Q
0	Q
1	$\overline{Q}$

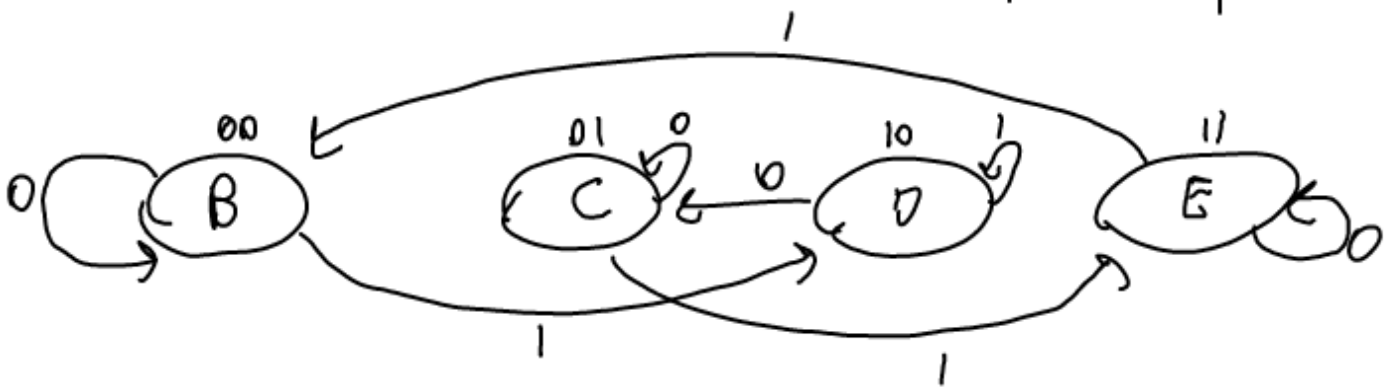
J K	Q
0 0	Q
0 1	0
1 0	1
1 1	$\overline{Q}$

Impact of FF selection on design procedure.

* The type of FF you pick can have an impact on the circuit complexity.

e.g., design a circuit for the following state table using each type of FF.

Curr. state $q_1 q_0$	next state (q_1, q_0) A=0	next state (q_1, q_0) A=1	DFF FF Inputs (d_1, d_0) A=0	DFF FF Inputs (d_1, d_0) A=1	TFF FF Inputs (d_1, d_0) A=0	TFF FF Inputs (d_1, d_0) A=1	J_1 K_1 A=0	J_1 K_1 A=1	J_0 K_0 A=0	J_0 K_0 A=1
B 0 0	00	10	00	10	00	10	0X	1X	0X	0X
C 0 1	01	11	01	11	00	10	0X	1X	X0	X0
D 1 0	01	10	01	10	11	01	X1	X0	1X	0X
E 1 1	11	00	11	00	00	11	X0	X1	X0	X1



Aside for JK

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

→

J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

→

J	K	Q(t)	Q(t+1)
0	X	0	0
1	X	0	1
X	0	1	1
X	1	1	0