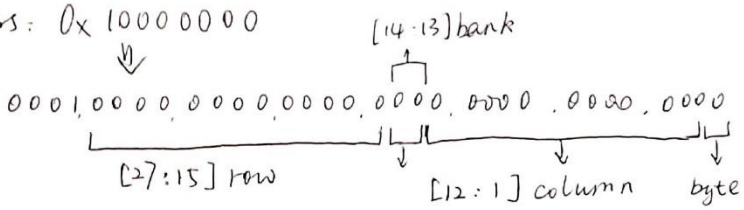
ECE #720 HW #6 Zhiping Wang 20026505

Prob. #1

Transaction 2 (1) address: 0x 10000000



(1) row high

(2) Data width: 16 bits ⇒ 2 bytes aword ⇒ 1 byte bit.

(3) column address width: 12 ⇒ [12:1]

(4) bank addr. width: 2 ⇒ [14:13]

(5) row addr. width: 13 ⇒ [27:15]

(2): /* did not specify what kind of latency */

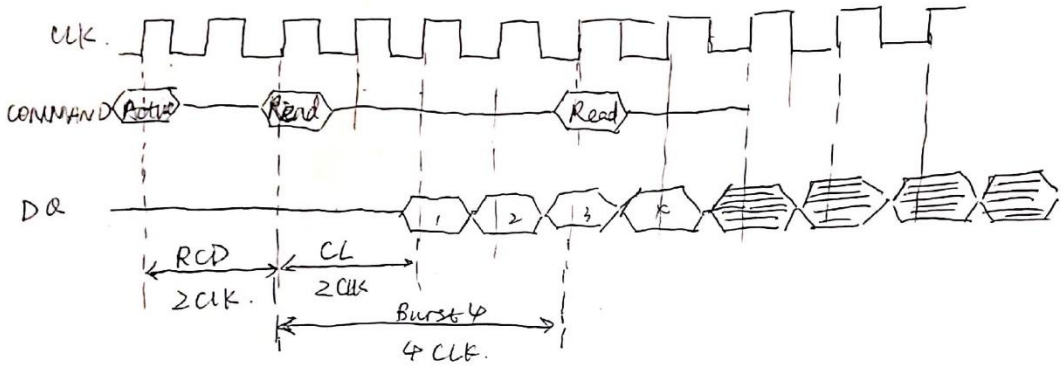
Accessing to same row and bank, commands: "Active, Read, Read"

latency between two transactions = burst 4 latency = 4 clock cycles,

(Frequency - 100 MHz ⇒) = 40 ns

Latency between "Read" and data output = CAS = 2 clocks

= 20 ns



(3):

Simulation latency: 100 ns There is discrepancy.

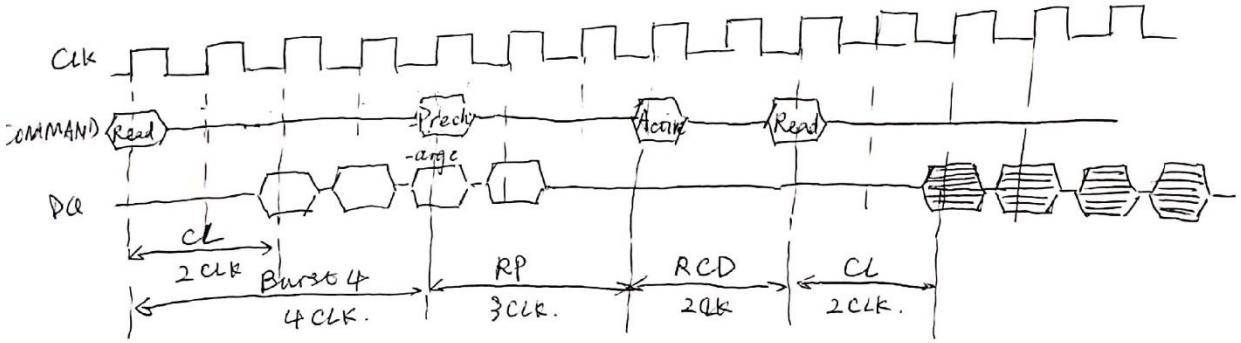
Transaction 3

(1) addr: 0x10008000 ⇒ row bits: "...001" different row

(2): Latency between two transactions: "Read, precharge, Active, Read"

burst 4 + RP + RCD = (4 + 3 + 2) = 9 clocks

= **90 ns**



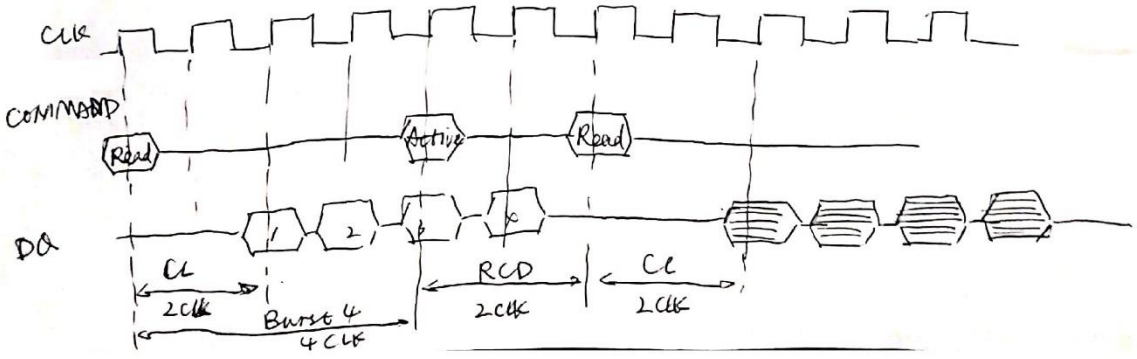
(3) simu. latency = 150 ns There is discrepancy.

Transaction #4

(1) address: 0x10002000 ⇒ bank address "01" different bank.

(2) Latency ⇒ commands: "Read Active Read"

burst 4 + RCD = 6 clocks = **60 ns**



(3) simu. latency = 100 ns There is discrepancy