Weichao Zhou

Date of Birth: 03/12/1990 Phone: 8672507548 Email: zwc662@bu.edu

Technical Skills

C/C++, Python, Perl, Shell Script, Java, Verilog, Verilog-A

Education

Fudan University 09/2012-06/2015

•Master of Science in Solid State Electronics, 2nd Scholarship Sponsored by Micron, Inc.

Fudan University 09/2008-07/2012

•Bachelor of Science in Microelectronics

Work Experience

Micron Technology, Inc. *Product Engineer* 05/2015-06/2016

UFS Product Verification

- Designed test cases according to JEDEC, SCSI, and product specifications for the verification of the latest UFS product, and writing test programs in Python.
- Set up test environment on Linux platforms for UFS Product Verification teams and UFS Firmware Development teams and wrote Shell Scripts to achieve test automation.
- Used JIRA to collaborate with teammates for Agile Development of the test programs.

3D NAND Product Validation

- Ran bench test by writing test scripts in Perl.
- Probed the wafer and control the Agilent Test Platform by writing test programs in C++ and Assembly Code.

Fudan University, *Teaching Assistant* 03/2013-06/2013

- Worked as TA of the course *Integrated Circuit technology Experiments.*

Project Experience

FinFET (Fin Field-Effect Transistor) Project 01/2014-01/2015

- Worked on designing a new FinFET with a U-shape channel and simulated by using Sentaurus software.
- Built compact model for this FinFET and used HSPICE to do circuit simulation.

TFET (Tunneling Field Effect Transistor) Project 03/2012-01/2014

- Fabricated and tested TFETs in cleanroom and simulated with Sentaurus software, aiming at enhancing the performance of TFETs and studying the possibility of practical industrial application.
- Collaborated with Chinese fab Huahong-NEC to fabricate TFET samples.

Evaluation of Buffer Organizations for Network-on-Chip 09/2010-05/2011

- Analyzed performance of the Network-on-Chip systems by changing the allocation and routing of virtual data channels and data buffer sizes under fixed buffer resources.
- Designed algorithms according to Queue Theory, and wrote C programs to realize.

• Papers

1. Wei-Chao Zhou, Peng-Fei Wang and David Wei Zhang, "A sub-10nm U-shape FinFET design with

suppressed leakage current and DIBL effect," Semiconductor Technology International Conference (CSTIC), 2015 China, Shanghai, 2015

2. W. C. Zhou et al., "Investigation of spin-on-dopant for fabricating high on-current tunneling field effect transistor," Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on, Guilin, 2014

3. M. Jing, P. Ren, W. Zhou, Z. Yu and X. Zeng, "Evaluation of buffer organizations for network-on-chip," Solid-State and Integrated Circuit Technology (ICSICT), 2012 IEEE 11th International Conference on, Xi'an, 2012, pp. 1-3.