**Weichao Zhou**

(857) 250-7548 Email: [zwc662@gmail.com](mailto:zwc662@gmail.com)

3 Ashford Ct, Allston, Boston, MA 02134, USA

LinkedIn: <https://www.linkedin.com/in/zhou-weichao-83a16bb6/>

Github: <https://github.com/zwc662>

**RESEARCH INTERESTS**

* Artificial Intelligence, Reinforcement Learning
* Formal Methods

**EDUCATION**

**Boston University**

* M.S in Computer Engineering 09/2016-present

**Fudan University**

* M.S in Microelectronics 09/2012-06/2015

**Fudan University**

* B.S in Microelectronics  09/2008-06/2012

**WORK & RESEARCH EXPERIENCE**

**Safety-Aware Inverse Reinforcement Learning** 09/2016-present

* Conducting a research on combining formal verification and inverse reinforcement learning to build up a safety-aware AI framework.

**Micron Technology, Inc.**, Product Engineer 05/2015-07/2016

* Designed test cases and wrote test scripts in Python to verify eMMC and UFS products.
* Wrote test programs and scripts in C++ and Perl to test NAND memory circuits.

**TFET’s (Tunneling Field-Effect Transistor) Application on Memory** 03/2012-01/2014

* Cooperated with semiconductor chip manufacturer to fabricate TFET units and DRAM cells based on TFETs.

**FinFET (Fin Field-Effect Transistor) Project** 01/2014-06/2015

* Used Sentaurus to simulate a new FinFET structure and used SPICE to simulate circuits based on the new FinFETs.

**High frequency AlGaN/GaN HEMT (High-electron-mobility Transistor) on Silicon Substrate** 05/2014-06/2015

* Fabricated high-frequency AlGaN/GaN HEMTs on Si substrate for RF circuit applications.

**Evaluation of Buffer Organizations for Network-on-Chip** 09/2010-05/2011

* Applied queueing theory to analyze Network-on-Chips performance under different allocations of virtual channels and channel buffer resources.

**PUBLICATIONS**

1. **Weichao Zhou,** Wenchao Li, “**Safety-Aware Apprenticeship Learning**”, International Conference on Computer-Aided Verification (CAV), 2018. <https://arxiv.org/abs/1710.07983>
2. **Weichao Zhou**; Peng-Fei Wang; Zhang, D.W., **"A sub-10nm U-shape FinFET design with suppressed leakage current and DIBL effect,"** in Semiconductor Technology International Conference (CSTIC), 2015 China , vol., no., pp.1-3, 15-16 March 2015 doi: 10.1109/CSTIC.2015.7153322
3. **Weichao Zhou**; Xi Lin; Xiao-Yong Liu; Xiang-Ming Xu; Chun-Min Zhang; Jin-Shan Shi; Peng-Fei Wang; Zhang, D.W., "**Investigation of spin-on-dopant for fabricating high on-current tunneling field effect transistor**," in Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on , vol., no., pp.1-3, 28-31 Oct. 2014 doi: 10.1109/ICSICT.2014.7021392
4. Ming'e Jing; Pengshuai Ren; **Weichao Zhou**; Zhiyi Yu; Xiaoyang Zeng, "**Evaluation of buffer organizations for network-on-chip**," in Solid-State and Integrated Circuit Technology (ICSICT), 2012 IEEE 11th International Conference on , vol., no., pp.1-3, Oct. 29 2012-Nov. 1 2012 doi: 10.1109/ICSICT.2012.6467882