Part 2: Peripheral Bus Signals using Signal Tap II

Now that you have your design working, we are going to add Altera’s SignalTap II Logic Analyzer which is a logic analyzer that is implemented in the FPGA and allows you to debug your design by allowing you access to the internal signals of your design.

Perform the following steps:

1. Open the SignalTap II window by selecting File > New. Choose SignalTap II Logic Analyzer File and click OK.

3. Before we do anything, lets save the file under the name Lab7.stp. In the dialog box that follows, click OK. For the dialog "Do you want to enable SignalTap II file Lab7.stp for the current project?" click Yes. The Lab7.stp is now the SignalTap file associated with the project

4. Before the SignalTap II analyzer can work, you need to specify what clock is going to run the SignalTap module that will be instantiated within your design. To do this, in the Clock box of the Signal Configuration pane of the SignalTap window, click , this will again bring up the Node Finder window. Select List to display all the nodes that can be added as the clock, and then double-click CLOCK\_50. Click OK.

5. You now need to add the nodes in the project that you wish to probe. In the Setup tab of the SignalTap II window, double-click in the area labeled Double-click to add nodes, bringing up the Node Finder window. For the Filter field, select SignalTap II: pre-synthesis. Click List. This will now display all the nodes that can be probed in the project. Click on the node you want and press the > button in the window to add them to your list. HINT: Refer to the waveform above for which signals you should add. When your list is complete, click OK. Note: Use the \*part\_of\_name\* in the named field to filter the list of nodes that are displayed.

• You can use the RTL schematic in Quartus or your VHDL file to determine the node names of the nodes you are interested in.

• As a minimum, you should include the peripheral registers and all of the avalon\_bridge signals in the bus interface. If your design is not working correctly, you will need to add more nodes for debugging purposes. For example, you can include signals inside of your slave peripheral or seven\_segment\_display driver.

6. With the Setup tab of the SignalTap II window selected, select the checkbox in the Trigger Conditions column. In the dropdown menu at the top of this column, select Basic. Determine which signal you would like to trigger on. Most likely it will be the rising edge of bus enable as that signal indicates the start of a write or read cycle. Right click in the Trigger Levels cell for your chosen signal and choose an edge.

7. For SignalTap II to work, you need to properly set up the hardware. First, make sure the DE2 board is plugged in and turned on. In the Hardware section of the SignalTap II window, located in the top right corner, click Setup. Double click USB-Blaster in the Available Hardware Items menu, and then click Close.

8. The last step in instantiating SignalTap in your design is to compile the design. In the main Quartus II window, select Processing > Start Compilation and indicate that you want to save the changes to the file by clicking Yes.

9. Program and configure the Cyclone II FPGA on the DE2 Board to implement the generated system.

10. Start Nios II Software Build Tools for Eclipse Program; configure your system and your program. Compile the program and download it to the Nios. Do not run the program yet.

11. Go back to the Signal Tap II window and choose Processing>Run Analysis. You should get a message indicating that it is waiting for the trigger. Now run your program. The Signal Tap II should trigger and you will be able to look at your signals in the data window.

12. Capture and obtain a screen capture of one complete write cycle to one of the four registers. Make sure the waveform is properly displayed so that all the signals are clearly seen. Add annotate on the waveform indicating what is happening with the signals and demonstrate your understanding of the bus write transaction.

13. Capture and obtain a screen capture of one complete read cycle to one of the four registers. Add annotate comments on the waveform indicating what is happening with the signals and demonstrate your understanding of the bus read transaction.

14. Demonstrate your working system and explain the SignalTap waveforms for a signoff.