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# Educational Objective

In this lab, you will learn how to…

1. Use TimeQuest to identify the slowest path in your design, and determine the maximum operating frequency.
2. Pipeline a combinatorial computation, resulting in improved timing parameters.

# Procedure

The project provided on my courses doubles the output frequency when switch 2 is pressed. The circuit used to accomplish this will be discussed in class.

1. Download and run the given project. Verify the predicted behavior as discussed above.
2. The given project does not have a timing constraints file (i.e. \*.sdc file). In the following steps we will create the constraints file and determine the basic timing parameters.
   1. In Quartus menus select Tools->TimeQuest Timing Analyzer.
   2. In TimeQuest menus select Netlist->Create Timing Netlist. In the dialog pop-up select **Post-Map**, leave all the other setting at the default.
   3. In TimeQuest menus select Constraints->Create Clock. In the resulting pop-up window make the following adjustments…
      1. Clock name is the clock port used in your VHDL top level. Enter **CLOCK2\_50** for the name.
      2. Period is 20 ns.
      3. The **Targets** entry box has a navigation button (small button with three dots). Click the navigation button. In the resulting dialog enter CLOCK2\_50 for the **filter**. Click on **list** and you should see the signal CLOCK2\_50. Click the right arrow to add this clock.
      4. Click OK
      5. Click RUN
   4. In the **Tasks** pane of TimeQuest double click on Update Timing Netlist.
   5. In the **Tasks** pane of TimeQuest double clock on Write SDC File.
   6. Back to Quartus, and re-compile the design.
   7. After the compilation in Quartus, go to the **Tasks** pane and select Time Quest Timing Analyzer-> View Report.
   8. In the report, expand **TimeQuest Timing Analyzer** and click on the **clocks** selection.
   9. Then find CLOCK2\_50 and right clock on it. In the menu select **Report Timing**.
   10. When the dialog box opens, click the **Report Timing** button.
   11. The resulting display shows you the ten slowest paths in your design. (i.e. the ones with the least slack). Record the slack for the slowest path.

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* 1. Based on the signal descriptions, where does this path appear to be in your logic?

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* 1. In the Tasks pane of TimeQuest find Data Sheet option and calculate max frequency. Recor the max frequency.

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1. Now change the given code to pipeline the logic operation such that the mux operation and the multiplier are done in separate clock cycles.
2. Re-compile and verify that the code still functions as before.
3. Once again record the maximum frequency and worst case slack. Did they improve? How much?

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