CAST CPET-563 Embedded Systems Design II **Dr. Kaputa**
Spring 2018
Lab 2

Student Name: _____

Introduction:

You are to create a module in VHDL that accepts a period and duty cycle and outputs an according PWM pulse train. The module shall be fully verified via simulation in Modelsim. Verify the module for all corner cases. Assume the input clock frequency is 100 MHz.

Requirements for the PWM module:

- shall module shall have an enable pulse.
- shall be able to control both the duty cycle and the period of the PWM pulse train.
- shall use basic entity inputs and not use 'generics' for the period and duty inputs.
- shall verify PWM operation for all corner cases.

Module Report:

Create a report for the module describing the module's functionality and limitations. Also include all necessary verification information such as screen shots, input/output files, etc. Assume that this module is an essential component of the engine control system of the 747 you will be flying to Disney World on.

Lab Submission:

1. Print out this lab with your name on the front and attach all code and verification report.
2. Submit all code by 4:40 pm on Feb 15th at: https://www.dropbox.com/request/FfZtp0h4GpT4JGScMKnm

Grading:

	Score	Pts
Code No tabs please. Proper spacing and formatting. Adequate variable names. Consistency.		/2
Comments Proper header and comments throughout		/2
Demonstration To be performed within lab week. Can show after due date with time stamped code.		/3
Report To be performed within lab week. Can show after due date with time stamped code.		/3
Final Grade		/10