Date: February 15th
From: Zachary Weeden
To: Dr. Kaputa
Subject: Lab 2 – PWM Module

Introduction

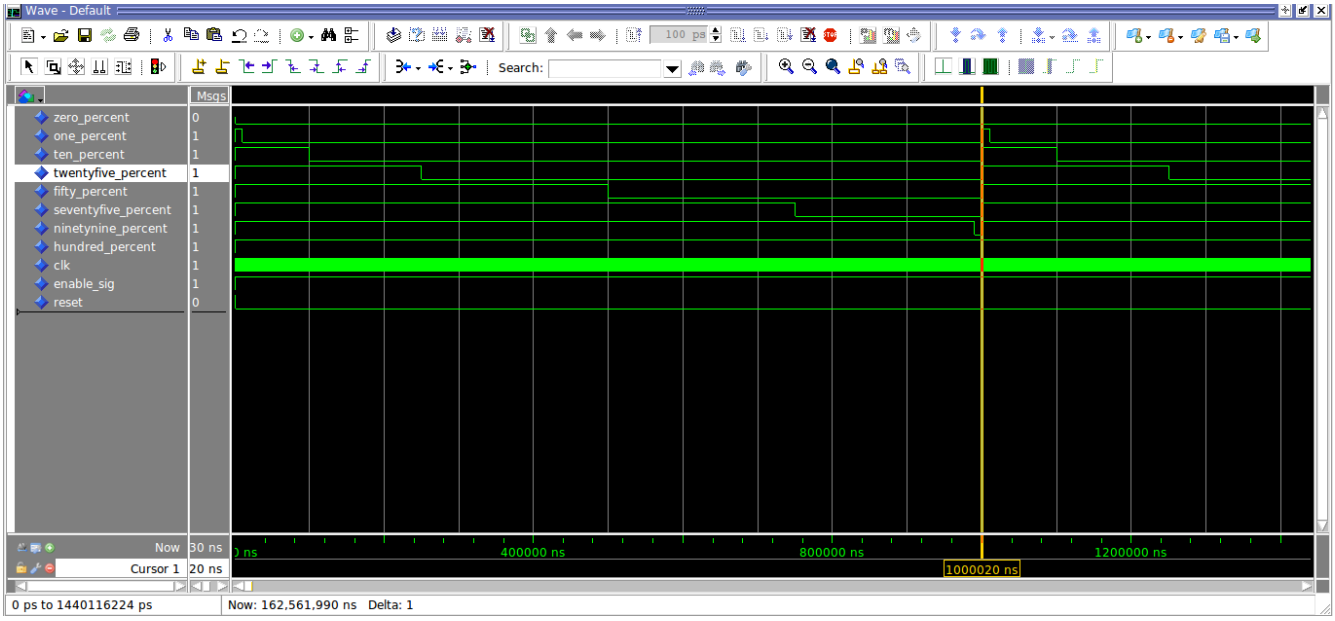
For the PWM module I chose to work off the baseline ‘blink’ example provided to us in class. As specified in the requirements, I made use of an enable input port as well as period and duty ports. The period and duty input ports were made into to 27 bit vectors to support a period up to 1 second. Both the period and duty inputs were to be input as a binary vectors that indicated the frequency for the period (eg. “00000000000000000001111101000” for 1KHz) and the respective ratio for a given duty cycle (eg. 50% duty desired of a 1KHz period “00000000000000000000111110100” for 500)

The vector sizes were calculated with the assumption of a 100MHz system clock to support a 1 second period. (log(100000000/1)/log(2) ~= 26.5 bits) With the use of the known system clock frequency, the number of ticks were calculated for both duty and period. An internal count signal (essentially a program counter) kept track of the increment. Outlier/edge case conditionals were added for 0% and 100% duty cycles.

This PWM module will be beneficial and will see use in the culminating rover project manifesting itself in the motor drive.

Analysis

A quick authored test bench proved to be enough to verify functionality. Below are varying cases of duty for a 1KHz period.



One case that was not tested/limitation of the PWM’s functionality is the case for a varying duty on the same port/signal. The above cases all had a constant input vector; testing for a change in the duty signal would be beneficial as this would emulate a real time system. From a brief and quick analysis I believe

the module would fail to the counter begin calculated at the beginning of the process. Further testing is required.

Conclusion

With the completion of the PWM module we can test a constant steady bit vector and rely on a correct output signal to modulate in an expected fashion. As noted in the Analysis section, further testing is required for a varying duty vector.