FPGA Memory

Distributed Memory

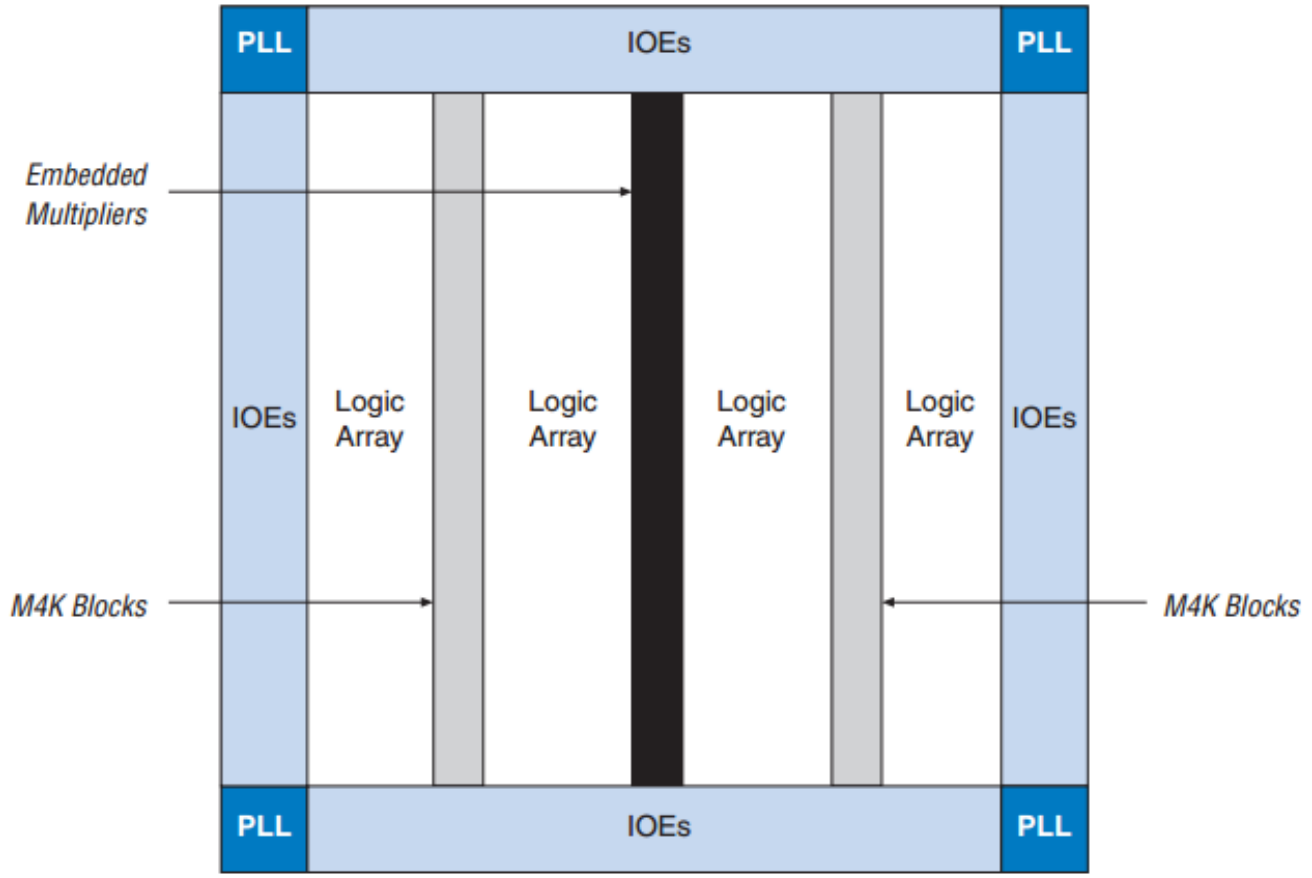
- Each LUT can be used for a couple bits of RAM
- Many LUTs can be chained together to create a larger RAM block

Block Memory

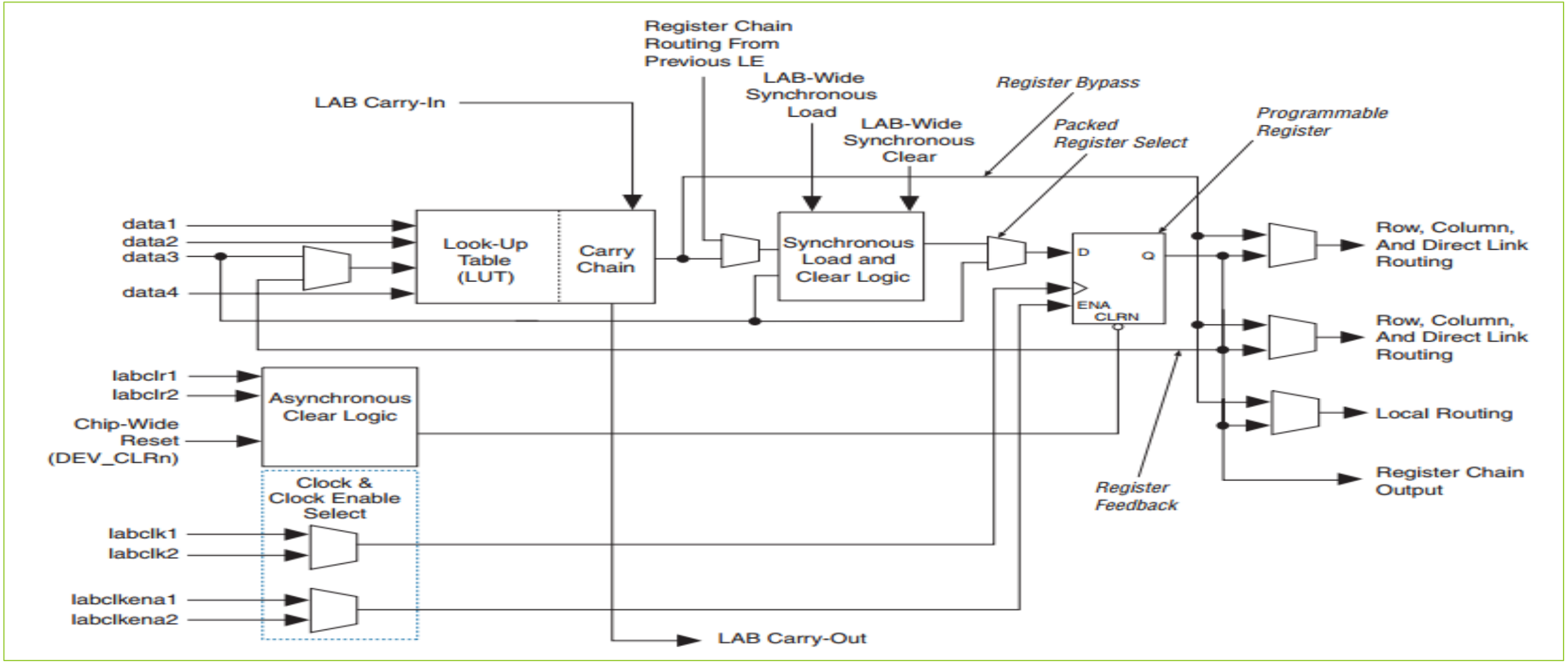
- Dedicated memory containing several kilobytes of RAM

DE2 Board

- Cyclone II 2C35 FPGA
- 105 M4K Blocks [4 kbits] => ~52 kB



Altera Logic Element [LE]



Working with Altera Block Memory

Synthesis

- Create Quartus II project
- Create new single port ROM IP block
  - Target M4K blocks
  - Single clock
  - Specify MIF file
  - Enable in-system memory editing
- Create ROM folder
  - /src/ROM
- Modify compile script
  - set_global_assignment -name QIP_FILE ../../src/rom/rom.qip
- Compile

Simulation

- Compile Quartus II simulation libraries
  - altera_mf folder is generated
- Copy Altera_mf folder to working directory
  - /src/altera_mf
- Modify sim.do file
  - vmap altera_mf ../../src/altera_mf
  - vcom -93 -work work ../../src/rom/rom.vhd
- Simulate

Altera Memory Initialization File [MIF]

Same file is used for hardware memory initialization as well as for simulation runs

```
DEPTH = 16; % Memory depth and width are required. DEPTH is the number of addresses %
WIDTH = 8; % WIDTH is the number of bits of data per word %
% DEPTH and WIDTH should be entered as decimal numbers %
ADDRESS_RADIX = DEC; % Address and value radixes are required %
DATA_RADIX    = DEC; % Enter BIN, DEC, HEX, OCT, or UNS; unless %
 % otherwise specified, radixes = HEX %
-- Specify values for addresses, which can be single address or range
CONTENT
BEGIN
0 : 2;
1 : 5;
2 : 2;
3 : 2;
4 : 2;
5 : 2;
6 : 2;
7 : 2;
8 : 2;
9 : 2;
10 : 2;
11 : 2;
12 : 2;
13 : 2;
14 : 2;
15 : 2;
END;
```

Altera In-System Memory Viewer

Can read and write memory while a program is running