計算機結構 HW4 G15 Report

施力維 b04502031
蔡承佑 b06901051

1. Screenshots

a) Readme.txt Content

```
cycle time: 9.5
FPU Single: Y
FPU Double: Y
FPU cycle time: 55
```

b) Baseline (RTL)

```
*Verdi* : End of traversing.
=======================The test result is ..... PASS=========================


        ************************************************
        **                                            **      /|__/|
        **              Congratulations !!            **     / 0,0  \
        **                                            **    /_____   \
        **   All instructions have been done successfully! **  /^ ^ ^ \  |
        **                                            **  |^ ^ ^ ^ |w|
        ************************************************   \m___m__|_|


==============================================================================
Simulation complete via $finish(1) at time 7316 NS + 0
./tb.v:160                      $finish;
```

c) Baseline (Gate-level)

```
using SDF File ./SingleCycleMIPS_syn.sdf  for this simulation.
=======================The test result is ..... PASS=========================


        ************************************************
        **                                            **      /|__/|
        **              Congratulations !!            **     / 0,0  \
        **                                            **    /_____   \
        **   All instructions have been done successfully! **  /^ ^ ^ \  |
        **                                            **  |^ ^ ^ ^ |w|
        ************************************************   \m___m__|_|


==============================================================================
Simulation complete via $finish(1) at time 7316 NS + 0
./tb.v:160                      $finish;
```

d) FPU (Baseline RTL)

```
*Verdi* : End of traversing.
=======================The test result is ..... PASS=========================


        ************************************************
        **                                            **      /|__/|
        **              Congratulations !!            **     / 0,0  \
        **                                            **    /_____   \
        **   All instructions have been done successfully! **   /^ ^ ^ \  |
        **                                            **  |^ ^ ^ ^ |w|
        ************************************************   \m___m__|_|


==============================================================================
Simulation complete via $finish(1) at time 46201 NS + 0
./tb.v:160                      $finish;
```

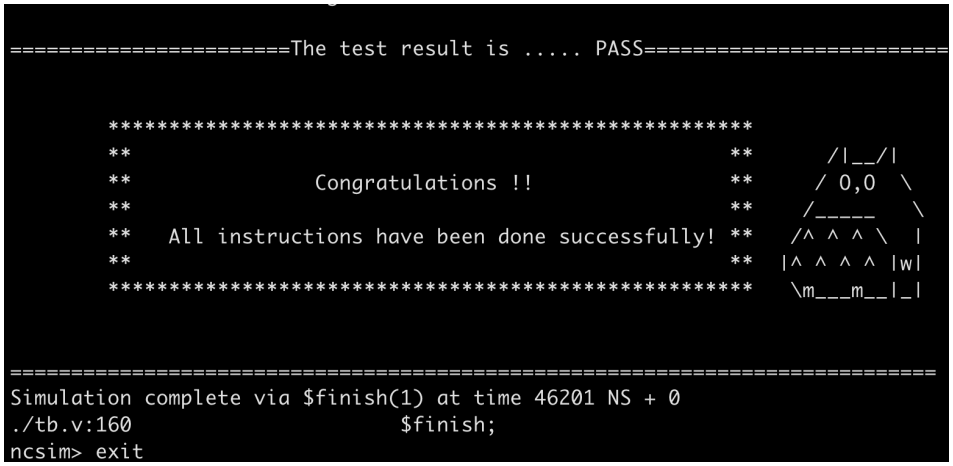
e) FPU (Single RTL)

```
*Verdi* : End of traversing.
=======================The test result is ..... PASS=========================


                              FPU Version

        ************************************************
        **                                            **      /|__/|
        **              Congratulations !!            **     / 0,0  \
        **                                            **    /_____   \
        **   All instructions have been done successfully! **   /^ ^ ^ \  |
        **                                            **  |^ ^ ^ ^ |w|
        ************************************************   \m___m__|_|


==============================================================================
Simulation complete via $finish(1) at time 961 NS + 0
./tb.v:160                      $finish;
```

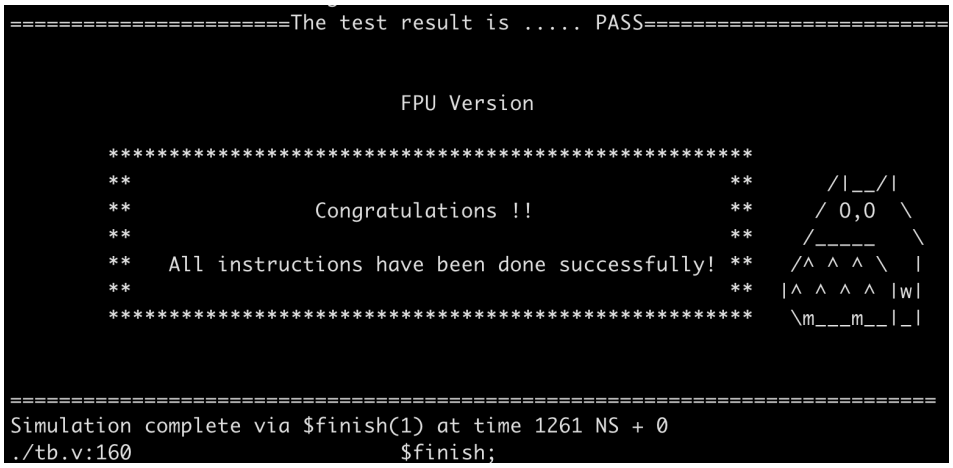
f) FPU (Double RTL)

```
*Verdi* : End of traversing.
=======================The test result is ..... PASS=========================


                              FPU Version

        ************************************************
        **                                            **      /|__/|
        **              Congratulations !!            **     / 0,0  \
        **                                            **    /_____   \
        **   All instructions have been done successfully! **   /^ ^ ^ \  |
        **                                            **  |^ ^ ^ ^ |w|
        ************************************************   \m___m__|_|


==============================================================================
Simulation complete via $finish(1) at time 1261 NS + 0
./tb.v:160                      $finish;
```

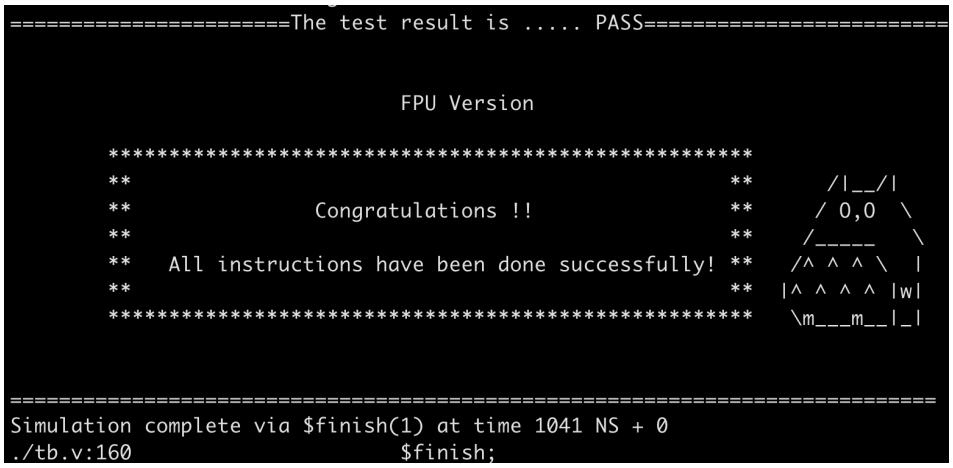
g) FPU (Baseline Gate-level)



h) FPU (Single Gate-level)



i) FPU (Double Gate-level)



j) Timing

- Baseline

```
data arrival time                                                   9.56

clock clk (rise edge)                                 9.50          9.50
clock network delay (ideal)                           0.50         10.00
clock uncertainty                                    -0.10          9.90
register/regs_reg_1__28_/CK (EDFFXL)                  0.00          9.90 r
library setup time                                   -0.34          9.56
data required time                                                  9.56
-------------------------------------------------------------------------
data required time                                                  9.56
data arrival time                                                  -9.56
-------------------------------------------------------------------------
slack (MET)                                                         0.00
```

- FPU

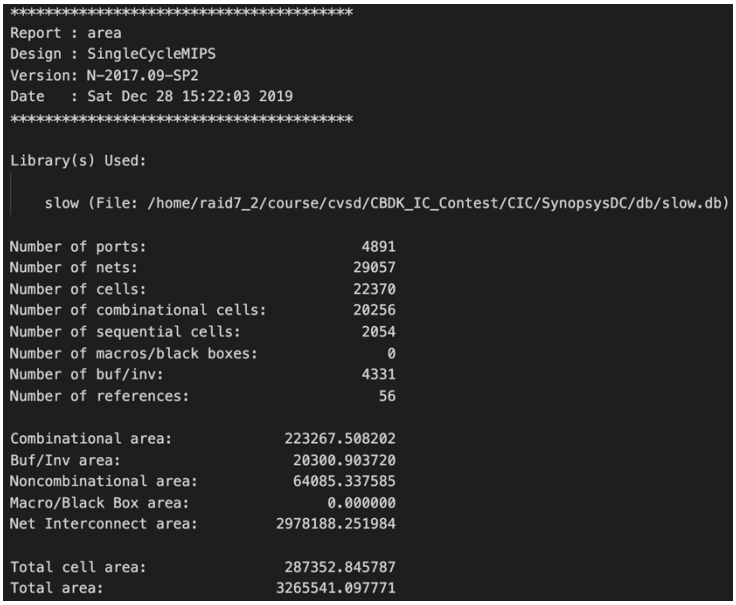
```
data arrival time                                                  50.06

clock clk (rise edge)                                50.00         50.00
clock network delay (ideal)                           0.50         50.50
clock uncertainty                                    -0.10         50.40
register_fp/regs_reg_8__24_/CK (DFFX1)                0.00         50.40 r
library setup time                                   -0.34         50.06
data required time                                                 50.06
-------------------------------------------------------------------------
data required time                                                 50.06
data arrival time                                                 -50.06
-------------------------------------------------------------------------
slack (MET)                                                        0.00
```

k) Area

- Baseline

```
****************************************
Report : area
Design : SingleCycleMIPS
Version: N-2017.09-SP2
Date   : Tue Dec 24 05:13:50 2019
****************************************

Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:                          698
Number of nets:                          4979
Number of cells:                         4260
Number of combinational cells:           3225
Number of sequential cells:              1028
Number of macros/black boxes:               0
Number of buf/inv:                        607
Number of references:                      54

Combinational area:              33937.815830
Buf/Inv area:                     3954.941993
Noncombinational area:           36134.252155
Macro/Black Box area:                0.000000
Net Interconnect area:          593836.352631

Total cell area:                 70072.067986
Total area:                     663908.420616
```

- FPU



```
****************************************
Report : area
Design : SingleCycleMIPS
Version: N-2017.09-SP2
Date   : Sat Dec 28 15:22:03 2019
****************************************

Library(s) Used:

    slow (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/slow.db)

Number of ports:                         4891
Number of nets:                         29057
Number of cells:                        22370
Number of combinational cells:          20256
Number of sequential cells:              2054
Number of macros/black boxes:               0
Number of buf/inv:                       4331
Number of references:                      56

Combinational area:             223267.508202
Buf/Inv area:                    20300.903720
Noncombinational area:           64085.337585
Macro/Black Box area:                0.000000
Net Interconnect area:         2978188.251984

Total cell area:                 287352.845787
Total area:                     3265541.097771
```

2. A*T Value

   A = 70072.067986, T = 9.5

   → A*T = 665684.645867

3. Design & Difficulties

   a) Design

   - Baseline:

     將原有結構加入對其他指令的支援，例如：

     PC Branch: (beq & zero) | (bne & ~zero)

     Write Reg: jal ? 5'd31 : (RegDst ? IR[15:11] : IR[20:16])

     PC input: jr ? read_data1 : original logic with modified branching

     Write data: jal ? PC_add4 : original wire

     ALU、ALU Control: 新增運算模式（shift, less than,…）

   - FPU SP:

     新增一個 FPU 的 32x32bits register，control 增加部分則新增 FPU instruction 的判斷，判斷由 ALU 還是 FPU 的結果寫入 mem 或 reg。並新增 fpcond 的 flip-flop 來紀錄 c.eq.s 的比較結果，用來進行判斷。

- FPU DP:

  由於 double precision 的 save 跟 load 需要用到兩個 clock 來完成，因此新增一個 dp_sl_stage 的 flip-flop 來紀錄當前為第幾個 clock。第一個 clock 時輸入的 PC_Addr 不會加四，因此再來獨到的還會是同一個 clock，第二個 clock 時則讀取或存取第二筆資料到 A+1 的 address。

b) Difficulties

Debug 時間花較久，RTL 較容易，而 Gate-level 則需要從波形中找出計算較慢的部分加以修改，但經常照著我們以為較好的方法改實際上卻差強人意。理論上將 submodule 盡量整併會獲得更好的 A*T，但是將原有的 wire 去除之後反而較差，需要多次調整。

此外，sdc 的 cycle time 在每次修改設計後多次測試才能找出最佳解，亦花費許多時間，而 compile 的順序經過多次測試後發現先將原有 map effort 調高為 high，執行後再以 compile_ultra 進行 incremental mapping，A*T 減少的效果顯著。

4. Work Distribution

   Baseline：collaborate

   FPU：力維

   Optimization：承佑

5. A*T Improvement

   a) ALU adder: 將一個 32-bit adder 改為 8 個 4-bit adder

   b) Output A: 將原本從 ALU 計算的答案拉出改為單獨計算(兩個和(a)共用的 4-bit adder + XOR for MSB)

   c) Register: 由 assign read_data = regs[read_reg];

   調整為:

```
always @(*) begin
  case(read_reg)
      5'dxx : read_data = regs[xx];
```

d) ALU Control: 合併至 ALU 內

e) ALU: 將 beq, bne 的運算從 ”–“ 改為 ”!=”

f) PC: 使用 30bit 計算

g) Control: 各個 output 對應的 opcode 做 K–map 化簡

h) run.tcl: 新增以下指令（effect: A: 73k→70k; T: 10→9.5）

```
set_structure    true
group_path –name clk –weight 15
report_path_group
compile –map_effort high    #改自 compile
compile_ultra –increment
```