

Si9933ADY

Dual P-Channel PowerTrench[®] MOSFET

General Description

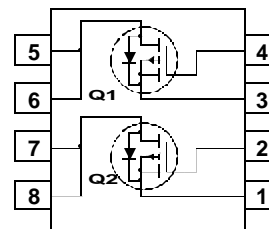
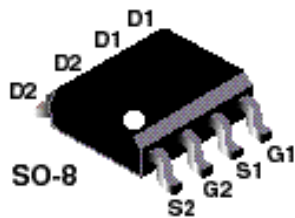
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 12V).

Applications

- Load switch
- Motor drive
- DC/DC conversion
- Power management

Features

- -5 A, -20 V, $R_{DS(ON)} = 75\text{ m}\Omega$ @ $V_{GS} = -4.5\text{ V}$
 $R_{DS(ON)} = 105\text{ m}\Omega$ @ $V_{GS} = -3.0\text{ V}$
 $R_{DS(ON)} = 115\text{ m}\Omega$ @ $V_{GS} = -2.7\text{ V}$
- Extended V_{GSS} range ($\pm 12\text{V}$) for battery applications
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_b	Drain Current – Continuous (Note 1a)	-3.4	A
	– Pulsed	-16	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
9933A	Si9933ADY	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		–12		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			–100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	–0.8	–1.0	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -3.2\text{ A}$ $V_{GS} = -3.0\text{ V}, I_D = -2.0\text{ A}$ $V_{GS} = -2.7\text{ V}, I_D = -1.0\text{ A}$		44 64 72	75 105 115	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	–16			A
g_{FS}	Forward Transconductance	$V_{DS} = -9\text{ V}, I_D = -3.4\text{ A}$		8		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		825		pF
C_{oss}	Output Capacitance			420		pF
C_{rss}	Reverse Transfer Capacitance			150		pF

Switching Characteristics (Note 2)

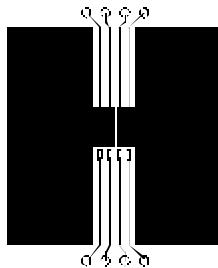
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -6\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		16	40	ns
t_r	Turn–On Rise Time			46	80	ns
$t_{d(off)}$	Turn–Off Delay Time			40	70	ns
t_f	Turn–Off Fall Time			25	40	ns
Q_g	Total Gate Charge	$V_{DS} = -6\text{ V}, I_D = -3.2\text{ A},$ $V_{GS} = -4.5\text{ V}$		10	20	nC
Q_{gs}	Gate–Source Charge			2.1		nC
Q_{gd}	Gate–Drain Charge			3.3		nC

Drain–Source Diode Characteristics and Maximum Ratings

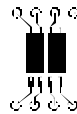
I _S	Maximum Continuous Drain–Source Diode Forward Current				–2.0	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –2.0 A (Note 2)		–0.7	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

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E ² CMOS™	MICROWIRE™	SILENT SWITCHER®	
EnSigna™	OPTOLOGIC™	SMART START™	
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