PROGRAMMING ASSIGNMENT #1
STATIC TIMING ANALYSIS

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Example: C17 Input

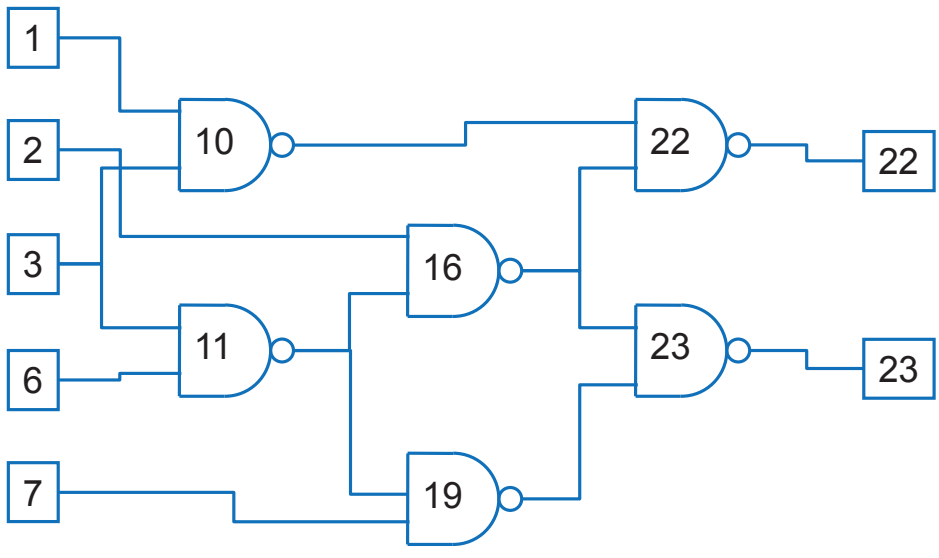
- **Primary inputs/primary outputs**
- **Connection**

```
INPUT(1)
INPUT(2)
INPUT(3)
INPUT(6)
INPUT(7)

OUTPUT(22)
OUTPUT(23)

10 = NAND(1, 3)
11 = NAND(3, 6)
16 = NAND(2, 11)
19 = NAND(11, 7)
22 = NAND(10, 16)
23 = NAND(16, 19)
```

10 is the output of a nand gate whose inputs are 1 and 3



Example: C17 Graph

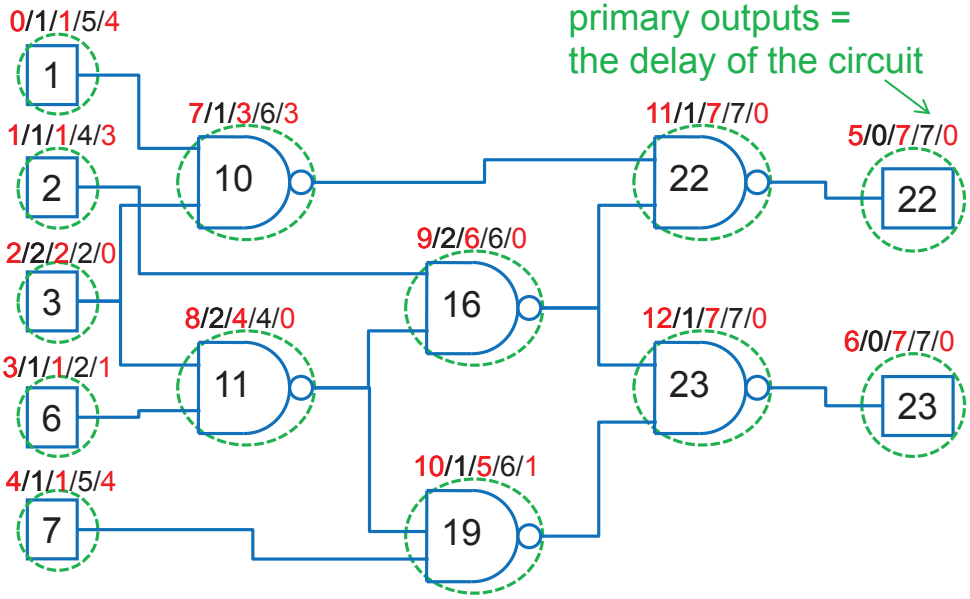
- **Vertex: gate/input/output: delay = # of fanout gates**
- **Edge: wire**

```
0  INPUT(1)
1  INPUT(2)
2  INPUT(3)
3  INPUT(6)
4  INPUT(7)

5  OUTPUT(22)
6  OUTPUT(23)

7  10 = NAND(1, 3)
8  11 = NAND(3, 6)
9  16 = NAND(2, 11)
10 19 = NAND(11, 7)
11 22 = NAND(10, 16)
12 23 = NAND(16, 19)
```

VertexID



VertexID/delay/arrival/required/slack

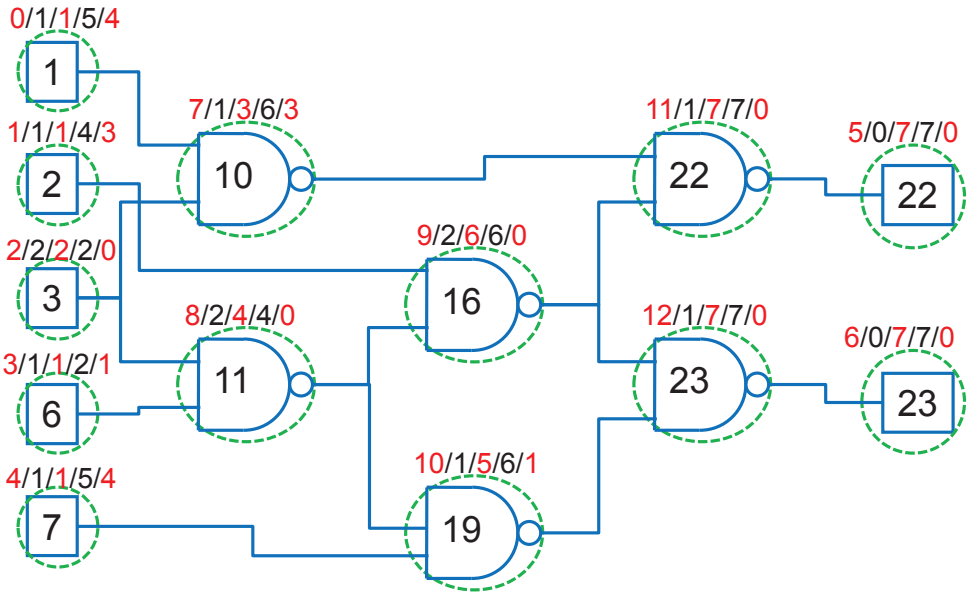
Programming assignment #1

Example: C17 Output

- **Critical path delay, input pins, output pins**
- **Delay info of each vertex**

```
7
5 0 1 2 3 4
2 5 6
0 1 4
1 1 3
2 2 0
3 1 1
4 1 4
5 7 0
6 7 0
7 3 3
8 4 0
9 6 0
10 5 1
11 7 0
12 7 0
```

VertexID in ascending order



VertexID/delay/arrival/required/slack

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