BK4811 Datasheet

Preliminary Specification

Analog Two Way Radios IC

Approvals

Name	*Date*	*Signature*

Beken Corporation
3A, 1278 Keyuan Rd, Shanghai 201203, China
PHONE: (86)21 5108 6811
FAX: (86)21 6087 1277

Revision History

Version	Date	Author(s)	Description
0.1	2011/12/12	Weifeng	Initial draft based on BK4833 datasheet and BK4800 datasheet at this day, based on BK4833V82
	2012/2/6	Weifeng	Give detail timing of channel programming
	2012/3/26	Weifeng	Update the pin list to 4x4 24-pin
0.2	2012/6/6	Weifeng	Update based on V12 test result

Content

1 General Description

The BK4811 is a half duplex TDD FM transceiver operating from 117 MHz to 525 MHz band for worldwide personal radio service. The transceiver integrated high performance PLL, ADC, DAC, and advanced digital signal processing capability on a single chip. The digital low-IF image rejection architecture enables it to work with a very simple MCU as a two way radio communication system. On-chip flexible and precise continuous and discrete tone generator and detector enable a secure link and digital signaling.

The BK4811 on-chip FSK data modem supports F2D and F1W emission to be used in both FRS and DPMR band for text message and GPS information exchange besides speech communication.

2 Key Features

- World wide band: 117 ~ 525 MHz
- 12.5/25 kHz channel spacing
- audio filter with four optional bandwidths
- On chip 4 dBm RF PA
- 2.4 V to 3.6 V power supply
- CTCSS tone receiver with up to parallel eight frequency detector
- 23/24 bit programmable DCS code
- Standard DTMF and programmable in-band dual tone
- SELCALL and programmable in-band single tone
- 1.2/2.4 kbps FSK data modem with either F2D or F1W modulation type
- Frequency inversion scrambler
- Voice activated switch (VOX) and time-out timer
- RF Signal strength measurement and signal quality measurement
- TX Audio signal strength indication and RX audio signal strength indication
- 3-wires interface with MCU with maximum 8 Mbps clock rate
- QFN 4x4 24-Pin package

3 Applications

- Personal radio service
- Toys
- Baby monitor

4 Chip Block Diagram

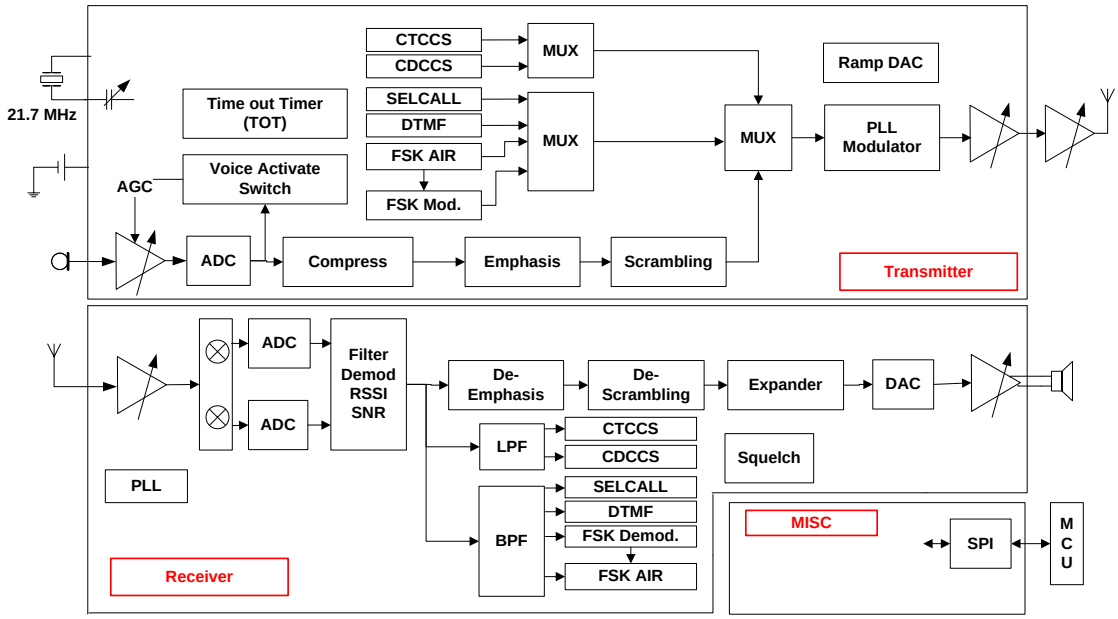

Figure 1 BK4811 Chip Block Diagram

5 Pin Information

Table 1 BK4811 4mmx4mm 24-Pin Definition

Pin #	Name	Direction	Function
1	VCCRF	Input	Power Supply, 2.4 V~ 3.6 V
2	LNAIN	Input	LNA input port
3	PAOUT	Output	RF PA output
4	VDDPA	Output	PA regulator output, with de-coupling capacitor to ground
5	VCCPA	Input	Power supply to PA regulator, 2.4 V~ 3.6 V
6	VDDRAMP	Output	Regulator output, with de-coupling capacitor to ground
7	VCCAUD	Input	Power supply to audio regulator, 2.4 V~ 3.6 V
8	EAROUT	Output	Earpiece output
9	MICIN	Input	Microphone input
10	GBAT	Input	Ground
11	CDVDD	Output	Regulator output, with de-coupling capacitor to ground
12	VBATD	Input	Power supply, 2.4 V to 3.6 V
13	SCK	Input	SPI clock
14	SCN	Input	SPI enable
15	SDATA	I/O	SPI data
16	INTN	Output	Interrupt Signal to MCU
17	GPIO1	I/O	GPIO1
18	GPIO0	I/O	GPIO0
19	CDVDD1	Output	Regulator output, with de-coupling capacitor to ground
20	VCCPLL	Input	Power Supply, 2.4 V~ 3.6 V
21	VCCDVCO	Input	Power Supply, 2.4 V~ 3.6 V
22	XTALP	Input	Crystal oscillator port, input
23	XTALN	Output	Crystal oscillator port, output
24	VCCXTAL	Input	Power supply to crystal, 2.4 V to 3.6 V

6 Clock and System Operation

The BK4811 uses 21.7 MHz crystal. It can operate from 117 MHz to 525 MHz with different register setting (REG3, REG113, REG114, REG126, and REG127). The transceiver can be set to TX, RX and idle state.

Table 1 Operation Frequency Band Control

Band (MHz)	REG3	REG126 [4]	REG127	REG113	REG114	N_IF	DIV
117~175	0x4	0x1	0xC504			1130727	24
Example: 129	0x4	0x1	0xC504	0x4744	0xDDC5		
140~210	0x3	0x1	0x7983			942269	20
Example: 155	0x3	0x1	0x7983	0x475F	0x561E		
175~262	0x2	0x1	0x2E02				
Example: 193	0x2	0x1	0x2E02	0x471B	0x6DBA	753812	16
233~350	0x1	0x0	0xE282				
Example: 258	0x1	0x0	0xE282	0x474D	0x7E38	565364	12
350~525	0x0	0x0	0x9701				
Example: 409.75	0x0	0x0	0x9701	0x4B81	0xEAC5	376906	8
Note 1. By default, the BK4811 will cover 400~500 MHz, 266~333 MHz and 134~250 MHz; For other special band, please ask Beken for the proper version							

To set the RF frequency with REG113 and REG114, please using the procedure as follows.

1. Set theREG126 and REG127 according to table above and REG3[15:13]=0
2. Set the REG113 and REG114 as follow.

$N\_RF = round(f * DIV * 2\text{^}23 / F\_REF - N\_IF)$; Where F_REF is the crystal frequency in Hz, and f is the RF frequency in Hz (for wideband, the f should be RF frequency subtracted by 3125. The REG113 is the 16 bits MSBs and the REG114 is the 16 bits LSBs of the N_RF.

3. Toggle the REG5[10] with 0, 1, 0 sequence
4. Set the REG3[15:13] according to the table 1

To avoid image frequency interference, user can change the IF to the opposite as follows.

5. REG117[10]=0，read RSSI0 of F0=(Fwanted - 2*IF)
6. REG117[10]=1，read RSSI1 of F1=(Fwanted + 2*IF), where REG113/REG113= f(Fwanted+2*IF+2*IF), where f is the formula to calculate the REG113/REG114 in step 2
7. If RSSI0<RSSI1，REG117[10]=0，else REG117[10]=1
8. If REG117[10]=0, REG113/REG114 = f(Fdesired), has the same formula as step 2; If REG117[10]=1, REG113/REG114 = f(Fdesired + 2*IF);

Normally, the IF frequency is 121.875 kHz for narrow band, user can use other IF frequency from 9 kHz to 131 kHz. The calculation of the register setting (REG16, REG126[4], REG127, REG113, REG114) is as follows.

```
1. REG16 = dec2hex(round(hex2dec('4B80')/(121.875e3/IF)));
2. CH_SPACE = 12.5e3/(121.875e3/IF);
3. IF_CONSTANT = 9.75;
4. REG127_dec = round(CH_SPACE*DIV/F_REF*2^24/2); % Get DIV from table 1
5. REG127 = dec2hex(REG127_dec);
6. if (length(REG127)>=5)
   a)     REG126_B4 = 1 % REG126[4]
   b)     REG127(1) = []; % only keep 16 LSBit for REG127
   c)else
   d)     REG126_B4 = '0;';
   e)end
7. N_IF = round(IF_CONSTANT*REG127_dec);
8.  N = round(f*REG3_B15toB13*2^24/F_REF/2 - N_IF);
9.  REGs = dec2bin(N, 32);
10.   REG113 = dec2hex(bin2dec(REGs(1:16)), 4); % MSB 16 bit
11.   REG114 = dec2hex(bin2dec(REGs(17:end)), 4); % K LSB 16 bit
```

For example, when the IF is 9.375 kHz, for 409.75 MHz the REG16=0x5CF，REG127=0xB9E，REG113=0x4B87，REG114=0x39CA.

The transceiver channel filter bandwidth can be set to either 12.5 kHz or 25 kHz (REG1 [15]), and the audio signal bandwidth can be set to one of four options (REG17 [1:0]) by user favorite.

The audio path has a digital compander to improve the dynamic range and reduce the background noise (REG17 [11]).

The TX and RX channel frequency calculation is the same: F_CHAN = F + CH_NUM * CH_SPACE, where channel number CH_NUM is set by REG112 and channel spacing CH_SPACE is set by REG01.

Deviation of audio band signal and sub-audible band signal can be programmed independently (REG40). The combined signal deviation can be further tuned by REG126 [3:0].

The BK4811 receiver can detect received signal strength and quality for squelch control as follows.
1. RF signal strength RSSI (REG68) with 1 dB resolution
2. RF signal quality SNR (REG68) with 1 dB resolution
3. Baseband signal glitch counters IMP_CNT (REG125)

The internal RF AFC (REG69, REG70) enables receiver to lock to the transmitter

frequency and user can read the residual frequency offset (REG70) for squelch control. If AFC is enabled, it works as long as the RSSI and SNR are greater than the threshold (REG71).

There are LNA RSSI (REG68 [7]) and IF RSSI (REG101) for RF AGC control; user can adjust the RF front end gain (REG108) to avoid saturation distortion.

1. Read LNA_RSSI (REG68[7]), AGC_H (REG101[15:8]) and AGC_L (REG101[7:0]), every SNR_TIME (REG[15:14]) such as 12.5 ms
2. If LNA_RSSI is 0, please set LNA_G (REG108[8]) to 0
3. If LNA_RSSI is 1, please set LNA_G (REG108[8]) to 1
4. If AGC_H is 0x80, decrease the PGA_M (REG108[7:4]) step by step until AGC_H is 0
5. If AGC_L is 0, please increase the PGA_M step by step until AGC_L is greater than 0

7 Power Management

Table 2 Power Control for Different Operational States

Blocks	Control Register	TX	RX	Idle
RX ADC	REG6[13]	1	0	1
RX VGA	REG6[12]	1	0	1
VCO	REG7[13]	1	0	x
AGC	REG7[11]	1	0	1
RX Audio	REG7[10]	1	0	1
Crystal Oscillator	REG7[7]	0	0	1
RF PLL	REG7[5]	0	0	1
TX Chain	REG7[4]	0	1	1
RX Chain	REG7[3]	1	0	1
LDOs	REG7[2]	0	0	1
DLDO	REG7[0]	0	0	1
TX Audio	REG10[2]	0	1	1
PA Ramping	REG43[15]	1	0	0
PA Ramping	REG43[14]	0	1	1
Digital State	REG112[14]	1	0	X
Current		39 mA	47 mA	140 uA

When switching from TX or RX mode to idle mode, register should be update in order of REG7, REG6, REG10, REG43, and REG112. When back from idle to active mode, register should be update in order of REG7, REG6, REG2, REG3,

REG4 , REG5, REG10, REG43, REG112, where REG2 to REG5 is re-filled here as their content is lost at idle mode.

8 TX Baseband

8.1 Audio

TX audio path has the following blocks:

- Digital AGC to automatically adjust microphone gain (REG44, REG45) before ADC
- Digital compressor to extent signal dynamic range (REG17)
- Volume control with 1 dB step from -25 dB to 6 dB (REG18)
- Optional pre-emphasis filter, 0 dB at 1 kHz and +6 dB per octave (REG18)
- Audio scrambling with programmable scrambling frequency (REG20)
- 300 Hz high pass filter to avoid interference to sub-audible signal, which has 30 dB attenuation for frequency below 250 Hz with respect to signal at 1 kHz (REG18)
- Low pass filter with 2.55 kHz corner for 12.5 kHz channel spacing and 3 kHz corner for 25 kHz channel spacing (REG18)
- Limiter to avoid unwanted out-of-band emission (REG18)
- Flexible block execution order (REG18)

Figure 2 TX Audio Block Diagram

The microphone gain can be control through REG44 and REG45.

When AGC is enabled, the microphone gain control word REG44 [5:0] is automatically controlled by internal AGC algorithm.

8.2 VOX and TOT

Voice activated switch (VOX) detects the background noise level (REG22) and microphone input signal level (REG21), when the ratio between the signal level and the background noise level is greater than a programmable threshold (REG22) and (REG19 [0] =0) (or (REG19 [0] =1)) the signal level is greater than an absolutely threshold (REG21), the VOX will output 1 and the VOX interrupt bit will be set (REG116).

VOX works only when receive signal strength (REG68) is lower than a programmable threshold (REG67).

In TX mode, time-out timer (TOT) detects the VOX output, if it is 0 (no active microphone input signal) for a programmable duration (REG23), the TOT interrupt bit will be set (REG116).

User can do its own VOX and TOT control based on the readable microphone signal level (REG21) and background noise level (REG22).

8.3 In-band Signaling

There are three types of in-band signaling: DTMF, SELCALL, and FSK (and FSK_AIR). Together with audio signal, they are total of four kinds of in-band signaling, of which only one can be sent at a time (REG40). The deviation of in-band signaling is programmable (REG40).

8.3.1 DTMF

DTMF is a dual tone signaling, it has programmable high band and low band frequency. The high band frequency can be programmable from 1209 Hz to 1633 Hz (REG25). The low band frequency can be programmable from 697 Hz to 941 Hz (REG24). The twist can be programmable from 0 to 15 dB with 1 dB resolution (REG26)). The suggested DTMF tone table is given below.

Table 2 Standard DTMF Table

DTMF Symbol		High Frequency (Hz)			
		1209	1336	1447	1633
Low Frequency (Hz)	697	1	2	3	A
	770	4	5	6	B
	852	7	8	9	C
	941	E	0	F	D

8.3.2 FSK

FSK is a high data rate signaling, which supports 1200 bps data mode at 12.5 kHz channel spacing and 2400 bps data mode at 25 kHz channel spacing. The frame structure of the data package is given below.

Pre-amble	Sync Word	Addr	Type	Size	CRC A	Payload	CRCB
16 bit	16 bit	Byte0	Byte1	Byte2	Byte3	0-127 Word	2/4 Byte

Figure 3 Frame Structure of Data Mode

User can write head field including Address/Type/Size/CRCA and the corresponding payload (REG28, REG29, REG30), and it will automatically calculate the CRC and packetize the data. Optional scrambling can be added to Address and subsequent bytes, and the scrambling seed is programmable (REG32).

Data receiver will automatically finish synchronization and data extraction that Address/Type/Size/CRCA and Payload can be read out through MCU interface.

The final over the air data package type can be setting with Type byte.

- Type 0: Only head, no payload
- Type 1: Head with payload
- Type 2: Head with FEC encoded payload
- Type 3: Head with FEC and interleaved encoded payload
- Type 4: Free format that no automatic CRC insertion, CRCA is a user writable byte

The payload write is through an 8 words (1 word = 2 bytes) FIFO, if the word number in FIFO is shorter than a threshold that a write operation requires, it will give an interrupt to MCU that MCU must refill the FIFO (REG31).

Note: if use type 3, the number of payload is restricted. The allowed payload number is either odd number less than 8 or even number greater than 9. Payload number 8 and 9 is not allowed for type 3.

The FSK packet can be transmitted either directly through FM modulation (FSK AIR) for DPMR band or with a MSK modulated sub-carrier (FSK modem) then to FM modulation for FRS band.

8.3.3 SELCALL

SELCALL is a single tone signaling, the frequency can be programmable from 400 Hz to 3000 Hz (REG34). To get high sensitivity the suggested tone frequency (EIA frequency group) is given below.

Table 3 EIA single tone frequency setting

Tone Number	0	1	2	3	4	5	6	7

Tone Frequency (Hz)	600	741	882	1023	1164	1305	1446	1587
Tone Number	8	9	A	B	C	D	E	F
Tone Frequency (Hz)	1728	1869	2151	2435	2010	2295	495	No Tone

8.4 Sub-audible Signaling

Sub-audible signaling includes both CTCSS and CDCSS. For CTCSS, the frequency is programmable with 18 bit resolution, and it can be set to have a 0/120/180 degree phase shift. For CDCSS, it supports both standard CDCSS code with programmable 9 bit raw code and user programmable 23/24 bits CDCSS code, and the transmitted CDCSS code can be inversed.

The CDCSS mode is set by REG38 [15:13]. The CDCSS mode and CDCSS code register are shared by both TX and RX.

Table 4 Reference CTCSS Frequency

Standard CTCSS Tone						
Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)
67.0	**85.4**	**103.5**	**127.3**	**156.7**	**192.8**	**241.8**
71.9	**88.5**	**107.2**	**131.8**	**162.2**	**203.5**	**250.3**
74.4	**91.5**	**110.9**	**136.5**	**167.9**	**210.7**	
77.0	**94.8**	**114.8**	**141.3**	**173.8**	**218.1**	
79.7	**97.4**	**118.8**	**146.2**	**179.9**	**225.7**	
82.5	**100.0**	**123.0**	**151.4**	**186.2**	**233.6**	
Non-Standard CTCSS Tone						
Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)	Freq. (Hz)
62.5	**69.3**	**183.5**	**196.6**	**206.5**		
64.7	**159.8**	**189.9**	**199.5**	**229.1**		

Table 5 Reference CDCSS Raw 9 bit Octal Word

023 025 026 031 032 036 043 047
051 053 054 065 071 072 073 074
114 115 116 122 125 131 132 134
143 145 152 155 156 162 165 172
174 205 212 223 225 226 243 244
245 246 251 252 255 261 263 265

266 271 274 306 311 315 325 331
332 343 346 351 356 364 365 371
411 412 413 423 431 432 445 446
452 454 455 462 464 465 466 503
506 516 523 526 532 546 565 606
612 624 627 631 632 654 662 664
703 712 723 731 732 734 743 754

9 RX Baseband

The RX baseband output is the FM demodulator output, whose amplitude can be scaled (REG66), and subsequent filter coefficient is selected according to the in-band signal type (REG66) and sub-audible signal type (REG66).

9.1 Audio

Audio path has blocks below.

- De-emphasis filter, 0 dB at 1 kHz and -6 dB per octave (REG72)
- Audio de-scrambling with programmable scrambling frequency (REG74)
- Low pass filter with 2.55 kHz corner for 12.5 kHz channel spacing and 3.1 kHz corner for 25 kHz channel spacing (REG72)
- 45 dB volume control range with 3 dB per step (REG73)
- Hard mute or soft mute control based on receive signal quality (REG73)
- Flexible block execution order (REG72)
- Expander to extent signal dynamic range (REG17)

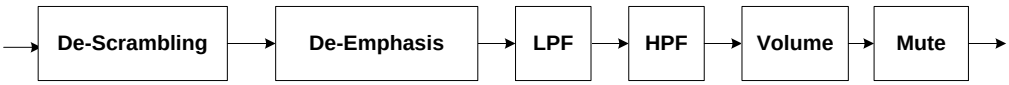

Figure 4 TX Audio Block Diagram

The RX signal strength before volume control module can be read out through REG74.

9.2 In-band Signaling

9.2.1 DTMF

DTMF decoder can detect up to 16 DTMF symbols simultaneously (REG78). High band tone frequency and low band tone frequency of each symbol can be programmed individually (REG77). When the decoder finds a symbol match, it will set corresponding bit and the found symbol address (REG78), and an

interrupt will be issued.

User can trade off detection sensitivity with response time by selection different match condition and their detection margin (REG75, REG76).

There are two symbol match conditions; the first (match condition 1) is the tone frequency variance less than a programmable margin DTMF_MARGIN2, and the second (match condition 2) is the tone frequency stay inside a deviation (DTMF_MARGIN1) from reference frequency for a programmable duration (DTMF_MARGIN3). User can enable either one of them or both of them for DTMF symbol match. SELCALL and CTCSS have the same match algorithm.

9.2.2 FSK

In FSK AIR mode, the slicer output of FM demodulator will be FSK symbol. In FSK mode, the FM demodulator output is taken as a sub-carrier, and will be demodulated with a FSK demodulator.

FSK receiver will search the sync word to establish synchronization with FSK transmitter. When it is synchronized and CRCA check is passed, a FSK head received interrupt (REG116) will be issued and it will continue to receive the payload. The payload data will be written to an 8 words FIFO, and when the data word number in FIFO is greater than a threshold that the FIFO needs to read out, it will issue an interrupt (REG116) and MCU should read out all data bytes in FIFO immediately (REG82, REG83). After all payload of one packet is received, the CRCB check result will be set (REG83) and a receive- finished interrupt will be issued to MCU that MCU should check this bit to know whether the read out payload is valid or invalid that should be discarded.

Note: With free format type (type 4), the “ FSK head received interrupt” will be given out immediately when it found the sync word , thus, this interrupt is earlier than that in other mode.

9.2.3 SELCALL

SELCALL decoder can detect up to 16 SELCALL symbols simultaneously (REG87). Frequency of each symbol can be programmed individually (REG86). When the decoder find a symbol match, it will set corresponding bit and the found symbol address (REG87), and an interrupt will be issued.

User can trade off detection sensitivity with response time by selection different match condition and their detection margin (REG84, REG85).

There is an optional high pass filter to filter out signal below 400 Hz (REG87), and user can bypass this filter to receive SELCALL symbol with frequency below 400 Hz.

9.3 Sub-audible Signaling

CTCSS decoder can detect up to 8 CTCSS symbols simultaneously (REG92). Frequency of each symbol can be programmed individually (REG91). When the decoder find a symbol match, it will set corresponding bit and the found symbol address (REG92), and an interrupt will be issued.

User can trade off CTCSS detection sensitivity with response time by selection different match condition and their detection margin (REG89, REG90). For example, setting REG89 [15:4] to 0xFF8 can improve the sensitivity and stability, at the cost of much longer response time. In practical use, initially user can set the REG89 [15:4] small to improve the response time, and after the CTCSS is found, user can change it to be larger to avoid link lose. It applies same for the REG90 where user can set the margin smaller initially and set them larger after the tone is found.

CTCSS decoder has an optional high pass filter to filter out DC signal (REG92), which can be used to get better RF frequency offset and low frequency noise immunity.

CDCSS decoder uses the same setting as CDCSS encoder, and has also an optional DC block filter (REG94).

10 MCU Interface

The MCU interface mainly consists of an IRQ interrupt and a 3-wires register access interface.

10.1 Interface Timing

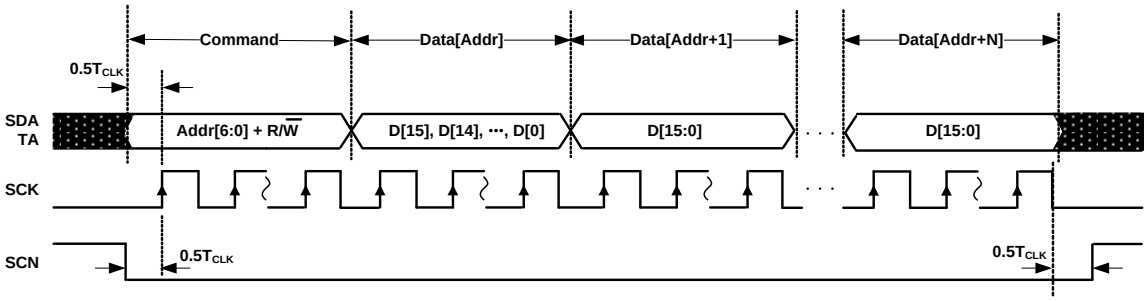

Figure 5 3-wires Interface Timing

The BK4811 always latch data at the SCK rising edge and output its data at SCK falling edge.

10.2 Interface Register Definition

Table 6 Interface Register Definition (Default setting for 409.75 MHz)

Address（DEC）	R/W	Recommend Setting	Sub-module	Description	
00	R	0x0000	Common	15:8	Device ID, read only
01	W/R	0x0000	Common	15	Channel spacing: 0: 12.5 kHz, 1: 25 kHz
				14	FSK_AIR data rate: 0:1.2kbps, 1:2.4kbps
				7:0	Chip ID
02 – 15			RF/Analog		
02	W/R	0x1804			
03	W/R	0x0800		15:13	VCO to LO divider number 0: 8; 1: 12; 2: 16; 3: 20; 4: 24
04	W/R	0x0055			
05	W/R	0xE023			
06	W/R	0x7FEA(Idle) 0x7FEA(TX) 0x4FEA(RX)		13	Power down RX IF ADC (1)
				12	Power down RX VGA (1)
07	W/R	0x9FFD(Idle) 0xFC49(TX) 0xD051(RX)		13	VCO state (0: RX, 1: TX)
				11	Power down RF AGC circuit (1)
				10	Power audio earpiece output (1)
				7	Power down crystal oscillator (1)
				5	Power down RF PLL (1)
				4	Power down TX chain blocks and their LDOs (1)

				3	Power down RX chain blocks and their LDOs (1)
				2	Power down the central bias, PLL and other common block (1)
				0	Using low power digital regulator (1)
08	W/R	0x7F95			
09	W/R	0xA1CF		Set to 0x61CF together with REG72[2:0]=2 and REG73[3:0]=F can improve the quality of compander, at the cost of higher back ground noise	
10	W/R	0x1C04(Idle) 0x1C00(TX) 0x1C04(RX)		2	Power down microphone (1)
11	W/R	0x8230			
13	W/R	0x8030			
14	W/R	0x08C0			
16	W/R	0x4B80		Used for IF = 121.875 kHz at narrow band mode	
17 – 63			Digital Transmitter		
17	W/R	0x8800	AUDIO	11	0: Enable digital compander 1: Disable digital compander
				1:0	Audio filter bandwidth 00: 2.55 kHz narrow band 01: 2.55 kHz width band 10: 3 kHz narrow band 11: 3 kHz width band
18	W/R	0x4068	AUDIO	15	Bypass Pre-emphasis (1)
				14	Bypass Frequency Inversion (1)
				11:9	PRE-emphasis/scrambling/ HPF order 3'd0: PRE->SCR->HPF 3'd1: PRE->HPF->SCR 3'd2: SCR->PRE->HPF 3'd3: SCR->HPF->PRE 3'd4: HPF->PRE->SCR 3'd5: HPF->SCR->PRE Others are not valid inputs
				8	Soft Limiter (1) or hard limiter (0)
				6:2	Volume: -25 dB (0) to 6 dB (31)

19	W/R	0x7000	AUDIO	15:12	Limiter level: -8 dBFS (0) ~ 7 dBFS (15)
				0	VOX trigger method 1: absolute level, 0: relative level
20	W/R	0x0000	AUDIO	15:13	Inversion frequency 3'd0: 2700, 3'd1: 2800 3'd2: 2900, 3'd3: 3000 3'd4: 3100, 3'd5: 3200 3'd6: 3300, 3'd7: 3400
21	R(15:8) W/R(7:0)	0x0000	AUDIO	15:8	Microphone signal level
				7:0	Microphone signal activity detection threshold
22	W/R(15:8) R(7:0)	0x3200	VOX	15	Enable VOX (1)
				14	Background noise detection speed 0: 1/65536, 1: 1/32768
				13	Speech detection speed 0: 1/512, 1: 1/256
				12:10	THD 3'd0: 2, 3'd1: 3, 3'd2: 4 3'd3: 6, 3'd4: 8, 3'd5: 12 3'd6: 16, 3'd7: 24
				9:8	VOX_DELAY 2'd0:100 ms, 2'd1:200 ms 2'd2:400 ms, 2'd3:800 ms
				7:0	Back ground noise level BACK_LEVEL
23	W/R	0x2000	TOT	15	Enable TOT 1: Enable 0: Disable
				14:12	TOT time out timer (Unit: second) 3'd0: 0.5, 3'd1: 1, 3'd2: 2 3'd3: 4, 3'd4: 8, 3'd5: 16 3'd6: 32, 3'd7: 64
24	W/R	0x086C	DTMF	15:0	Low frequency; Unit: 0.3234 Hz
25	W/R	0x13BA	DTMF	15:0	High frequency; Unit: 0.3234 Hz
26	W/R	0x0000	DTMF	15:12	Twist (Unit: dB); 4'd0: 0, 4'd1: 1 1 dB per step, 4'd15: 15
27	W/R	0x0000	FSK	15:0	Sync Word (Only be used in free frame type)

28	W/R	0x0000	FSK	15:8	Address
				7:0	Type 8'd0: Type 0, 8'd1: Type 1 8'd2: Type 2, 8'd3: Type 3 8'd4: Type 4 Others are not valid
29	W/R	0x0000	FSK	15:9	Size
				7:0	CRCA (Only be used in free frame type)
30	W	0x0000	FSK	15:0	Payload FIFO
31	W/R	0x8000	FSK	15:13	FIFO Threshold
				12	FIFO needs refilling 1: Needs refilling 0: No needs refilling
				3:0	Total words in write FIFO
32	WR	0x0000	FSK	15	Enable scrambling (1)
				14:8	Scrambling initial value
34	W/R	0x0740	SELCALL	15:0	SELCALL tone Frequency Unit: 0.3234 Hz
36	W/R	0x8000	CTCSS	15	CTCSS mode 0: Use internal frequency table (Not supported yet) 1: Frequency set by user
				14:13	The high 2 bits of CTCSS frequency
				1:0	Phase change (Unit: Degree) 0: 0, 1: 120, 2: 180. 3: 240
37	W/R	0x04D5	CTCSS	15:0	The low 16 bits of CTCSS frequency Unit: 0.0808 Hz

<table>
<tr><td>38</td><td>W/R</td><td>0xE000</td><td>CDCSS</td><td>
<table>
<tr><td>15</td><td>0: CDCSS is set by register
1: CDCSS symbol generated internal by low 9 bit of CDCSS code
Shared by both TX and RX</td></tr>
<tr><td>14</td><td>0: CDCSS not inversed
1: CDCSS inversed
Shared by both TX and RX</td></tr>
<tr><td>13</td><td>0: 23 bits CDCSS
1: 24 bits CDCSS
Shared by both TX and RX</td></tr>
<tr><td>11:0</td><td>High 12 bits of CDCSS if it has 24 bits or high 11 bits of CDCSS if it has 23 bits
Shared by both TX and RX</td></tr>
</table>
</td></tr>
<tr><td>39</td><td>W/R</td><td>0x0013</td><td>CDCSS</td><td>
<table>
<tr><td>11:0</td><td>Low 12 bits of CDCSS
Shared by both TX and RX</td></tr>
</table>
</td></tr>
<tr><td>40</td><td>W/R</td><td>0x9020</td><td>Transmitter</td><td>
<table>
<tr><td>15</td><td>1: In-band signal exists
0: No in-band signal</td></tr>
<tr><td>14:13</td><td>In-band signal type
00: Audio
01: DTMF
10: FSK
11: SELCALL</td></tr>
<tr><td>12:9</td><td>In-band signal deviation
0.2~1.9 (8 is about 1.5 kHz deviation by default)</td></tr>
<tr><td>7</td><td>1: Sub-audible signal exists
0: No sub-audible</td></tr>
<tr><td>6</td><td>Sub-audible signal type
0: CTCSS
1: CDCSS</td></tr>
<tr><td>5:2</td><td>Sub-audible signal deviation
0.08~ 0.38 (8 is about 300 Hz deviation by default)</td></tr>
</table>
</td></tr>
<tr><td>42</td><td>W/R</td><td>0x0000</td><td>RAMP</td><td>RAMP TABLE, should be written to address from 0 to
<table>
<tr><td>15:10</td><td>RAMP memory address</td></tr>
<tr><td>9:0</td><td>RAMP data</td></tr>
</table>
63, with linear up data</td></tr>
</table>

<table>
<tr>
<td>43</td>
<td>W/R</td>
<td>0x403F(Idle)
0x803F(TX)
0x403F(RX)</td>
<td>RAMP</td>
<td>
<table>
<tr><td>15</td><td>RAMP up enable
1: Enable
0: Disable</td></tr>
<tr><td>14</td><td>RAMP down enable
1: Enable
0: Disable</td></tr>
<tr><td>5:3</td><td>RAMP up speed
3’d0: 0.16 ms
3’d1: 0.16*2 ms
…
3’d6: 0.16*2^6 ms
3’d7: 0.16*2^6 ms</td></tr>
<tr><td>2:0</td><td>RAMP down speed, same as ramp up speed definition</td></tr>
</table>
</td>
</tr>
<tr>
<td>44</td>
<td>W/R</td>
<td>0xAA26</td>
<td>AUD_AGC</td>
<td>Microphone AGC
<table>
<tr><td>15</td><td>Audio AGC Enable (1)
When AGC is enabled, gain will be set internally by AGC, else can be set through bit 5:0 of this register</td></tr>
<tr><td>14:12</td><td>AGC target level
0: -3, 1: -6, 2: -9, 3: -12, 4: -15, 5: -18, 6: -21 (Default), 7: -24 dBFS</td></tr>
<tr><td>11</td><td>AGC gain change mode
1 (Default): step by step mode
0: one step mode</td></tr>
<tr><td>5:0</td><td>Audio AGC set value, 0.5 db each step</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr><td>45</td><td>W/R</td><td>0x1980</td><td>AUD_AGC</td><td><table>
<tr><td>15:14</td><td>Time taken by the output signal decrease to the target level when the input signal is greater than the target level + HYS
0: 12.5 ms, 1: 25 ms, 2: 50ms (Default), 3: 100 ms (Step Mode 0)
0: 1.25 ms, 1: 2.5 ms, 2: 5 ms (Default), 3: 10 ms (Step Mode 1)</td></tr>
<tr><td>13:12</td><td>Time taken by the output signal increase to the target level when the input signal is smaller than the target level
0: 250, 1: 500 (Default), 2: 1000, 3: 2000 (Unit: ms, Step Mode 0)
0: 5, 1: 10 (Default), 2: 20 , 3: 40 (Unit: ms, Step Mode 1)</td></tr>
<tr><td>11:6</td><td>Maximum value of AGC gain, 0..63, Default is 63</td></tr>
<tr><td>5:0</td><td>Minimum value of AGC gain, 0..63, Default is 32</td></tr>
</table></td></tr>
<tr><td>64 – 111</td><td></td><td></td><td>Digital Receiver</td><td></td></tr>
<tr><td>64</td><td>W/R</td><td>0x0000</td><td></td><td></td></tr>
<tr><td>65</td><td>W/R</td><td>0x0000</td><td></td><td></td></tr>
<tr><td>66</td><td>W/R</td><td>0xD083</td><td>FM_DEM</td><td><table>
<tr><td>15:14</td><td>Demodulator output amplitude
12.5 kHz space:
0: 1/2, 1: 1, 2: 2, 3: 4
25 kHz space:
0: 1/4, 1: 1/2, 2: 1, 3: 2</td></tr>
<tr><td>12</td><td>Parallel Audio enable</td></tr>
<tr><td>11</td><td>Parallel DTMF enable</td></tr>
<tr><td>10</td><td>Parallel FSK enable (can’t be set to 1 with FSK air enable at the same time)</td></tr>
<tr><td>9</td><td>Parallel SELCALL enable</td></tr>
<tr><td>8</td><td>Parallel FSK air enable (can’t be set to 1 with FSK enable at the same time)</td></tr>
<tr><td>7</td><td>1: Enable in-band signal receive
0: Disable in-band signal receive</td></tr>
<tr><td>4</td><td>1: Enable sub-audible signal receive
0: Disable sub-audible signal receiver</td></tr>
<tr><td>3</td><td>Sub-audible signal type
0: CTCSS, 1: CDCSS</td></tr>
<tr><td>2</td><td>Is in-band signaling FSK_AIR mode</td></tr>
</table></td></tr>
</table>

					1: Yes 0: No, determined by [6:5]
67	W/R	0xDA1D	RSSISNR	15:14	SNR/RSSI update period 11: 12.5 ms; 10: 25 ms 01: 50 ms; 00: 100 ms
				13:8	SNR threshold for auto soft mute
				6:0	RSSI threshold for auto soft mute
68	R	Ready Only	RSSISNR	14	SNR invalid 1: SNR result is invalid 0: SNR result is valid
				13:8	SNR indicator, 1 dB per step, 0 is minimum
				7	LNA RSSI 1: LNA gain should be set to 1 0: LNA gain should be set to 0
				6:0	RSSI indicator, 1 dB per step, 0 is minimum
69	W/R	0x1FFF	AFC	15	1: Disable AFC 0: Enable AFC
				14:13	AFC control gain 0: 1/8, 1: 1/4, 2: 1/2, 3: 1
				12:0	AFC threshold (Unit: Hz)

70	R	0x0000	AFC	5	AFC rail 1: AFC indicator > AFC threshold 0: Else
				14	Link state 1: Link is active 0: Link is lost
				13:0	AFC residue frequency offset (Hz)
71	W/R	0x1E20		13:8	SNR threshold for AFC
				6:0	RSSI threshold for AFC
72	W/R	0x2006	BB_FLT	13	1: Bypass Frequency Inversion 0: Not Bypass
				12	1: Bypass De-emphasis 0: Not Bypass De-emphasis
				9:7	HPF/ de-scrambling /de-emphasis execution order 3'b000: HPF->SCR->EMP 3'b001: HPF->EMP->SCR 3'b010: SCR->HPF->EMP 3'b011: SCR->EMP->HPF 3'b100: EMP->HPF->SCR 3'b101: EMP-> SCR->HPF
				3:0	RX volume control before DAC
73	W/R	0x230D	AUDIO	15	1: Hard Mute
				3:0	Volume 4'd0: -39dB, 4'd1: -36dB 3 dB per step 4'd15: 6 dB
74	W/R	0x0000	AUDIO	15:13	Inversion frequency (Unit: Hz) 3'd0: 2700, 3'd1: 2800 3'd2: 2900, 3'd3: 3000 3'd4: 3100, 3'd5: 3200 3'd6: 3300, 3'd7: 3400
				7:0	RX_AUDIO_LEVEL (Read only)
75	W/R	0x7A80	DTMF	15:5	DTMF detection speed Suggest value: 1960
				2	DTMF_MARGIN1 mode 0: 0-6.3% 1: 0-63 Hz

				1	DTMF_MARGIN2 mode 0: 0-6.3% 1: 0-63 Hz
				0	DTMF_MARGIN3, 0: 5 ms; 1:10 ms
76	W/R	0xE204	DTMF	15:10	DTMF_MARGIN1 0: 0% or 0 Hz 0.1% or 1 Hz per step 63: 6.3% or 63 Hz
				9:4	DTMF_MARGIN2 Same definition as DTMF_MARGIN1
				2	1: Use match condition 1
				1	1: Use match condition 2
				0	0: Use set frequency as reference 1: Use detected frequency as reference
77	W	0x0000	DTMF	DTMF_TABLE	
				15:12	DTMF symbol address
				11	DTMF Symbol frequency band 0: low band, 1: high band
				10:0	DTMF symbol low band or high band tone frequency Unit: 1.0347 Hz
78	W/R	0x8000	DTMF	15	0: DTMF symbol frequency uses internal table (Not supported yet) 1: DTMF symbol frequency is set by user
				7:4	Address of found DTMF symbol
				3:0	DTMF symbol numbers in search table
79	R	0x0000	FSK	15:8	Address
				7:0	Type
80	R	0x0000	FSK	15:9	Size
				7:0	CRCA (Only used in free frame type
81	W/R	0xB200	FSK	15:5	Symbol detection speed Suggest value: 1424
82	R	0x0000	FSK	15:0	Payload FIFO

83	W/R	0x8000	FSK	15:13	FIFO Threshold
				12	FIFO needs reading out
				5	Free format type
				4	CRCB_OK 1: No error in payload 0: Error in payload, will be automatically updated at the end of new RX packet
				3:0	Total words in read FIFO
84	W/R	0xFC40	SELCALL	15:5	SELCALL detection speed Suggest value: 2018
				2	MARGIN 1 mode 0: 0-6.3% 1: 0-63 Hz
				1	MARGIN2 mode 0: 0-6.3% 1: 0-63 Hz
				0	MARGIN3 0: 5 ms, 1: 10 ms
85	W/R	0x70A6	SELCALL	15:10	MARGIN1
				9:4	MARGIN2
				2	1: Use match condition 1
				1	1: Use match condition 2
				0	0: Use set frequency as reference 1: Use detected frequency as reference
86	W	0x03A0	SELCALL	15:12	SELCALL Symbol Address
				11:0	SELCALL symbol frequency Unit: 0.6467 Hz
87	W/R	0x8000	SELCALL	15	0: SELCAL symbol frequency uses internal table (Not supported yet) 1: SELCALL symbol frequency is set by user
				14	HPF_BYPASS 0: No bypass 1: Bypass
				13	1: Found symbol is lost
				7:4	The address of found SELCALL symbol
				3:0	SELCALL symbol numbers in search table
89	W/R	0xF7A1	CTCSS	15:4	CTCSS detection speed

					Suggest value: 3962
				2	MARGIN 1 mode 0: 0-6.3% 1: 0-63 (Unit: 0.1616 Hz)
				1	MARGIN2 mode 0: 0-6.3% 1: 0-63 (Unit: 0.0404 Hz)
				0	MARGIN3 0: 20 ms, 1: 40 ms
90	W/R	0x3C66	CTCSS	15:10	MARGIN1
				9:4	MARGIN2
				2	1: Use match condition 1
				1	1: Use match condition 2
				0	0: Use set frequency as reference 1: Use detected frequency as reference
91	W	0x09aa	CTCSS	CTCSS TABLE	
				15:13	CTCSSS symbol address
				12:0	CTCSSS symbol frequency Unit: 0.0404 Hz
92	W/R	0x8000	CTCSS	15	0: CTCSS symbol frequency uses internal table (Not supported yet) 1: CTCSS symbol frequency is set by user
				14	1: Bypass HPF
				13	1: Found CTCSS symbol is lost
				7:4	The address of found CTCSS symbol
				2:0	CTCSS symbol numbers in search table
94	W/R	0x8000	CDCSS	15	1: Bypass HPF
				1	1: CDCSS code lost match
				0	1: CDCSS code is matched
101	R	Read Only	RF AGC	15:8	AGC_H; IF RSSI high level indicator
				7:0	AGC_L; IF RSSI low level indicator
108	W/R	0x81A2	RF AGC	15	RF AGC disable 0: Enable RF AGC 1: Use manually set value
				8	LNA gain manually set value 1: High gain, 0: low gain
				7:4	PGA manually set value

112-119	W/R		Control and Interrupt	
112	W/R	0xA000 (Idle) 0xE000 (TX) 0xA000 (RX)	Operation Control	15: Power up digital section (1), Power down digital section (0) 14: Digital logic operation mode 1: TX mode, 0: RX mode 13: 1: Normal work, 0: Software reset, it will not reset interface registers 4:0: Channel Number Frequency = First Channel Frequency + Channel Number * Channel Space
113	W/R	0x4B81	Frequency control	15:0: High 16 bits of First Channel Frequency
114	W/R	0xEA5C	Frequency control	15:0: Low 16 bits of First Channel Frequency
115	W/R	0x0000	Interrupt MASK	15: 1: Enable interrupt 0: Disable all interrupt 14: Enable FSK transmit success interrupt 13: Enable FSK transmitter FIFO need fill interrupt 12: Enable FSK head receive success interrupt 11: Enable FSK receiver FIFO need read interrupt 10: Enable DTMF receive interrupt 9: Enable SELCALL receive interrupt 8: Enable CTCSS receive interrupt 7: Enable CTCSS tone loss interrupt 6: Enable link lost interrupt (RSSI and SNR are less than their threshold) 5: Enable CDCSS receive interrupt 4: Enable CDCSS code lost match interrupt 3: Enable VOX voice detected interrupt 2: Enable TOT time out interrupt 1: Enable FSK receive complete interrupt 0: Enable image calibration finished interrupt
116	W/R	0x0000	Interrupt flags (Active high) Set by hardware	15: 1: Reset all flags to zeros 14: FSK transmit success interrupt 13: FSK transmitter FIFO need fill interrupt 12: FSK head receive success interrupt

			and reset by software (write 1 will clear interrupt bit to 0)	11	FSK receiver FIFO need read interrupt
				10	DTMF receive interrupt
				9	SELCALL receive interrupt
				8	CTCSS receive interrupt
				7	CTCSS tone loss interrupt
				6	Link lose interrupt
				5	CDCSS receive interrupt
				4	CDCSS code lost match interrupt
				3	VOX voice detected interrupt (Can only be cleared in TX mode)
				2	TOT time out interrupt (Can only be cleared in RX mode)
				1	FSK receive complete interrupt
				0	Image calibration finished interrupt
117	W/R	0x0000	GPIO	12	1: Loop TX in-band signal to RX audio path
				10	0: Normal IF, low side injection 1: Opposite IF, high side injection
				5:4	GPIO2 mode control 00: as input 01: output low 10: output high 11: reserved
				3:2	GPIO1 mode control, as GPIO2
				1:0	GPIO0 mode control, as GPIO2
118	R	0x0000	GPIO	2	GPIO2 input value
				1	GPIO1 input value
				0	GPIO0 input value
125	W/R	0x0000	Squelch	8	Threshold for glitch pulse 1: 3/4pi, 0: pi/2
				7:0	Glitch counter (ready only)
126	W/R	0x0048	Frequency control	4	IF constant, different for each operation band
				3:0	TX deviation gain control 0: 1/8; 1: 2/8; 15: 2
127	W/R	0x9701	Frequency control	IF constant, different for each operation band	

Note: Please don’t modify reserved registers and registers without definition.

11 Electrical Specification

Table 7 BK4811 Characteristics – Preliminary

Name	Parameter (Condition)	Min	Typical	Max	Unit
VBAT	Battery voltage VBAT, VCCx	2.4	3.3	3.6	V
TEMP	Temperature	-20	+27	+65	ºC
IVDD	Power down current via register	10	140		uA
IVDD	RX current		47		mA
IVDD	TX current		39		mA
FOP	Operating frequency		117 ~ 525		MHz
FXTAL	Crystal frequency		21.7		MHz
MICSEN	Microphone sensitivity to 1. 5 kHz deviation		3.3		mV
PRF	Output power		4		dBm
PRF1	Adjacent channel emission(12.5 kHz channel spacing)		-65		dBc
TSINAD	Transmit signal to noise ratio		46		dB
RXSENS	12 dB SINAD sensitivity [1]		-123		dBm
C/I1ST	Adjacent channel selectivity		59		dB
BLOCK	Block selectivity		69		dB
	Audio				dB
EARO	Earpiece output level at 1.5 kHz deviation		144		mVrms
ASNR	SINAD [1]		52		dB
ARES	Amplitude response	-3		3	dB
ANF	Audio noise floor		-81		dBm
	CTCSS/XTCSS				
CTSEN	CTCSS sensitivity [2]		-120		dBm
CTRES	CTCSS response time	75		125	ms
SAF	Frequency range	62.5		250.3	Hz
SAA	Frequency accuracy		0.3%		
	DCS				
CDSEN	CDCSS sensitivity [2]		-120		
CDRES	CDCSS response time		350		ms
CLEN	Code length	23		24	Bit
BRATE	Bit rate		134.4		Hz
BRA	Bit rate accuracy		0.5		Hz
	SELCALL				
SELSEN	SELCALL sensitivity [1]		-120		dBm
SELRES	SELCALL response time		30		ms
IBSF	Frequency range	400		3000	Hz
IBSA	Frequency accuracy		0.3%		
	DTMF				
DTSEN	DTMF sensitivity [1]		-118		dBm
DTRES	DTMF response time		20		ms
FH	High band frequency range	1209		1633	Hz
FL	Low band frequency range	697		941	Hz
	FSK data modem (F3E and F2D)				
FSKSEN	FSK sensitivity (1E-3 BER) [1]		-120		dBm
FSKBEST	FSK Best PER (32 bytes payload)		0.1%	1%	
BAUD	Over the air data rate	1200		2400	bps

12 Package

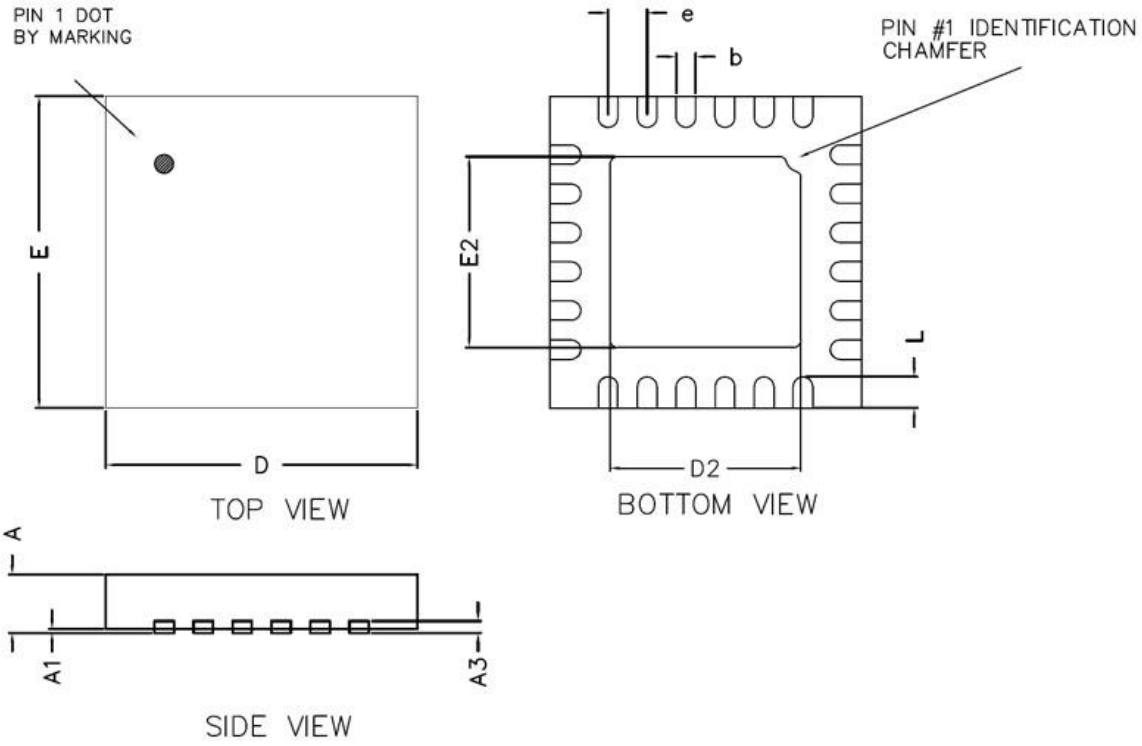

Table 8 QFN4*4 24 Pin Package Dimensions

Parameter	Min	Typ	Max	Unit
A	0.70	0.75	0.80	mm
A1	0.00	-	0.05	mm
A3		0.20 REF		mm
D	3.95	4.00	4.05	mm
E	3.95	4.00	4.05	mm
b	0.20	0.25	0.30	mm
L	0.35	0.40	0.45	mm
D2	2.30	2.45	2.55	mm
E2	2.30	2.45	2.55	mm
e		0.50 REF		mm

13 Order Information

Table 9 BK4811 Order Information

Part number	Package	Packing	MOQ (ea)
BK4811QB	QFN	Tape Reel	3 k
BK4811QC	QFN	Tray	10 k

Remark:

MOQ: Minimum Order Quantity

14 Application Schematic

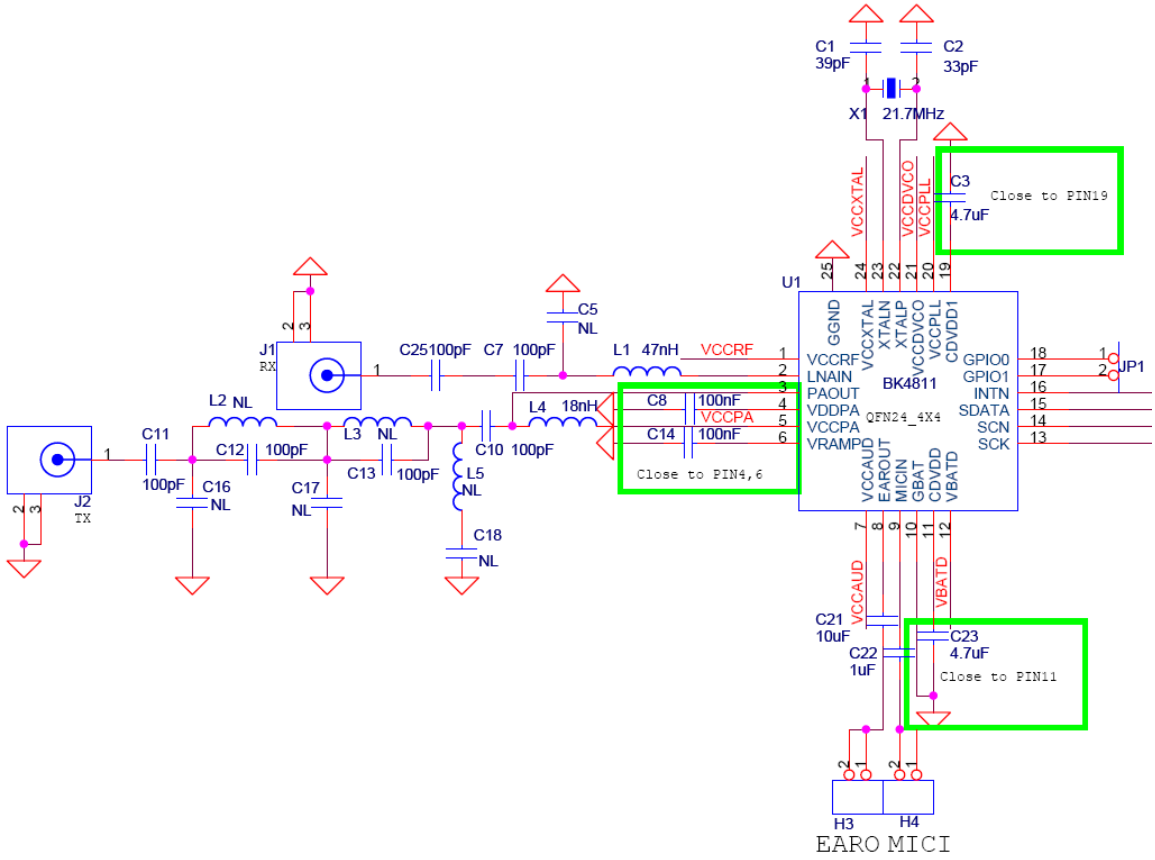

Figure 6 Application Schematic of BK4811