WENTAO ZHANG

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EDUCATION

University of Michigan, Michigan *Expected Dec 2021*
M.S in Computer Science *GPA:3.854/4.00*

University of Michigan, Michigan *May 2020*
B.S.E in Computer Engineering *GPA:3.854/4.00*

Shanghai Jiao Tong University, Shanghai *August 2020*
B.S.E in Electrical and Computer Engineering *GPA:3.4/4.00*

PROJECT EXPERIENCE

Out-of-Order P6 Schematic Processor Jan. 2020 - Apr. 2020
EECS470-Computer Architecture Final Project, Group Project, Leader Ann Arbor, MI

- Designed and implemented a 2-way out-of-order processor in P6 schematic with System Verilog. The processor includes the following feature:
  Instruction cache prefetcher, Local Branch Predictor, Return Address Stack, Load Store Queue, Write-back 2-way Set Associative Data Cache.
- Debugged and tested the processor with shell script.

Customized Accelerator for Attention Based CNN Sep. 2019 - Dec. 2019
EECS498-Accelerator for AI and Health, Group Project, Member Ann Arbor, MI

- Designed an accelerator for the Attention Based CNN convolution layer in System Verilog. We use the look-up table for the multiplication result and use systolic array to speed up the addition procedure in CNN layer to accelerate the CNN computation.
- We got 23X performance improvement, compared with the CPU version. (CPU version: Intel 9th i7, 2.60GHz, Data Set: DeepLearns dataset "glove.6B.300d.txt".)
- Analyzed the workload of the BWA gene seed extension algorithm using Perf.

GPU optimization for MXNet Library Sep. 2019 - Dec. 2019
EECS498- Applied GPU Programming Final Project Ann Arbor, MI

- Used webGPU to optimize the calculation of the forward pass convolution layer in MXNet Library (written in CUDA).
- Utilized shared memory, kernel fusion for matrix-multiplication to get 51X performance improvement in convolution.

Improvement of Saliency Optimization from Robust Background Detection May. 2020
EECS442- Computer Vision Final Project Ann Arbor, MI

- Implemented the Saliency Optimization from Robust Background Detection.
- Improved the algorithm by pre-processing the image using edge detection.

16-bit Lookahead Adder Sep. 2018 - Dec. 2018
EECS312- Digital Integrated Circuits Final Project Ann Arbor, MI

- Implemented a 16-bit adder with lookahead feature with Cadence.

RESEARCH EXPERIENCE

VLSI Design and Automation Lab May. 2019 - Feb. 2020
Research Intern, Advised by Prof David Blaauw Ann Arbor, MI

- Programmed the Arm cortex-M4 processor to communicate other layers in micro sensor stacks through Mbus protocol.
- Used Labview to develop a control system to collect the maximum load current and power efficiency information of the PMU under 600 different settings automatically.

CADRE Lab Nov. 2018 - May. 2019
Research Assistant Ann Arbor, MI

- Developed circuit features extraction tool to collect circuits and pin information from 2k circuit data sheets with an accuracy of 90%.
- Researched in using Bag of Words and Multinomial Bayes Classifier to classify the circuit data sheets.

Yoon's Lab Jan. 2019 - May. 2019
Research Assistant Ann Arbor, MI

- Programmed the new developed hardware board supported by Opal Kelly FPGA to generate 12 independent output current in user defined waveform in 12 different ports.
- Participated in GUI design of the control system based on the Opal Kelly FPGA.

LEADERSHIP EXPERIENCE

Multidisciplinary Design Program: Sensor Network Laboratory Jan. 2019 - Now
The Multidisciplinary Design program is aimed to cultivating the sense of cooperation, innovation and communication skills of students and let them prepared for the industry.
Member Ann Arbor, MI

- Communicate with the team members every two weeks to check the project progress and report the result to team leader.
- Modified the Maple seed V3R1 PCB board memory communication protocol from SPI to I2C to reduce the pins it uses for data communication.

SKILLS

Language: System Verilog, C, C++, Python, Cuda, Arduino, Matlab, Labview