

WENTAO ZHANG

1760 Broadway Street, Ann Arbor, MI, 48105
(+1)7343539808 ◊ zwtao@umich.edu

EDUCATION

University of Michigan, Michigan
B.S.E in Computer Engineering

May 2020
GPA:3.854/4.00

Shanghai Jiao Tong University, Shanghai
B.S.E in Electrical and Computer Engineering

Expected August 2020
GPA:3.4/4.00

PROJECT EXPERIENCE

Out-of-Order P6 Schematic Processor Jan. 2020 - Apr. 2020
EECS470-Computer Architecture Final Project, Group Project, Leader Ann Arbor, MI

- Designed and implemented a 2-way out-of-order processor in P6 schematic with System Verilog. The processor includes the following feature:
Instruction cache prefetcher, Local Branch Predictor, Return Address Stack, Load Store Queue, Write-back 2-way Set Associative Data Cache.
- Debugged and tested the processor with shell script.

Customized Accelerator for Attention Based CNN Sep. 2019 - Dec. 2019
EECS498-Accelerator for AI and Health, Group Project, Member Ann Arbor, MI

- Designed an accelerator for the Attention Based CNN convolution layer in System Verilog. We use the look-up table for the multiplication result and pipeline the addition procedure in CNN layer to accelerate the CNN computation.
- We got 23X performance improvement, compared with the CPU version. (CPU version: Intel Intel 9th i7, 2.60GHz, Data Set: DeepLearns dataset "glove.6B.300d.txt.")
- Analyzed the workload of the BWA gene seed extension algorithm using Perf.

GPU optimization for MXNet Neutral Network Sep. 2019 - Dec. 2019
EECS498- Applied GPU Programming Final Project Ann Arbor, MI

- Used webGPU to optimize the calculation in the forward pass convolution layer of MXNet (written in CUDA).
- Utilized shared memory, kernel fusion for enrolling and matrix-multiplication to get 51X performance improvement in convolution.

16-bit Lookahead Adder Sep. 2018 - Dec. 2018
EECS312- Digital Integrated Circuits Final Project Ann Arbor, MI

- Implemented a 16-bit adder with lookahead feature with Cadence.

RESEARCH EXPERIENCE

VLSI Design and Automation Lab May. 2019 - Feb. 2020
Research Intern, Advised by Prof David Blaauw Ann Arbor, MI

- Programmed the Arm cortex-M4 processor to communicate other layers in micro sensor stacks through Mbus protocol.
- Used Labview to develop a control system to collect the maximum load current and power efficiency information of the PMU under 600 different settings automatically.