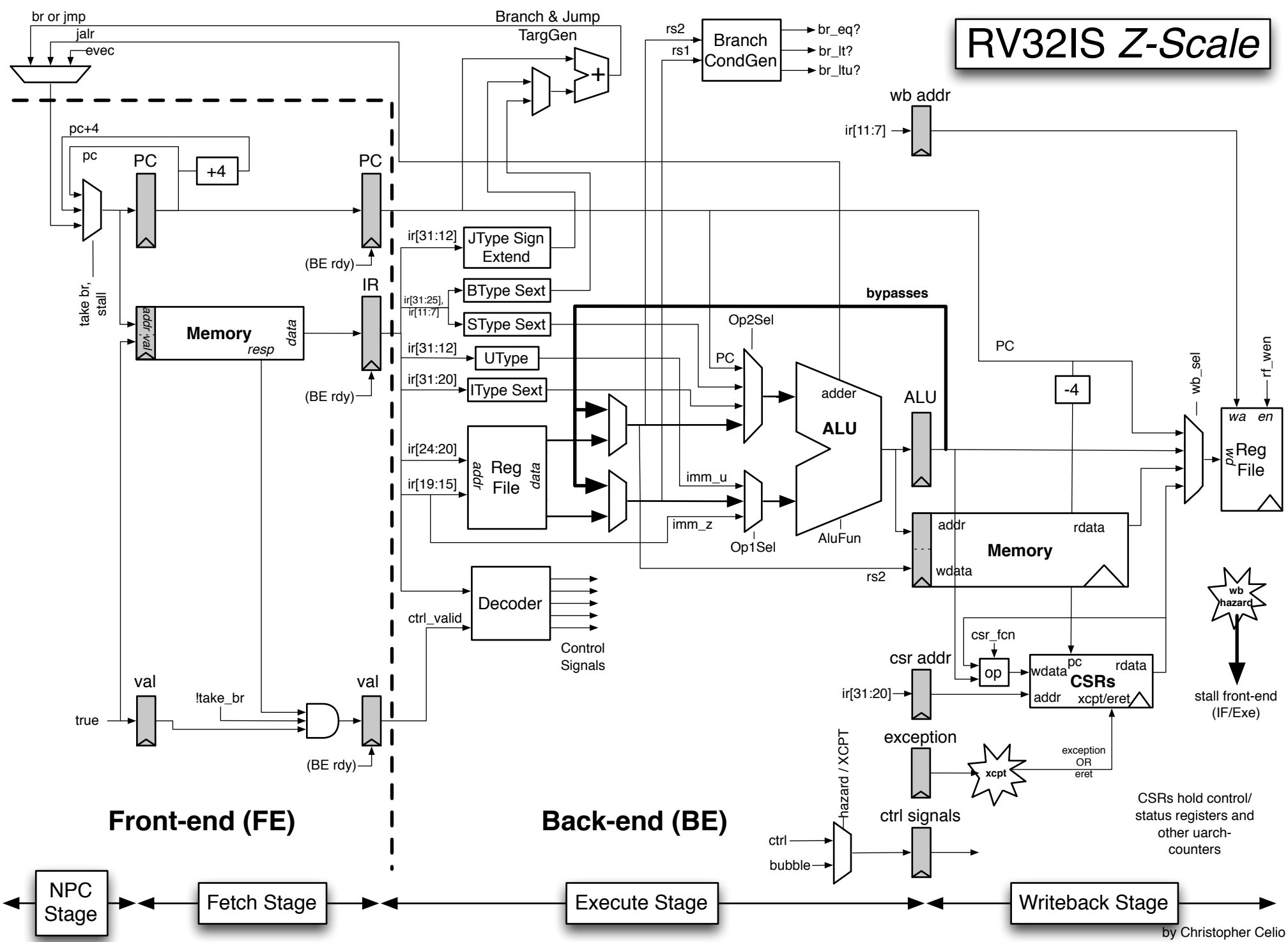
RV32IS Z-Scale
br or jmp
jalr
evec
Branch & Jump
TargGen
rs2
rs1
Branch
CondGen
br_eq?
br_lt?
br_ltu?
wb addr
ir[11:7]
pc+4
pc
PC
+4
PC
(BE rdy)
take br,
stall
IR
Memory
addr
val
data
resp
(BE rdy)
ir[31:12]
JType Sign
Extend
ir[31:25],
ir[11:7]
BType Sext
SType Sext
ir[31:12]
UType
ir[31:20]
IType Sext
ir[24:20]
ir[19:15]
Reg
File
addr
data
Decoder
ctrl_valid
Control
Signals
bypasses
Op2Sel
PC
adder
ALU
ALU
imm_u
imm_z
Op1Sel
AluFun
rs2
PC
-4
wb_sel
rf_wen
wa
en
wd
Reg
File
addr
rdata
Memory
wdata
wb
hazard
stall front-end
(IF/Exe)
csr_fcn
csr addr
op
wdata
pc
rdata
CSRs
addr
xcpt/eret
ir[31:20]
exception
xcpt
exception
OR
eret
hazard / XCPT
ctrl signals
ctrl
bubble
CSRs hold control/
status registers and
other uarch-
counters
val
!take_br
val
true
(BE rdy)
Front-end (FE)
Back-end (BE)
NPC
Stage
Fetch Stage
Execute Stage
Writeback Stage
by Christopher Celio