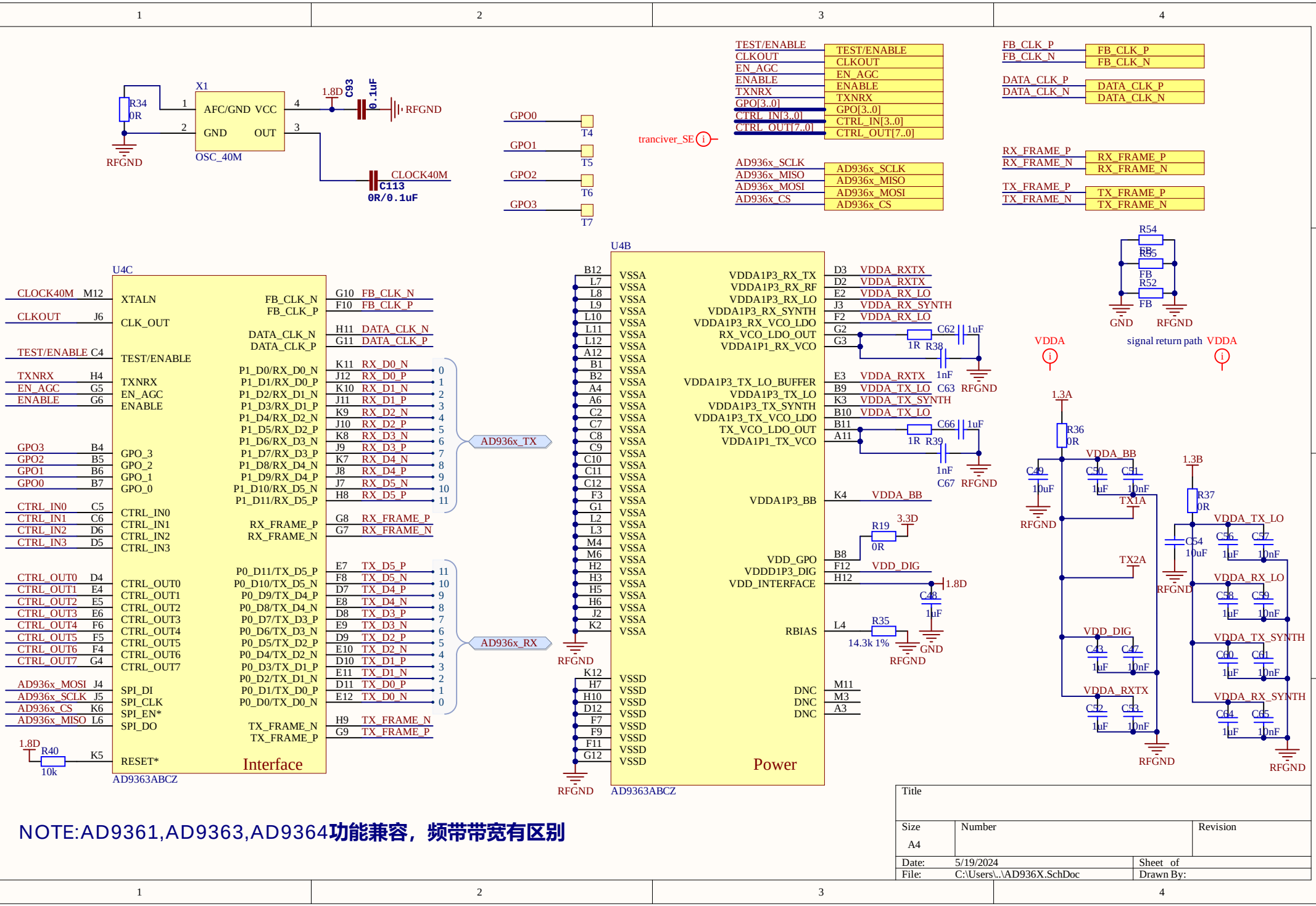
X1
R34
0R
AFC/GND
VCC
GND
OUT
OSC_40M
1.8D
C93
0.1uF
RFGND
CLOCK40M
C113
0R/0.1uF
GPO0
GPO1
GPO2
GPO3
T4
T5
T6
T7
tranciver_SE
TEST/ENABLE
CLKOUT
EN_AGC
ENABLE
TXNRX
GPO[3..0]
CTRL_IN[3..0]
CTRL_OUT[7..0]
AD936x_SCLK
AD936x_MISO
AD936x_MOSI
AD936x_CS
FB_CLK_P
FB_CLK_N
DATA_CLK_P
DATA_CLK_N
RX_FRAME_P
RX_FRAME_N
TX_FRAME_P
TX_FRAME_N
U4C
CLOCK40M M12
XTALN
CLKOUT J6
CLK_OUT
TEST/ENABLE C4
TXNRX H4
EN_AGC G5
ENABLE G6
GPO3 B4
GPO2 B5
GPO1 B6
GPO0 B7
GPO_3
GPO_2
GPO_1
GPO_0
CTRL_IN0 C5
CTRL_IN1 C6
CTRL_IN2 D6
CTRL_IN3 D5
CTRL_IN0
CTRL_IN1
CTRL_IN2
CTRL_IN3
CTRL_OUT0 D4
CTRL_OUT1 E4
CTRL_OUT2 E5
CTRL_OUT3 E6
CTRL_OUT4 F6
CTRL_OUT5 F5
CTRL_OUT6 F4
CTRL_OUT7 G4
CTRL_OUT0
CTRL_OUT1
CTRL_OUT2
CTRL_OUT3
CTRL_OUT4
CTRL_OUT5
CTRL_OUT6
CTRL_OUT7
AD936x_MOSI J4
AD936x_SCLK J5
AD936x_CS K6
AD936x_MISO L6
SPI_DI
SPI_CLK
SPI_EN*
SPI_DO
1.8D
R40
10k
K5
RESET*
Interface
AD9363ABCZ
FB_CLK_N G10
FB_CLK_P F10
DATA_CLK_N H11
DATA_CLK_P G11
P1_D0/RX_D0_N K11 RX_D0_N 0
P1_D1/RX_D0_P J12 RX_D0_P 1
P1_D2/RX_D1_N K10 RX_D1_N 2
P1_D3/RX_D1_P J11 RX_D1_P 3
P1_D4/RX_D2_N K9 RX_D2_N 4
P1_D5/RX_D2_P J10 RX_D2_P 5
P1_D6/RX_D3_N K8 RX_D3_N 6
P1_D7/RX_D3_P J9 RX_D3_P 7
P1_D8/RX_D4_N K7 RX_D4_N 8
P1_D9/RX_D4_P J8 RX_D4_P 9
P1_D10/RX_D5_N J7 RX_D5_N 10
P1_D11/RX_D5_P H8 RX_D5_P 11
AD936x_TX
RX_FRAME_P G8
RX_FRAME_N G7
P0_D11/TX_D5_P E7 TX_D5_P 11
P0_D10/TX_D5_N F8 TX_D5_N 10
P0_D9/TX_D4_P D7 TX_D4_P 9
P0_D8/TX_D4_N E8 TX_D4_N 8
P0_D7/TX_D3_P D8 TX_D3_P 7
P0_D6/TX_D3_N E9 TX_D3_N 6
P0_D5/TX_D2_P D9 TX_D2_P 5
P0_D4/TX_D2_N E10 TX_D2_N 4
P0_D3/TX_D1_P D10 TX_D1_P 3
P0_D2/TX_D1_N E11 TX_D1_N 2
P0_D1/TX_D0_P D11 TX_D0_P 1
P0_D0/TX_D0_N E12 TX_D0_N 0
AD936x_RX
TX_FRAME_N H9
TX_FRAME_P G9
U4B
B12 VSSA
L7 VSSA
L8 VSSA
L9 VSSA
L10 VSSA
L11 VSSA
L12 VSSA
A12 VSSA
B1 VSSA
B2 VSSA
A4 VSSA
A6 VSSA
C2 VSSA
C7 VSSA
C8 VSSA
C9 VSSA
C10 VSSA
C11 VSSA
C12 VSSA
F3 VSSA
G1 VSSA
L2 VSSA
L3 VSSA
M4 VSSA
M6 VSSA
H2 VSSA
H3 VSSA
H5 VSSA
H6 VSSA
J2 VSSA
K2 VSSA
K12 VSSD
H7 VSSD
H10 VSSD
D12 VSSD
F7 VSSD
F9 VSSD
F11 VSSD
G12 VSSD
RFGND
VDDA1P3_RX_TX D3 VDDA_RXTX
VDDA1P3_RX_RF D2 VDDA_RXTX
VDDA1P3_RX_LO E2 VDDA_RX_LO
VDDA1P3_RX_SYNTH J3 VDDA_RX_SYNTH
VDDA1P3_RX_VCO_LDO F2 VDDA_RX_LO
RX_VCO_LDO_OUT G2
VDDA1P1_RX_VCO G3
C62 1uF
1R R38
1nF
C63 RFGND
VDDA1P3_TX_LO_BUFFER E3 VDDA_RXTX
VDDA1P3_TX_LO B9 VDDA_TX_LO
VDDA1P3_TX_SYNTH K3 VDDA_TX_SYNTH
VDDA1P3_TX_VCO_LDO B10 VDDA_TX_LO
TX_VCO_LDO_OUT B11
VDDA1P1_TX_VCO A11
C66 1uF
1R R39
1nF
C67 RFGND
VDDA1P3_BB K4 VDDA_BB
R19 3.3D
0R
VDD_GPO B8
VDDD1P3_DIG F12 VDD_DIG
VDD_INTERFACE H12
1.8D
C48 1uF
RBIAS L4
R35
14.3k 1%
GND
RFGND
DNC M11
DNC M3
DNC A3
Power
AD9363ABCZ
R54
R55
FB
R52
FB
GND
RFGND
VDDA
signal return path VDDA
1.3A
R36
0R
VDDA_BB
C49 10uF
C50 1uF
C51 10nF
TX1A
RFGND
TX2A
VDD_DIG
C46 1uF
C47 10nF
VDDA_RXTX
C52 1uF
C53 10nF
RFGND
1.3B
R37
0R
C54 10uF
RFGND
VDDA_TX_LO
C56 1uF
C57 10nF
VDDA_RX_LO
C58 1uF
C59 10nF
VDDA_TX_SYNTH
C60 1uF
C61 10nF
VDDA_RX_SYNTH
C64 1uF
C65 10nF
RFGND
RFGND
NOTE:AD9361,AD9363,AD9364功能兼容，频带带宽有区别
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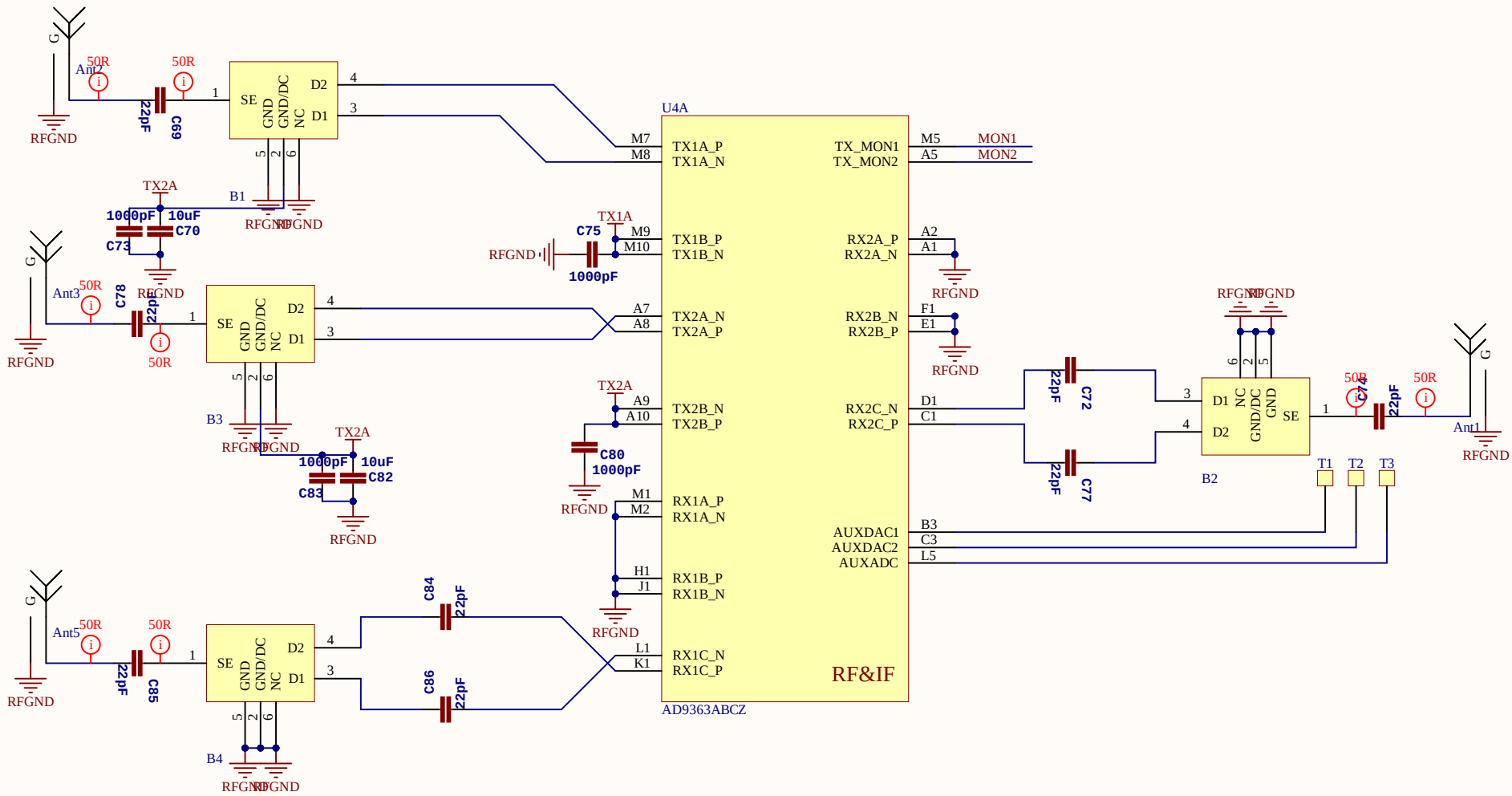

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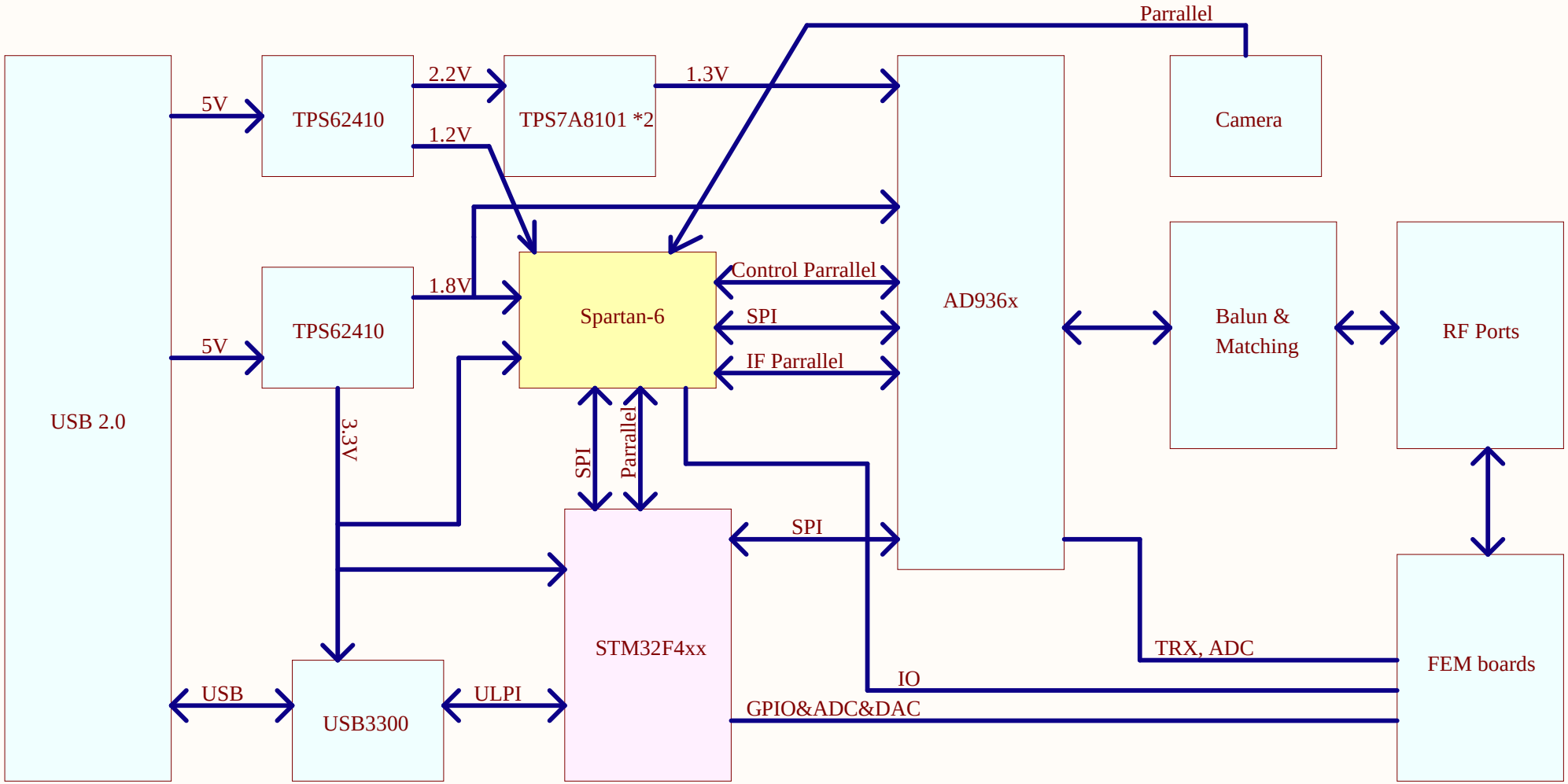

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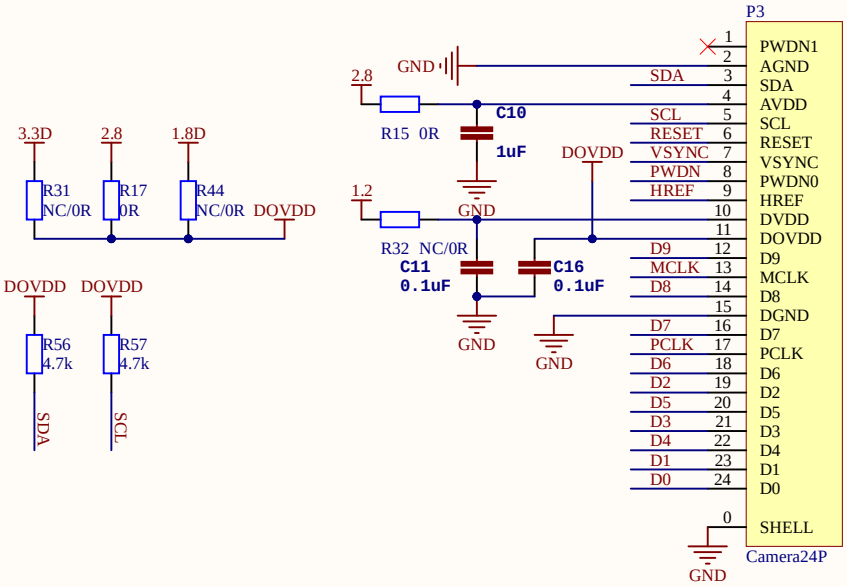

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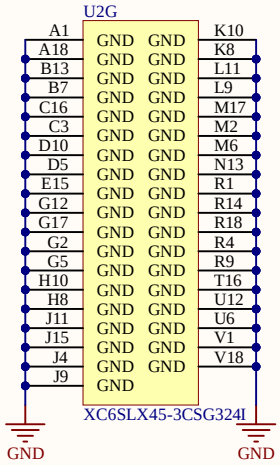
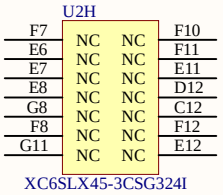
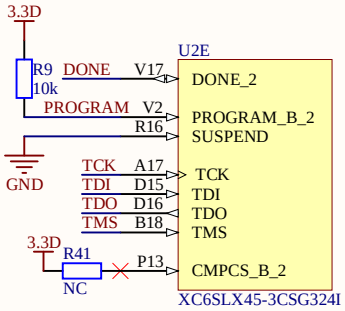
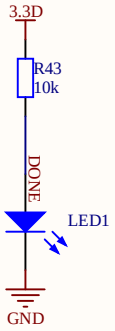








IO voltage notes:

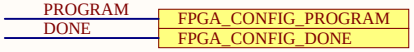
VCCAUX :all JTAG IO, SUSPEND, VFS, VBATT

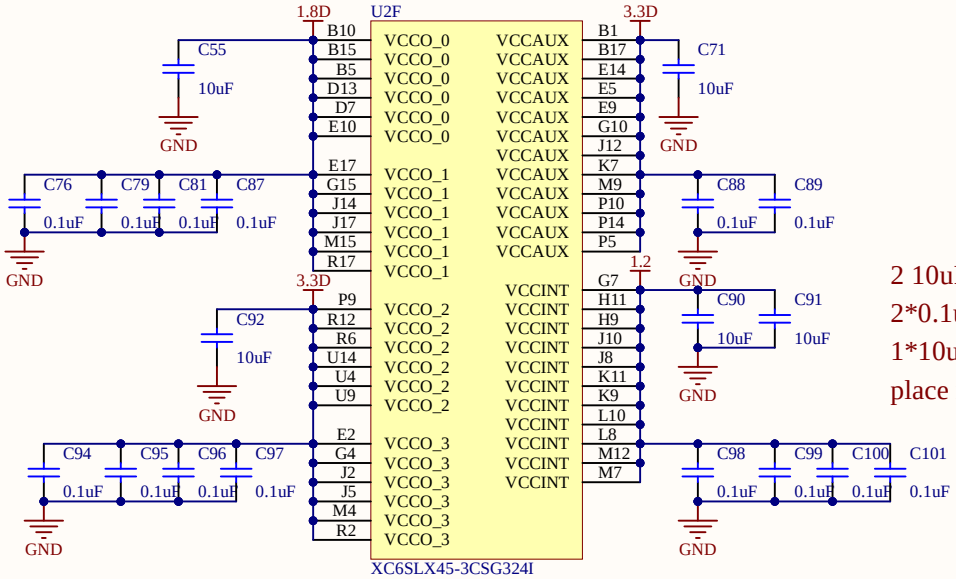
VCCO_0 HSWAPEN

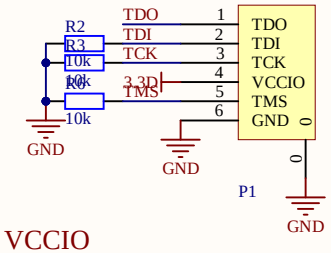
VCCO_1: DOUT

VCCO_2: M0,M1,PROGRAM_B,CCLKC,DIN, INIT_B,DONE

configuration port on BANK2







2 10uF for VCCINT, 1 10uF for each VCCIO

2*0.1uF for each bank, 4*0.1uF for VCCINT

1*10uF + 2*0.1uF for VCCAUX

place near vias

note: FLASH pins on bank2

Title		
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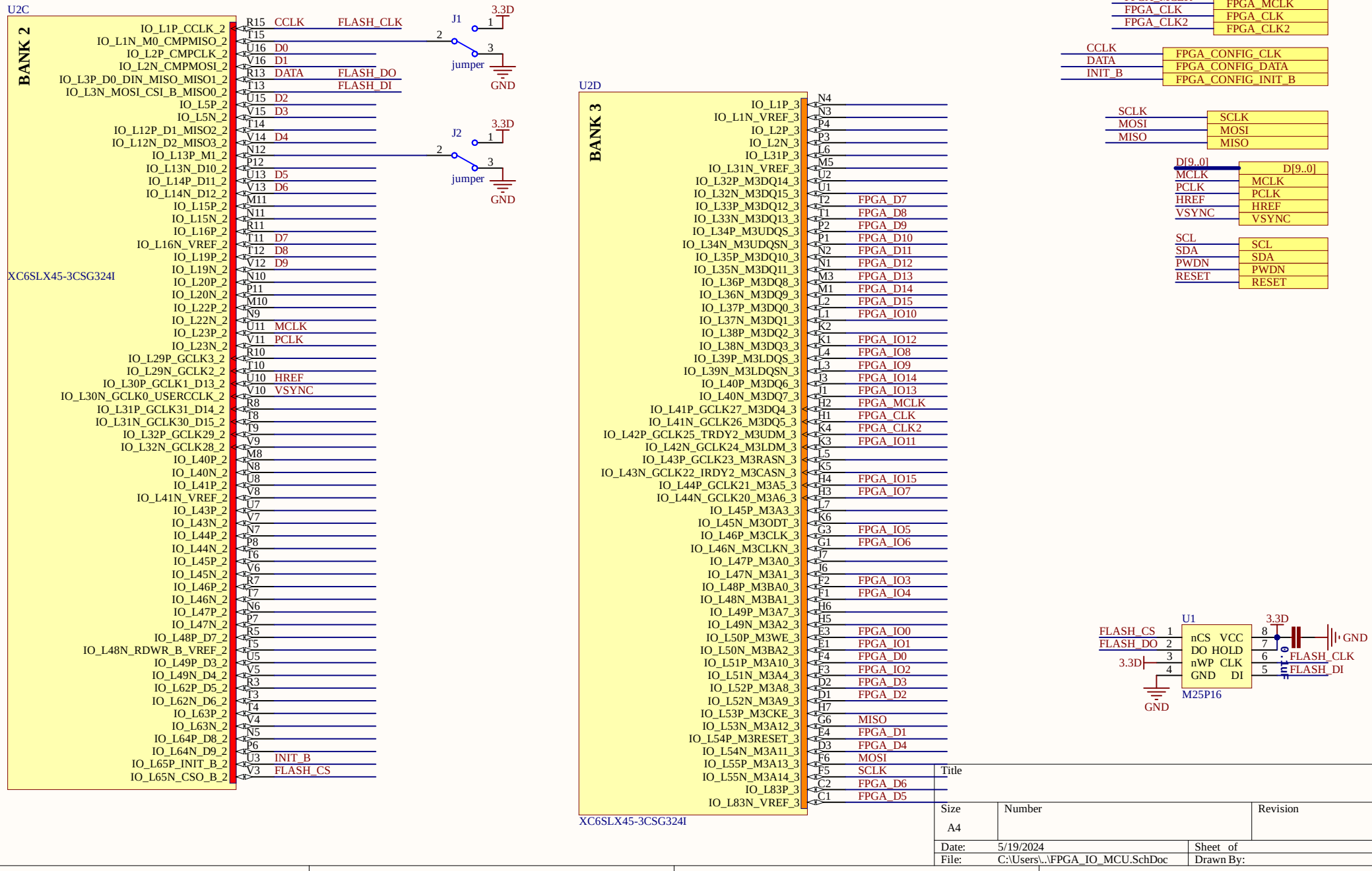
U2C
BANK 2
XC6SLX45-3CSG324I
IO_L1P_CCLK_2 R15 CCLK FLASH_CLK
IO_L1N_M0_CMPMISO_2 T15
IO_L2P_CMPCLK_2 U16 D0
IO_L2N_CMPMOSI_2 V16 D1
IO_L3P_D0_DIN_MISO_MISO1_2 R13 DATA FLASH_DO
IO_L3N_MOSI_CSI_B_MISO0_2 T13 FLASH_DI
IO_L5P_2 U15 D2
IO_L5N_2 V15 D3
IO_L12P_D1_MISO2_2 T14
IO_L12N_D2_MISO3_2 V14 D4
IO_L13P_M1_2 N12
IO_L13N_D10_2 P12
IO_L14P_D11_2 U13 D5
IO_L14N_D12_2 V13 D6
IO_L15P_2 M11
IO_L15N_2 N11
IO_L16P_2 R11
IO_L16N_VREF_2 T11 D7
IO_L19P_2 T12 D8
IO_L19N_2 V12 D9
IO_L20P_2 N10
IO_L20N_2 P11
IO_L22P_2 M10
IO_L22N_2 N9
IO_L23P_2 U11 MCLK
IO_L23N_2 V11 PCLK
IO_L29P_GCLK3_2 R10
IO_L29N_GCLK2_2 T10
IO_L30P_GCLK1_D13_2 U10 HREF
IO_L30N_GCLK0_USERCCLK_2 V10 VSYNC
IO_L31P_GCLK31_D14_2 R8
IO_L31N_GCLK30_D15_2 T8
IO_L32P_GCLK29_2 T9
IO_L32N_GCLK28_2 V9
IO_L40P_2 M8
IO_L40N_2 N8
IO_L41P_2 U8
IO_L41N_VREF_2 V8
IO_L43P_2 U7
IO_L43N_2 V7
IO_L44P_2 N7
IO_L44N_2 P8
IO_L45P_2 T6
IO_L45N_2 V6
IO_L46P_2 R7
IO_L46N_2 T7
IO_L47P_2 N6
IO_L47N_2 P7
IO_L48P_D7_2 R5
IO_L48N_RDWR_B_VREF_2 T5
IO_L49P_D3_2 U5
IO_L49N_D4_2 V5
IO_L62P_D5_2 R3
IO_L62N_D6_2 T3
IO_L63P_2 T4
IO_L63N_2 V4
IO_L64P_D8_2 N5
IO_L64N_D9_2 P6
IO_L65P_INIT_B_2 U3 INIT_B
IO_L65N_CSO_B_2 V3 FLASH_CS
J1
3.3D
1
2
3
jumper
GND
J2
3.3D
1
2
3
jumper
GND
U2D
BANK 3
XC6SLX45-3CSG324I
IO_L1P_3 N4
IO_L1N_VREF_3 N3
IO_L2P_3 P4
IO_L2N_3 P3
IO_L31P_3 L6
IO_L31N_VREF_3 M5
IO_L32P_M3DQ14_3 U2
IO_L32N_M3DQ15_3 U1
IO_L33P_M3DQ12_3 T2 FPGA_D7
IO_L33N_M3DQ13_3 T1 FPGA_D8
IO_L34P_M3UDQS_3 P2 FPGA_D9
IO_L34N_M3UDQSN_3 P1 FPGA_D10
IO_L35P_M3DQ10_3 N2 FPGA_D11
IO_L35N_M3DQ11_3 N1 FPGA_D12
IO_L36P_M3DQ8_3 M3 FPGA_D13
IO_L36N_M3DQ9_3 M1 FPGA_D14
IO_L37P_M3DQ0_3 L2 FPGA_D15
IO_L37N_M3DQ1_3 L1 FPGA_IO10
IO_L38P_M3DQ2_3 K2
IO_L38N_M3DQ3_3 K1 FPGA_IO12
IO_L39P_M3LDQS_3 L4 FPGA_IO8
IO_L39N_M3LDQSN_3 L3 FPGA_IO9
IO_L40P_M3DQ6_3 J3 FPGA_IO14
IO_L40N_M3DQ7_3 J1 FPGA_IO13
IO_L41P_GCLK27_M3DQ4_3 H2 FPGA_MCLK
IO_L41N_GCLK26_M3DQ5_3 H1 FPGA_CLK
IO_L42P_GCLK25_TRDY2_M3UDM_3 K4 FPGA_CLK2
IO_L42N_GCLK24_M3LDM_3 K3 FPGA_IO11
IO_L43P_GCLK23_M3RASN_3 L5
IO_L43N_GCLK22_IRDY2_M3CASN_3 K5
IO_L44P_GCLK21_M3A5_3 H4 FPGA_IO15
IO_L44N_GCLK20_M3A6_3 H3 FPGA_IO7
IO_L45P_M3A3_3 L7
IO_L45N_M3ODT_3 K6
IO_L46P_M3CLK_3 G3 FPGA_IO5
IO_L46N_M3CLKN_3 G1 FPGA_IO6
IO_L47P_M3A0_3 J7
IO_L47N_M3A1_3 J6
IO_L48P_M3BA0_3 F2 FPGA_IO3
IO_L48N_M3BA1_3 F1 FPGA_IO4
IO_L49P_M3A7_3 H6
IO_L49N_M3A2_3 H5
IO_L50P_M3WE_3 E3 FPGA_IO0
IO_L50N_M3BA2_3 E1 FPGA_IO1
IO_L51P_M3A10_3 F4 FPGA_D0
IO_L51N_M3A4_3 F3 FPGA_IO2
IO_L52P_M3A8_3 D2 FPGA_D3
IO_L52N_M3A9_3 D1 FPGA_D2
IO_L53P_M3CKE_3 H7
IO_L53N_M3A12_3 G6 MISO
IO_L54P_M3RESET_3 E4 FPGA_D1
IO_L54N_M3A11_3 D3 FPGA_D4
IO_L55P_M3A13_3 F6 MOSI
IO_L55N_M3A14_3 F5 SCLK
IO_L83P_3 C2 FPGA_D6
IO_L83N_VREF_3 C1 FPGA_D5
FPGA_D[15..0]
FPGA_IO[15..0]
FPGA_MCLK
FPGA_CLK
FPGA_CLK2
FPGA_D[15..0]
FPGA_IO[15..0]
FPGA_MCLK
FPGA_CLK
FPGA_CLK2
CCLK
DATA
INIT_B
FPGA_CONFIG_CLK
FPGA_CONFIG_DATA
FPGA_CONFIG_INIT_B
SCLK
MOSI
MISO
SCLK
MOSI
MISO
D[9..0]
MCLK
PCLK
HREF
VSYNC
D[9..0]
MCLK
PCLK
HREF
VSYNC
SCL
SDA
PWDN
RESET
SCL
SDA
PWDN
RESET
U1
3.3D
FLASH_CS 1
FLASH_DO 2
3.3D 3
4
GND
nCS VCC
DO HOLD
nWP CLK
GND DI
8
7
6
5
0.1uF
GND
FLASH_CLK
FLASH_DI
M25P16
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Revision
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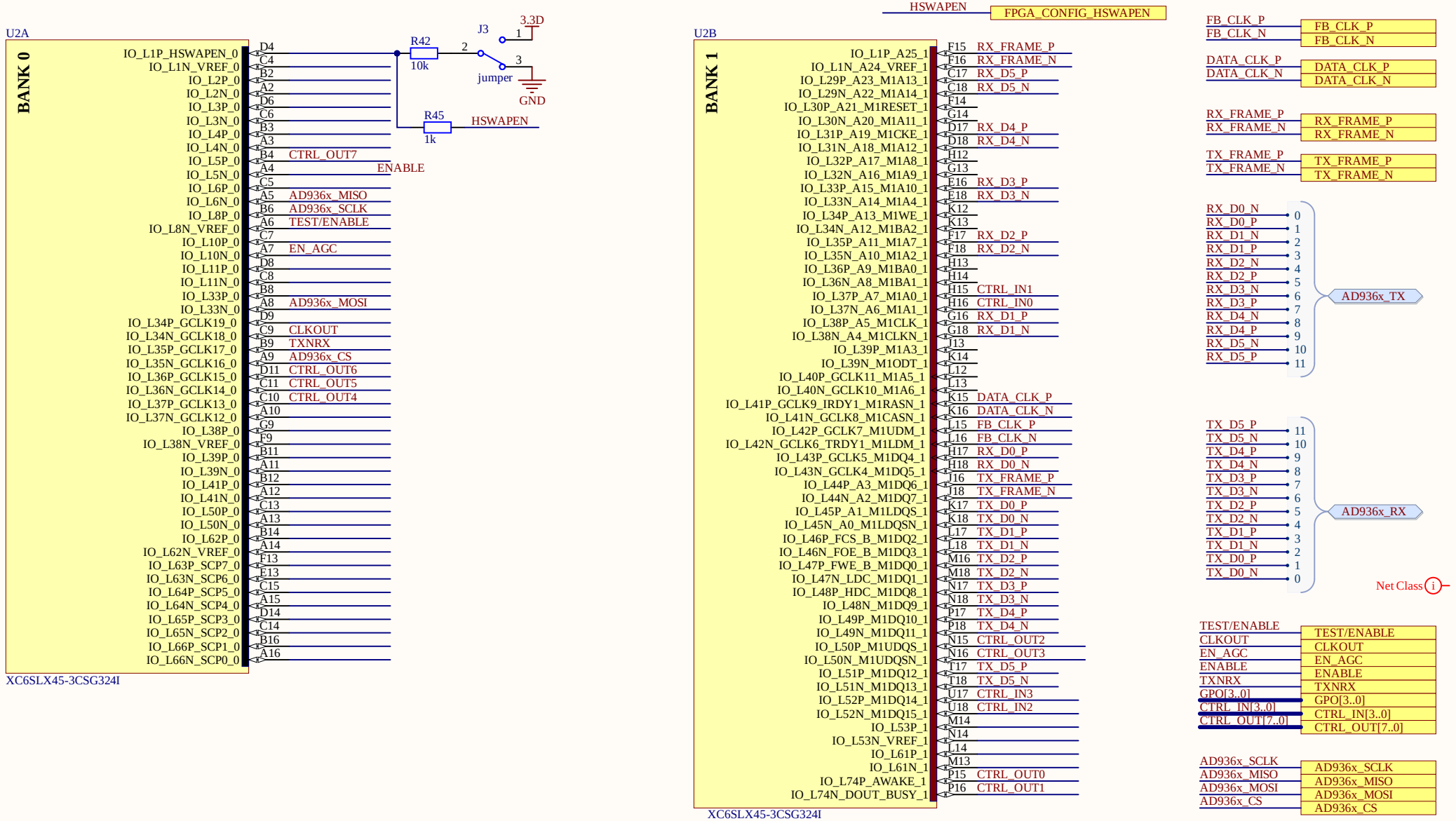
U2A
BANK 0
IO_L1P_HSWAPEN_0
IO_L1N_VREF_0
IO_L2P_0
IO_L2N_0
IO_L3P_0
IO_L3N_0
IO_L4P_0
IO_L4N_0
IO_L5P_0
IO_L5N_0
IO_L6P_0
IO_L6N_0
IO_L8P_0
IO_L8N_VREF_0
IO_L10P_0
IO_L10N_0
IO_L11P_0
IO_L11N_0
IO_L33P_0
IO_L33N_0
IO_L34P_GCLK19_0
IO_L34N_GCLK18_0
IO_L35P_GCLK17_0
IO_L35N_GCLK16_0
IO_L36P_GCLK15_0
IO_L36N_GCLK14_0
IO_L37P_GCLK13_0
IO_L37N_GCLK12_0
IO_L38P_0
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IO_L41N_0
IO_L50P_0
IO_L50N_0
IO_L62P_0
IO_L62N_VREF_0
IO_L63P_SCP7_0
IO_L63N_SCP6_0
IO_L64P_SCP5_0
IO_L64N_SCP4_0
IO_L65P_SCP3_0
IO_L65N_SCP2_0
IO_L66P_SCP1_0
IO_L66N_SCP0_0
D4
C4
B2
A2
D6
C6
B3
A3
B4
A4
C5
A5
B6
A6
C7
A7
D8
C8
B8
A8
D9
C9
B9
A9
D11
C11
C10
A10
G9
F9
B11
A11
B12
A12
C13
A13
B14
A14
F13
E13
C15
A15
D14
C14
B16
A16
CTRL_OUT7
ENABLE
AD936x_MISO
AD936x_SCLK
TEST/ENABLE
EN_AGC
AD936x_MOSI
CLKOUT
TXNRX
AD936x_CS
CTRL_OUT6
CTRL_OUT5
CTRL_OUT4
XC6SLX45-3CSG324I
R42
10k
R45
1k
J3
1
2
3
jumper
3.3D
GND
HSWAPEN
HSWAPEN
FPGA_CONFIG_HSWAPEN
U2B
BANK 1
IO_L1P_A25_1
IO_L1N_A24_VREF_1
IO_L29P_A23_M1A13_1
IO_L29N_A22_M1A14_1
IO_L30P_A21_M1RESET_1
IO_L30N_A20_M1A11_1
IO_L31P_A19_M1CKE_1
IO_L31N_A18_M1A12_1
IO_L32P_A17_M1A8_1
IO_L32N_A16_M1A9_1
IO_L33P_A15_M1A10_1
IO_L33N_A14_M1A4_1
IO_L34P_A13_M1WE_1
IO_L34N_A12_M1BA2_1
IO_L35P_A11_M1A7_1
IO_L35N_A10_M1A2_1
IO_L36P_A9_M1BA0_1
IO_L36N_A8_M1BA1_1
IO_L37P_A7_M1A0_1
IO_L37N_A6_M1A1_1
IO_L38P_A5_M1CLK_1
IO_L38N_A4_M1CLKN_1
IO_L39P_M1A3_1
IO_L39N_M1ODT_1
IO_L40P_GCLK11_M1A5_1
IO_L40N_GCLK10_M1A6_1
IO_L41P_GCLK9_IRDY1_M1RASN_1
IO_L41N_GCLK8_M1CASN_1
IO_L42P_GCLK7_M1UDM_1
IO_L42N_GCLK6_TRDY1_M1LDM_1
IO_L43P_GCLK5_M1DQ4_1
IO_L43N_GCLK4_M1DQ5_1
IO_L44P_A3_M1DQ6_1
IO_L44N_A2_M1DQ7_1
IO_L45P_A1_M1LDQS_1
IO_L45N_A0_M1LDQSN_1
IO_L46P_FCS_B_M1DQ2_1
IO_L46N_FOE_B_M1DQ3_1
IO_L47P_FWE_B_M1DQ0_1
IO_L47N_LDC_M1DQ1_1
IO_L48P_HDC_M1DQ8_1
IO_L48N_M1DQ9_1
IO_L49P_M1DQ10_1
IO_L49N_M1DQ11_1
IO_L50P_M1UDQS_1
IO_L50N_M1UDQSN_1
IO_L51P_M1DQ12_1
IO_L51N_M1DQ13_1
IO_L52P_M1DQ14_1
IO_L52N_M1DQ15_1
IO_L53P_1
IO_L53N_VREF_1
IO_L61P_1
IO_L61N_1
IO_L74P_AWAKE_1
IO_L74N_DOUT_BUSY_1
F15
F16
C17
C18
F14
G14
D17
D18
H12
G13
E16
E18
K12
K13
F17
F18
H13
H14
H15
H16
G16
G18
J13
K14
L12
L13
K15
K16
L15
L16
H17
H18
J16
J18
K17
K18
L17
L18
M16
M18
N17
N18
P17
P18
N15
N16
T17
T18
U17
U18
M14
N14
L14
M13
P15
P16
RX_FRAME_P
RX_FRAME_N
RX_D5_P
RX_D5_N
RX_D4_P
RX_D4_N
RX_D3_P
RX_D3_N
RX_D2_P
RX_D2_N
CTRL_IN1
CTRL_IN0
RX_D1_P
RX_D1_N
DATA_CLK_P
DATA_CLK_N
FB_CLK_P
FB_CLK_N
RX_D0_P
RX_D0_N
TX_FRAME_P
TX_FRAME_N
TX_D5_P
TX_D5_N
TX_D4_P
TX_D4_N
TX_D3_P
TX_D3_N
TX_D2_P
TX_D2_N
TX_D1_P
TX_D1_N
TX_D0_P
TX_D0_N
CTRL_OUT2
CTRL_OUT3
CTRL_OUT0
CTRL_OUT1
XC6SLX45-3CSG324I
FB_CLK_P
FB_CLK_N
DATA_CLK_P
DATA_CLK_N
RX_FRAME_P
RX_FRAME_N
TX_FRAME_P
TX_FRAME_N
RX_D0_N
RX_D0_P
RX_D1_N
RX_D1_P
RX_D2_N
RX_D2_P
RX_D3_N
RX_D3_P
RX_D4_N
RX_D4_P
RX_D5_N
RX_D5_P
0
1
2
3
4
5
6
7
8
9
10
11
AD936x_TX
TX_D5_P
TX_D5_N
TX_D4_P
TX_D4_N
TX_D3_P
TX_D3_N
TX_D2_P
TX_D2_N
TX_D1_P
TX_D1_N
TX_D0_P
TX_D0_N
AD936x_RX
Net Class
TEST/ENABLE
CLKOUT
EN_AGC
ENABLE
TXNRX
GPO[3..0]
CTRL_IN[3..0]
CTRL_OUT[7..0]
AD936x_SCLK
AD936x_MISO
AD936x_MOSI
AD936x_CS
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Number
Revision
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5/19/2024
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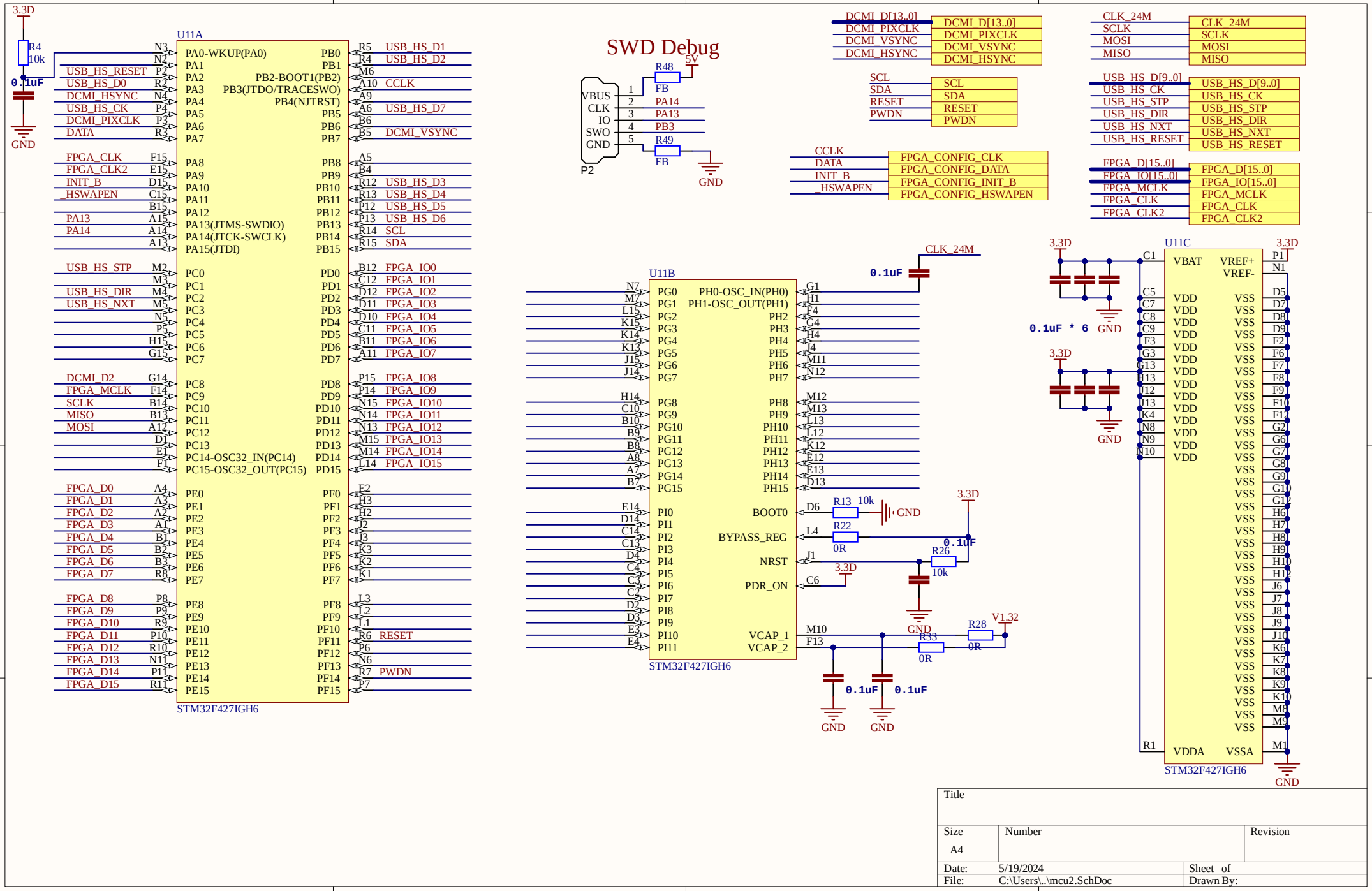

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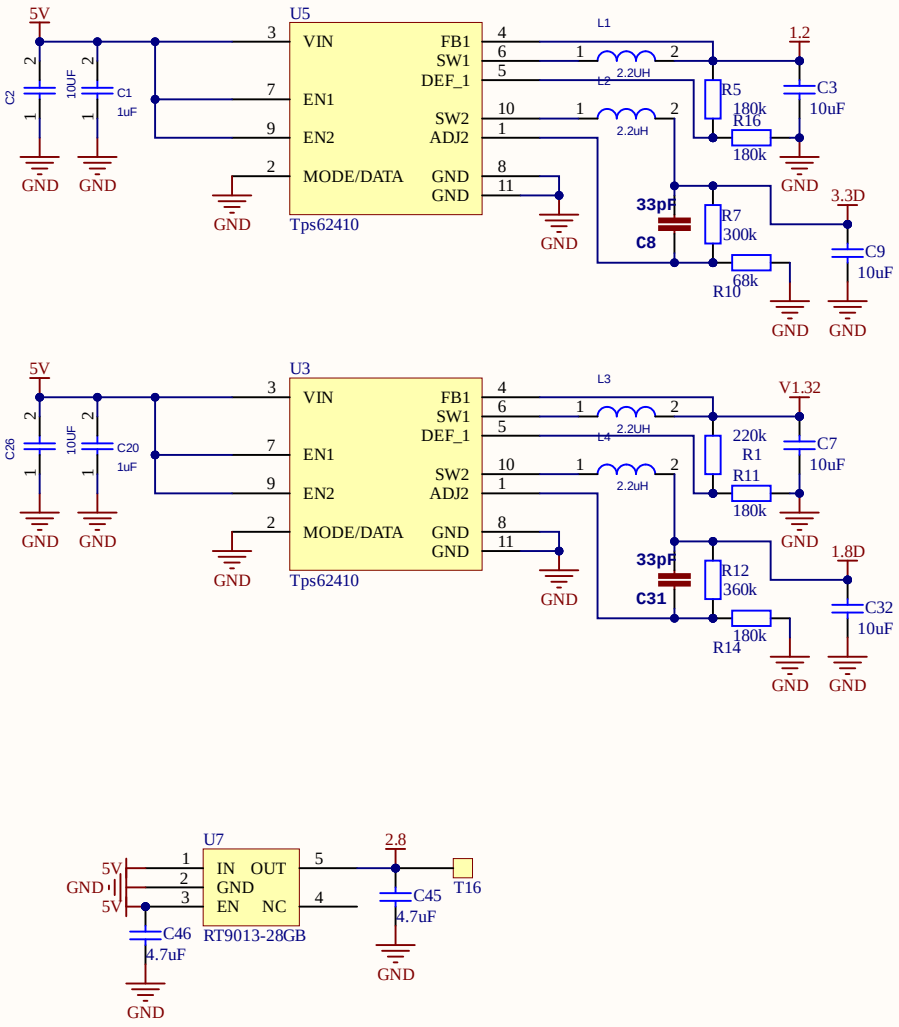
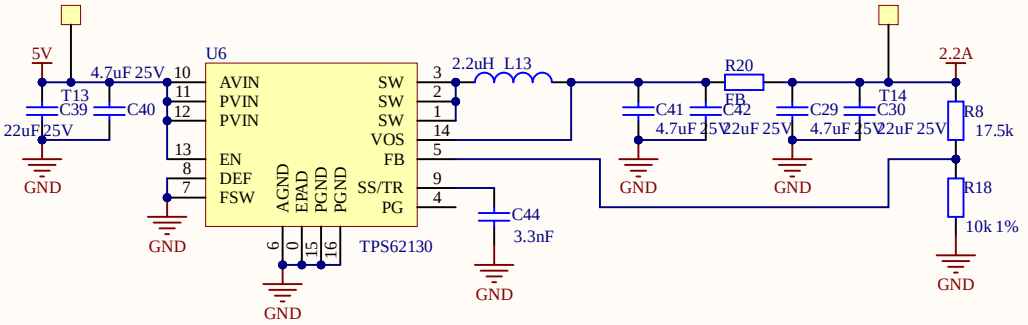
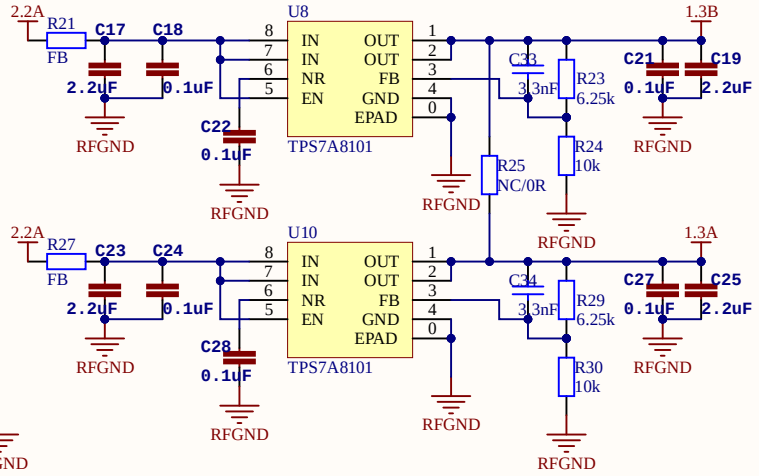
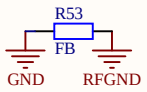




these two 1.3V are for AD9363, which has its own decoupling





power return path

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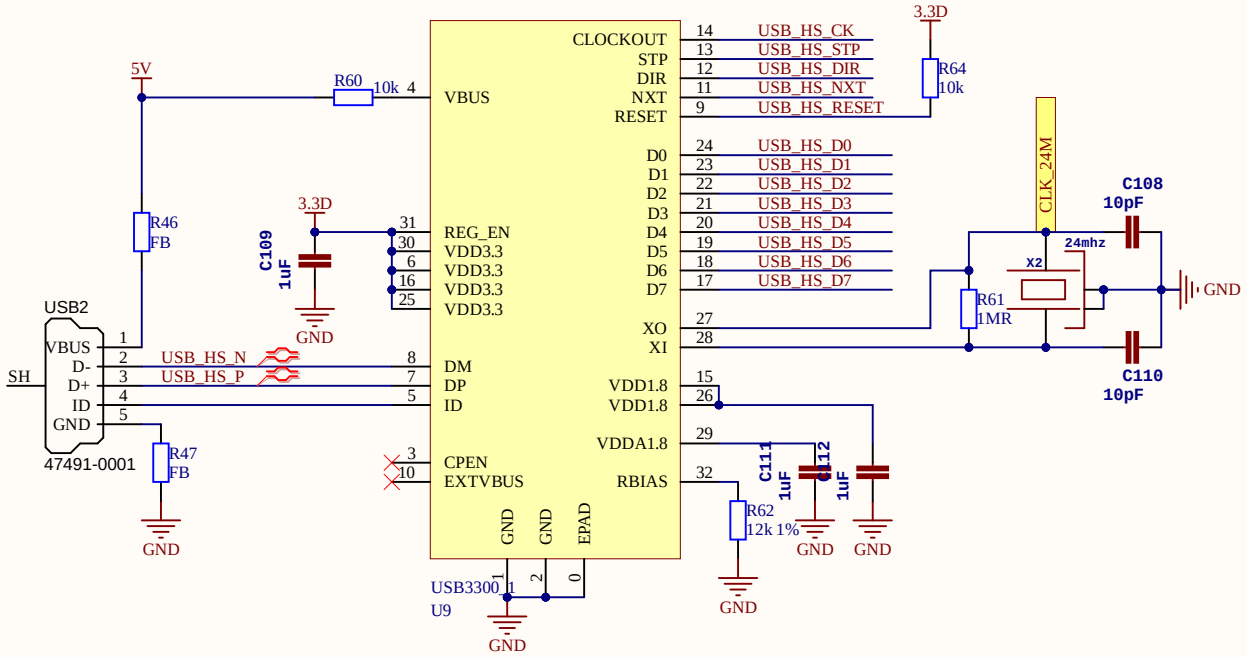

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