12V/3A Switching Li+Battery Charger and 5V/1A OTG with I²C Control

DESCRIPTION

The ETA6937 is a new generation of highly integrated synchronous switch-mode charger, featuring integrated FETs and small external components, targeted at extremely space-limited portable applications powered by 1-cell Li-Ion or Li-polymer battery pack. Unlike previous generation of charging ICs (BQ2415X and FAN54015 etc.) that can barely deliver charge current up to 1.5A, thanks to ETA's proprietary technology, ETA6937 packs a powerful punch and can delivery up to 3A of charge current, while still maintaining a small footprint of 2mmx1.6mm. ETA6937 has bi-directional operation to achieve boost function for USB OTG support. The ETA6937 have three operation modes: charge mode, boost mode, and high impedance mode. In charge mode, the IC supports a precision Li-ion or Li-polymer charging system for single-cell applications. In boost mode, the IC boosts the battery voltage to VBUS for powering attached OTG devices. In high impedance mode, the IC stops charging or boosting and operates in a mode with very low current from VBUS or battery, to effectively reduce the power consumption when the portable device is in standby mode. Through I2C communication with a host, referred to as "HOST" control/mode, the IC achieves smooth transition among the different operation modes. Even when no I2C communication is available, the IC starts in default mode. During default mode operation, the charger will still charge the battery but using each register's default values.

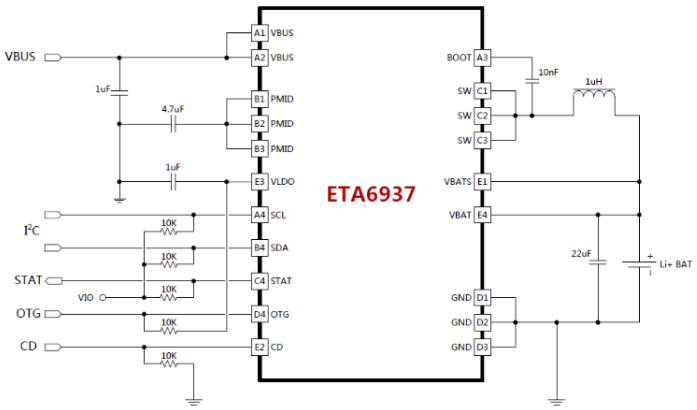
FEATURES

- Up to 3A Max charging current Switching Charger
- 93% Charging Efficiency at 5V input 2A CC current
- 12V Input operating voltage
- 20V Maximum Input standoff voltage
- No External Sense resistor
- Integrate linear charger for accurate Iterm control
- Input DPPM
- Input current limiting
- Bad Adaptor detection
- No-Battery detection
- Safety limit register for Vcharge and Icharge limits
- Programmable charging parameters through I2C
- Status Output for charging and faults
- 5V OTG boost mode up to 1A output current
- Input OVP
- Reverse leakage protection for Battery
- Boost output current limiting

APPLICATIONS

- Smart Phone
- Tablet, MID
- Power Bank

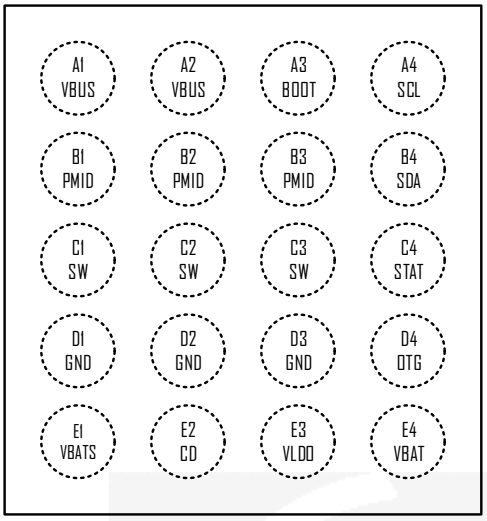
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA6937CSU	CSP-20	6937 YWWL	3000

PIN CONFIGURATION



ABSOLUTEMAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VBUS, PMID, STAT Voltage .....–0.3V to 20V
SW Voltage. . .....–0.3V to 20V
BOOT to SW Voltage .....–0.3V to 6V
All Other Pin to PGND Voltage .....–0.3V to 6V
SW, VBUS, VBAT, VBATS to PGND current .....Internally limited
Operating Temperature Range .....–40℃ to 85℃
Storage Temperature Range.....–55℃ to 150℃
Thermal Resistance θ_{JA}
CSP2.0X1.6-20 .....35 .....℃/W
Lead Temperature (Soldering,10ssec) .....260℃
ESD HBM (Human Body Mode) 2KV
ESD MM (Machine Mode) 200V

ELECTRICAL CHACRACTERISTICS

PARAMETERS		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
$I_{(VBUS)}$	VBUS supply current control	$V_{BUS} > V_{BUS\_MIN}$, PWM switching		10		mA
		$V_{BUS} > V_{BUS\_MIN}$, PWM NOT switching			5	mA
		0℃ < T_J<85℃, CD = 1 or HZ_MODE = 1		25		μA
I_{LK}	Leakage current from battery to VBUS pin	0℃ < T_J< 85℃, V_{BAT} = 4.2V, High Impedance mode, V_{BUS}=0V			5	μA
	Battery discharge current in High Impedance mode	0℃ < T_J< 85℃, V_{BAT} = 4.2 V, High Impedance mode, SCL, SDA, OTG = 0 V or 1.8 V		28		μA
VOLTAGE REGULATION						
$V_{(OREG)}$	Output regulation voltage programmable range	Operating in voltage regulation, programmable	3.5		4.44	V
	Voltage regulation accuracy	T_J = 25℃	4.179	4.2	4.221	V
		T_J = -10℃~50℃	4.158	4.2	4.242	V
CURRENT REGULATION (FAST CHARGE)						
$I_{(OCHARGE)}$	Output charge current programmable range		550		3050	mA
	Low charge current (default after POR in 30 min mode)	$V_{SHORT} \le V_{BAT} < V_{OREG}$, $V_{BUS} > V_{SLP}$		550		mA
	Regulation accuracy of the charge current	$I_{OCHARGE}$ = 1350mA	-10		+10	%
WEAK BATTERY DETECTION						
$V_{(LOWV)}$	Weak battery voltage threshold programmable range	Adjustable using I^2C control	3.4		3.7	V
	Weak battery voltage accuracy	Battery voltage rising	-5		+5	%
	Hysteresis for V_{LOWV}	Battery voltage falling		300		mV
	Deglitch time for weak battery threshold	Rising voltage, 2mV over drive, t_{RISE}=100ns		30		ms

PARAMETERS		TEST CONDITION	MIN	TYP	MAX	UNIT
LOGIC INPUT THRESHOLD (CD, OTG)						
V_{IL}	Input low threshold level	Falling			0.4	
V_{IH}	Input high threshold level	Rising	1.2			
$I_{(BIAS)}$	Input bias current	Voltage on control pin is 5V			1	μA
CHARGE TERMINATION DETECTION						
$I_{(TERM)}$	Termination charge current programmable range	$V_{BAT} > V_{OREG}-V_{RECH}$, $V_{BUS} > V_{SLP}$, Programmable	50		400	mA
	Deglitch time for charge termination	Both rising and falling, 2mV overdrive, t_{RISE}, t_{FALL}= 100ns		30		ms
	Regulation accuracy for termination current	ITERM[2:0] =011	150		240	mA
BAD ADAPTOR DETECTION						
$VIN_{(MIN)}$	Input voltage lower limit	BAD ADAPTOR DETECTION		3.8		V
	Hysteresis for V_{IN_MIN}	Input Voltage Rising		150		mV
	Deglitch time for VBUS rising above V_{IN_MIN}	Rising voltage, 2-mV overdrive, t_{RISE}=100ns		30		ms
$I_{(DETECT)}$	Detect current to PGND	During bad adaptor detection		30		mA
T_{INT}	Detection Interval	Input power source detection		2		S
INPUT BASED DYNAMIC POWER MANAGEMENT						
V_{IN_DPM}	Input Voltage DPM threshold programmable range		4.2		14.36	V
	V_{INDPM} threshold accuracy			4.52		V
INPUT CURRENT LIMITING						
I_{IN_LIMIT}	Input current limiting threshold range	Programmable, unless no limit option	100		5000	mA
VLDO REGULATOR						
V_{LDO}	Internal bias regulator voltage	V_{PMID}> 5.1V, I_{VLDO} = 1mA, C_{LDO}=1μF		4.9		V
	V_{LDO} output short current limit	V_{VLDO} = 90% regulation		50		mA
BATTERY RECHARGE THRESHOLD						
$V_{(RECH)}$	Recharge threshold voltage	Below V_{OREG}		120		mV
	Deglitch time	V_{BAT} decreasing below threshold, t_{FALL}=100ns, 10-mV overdrive		30		ms
STAT OUTPUTS						
$V_{OL(STAT)}$	Low-level output saturation voltage, STAT pin	I_{STAT} = 10mA, sink current			0.55	V
	High-level leakage current for STAT	V_{STAT} = 16V			1	μA
I²C BUS LOGIC LEVELS AND TIMING CHARACTERISTICS						
V_{OL}	Output low threshold level	I_O= 10mA, sink current			0.4	V
V_{IL}	Input low threshold level	V_{PULL_UP}=1.8V, SDA and SCL			0.4	V
V_{IH}	Input high threshold level	V(pull-up)=1.8V,SDA and SCL	1.2			V
$I_{(BIAS)}$	Input bias current	V(pull-up)=1.8V,SDA and SCL			1	μA
$F_{(SCL)}$	SCL clock frequency				3.4	Mhz
BATTERY DETECTION						
$I_{(DETECT)}$	Battery detection current before charge done, (sink current)	Begins after termination detected, $V_{BAT} \leq V_{OREG}$		-0.5		mA

PARAMETERS		TEST CONDITION	MIN	TYP	MAX	UNIT
	Battery detection time			262		ms
SLEEP COMPARATOR						
$V_{(SLP)}$	Sleep-mode entry threshold, V_{BUS} - V_{BAT}	2.3V ≤ V_{BAT} ≤ V_{OREG}, V_{BUS} falling		60		mV
$V_{(SLP\_EXIT)}$	Sleep-mode exit hysteresis	2.3V ≤ V_{BAT} ≤ V_{OREG}		200		mV
	Deglitch time for VBUS rising above V_{SLP}+V_{SLP_EXIT}	Rising voltage, 2-mV overdrive, t_{RISE}=100ns		30		ms
UNDER VOLTAGE LOCKOUT (UVLO)						
UVLO	IC active threshold voltage	VBUS rising - Exits UVLO		3.30		V
$UVLO_{(HYS}$	IC active hysteresis	VBUS falling below UVLO – Enters UVLO		150		mV
PWM						
	Voltage from BOOT pin to SW pin	During charge or boost operation		4		V
	Internal top reverse blocking MOSFET on-resistance	IIN_LIMIT = 500mA, Measured from VBUS to PMID		55		mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMID to SW, V_{BOOT}–V_{SW} = 4V		60		mΩ
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		40		mΩ
$F_{(OSC)}$	Oscillator frequency, programmable	Boost Mode		1300		kHz
	Maximum duty cycle	Buck Mode		99		%
CHARGE MODE PROTECTION						
V_{OVP_VBUS}	Input OVP threshold voltage	VBUS threshold to turn off converter during charge		16.0		V
	OVP threshold hysteresis	VBUS falling		1		V
V_{OVP}	Output OVP threshold voltage	VBAT threshold over V_{OREG} to turn off charger during charge		117		$\%V_{OREG}$
	V_{BAT_OVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BAT_OVP}		11		$\%V_{OREG}$
V_{SHORT}	Trickle to fast charge threshold	V_{BAT} rising, Typical application		2.1		V
	V_{SHORT} hysteresis	V_{BAT} falling below V_{SHORT}, typical application		100		mV
I_{SHORT}	Trickle charge charging current	V_{BAT} ≤ V_{SHORT}		50		mA
BOOST MODE OPERATION FOR VBUS (OPA_MODE=1,HZ_MODE=0)						
V_{BUS_B}	Boost output voltage (to VBUS pin)	2.5V < VBAT<4.5V		5.05		V
	Boost output voltage accuracy	Including line and load regulation	-3		3	%
I_{BILIM}	Output current limit for boost	3V < V_{BUS}, 2.5V < V_{BAT}< 4.5V, TJ=0℃–125℃		1200		mA
		3V > V_{BUS_B}, 2.5V < V_{BAT}< 4.5V, TJ=0℃–125℃		500		mA
V_{BUSOVP}	Overvoltage protection threshold for boost (VBUS pin)	Threshold over VBUS to turn off converter during boost		6.00		V
	V_{BUSOVP} hysteresis	VBUS falling from above V_{BUSOVP}		200		mV
V_{BATMAX}	Maximum battery voltage for boost (VBAT pin)	V_{BAT} rising edge during boost		4.90		V
	V_{BATMAX} hysteresis	V_{BAT} falling from above V_{BATMAX}		200		mV
V_{BATMIN}	Minimum battery voltage for boost (VBAT pin)	During boosting		2.5		V
	V_{BATMIN} hysteresis	Before boost starts		2.9		V
PROTECTION						
$T_{SHTDOWN}$	Thermal trip			165		℃

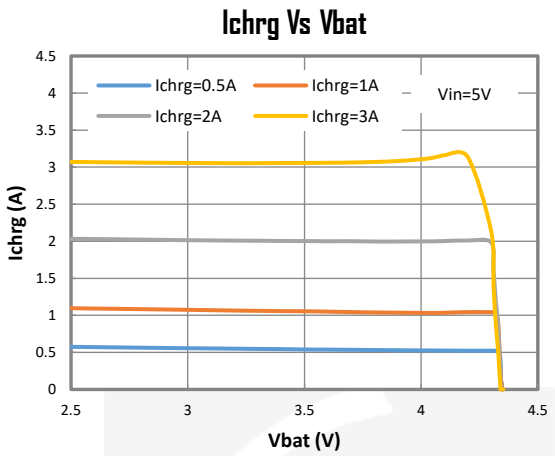
PARAMETERS		TEST CONDITION	MIN	TYP	MAX	UNIT
	Thermal hysteresis			30		°C
T_{OF}	Thermal regulation threshold	Charge current begins to reduce		120		°C
	32 second watchdog (WD) timer	32 Second or HOST mode		32		s
	30 minute safety timer			30		Min

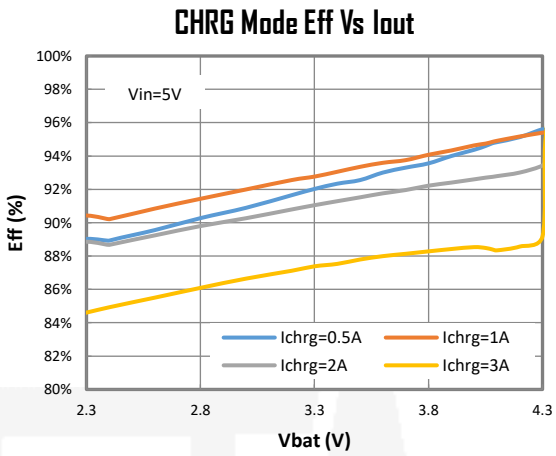
PIN DESCRIPTION

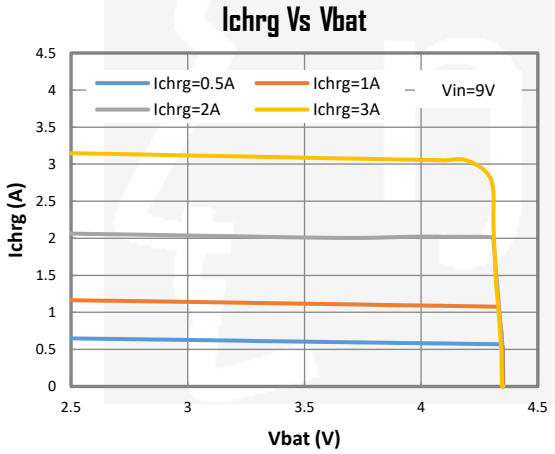
PIN #	NAME	DESCRIPTION
A1, A2	VBUS	Charger input voltage. Bypass it with a 1μF ceramic capacitor from VBUS to PGND. It also provides power to the load during boost mode.
A3	BOOT	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10nF ceramic capacitor (voltage rating ≥ 10 V) from BOOT pin to SW pin.
A4	SCL	I^2C interface clock. Connect a 10kΩ pull up resistor to 1.8V rail.
B1, B2, B3	PMID	Connection point between reverse blocking FET and high-side switching FET. Bypass it with a minimum of 4.7μF capacitor from PMID to PGND.
B4	SDA	I^2C interface data. Connect a 10kΩ pull up resistor to 1.8V rail.
C1, C2, C3	SW	Internal switch to output inductor connection.
C4	STAT	Charge status pin. Pull low when charge in progress. Open drain for other conditions. During faults, a 128μs pulse is sent out. STAT pin can be disabled by the EN_STAT bit in control register. STAT can be used to drive a LED or communicate with a host processor.
D1, D2, D3	PGND	Power Ground
D4	OTG	Boost mode enable control or input current limiting selection pin. When OTG is in active status, is forced to operate in boost mode. It has higher priority over I2C control and can be disabled using the control register. At POR while in 15-min mode, the OTG pin is default to be used as the input current limiting selection pin. The I^2C register is ignored at startup. When OTG=High, IIN_LIMIT=500mA and when OTG=Low, IIN_LIMIT=100mA.
E1	VBATS	VBATS pin is always shorted to VBAT pin.
E2	CD	Charge disable control pin. CD=0, charge is enabled. CD=1, charge is disabled and VBUS pin is high impedance to GND.
E3	VLDO	LDO Output Voltage. Bypass it with 1μF capacitor from VLDO to PGND.
E4	VBAT	Positive battery terminal

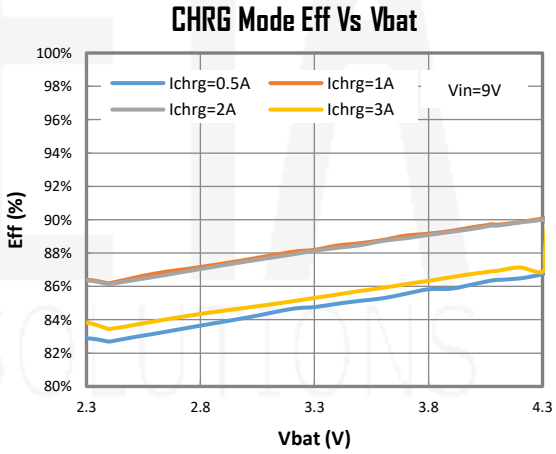
TYPICAL CHARACTERISTICS

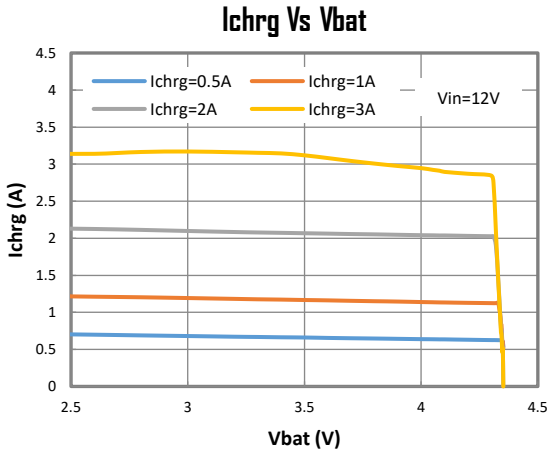
(Typical values are at T_A = 25°C unless otherwise specified.)

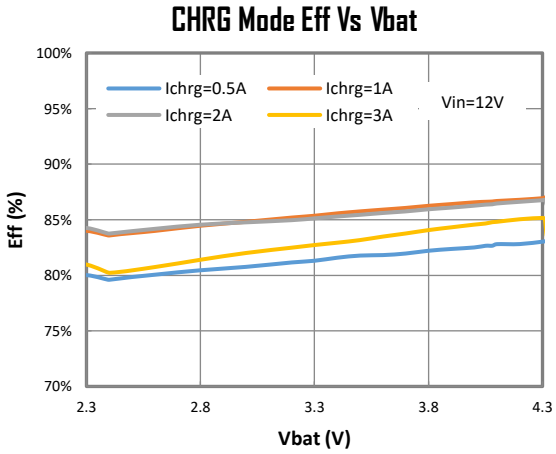


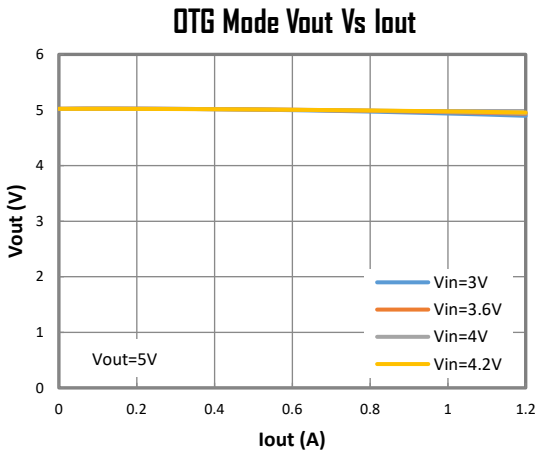


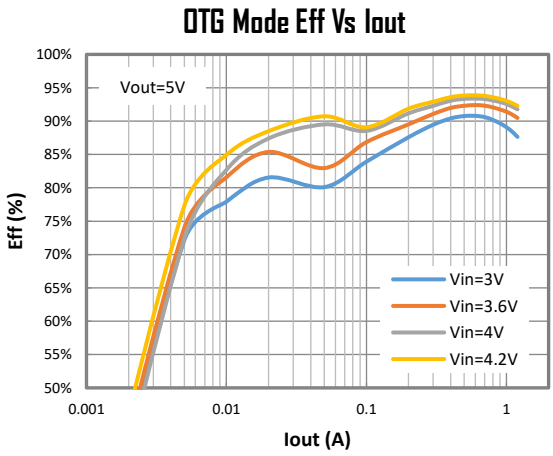


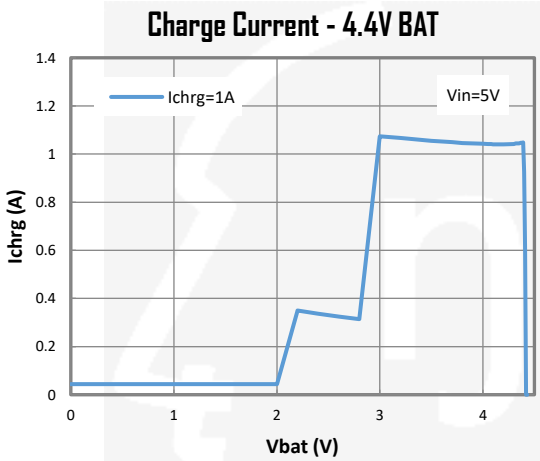


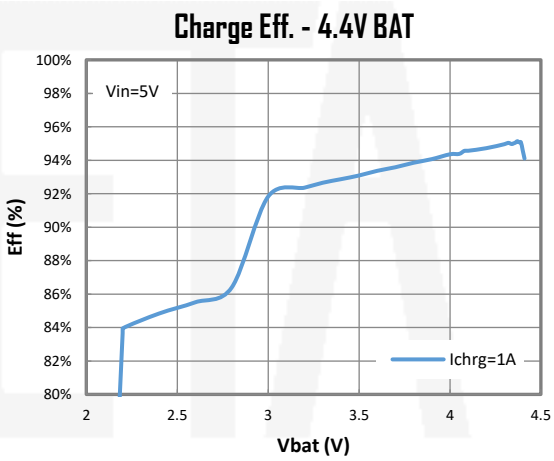





OTG Mode Vout Vs Iout
Vout (V)
Iout (A)
Vout=5V
Vin=3V
Vin=3.6V
Vin=4V
Vin=4.2V


OTG Mode Eff Vs Iout
Eff (%)
Iout (A)
Vout=5V
Vin=3V
Vin=3.6V
Vin=4V
Vin=4.2V


Charge Current - 4.4V BAT
Ichrg (A)
Vbat (V)
Ichrg=1A
Vin=5V


Charge Eff. - 4.4V BAT
Eff (%)
Vbat (V)
Vin=5V
Ichrg=1A

REGISTER MAP

DEVICE ADDRESS: D4H (11010100)

Status/Control Register (Read/Write)
Memory Location: 00, Reset State: x1xx 0xxx

BIT	NAME	RESET	TYPE	FUNCTION
7	TMR_RST OTG_STAT	0	RD/WR	Write: TMR_SRT Function ⇨ Write '1' to reset the safety timer (auto clear) ⇨ Write '0' to do nothing Read: OTG pin status ⇨ '0' - OTG pin at low level ⇨ '1' - OTG pin at high level
6	EN_STAT	1	RD/WR	STAT Pin function Enable: ⇨ '0' - Disable STAT pin Function ⇨ '1' – Enable STAT pin function (default 1)
5	STAT2	0	Read Only	Charging Status Bits: ⇨ '00' - Ready ⇨ '01' - Charge in Progress ⇨ '10' - Charge Done ⇨ '11' - Fault
4	STAT1	0	Read Only	
3	BOOST	0	Read Only	Boost Mode Status Bits: ⇨ '1' - Boost mode ⇨ '0' – Not in boost mode
2 1 0	FAULT<2:0>	000	Read Only	Fault Indication Flags: CHARGE MODE / DISCHARGE MODE ⇨ '000' NORMAL / NORMAL ⇨ '001' VBUS_OVP / VBUS_OVP ⇨ '010' SLEEP_MODE / OVER_LOAD ⇨ '011' BAD_ADAPTER Or VBUS_UVLO / VBAT_UVLO ⇨ '100' VBAT_OVP / VBAT_OVP ⇨ '101' THERMAL_SD / THERMAL_SD ⇨ '110' TIMER_FAULT / TIMER_FAULT ⇨ '111' NA / NA

Control Register (Read/Write)
Memory Location: 01, Reset State: 0011 0000

BIT	NAME	RESET	TYPE	FUNCTION
7 6	IIN_LIMIT_1<1:0>	00	RD/WR	VBUS Input Current Limit. Active when EN_ILIM2 = '0': ⇨ '00' - 100mA ⇨ '01' - 500mA ⇨ '10' - 800mA ⇨ '11' - No Input Current Limit
5 4	VLOWV<1:0>	11	RD/WR	Weak Battery Voltage Level: ⇨ '00' - 3.4V ⇨ '01' - 3.5V ⇨ '10' - 3.6V ⇨ '11' - 3.7V (Default)
3	TE	0	RD/WR	Termination Charge Current Enable ⇨ '0' – Disable ⇨ '1' – Enable (default)

2	nCE	0	RD/WR	Charge Disable: ⇨ '0' – Enable (default) ⇨ '1' – Disable
1	HZ_MODE	0	RD/WR	High Impedance Mode Command: ⇨ '0' - Not in HiZ Mode (default) ⇨ '1' - HiZ Mode
0	OPA_MODE	0	RD/WR	Operation Mode Select: ⇨ '0' - Charge Mode (default) ⇨ '1' - Boost Mode

Control/Battery Voltage Register (Read/Write)
Memory Location: 02, Reset State: 0000 1010

BIT	NAME	RESET	TYPE	FUNCTION
7	VOREG<5:0>	000110	RD/WR	Battery Regulation Voltage Configuration.
6				
5				
4				
3				
2				
1	OTG_PL	1	RD/WR	OTG Pin Polary Setting: ⇨ '0' - BOOST Enable when OTG = Logic_LO ⇨ '1' - BOOST Enable when OTG = Logic_HI (default)
0	OTG_EN	0	RD/WR	OTG Pin Control Enable: ⇨ '0' - Disable OTG pin Function (default) ⇨ '1' - Enable OTG pin Function

Vender/Part/Revision Register (Read only)
Memory Location: 03, Reset State: 0101 000x

BIT	NAME	RESET	TYPE	FUNCTION
7	VENDER<2:0>	010	Read Only	Vender Code
6				
5				
4	PN<1:0>	10	Read Only	Part Number Code
3				
2	REVISION<2:0>	001	Read Only	Revision Code
1				
0				

Battery Termination/Fast Charge Current Register (Read/Write)
Memory Location: 04, Reset State: 0000 0001

BIT	NAME	RESET	TYPE	FUNCTION
7	RESET	0	RD/WR	Charger Reset. (No function in BOOST Mode) ⇨ Write '0' - No effect ⇨ Write '1' - Reset Charge Mode
6 5 4	ICHG<2:0>	000	RD/WR	Charge Current Setting Bits: ⇨ LSB = 100mA; ⇨ MSB=400mA
3	ICHRG_OFFSET	0	RD/WR	Min Charge Current Level: ⇨ 0 - 550mA ⇨ 1 – 650mA
2 1 0	ITERM<2:0>	001	RD/WR	Termination Current Setting Bits: ⇨ LSB= 50mA ⇨ MSB = 200mA

Special Charger Voltage/Enable Pin Status Register
Memory location: 05, Reset state: 001X X100

BIT	NAME	RESET	TYPE	FUNCTION
7	ICHG<4>	0	RD/WR	Extra Added Charge Current Setting Bit: ⇨ 0 – Add more 0mA ⇨ 1 – Add more 1600mA
6	ICHG<3>	0	RD/WR	Extra Added Charge Current Setting Bit: ⇨ 0 – Add more 0mA ⇨ 1 – Add more 800mA
5	LOW_CHG	0	RD/WR	Force Low Charge Current: ⇨ '0' - Configured by ICHG<4:0> ⇨ '1' - Force 550mA
4	DPM_STATUS	0	Read Only	DPM Status: ⇨ '0' - DPM_Mode is Not Active ⇨ '1' - DPM_Mode is Active
3	CD_STATUS	0	Read Only	CD Pin Status: ⇨ '0' - CD pin is at Logic_LO ⇨ '1' - CD pin is at Logic_HI
2 1 0	VINDPM<2:0>	100	RD/WR	Special Charger Voltage: ⇨ MSB = 320mV step ⇨ LSB = 80mV step

Safety Limit Register (READ/WRITE, Write only once after reset!)
Memory location: 06, Reset state: 01000000

BIT	NAME	RESET	TYPE	FUNCTION
7	IMCHRG<3:0>	0100	RD/WR	Maximum Charge Current: ⇨ Battery Charge Current is set by ICHG<4:0> or IMCHRG<3:0> which is lower.
6				
5				
4				
3	VMREG<3:0>	0000	RD/WR	Maximum Battery Regulation Voltage: ⇨ Battery Regulation voltage is set by VMREG<3:0> or VOREG<5:0> which is lower.
2				
1				
0				

Extra Current Limit and DPM level setting(READ/WRITE)
Memory location: 07, Reset state: 00000000

BIT	NAME	RESET	TYPE	FUNCTION
7	VINDPM<6:3>	0000	RD/WR	Special Charger Voltage Addition: 5.12V
6				Special Charger Voltage Addition: 2.56V
5				Special Charger Voltage Addition: 1.28V
4				Special Charger Voltage Addition: 640mV
3	EN_ILIM2	0	RD/WR	Input Limit Setting Selection: ⇨ 0 - Input Limit is set by IIN_LIMIT_1<1:0> = REG01<7:6> ⇨ 1 - Input Limit is set by IIN_LIMIT_2<2:0> = REG07<2:0>
2	IIN_LIMIT_2 <2:0>	000	RD/WR	VBUS Input Current Limit Active when EN_ILIM2=1 : ⇨ '000' - 300mA ⇨ '001' - 500mA ⇨ '010' - 800mA ⇨ '011' - 1200mA ⇨ '100' - 1500mA ⇨ '101' - 2000mA ⇨ '110' - 3000mA ⇨ '111' - 5000mA
1				
0				

APPLICATION INFORMATION

VBUS INPUT/OUTPUT CURRENT LIMIT

ETA6937 is able to configure VBUS Input/Output current limit by I2C.

For input current limit, there are 2 ways to configure, IIN_LIM_1[1:0] when EN_ILIM2[ ] =0, or IIN_LIM_2[2:0] when EN_ILIM2[ ] =1.

EN_ILIM2[ ]	IIN_ILIM_2[2:0]	IIN_ILIM_1[1:0]	VBUS INPUT CURRENT LIMIT (mA)
0	XXX	00	100
	XXX	01	500
	XXX	10	800
	XXX	11	No Current Limit
1	000	XX	300
	001	XX	500
	010	XX	800
	011	XX	1200
	100	XX	1500
	101	XX	2000
	110	XX	3000
	111	XX	5000

Output current limit is understood as BOOST output current limit is 1.2A. Beside the current limit, BOOST output current limit is reduced to 500mA when VBUS is under 3.0V (Typically).

DPM LEVEL CONFIGURATION

VINDPM<0> = 80mV, VINDPM<1> = 160mV, VINDPM<2> = 320mV, VINDPM<3> = 640mV, VINDPM<4> = 1280mV, VINDPM<5> = 2560mV, VINDPM<6> = 5120mV, and OFFSET = 4.2V

VHOLD (V)= 4.2 + 0.08*VINDPM<0> + 0.16*VINDPM<1> + 0.32*VINDPM<2> + 0.64*VINDPM<3> + 1.28*VINDPM<4> + 2.56*VINDPM<5> + 5.12*VINDPM<6>

BATTERY TERMINATION CURRENT

ITERM[2:0]	TERMINATION CURRENT ITERM(mA)
000	50
001	100
010	150
011	200
100	250
101	300
110	350
111	400

BATTERY CHARGE CURRENT

ETA6937 uses ICHG[4:0], ICHG_OFFSET[ ] and IMCHG[3:0] to configure Battery Charge Current. While ICHG[4:0], and ICHG_OFFSET[ ] are bits to configure the regulation target, IMCHG[3:0] are bits to set maximum Battery Charge Current IC can do. This means Loop will regulate Battery Charge Current at which is lower.

ICHG[4:0]	CHARGE CURRENT ICHRG (mA)	
	ICHG_OFFSET[ ]=0	ICHG_OFFSET[ ]=1
00000	550	650
00001	650	750
00010	750	850
00011	850	950
00100	950	1050
00101	1050	1150
00110	1150	1250
00111	1250	1350
01000	1350	1450
01001	1450	1550
01010	1550	1650
01011	1650	1750
01100	1750	1850
01101	1850	1950
01110	1950	2050
01111	2050	2150
10000	2150	2250
10001	2250	2350
10010	2350	2450
10011	2450	2550
10100	2550	2650
10101	2650	2750
10110	2750	2850
10111	2850	2950
11000	2950	3050
11001	3050	3150
11010	3050	3150
11011	3050	3150
11100	3050	3150
11101	3050	3150
11110	3050	3150
11111	3050	3150

IMCHRG[3:0]	MAXIMUM LIMIT CHARGE CURRENT IMCHRG(mA)	
	ICHG_OFFSET[ ]=0	ICHG_OFFSET[ ]=1
0000	550	650
0001	750	850
0010	950	1050
0011	1150	1250
0100	1350	1450
0101	1550	1650
0110	1750	1850
0111	1950	2050
1000	2150	2250
1001	2350	2450
1010	2550	2650
1011	2750	2850
1100	2950	3050
1101	3050	3150
1110	3050	3150
1111	3050	3150

BATTERY REGULATION VOLTAGE

ETA6937 uses VOREG[5:0] and VMREG[3:0] to configure Battery regulation voltage. While VOREG[5:0] are bits to configure the regulation target, VMREG[3:0] are bits to set maximum Battery voltage IC can do. This means Loop will regulate battery voltage at which is lower.

VOREG[5:0]	VBAT (V)	VOREG[5:0]	VBAT (V)
000000	3.5	100000	4.14
000001	3.52	100001	4.16
000010	3.54	100010	4.18
000011	3.56	100011	4.2
000100	3.58	100100	4.22
000101	3.6	100101	4.24
000110	3.62	100110	4.26
000111	3.64	100111	4.28
001000	3.66	101000	4.3
001001	3.68	101001	4.32
001010	3.7	101010	4.34
001011	3.72	101011	4.36
001100	3.74	101100	4.38
001101	3.76	101101	4.4
001110	3.78	101110	4.42
001111	3.8	101111	4.44
010000	3.82	110000	4.44
010001	3.84	110001	4.44
010010	3.86	110010	4.44
010011	3.88	110011	4.44
010100	3.9	110100	4.44
010101	3.92	110101	4.44
010110	3.94	110110	4.44
010111	3.96	110111	4.44
011000	3.98	111000	4.44
011001	4	111001	4.44
011010	4.02	111010	4.44
011011	4.04	111011	4.44
011100	4.06	111100	4.44
011101	4.08	111101	4.44
011110	4.1	111110	4.44
011111	4.12	111111	4.44

VMREG[3:0]	MAX BATTERY REGULATION (V)
0000	4.2
0001	4.22
0010	4.24
0011	4.26
0100	4.28
0101	4.3
0110	4.32
0111	4.34
1000	4.36
1001	4.38
1010	4.4
1011	4.42
1100	4.440 (Max)
1101	4.440 (Max)
1110	4.440 (Max)
1111	4.440 (Max)

FUNCTION DESCRIPTION

MAIN OPERATION STATE DIAGRAM

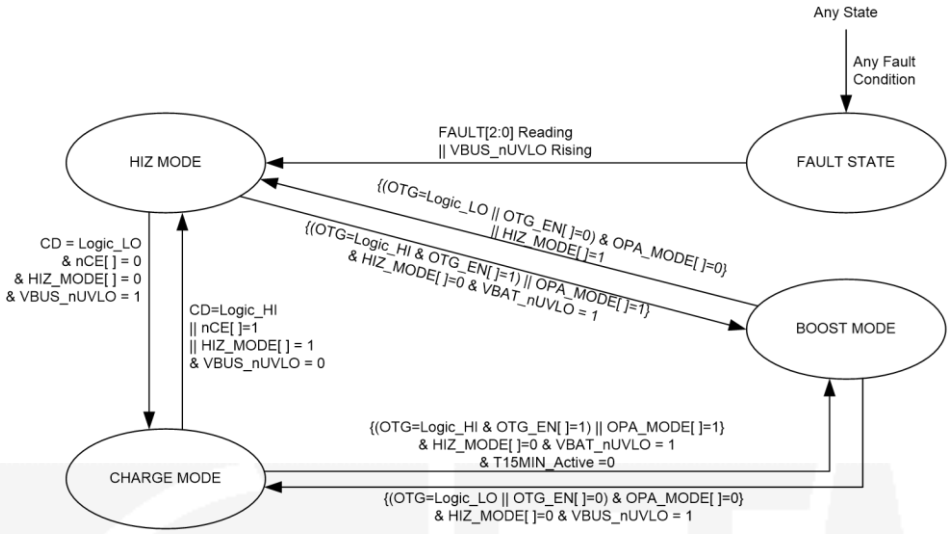
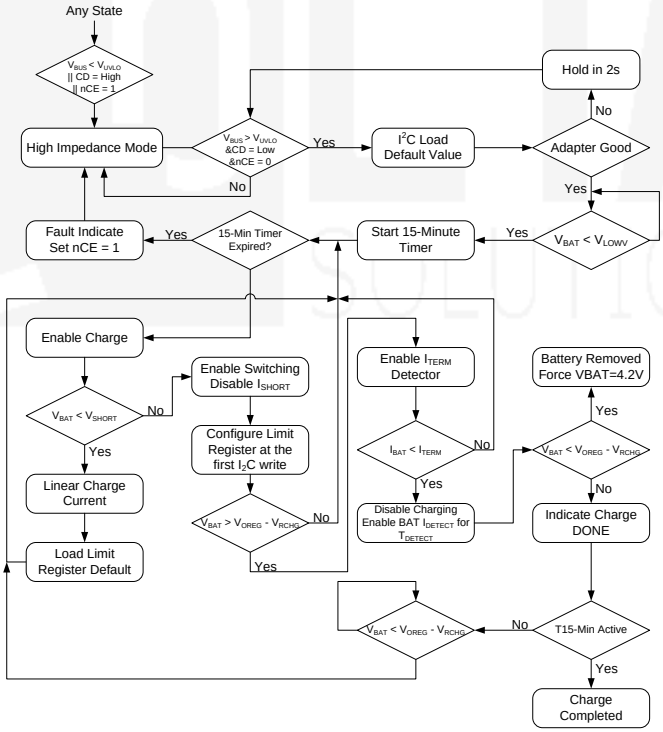


Figure 1: Main State Machine Chart

CHARGER OPERATION

OPERATION CHART FLOW IN CHARGE MODE



BAD ADAPTOR DETECTION

IC performs the bad adaptor detection by applying a current sink to VBUS. If the VBUS is higher than V_{IN_MIN} for 30ms, the adaptor is good and the charge process begins. Otherwise, if the VBUS drops below V_{IN_MIN}, a bad adaptor is detected. Then, the IC disables the current sink, sends STAT pin a fault pulse, and set FAULT[2:0] following related condition. After a holding time in 2s, the IC repeats adaptor detection process.

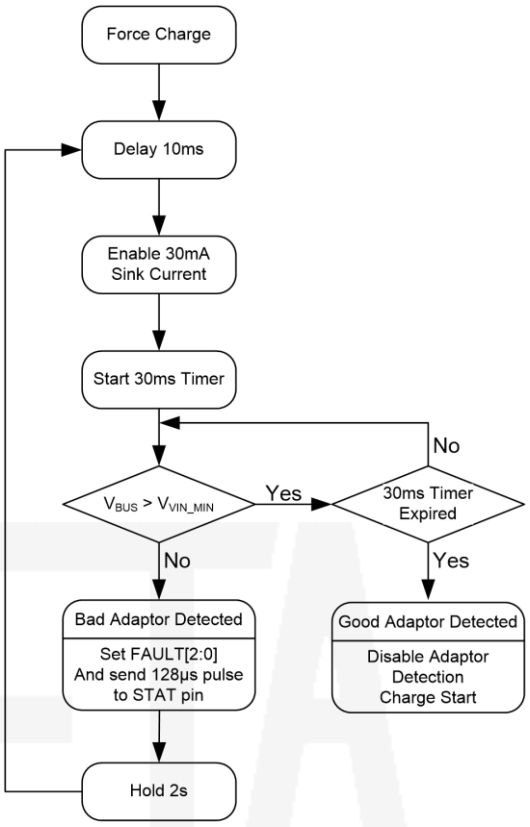


Figure 2: Bad Adaptor Detection Process Flow Chart

CHARGING PROFILE

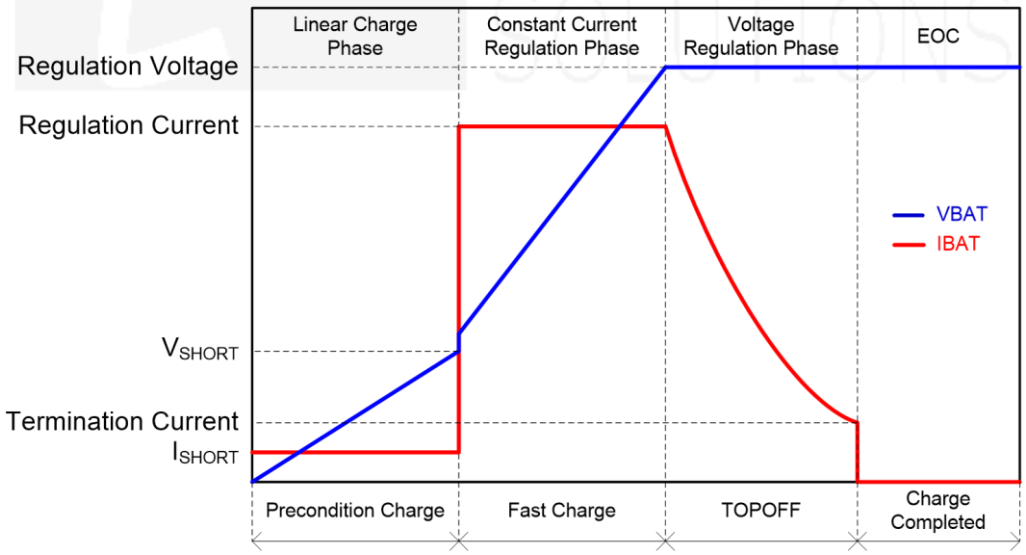


Figure 3: Typical Charging Profile. Case of being without Input Current Limit

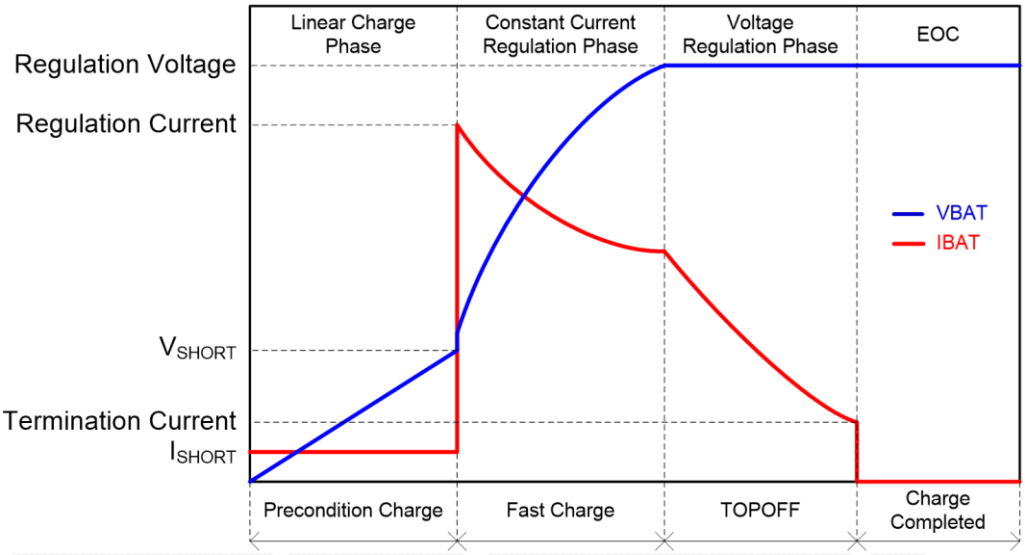


Figure 4: Typical Charging Profile. Case of being with Input Current Limit

CHARGER 30-MINNUTE SAFETY TIMER / 32-SECOND WATCHDOG TIMER / HOLD RECHARGE CYCLE

When a good adapter is attached, IC always starts 30-Minute Mode. In 30-Minute Mode, IC enable 30 minute timer. If 30 minute timer is expires, IC enters Fault State, sends STAT a fault pulse, sets FAULT[2:1] = [110].

Any writing action from I2C will make IC exit 30-Minute Mode to enter 32-Second Mode.

During 32-Second Mode, IC enables 32s timer. The timer is reset when I2C writes '1' to TMR_RST[ ]. If 32s timer expires, IC exits 32-Second Mode then back to 30-Minute Mode.

Then follow different battery conditions IC will behave different ways:

- VBAT is below HOST supply Power Good Level. VBAT is too low that not enough to supply the HOST. Then Charger stays in 30-Minute Mode with low charge current. This operation is maintained until HOST sends any writing command via I2C. Otherwise, IC will enter FAULT_STATE when 30 minute expires.
- VBAT is good for HOST but not too high, below VBAT_LOW level (close to full power level), HOST is able to send writing command to IC via I2C, then IC disable 30-Minute Mode and enter 32-Second Mode. In 32-Second Mode, Charger operates at Register Configured Charge Current , IOREG[5:0] and IMREG[3:0]. In case need to maintain full charge condition, HOST must write "1" to TMR_RST[ ] before 32 second expires to restart 32 minute counter. Otherwise, IC will exits 32-Minute Mode when 32 minute timer expires, then back to 30-Minute Mode.
- VBAT is higher than VBAT_LOW. Some system battery is not recharge when Battery voltage level is close to full level to avoid more battery recharge cycle. HOST will decide to start new charge cycle by sending a writing command to IC via I2C. Or keep IC in Standby time.

SAFETY LIMIT REGISTER

It is required to change safety Limit Register at first before do any writing action to other register. Otherwise safety limit register is writing protected. Protection is released either reset charger cycle or if battery voltage is decreased to under VSHORT.

INPUT CURRENT LIMIT REGULATION

During the charging process, if the Q1 current exceeds input current limit, Q1 will be controlled into limit loop, PMID voltage will decrease. Once charge detects PMID voltage drop for more than $I_{IN\_LIM} * R_{Q1}$,), the charge current begins to taper down to prevent any further drop of PMID voltage. When the IC enters this mode, the charge current is lower than the set value and the VIN_ILIM bits are set. This feature makes the part be not over power that heat the part much.

DYNAMIC POWER MANAGEMENT

During the charging process, if the input power source is not able to support the programmed or default charging current, the VBUS voltage will decrease. Once the VBUS drops to VIN_DPM (default 4.52V), the charge current begins to taper down to prevent any further drop of VBUS. When the IC enters this mode, the charge current is lower than the set value and the special charger bit is set. This feature makes the IC compatible with adapters having different current capabilities.

THERMAL REGULATION

During the charging process, if the junction temperature is above T_{FB} (120°C), the charge current is reduced. Charge current is reduced to minimum level (550mA) when junction temperature hits 130°C. This feature makes the IC be not over temperature during high charge current at low battery voltage. When battery voltage high enough, power crosses the part is lower, junction temperature is lower, then battery is charged with full set current.

Beside the thermal regulation, part is protected by second temperature protection, thermal shutdown. When junction temperature hit T_{SHUT}, IC will be turn off until part cold down 20°C. This feature is active for both Charge Mode and Boost Mode.

LINEAR CHARGE – PRECONDITION CHARGE

To prevent battery from explosion when the voltage is too low, under V_{BAT_SHORT}, IC charges battery with a linear current, I_{SHORT}. I_{SHORT} is programmed by level of VBUS.

ETA6937 also swaps to use linear charge when charge current is less than 250mA. Condition is from FOLDBACK or TOPOFF conditions.

CHARGE COMPLETE

When Charge Current hits termination threshold and IC still detect valid battery, IC indicates charge complete. In this condition, if IC is still in 32-Second Mode, IC allows to recharge when battery voltage drops below recharge threshold. In case 32-Second timer expire, IC will set nCE[ ] = 1 to not allow recharge. New charge cycle will not start until nCE[ ] is cleared to '0' or re-plugging VBUS.

BOOST MODE OPERATION

BOOST 32-SECOND WATCHDOG TIMER

Boost always operates in 32-Second Mode. Once Boost is enabled, IC starts 32 second timer. This timer could be reset by writing '1' to TMR_RST[ ] via I2C. Once the 32-second timer expires, the IC turns off the boost converter by clear OTG_EN[ ] or OPA_MODE[ ], enunciates the fault pulse from the STAT pin and sets fault status bits in the status register.

BOOST START-UP

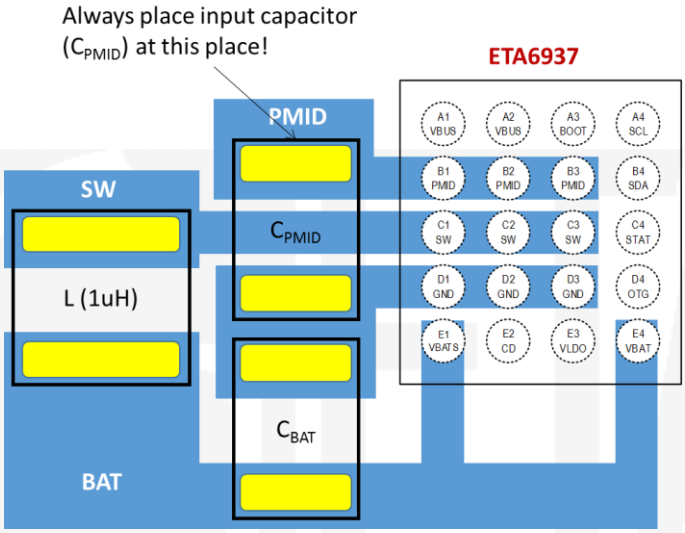
Boost starts when either {OTG is held at Logic_HI and OTG_EN[ ] =1} or OPA_MODE[ ] = 1. When one of these conditions occurs, IC starts to monitor battery voltage. If battery voltage is above UVLO and under OVP thresholds, IC enables BOOST Converter.

Q1 is enabled right Boost Converter is enabled. There is a Boost output current limit is integrated in Q1 Module. IC also provide BST_ILIM[ ] to configure Boost Output Current Limit.

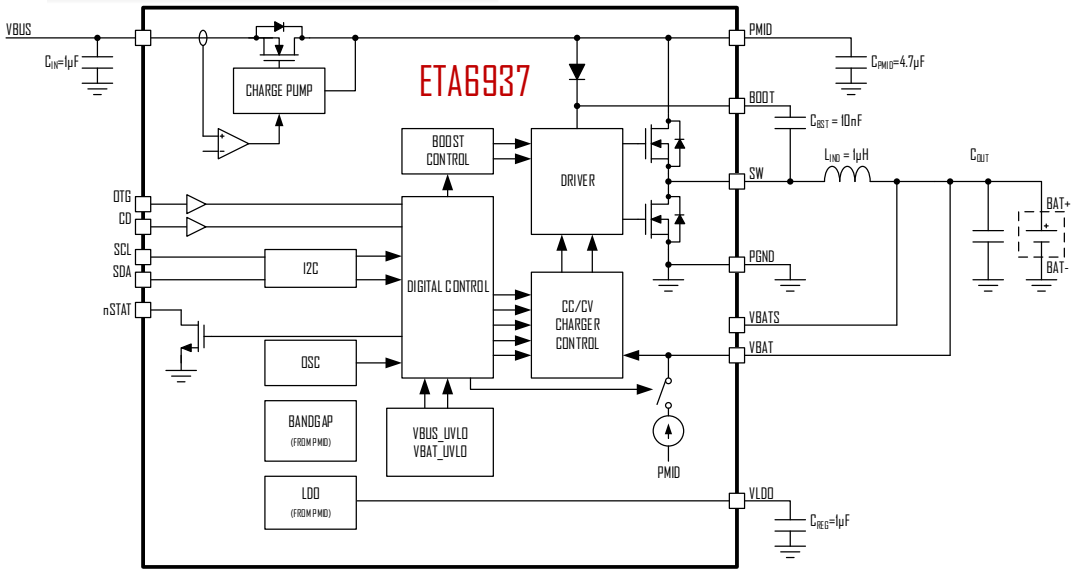
PCB GUIDELINES

Please always put PMID capacitor closet to the PMID pins and GND pins, with wires directly connected to the PMID and GND balls. DONOT connect the negative terminal of PMID capacitor to the ground plane, while the GND balls are also connected to the ground plane. As such PMID capacitor serves as the input capacitor of switching charger, and if the capacitor is connected to the GND pins thru ground plane, 2 serial vias (capacitor to ground plane and ground plane to GND pins) are introduced, which means a serial parasitic inductor is placed between the input capacitor and the real input pins. And thus, the decoupling function of such input capacitor is compromised. So, lots of switching noise may no longer be filtered by the input capacitor, and it leads to instability of the switching charger.

Following illustration shows the correct way to place the input capacitor.



BLOCK DIAGRAM



PACKAGE OUTLINE

Package: CSP-20 (4x5 balls)