ELEC-E3540 Digital Microelectronics II – Exercise 1

Book: Peter J. Ashenden, "The designer's guide to VHDL", 3rd edition

Acquaint yourself with the following chapters: 1, 2, 5 (we will return to these quite often). Particularly familiarize yourself with sections: 1.1-1.4, 2.1-2.2, 2.5, 5.1-5.2.

Things to learn:

- Types: bit, bit_vector, boolean, integer.
- Signals, process, variables, sensitivity lists of the processes, process as a part of a test bench, wait-statement, self-terminating simulation.
- Simulation environment (Questasim), compilation of the code, project management, windows, monitoring the signals, basics of debugging.
- Basics of Git version control

Pre-exercise tasks: Sketch a VHDL-code with correct definitions in correct place of the following elements (at this point the elements do not have to perform any kind of logical task):

- entity
- architecture
- signal
- constant
- process

Before developing your first code, set up your version control environment:

1. Log in to Aalto Gitlab and check the course group by address `https://version.aalto.fi/gitlab/elec-e3540-exec`. It will contain a subgroup with your username – this is your git workspace.
2. In your Gitlab user settings, add your public SSH key from your Vspace machine. If you don't have a file starting with "`id_`" in `.ssh` folder of your home directory, you can generate one using following tutorial: `https://docs.gitlab.com/ee/ssh/README.html`. Use RSA key type, and your Aalto email as identifier.
3. In the course git group, find a project named "Exercise_template". Follow instructions provided on the front page to set up your first git project.

Exercise task: Write a test bench with proper entity and architecture definitions. Inside the architecture of the test bench, write a process which models the functionality of the multiplexer. Do not create a separate entity for the multiplexer in this exercise. The input signals of the multiplexer are 8-bit bit_vectors, A and B. Selector signal S is of type bit. The 8-bit output signal is Q and its type is bit_vector. Ideal multiplexer is modeled with a process which selects one of the signals A and B to signal Q depending on the state of S as described with the truth table below.

S	Q
0	A
1	B

Goal: Student can produce independently a VHDL code that can be simulated. Code consists of the structures entity, architecture and process and some basic type signals.

Workload: Preparations 4h + exercise 2h