Fully Integrated GaAs MMIC Bandpass Filtering Power Amplifier Chip With Compact Couple-Line-Based Matching Network

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***Abstract*—This letter presents a novel bandpass filtering power amplifier (FPA) structure featuring a dc-block input matching network (IMN), which utilizes a filtering impedance transformer consisting of two cascaded coupled-lines, a short-circuit coupled-line (SCCL), and a parallel resonator (PR). The SCCL generates transmission zeros (TZs) near the passband, enabling sharp roll-off characteristics. The PR enhances filtering response while occupying minimal circuit area. For verification, a monolithic microwave-integrated circuit (MMIC) FPA using 0.25-μm GaAs process was designed and fabricated, implementing serpentine routing for a highly compact layout. The measurement results demonstrate 30-dB out-of-band rejection, 27-dBm output power, and 46%–55% drain efficiency (DE) in 9–11 GHz. The adjacent channel power ratio (ACPR) is lower than −48.4 dBc with digital predistortion (DPD) using a 60-MHz 64-QAM 5G-NR signal.**

***Index Terms*—Bandpass, coupled-line, filtering, GaAs, monolithic microwave-integrated circuit (MMIC), power amplifier (PA).**

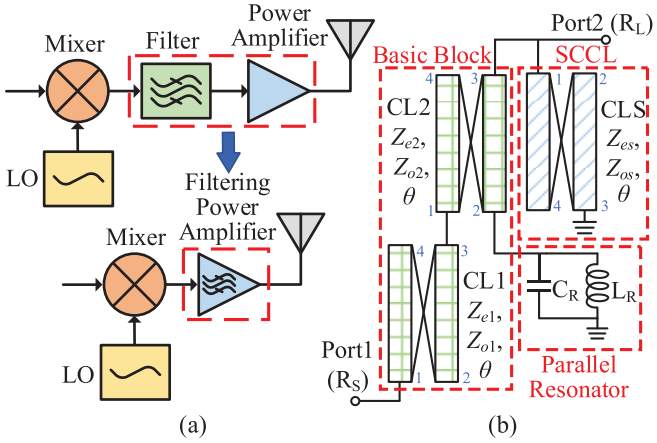

Fig. 1. Block diagram of (a) FPAs in RF transmitters and (b) proposed filtering impedance transformer.

I. Introduction

TO DATE, the accumulation of existing communication standards has led to escalating complexity in wireless communication systems. The working bands of radio frequency (RF) front-end modules (FEMs) also expand in number continuously, driving a substantial increase in filter utilization. Consequently, filtering power amplifiers (FPAs) have been persistently studied to reduce system complexity. As shown in Fig. 1(a), FPAs integrate the functionalities of both filters and power amplifiers (PAs), thereby simplifying the system architecture while reducing overall insertion loss and improving gain and efficiency.

Various FPA designs have been proposed in previous works. In [1] and [2], cavity filter and substrate-integrated waveguide are used in the output matching network (OMN) to create filtering response. For higher out-of-band rejection, coupled-line-based FPAs implemented on printed circuit boards (PCBs) are reported in [3], [4], and [5]. Fully integrated devices represent the evolutionary direction in RF research [6], [7]. To meet compact integration requirements, monolithic microwave-integrated circuit (MMIC) FPAs have been proposed recently. Estrada et al. [8] demonstrate a MMIC FPA design using arbitrary complex impedance loads. The MMIC FPA in [9] applies the transformer-based filtering combiner, achieving relatively high gain and output power. However, the co-optimization of power amplification performance and out-of-band rejection in a compact footprint still remains challenging.

In this letter, a 0.25-μm GaAs MMIC FPA with high out-of-band rejection and superior power performance is proposed based on a bandpass filtering impedance transformer (BFIT). A parallel resonator (PR) and serpentine routing are adopted to reduce the chip area. The results show that the MMIC FPA has a high out-of-band suppression level in wide stopbands. It also exhibits competent power-efficiency characteristics.

II. Circuit Design

A. Filtering Impedance Transformer Design

The schematic of the proposed BFIT is shown in Fig. 1(b). The BFIT comprises three key components: a basic block (BB), a short-circuited coupled-line (SCCL), and a PR. The BB contains a pair of cascaded coupled-lines (CL1 and CL2), where port 2 and 4 are open. The PR is loaded on port 2 of CL2. The SCCL (CLS) is a coupled-line with port 2 and 4 open and port 3 shorted.

Received 17 April 2025; revised 21 May 2025; accepted 6 June 2025. This work was supported by the National Natural Science Foundations of China under Grant 62320106002, Grant U21A20510, and Grant U22A2014. *(Corresponding author: Yongle Wu.)*

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Digital Object Identifier 10.1109/LMWT.2025.3578722

From the holistic perspective, the BB provides fundamental impedance transformation and bandpass filtering capability.

According to [10], the *ABCD* matrix of the two cascaded CLs in BB is derived as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{CL}} = \begin{bmatrix} \dfrac{Z_a\cos(\theta)}{Z_b} & jZ_b\dfrac{\csc\theta}{2} - \dfrac{jZ_a^2\cos^2(\theta)}{2Z_b\sin(\theta)} \\ \dfrac{2j\sin(\theta)}{Z_b} & \dfrac{Z_a\cos(\theta)}{Z_b} \end{bmatrix} \quad (1)$$

where

$$Z_a = Z_e + Z_o, Z_b = Z_e - Z_o. \quad (2)$$

Combining the *ABCD* matrix of CL1 and CL2 with the electrical length θ of 90°, the *ABCD* matrix of BB is given as

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{\mathrm{BB}} = \begin{bmatrix} \dfrac{Z_{e1}-Z_{o1}}{Z_{e2}-Z_{o2}} & 0 \\ 0 & \dfrac{Z_{e2}-Z_{o2}}{Z_{e1}-Z_{o1}} \end{bmatrix}. \quad (3)$$

Assuming the impedance ratio $r = R_L/R_S$ ($R_L > R_S$) and converting the *ABCD* matrix to *S* matrix [11], the S_{11} of BB is calculated as

$$[S_{11}]_{\mathrm{BB}} = \frac{r(Z_{e1}-Z_{o1})^2 - (Z_{e2}-Z_{o2})^2}{r(Z_{e1}-Z_{o1})^2 + (Z_{e2}-Z_{o2})^2}. \quad (4)$$

When matching at the center frequency, the magnitude of S_{11} will be 0, then r can be obtained as

$$r = \left(\frac{Z_{e2}-Z_{o2}}{Z_{e1}-Z_{o1}}\right)^2. \quad (5)$$

By utilizing this formula and setting appropriate Z_e and Z_o, the BB can realize arbitrary impedance ratio ($r > 1$).

The impedance of the PR loaded on BB can be given as

$$Z_{\mathrm{PR}} = \frac{j\omega L_R}{1-\omega^2 L_R C_R}. \quad (6)$$

When $\omega = 1/\sqrt{L_R C_R}$, the PR behaves as an open circuit. At other frequencies, it will affect the impedance transformation capability of BB, thereby effectively enhancing out-of-band rejection for the BFIT. The SCCL generates two transmission zeros (TZs) proximate to the passband, enabling sharp roll-off characteristics. Assuming the frequency of TZs generated by the SCCL as $f_z = f_0(1+\alpha)$. According to [12], α is derived as

$$\alpha = \pm\frac{2}{\pi}\sin^{-1}\sqrt{\frac{Z_{e2}-Z_{o2}}{Z_{e2}+Z_{o2}}}. \quad (7)$$

Fig. 2(a) depicts the simulated *S*-parameters of the BFIT with different parts loaded. Fig. 2(b) shows the simulated *S*-parameters under different α. The value of α is set to 0.1 in the proposed design, which strikes a balance between sharper roll-off response and a desirable level of out-of-band rejection. Fig. 2(c) presents the comparison of the insertion loss between BFIT and a conventional matching network combined with a BFIT-like 50-to-50 Ω filter. The minimum insertion loss of the simulated input matching network (IMN) is 2.73 dB.

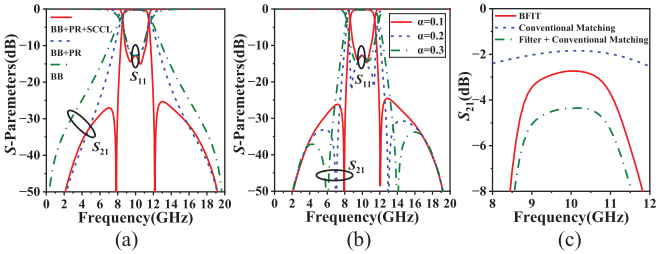

Fig. 2. Ideal simulated *S*-parameters of (a) 10-to-50 Ω BFIT with different parts and (b) 10-to-50 Ω BFIT under different α. (c) Simulated S_{21} of the IMN in the designed MMIC FPA using BFIT, compared with a conventional matching network combined with a BFIT-like 50-to-50 Ω filter.

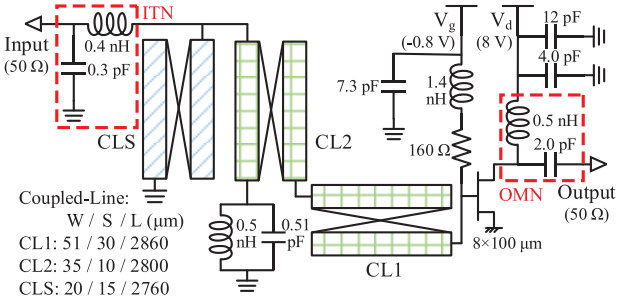

Fig. 3. Schematic of the designed MMIC FPA.

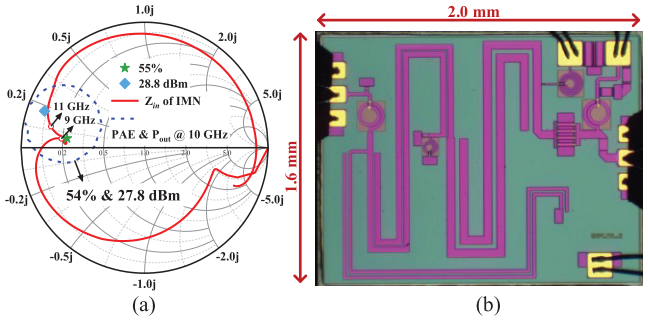

Fig. 4. (a) Simulated impedance curve of the IMN and the source-pull contour of the transistor at 10 GHz. (b) Photograph of the fabricated MMIC FPA chip.

B. FPA Design

The schematic of the designed MMIC FPA is shown in Fig. 3. It is implemented in a 0.25-μm GaAs pHEMT process. The size of the selected transistor is 8×100 μm for higher output power. The BFIT adopted in the IMN is designed at 10 GHz. The passband is located within 9–11 GHz. To precisely adjust the impedance of IMN, an impedance tuning network (ITN) is employed, enabling optimal conjugate matching with the transistor. The resistor in the gate bias circuit enhances low-frequency stability [13]. Due to the out-of-band rejection, the FPA requires no extra stabilization circuit to ensure full-band unconditional stability, which reduces overall circuit design complexity. Moreover, the BFIT inherently possesses dc-blocking characteristics, obviating the need for additional dc-blocking capacitors, thereby avoiding extra insertion loss. Fig. 4(a) presents the simulated impedance of IMN with the source-pull contour of output power P_{out} and power added efficiency (PAE). The optimal PAE and output power of the transistor are about 54% and 27.8 dBm at 10 GHz. The IMN achieves well-matched impedance at

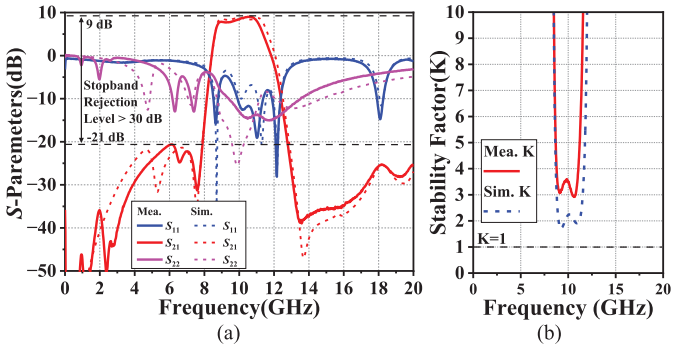

Fig. 5. Simulated and measured (a) small-signal *S*-parameters and (b) *K*.

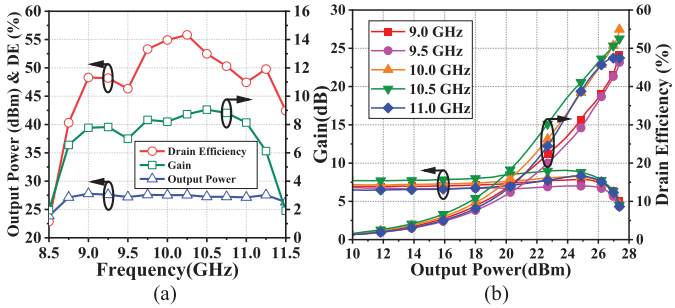

Fig. 6. (a) Measured CW DE, output power, and gain versus frequency. (b) Measured DE and gain versus output power.

the target frequencies. The OMN includes the bias inductor and the output capacitor, simplifying the design and improving power performance.

C. MMIC Layout Design

Photograph of the fabricated MMIC FPA chip is presented in Fig. 4(b). To minimize the chip size, the cascaded coupled-lines in BB adopt serpentine routing. The SCCL employs encircling routing around the BB. The PR is placed between the two coupled-lines of BB. Finally, the compact layout design reduces the overall chip size to 2.0×1.6 mm^2.

III. Simulation and Measurement Results

The manufactured MMIC FPA is mounted on an external PCB with power supply connections established through wire bonding. The drain voltage is 8 V with a gate voltage of −0.8 V. RF signal interfacing is achieved via RF probe contacts.

Fig. 5(a) illustrates the simulation and measurement results of small-signal *S*-parameters, which demonstrate excellent correlation. The measured S_{21} is 7.7–9.0 dB in 9–11 GHz, and the measured minimum stopband rejection is 30 dB, exhibiting good bandpass filtering response and sharp roll-off behavior. At all frequencies, $K > 1$, which demonstrates the FPA is unconditionally stable in the full band. Moreover, the out-of-band *K* factors are relatively high, implying exceptional out-of-band stability.

The large signal performance under continuous wave (CW) versus frequency is delivered in Fig. 6(a). In 9–11 GHz, the measured saturated output power is 27.1–27.6 dBm with drain efficiency (DE) of 46%–55%. The measured DE and gain versus output power are shown in Fig. 6(b). Throughout the entire target passband, the designed FPA presents excellent

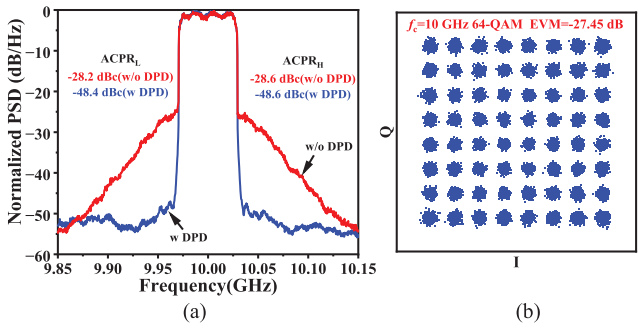

Fig. 7. Measured (a) output spectrum and (b) constellation using a 60-MHz 64-QAM 5G-NR signal.

TABLE I
State-of-the-Art of FPAs

Ref.	Freq. (GHz)	Process	Circuit Size (mm^2)	Stopband Rejection (dB)	Output Power (dBm)	Gain (dB)	Efficiency (%)
[1]	3.03	Cavity Filter	4800	-	40	>10	DE: 72%
[2]	5.4-5.6	SIW	29516	-	38.5	12.5	PAE: 48.7%
[4]	2.0-2.4	PCB	4800	>31	39-40.4	10.6	DE: 69-78.2%
[5]	1.85-2.1	PCB	7080*	>59.7	38.6-39	8.9-10.2	DE: 58.5-73%
[8]	27-29	GaAs MMIC	6.25	8	23	8	PAE: 30%
[9]	5.1-5.9	GaAs MMIC	3.57	>30*	33.3	26.0-26.8	PAE: 30.6%
This work	**9-11**	**GaAs MMIC**	3.2	**>30**	**27.1-27.6**	**7.7-9.0**	**DE: 46-55% PAE: 37-48%**

*: estimated value

power capability and high efficiency, indicating significant practical value for this design.

To evaluate the linearity, Fig. 7(a) illustrates the power spectrum density (PSD) with and without digital predistortion (DPD) using a 60-MHz 64-QAM 5G-NR signal. The adjacent channel power ratio (ACPR) is -28.2 dBc at 10 GHz before DPD, and improved to −48.4 dBc with DPD employed. The measured constellation shows that the EVM is −27.45 dB. It is confirmed that the linearity performance of the proposed FPA meets the requirements of modern communication systems, indicating the practical application potential and compatibility with DPD of the BFIT-based matching network. The FPA performance comparisons with the state-of-the-art works are delivered in Table I.

IV. Conclusion

This letter presents a novel FPA structure featuring a dc-block IMN based on BFIT. The BFIT comprises two cascaded coupled-lines, a SCCL and a PR. A MMIC FPA using 0.25-μm GaAs process was designed and fabricated, implementing serpentine routing for a highly compact layout. The simulated and measured results are in good agreement, showing that it has excellent out-of-band rejection. It also exhibits good large signal performance and linearity meeting the requirements of modern communication systems. The proposed FPA validates the applicability of the BFIT in PA design. In future designs, additional amplifier stages can be conveniently integrated to further enhance the gain performance of FPAs.

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