



## Regular paper

**A 22–26 GHz 6-Bit digitally controlled two-stage current-steering variable gain amplifier for differential signal processing**Shuchen Zhen, Yongle Wu <sup>\*</sup>, Zhuoyin Chen, Xiaopan Chen, Weimin Wang

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## ABSTRACT

A 22–26 GHz 6-bit digitally controlled two-stage differential variable gain amplifier (VGA) in a 180-nm CMOS process is presented. The first-stage amplifier employs a six-unit current-steering structure, enabling 6-bit gain control through six control voltages. The second-stage amplifier utilizes a neutralization capacitance architecture to further enhance the overall gain of the VGA. Additionally, signal transmission between the circuits is achieved through transformer-based matching networks by way of magnetic coupling. Furthermore, the VGA was designed, fabricated, and comprehensively measured. Its performance was evaluated through both *S*-parameter and linearity experiments. The measured *S*-parameters results demonstrate that at the center frequency of 24 GHz, the VGA achieves a gain control range of 15.37 dB, with the maximum gain reaching −1.97 dB. Within the 22–26 GHz, the  $S_{11}$  and  $S_{22}$  are better than −10 dB and −7 dB, respectively, while the phase variation remains below 16.48°. Moreover, the input 1-dB compression point ( $IP_{1dB}$ ) and output 1-dB compression point ( $OP_{1dB}$ ) are better than 3.71 dBm and −1.83 dBm, respectively. The VGA consumes 19.27 mA from a 1.8 V supply, and the core area is  $1.24 \times 0.26 \text{ mm}^2$  excluding the testing pad.

**1. Introduction**

With the relentless pursuit of high-speed and instant communication in human society, mobile communication has evolved from 5G to the exploration of 6G. To address the intrinsic shortcomings of 5G millimeter-wave signal transmission, such as high loss and short propagation distance, phased array technology that can achieve beamforming has been increasingly studied and applied [1–10]. High-precision and high-resolution phase shifters (PS) and variable gain amplifiers (VGA) serve as the core components of phased arrays. By controlling the phase and amplitude of each channel or sub-element, they can respectively adjust the beam direction and control the sidelobe level to suppress multipath and adjacent-frequency interference in communication anti-jamming scenarios. In the research of phased arrays targeting different scenarios and functional positioning, customized VGAs have been proposed and integrated into systems. For example, a 3-bit VGA was applied to a phased array receiver, achieving 8 dB gain control in the 2–16 GHz [1]. A K-band phased array receiver was proposed in [3], which includes a 4-bit current-steering VGA with a gain control precision of 0.4 dB/step within the operating band. An 8-element 4-beam

phased array operating in the Ka-band was proposed in [10], featuring a hybrid VGA composed of a digitally controlled VGA and an analog VGA based on a Gilbert cell. This VGA was applied to a  $4 \times 4$  beamforming architecture system, with a gain tuning range of 27 dB and a gain step of 0.25 dB.

Many studies have been conducted on analog [12–14] and digitally [15–23] controlled VGAs. On the one hand, analog-controlled VGAs generally achieve gain control by adjusting bias voltages, which can be implemented through Gilbert cells or transistor variable load structures. For instance, a two-stage current-reuse wideband analog-controlled VGA was proposed in [14]. By adjusting the drain bias of the complementary common-source stage within the range of 0.6–1.6 V, the VGA achieved a gain control range of 23.4 dB (from −5.4 dB to 18 dB) in the 3.1–23.7 GHz. However, analog-controlled VGAs have limited gain control precision and are not easily compatible with or integrated into multi-bit digitally controlled phased arrays. On the other hand, digitally controlled VGAs are mainly based on current-steering architectures. The VGA proposed in [18] paralleled a 4-bit digital current-steering structure to the drain of the cascode common-source transistor. By regulating the current in the cascode signal path, it achieved a peak gain of 16.3 dB

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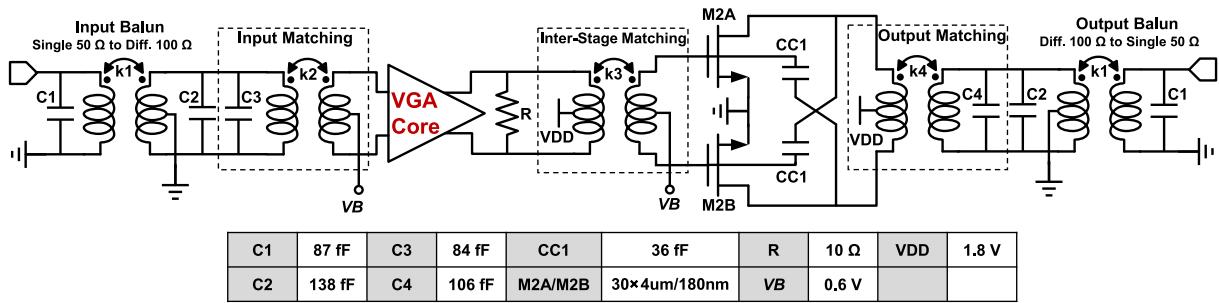


Fig. 1. Circuit topology of the proposed VGA.

at 28 GHz and a gain control range of 8.4 dB in the 27–43 GHz. Works [15,17,19] implemented multi-bit digitally controlled wideband VGAs in the same or similar manner as [18]. However, these works [15,17–19] all designed VGAs with unbalanced input and output. Since differential structures are commonly used in millimeter-wave phased arrays to implement PS and VGA, unbalanced input and output VGAs are difficult to integrate into differential phased array systems, and cannot take advantage of the wideband matching and compact area benefits brought by transformer-based matching networks.

Furthermore, in recent years, millimeter-wave phased arrays have increasingly adopted differential structures to transmit signals to combat common-mode interference, improve signal gain, and facilitate symmetric layout using transformer-based matching networks based on magnetic coupling theory [11] and impedance matching theory [24]. Works [20–23] designed millimeter-wave differential digitally controlled VGAs. For example, a two-stage 6-bit current-steering VGA connected by decoupling transformers was proposed in [20]. Measured results showed that it achieved –1 to 6 dB gain control with a step of 0.5 dB in the 53–63 GHz. A single-stage differential VGA based on the current-steering structure and 4-bit digital control was designed in [21], achieving 7.5 dB gain control in the 30–38 GHz. However, [20] and [21] directly matched the core circuits to single-ended 50 Ω using baluns. When integrating those VGAs into differential systems, it becomes necessary to redesign the interstage matching transformers to achieve impedance matching between the VGA core circuits and the system's differential impedance. This not only reduces the reusability of the VGAs but also increases the complexity of integrating them into differential systems.

In this brief, a two-stage differential 6-bit digitally controlled VGA is proposed. The first stage employs a 6-bit current-steering circuit based on symmetric units, while the second stage utilizes a neutralization capacitance topology to compensate for the overall gain of the VGA. Transformer-based matching networks are applied to the impedance matching between circuits. Notably, the input and output ends are first matched to differential 100 Ω and then transformed from differential 100 Ω to single-ended 50 Ω through baluns. Therefore, by removing the baluns, the VGA in this work can be directly applied to differential 100 Ω RF systems, increasing the reusability of the VGA.

The organization of this paper is as follows. Section II presents the overall circuit topology of the proposed VGA, analyzes the 6-bit digital current-steering core circuit and the unit circuit, and discusses the three-dimensional (3D) topology and corresponding parameters of the transformers used in this work. Section III analyzes the gain control range, phase variation, and 1-dB compression points based on the measured results of S-parameters and linearity experiments. Finally, the work of this paper is summarized in Section IV.

## 2. Design and analysis of the proposed VGA

### 2.1. Circuit topology

The diagram of the proposed digitally controlled VGA is shown in

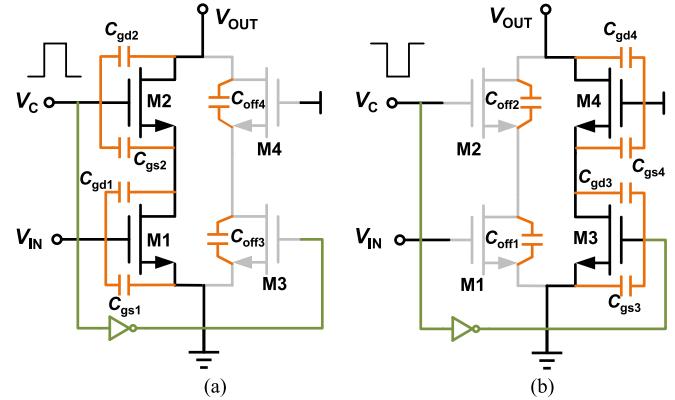


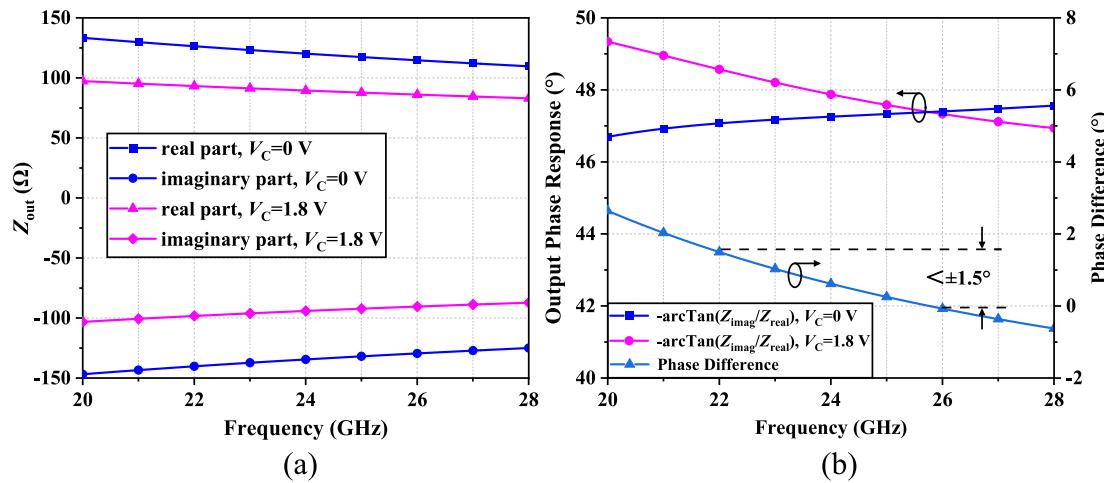
Fig. 2. The operating state of the transistors and the corresponding parasitic parameters of the unit circuit when the digital control voltage is in the (a) high and (b) low voltage state.

Fig. 1. It consists of a VGA core circuit, a second-stage amplifier based on the neutralization capacitance technique, and five transformer-based matching networks. The VGA core circuit employs a differential structure to suppress common-mode interference. The second-stage amplifier adopts the traditional neutralization capacitance architecture to ensure the stability of this stage, and improves the overall gain of the VGA. The matching network composed of a transformer embedded with parallel capacitors completes the complex impedance matching between circuits based on the magnetically coupled resonator [11], providing wideband matching and significantly reducing the area occupied by passive elements.

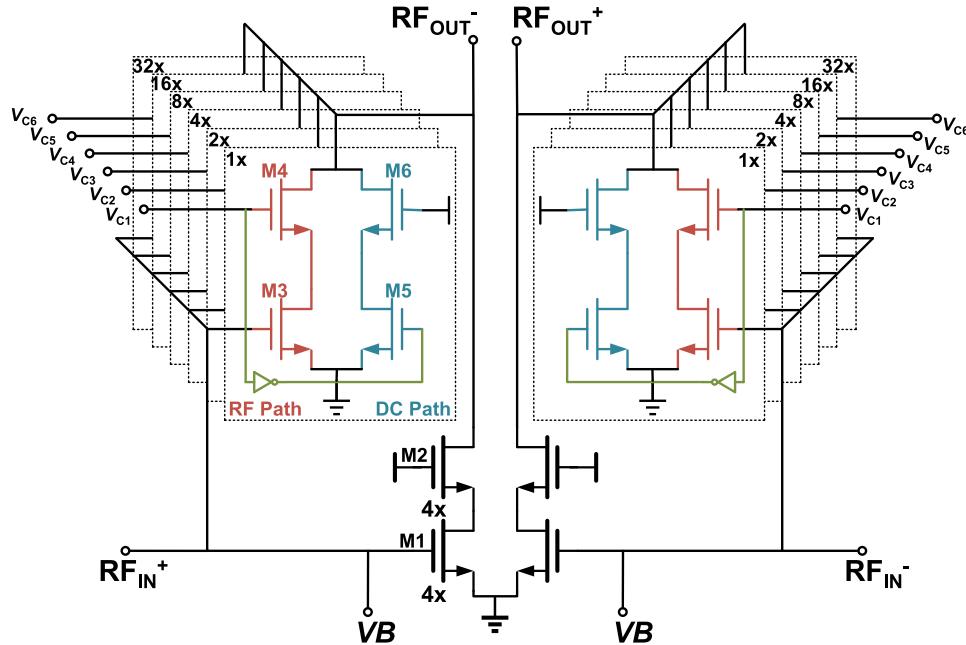
In addition, the input matching network and the output matching network achieve the impedance matching from the internal circuit to the external 100 Ω, which is the commonly used impedance in differential RF systems. For convenience of testing, baluns are placed at both the input and output ends to achieve the impedance matching between differential 100 Ω and single-ended 50 Ω. Importantly, compared to directly using a transformer for impedance matching from the internal circuit to single-ended 50 Ω, this design significantly enhances the reusability of the VGA in differential systems. The VGA, with baluns removed from the input and output ends, can be easily integrated into differential RF systems.

### 2.2. Analysis of the unit circuit

Fig. 2 illustrates the conduction and cutoff conditions of the transistors, as well as the parasitic parameter distribution of the unit circuit when the control voltage  $V_C$  is at the high and low voltage states.  $C_{gs}$  and  $C_{gd}$  represent the parasitic gate-source and gate-drain capacitances of the transistor when it is on, and  $C_{off}$  represents the equivalent cutoff capacitance of the transistor when it is off. The unit circuit employs a symmetrical structure, so the output impedance can be as close as



**Fig. 3.** When  $V_c$  is at 0 V and 1.8 V, (a) the real and imaginary parts of the output impedance of the 1x unit circuit shown in Fig. 4, and (b) the phase response based on the output impedance with the phase difference between the two states.



**Fig. 4.** The diagram of the VGA core circuit structure.

possible under both high and low  $V_c$  states. When  $V_c$  is at a high voltage state, M1 and M2 operate in the saturation region and form a cascode structure, while M3 and M4 are in the cutoff region and are equivalent to the cutoff capacitances  $C_{off3}$  and  $C_{off4}$ . Conversely, when  $V_c$  is at a low voltage state, M1 and M2 are in the cutoff region and are equivalent to the cutoff capacitances  $C_{off1}$  and  $C_{off2}$ , while M3 and M4 operate in the saturation region and form a cascode structure.

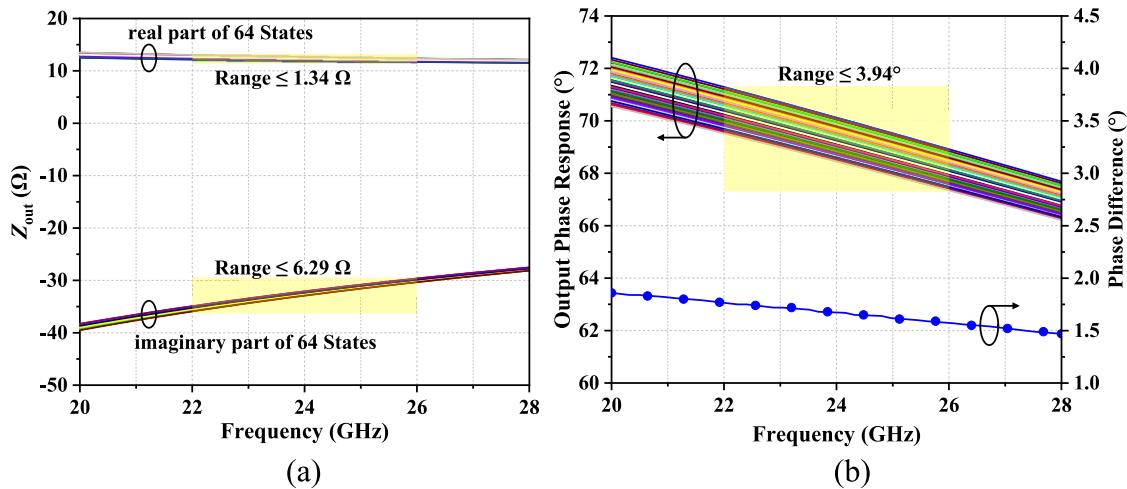
The phase of the output signal can be expressed as the ratio of the imaginary part to the real part of the output impedance. Simulations were performed on the 1x unit circuit depicted in Fig. 4 at  $V_c$  levels of 0 V and 1.8 V. The output impedance for both the low and high voltage states of  $V_c$  is illustrated in Fig. 3(a). Additionally, the phase response at the output was calculated based on the ratio of the imaginary part to the real part of the output impedance, with the phase difference between the two states shown in Fig. 3(b). At the center frequency of 24 GHz, the phase difference is 0.62°, and within the 22–26 GHz, the phase difference remains below ± 1.5°. Although there is a certain gap in the impedance between the two states as shown in Fig. 3(a), from the

perspective of phase response, the symmetrical structure of the unit circuit can provide as consistent an output signal phase as possible under both high and low  $V_c$  states.

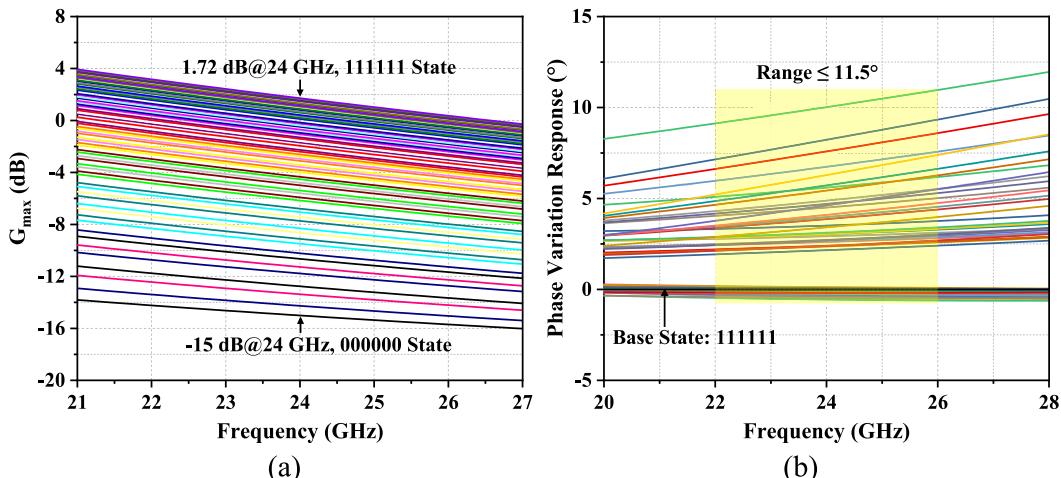
### 2.3. Analysis of the VGA core circuit

The diagram of the VGA core circuit with symmetric topology is shown in Fig. 4. Each half of the VGA core circuit consists of two fixed-gain transistors M1 and M2 that are always on, as well as six unit circuits with transistor sizes increasing in powers of two. Each unit circuit is composed of four transistors with the same size and features two signal paths: an RF path and a DC path, as shown in Fig. 4.

When the control voltage  $V_c$  is at a high level of 1.8 V, the common-source transistor in the DC path is turned off, while the RF signal is amplified through the RF path. Conversely, when the control voltage  $V_c$  is at a low level of 0 V, the common-gate transistor in the RF path is turned off. Meanwhile, the gate voltage of the common-source transistor in the DC path is 0.6 V, and the DC path becomes conductive. In this



**Fig. 5.** (a) The real and imaginary parts of the output impedance and (b) the phase response based on the output impedance, of different gain states for the VGA core circuit with a  $5 \Omega$  resistor connected in series at each differential output end.



**Fig. 6.** (a) The maximum available gain  $G_{max}$  and (b) the phase variation response based on  $S_{21}$ , of different gain states for the VGA core circuit with a  $5 \Omega$  resistor connected in series at each differential output end.

case, the unit circuit does not contribute to the amplification of the RF signal. By combining the six control voltages  $V_{C6}-V_{C1}$ , the VGA core circuit can achieve 64 different gain states. When  $V_{C6}-V_{C1}$  is “000000”, it represents the lowest gain state, with the gain contributed only by M1 and M2. In contrast, when  $V_{C6}-V_{C1}$  is “111111”, it represents the highest gain state, with all the RF paths of the unit circuits turned on to contribute to the gain. Moreover, the output impedance of the VGA core circuit is approximately  $2 \Omega$ . To optimize the matching, a  $5 \Omega$  resistor is connected in series at each differential output end. This is equivalent to the  $10 \Omega$  resistor R connected in parallel at the VGA core output, as illustrated in Fig. 1. This arrangement raises the resistance of the left-side resonator of the interstage matching network to approximately  $10 \Omega$ , simplifying the design of the interstage matching network.

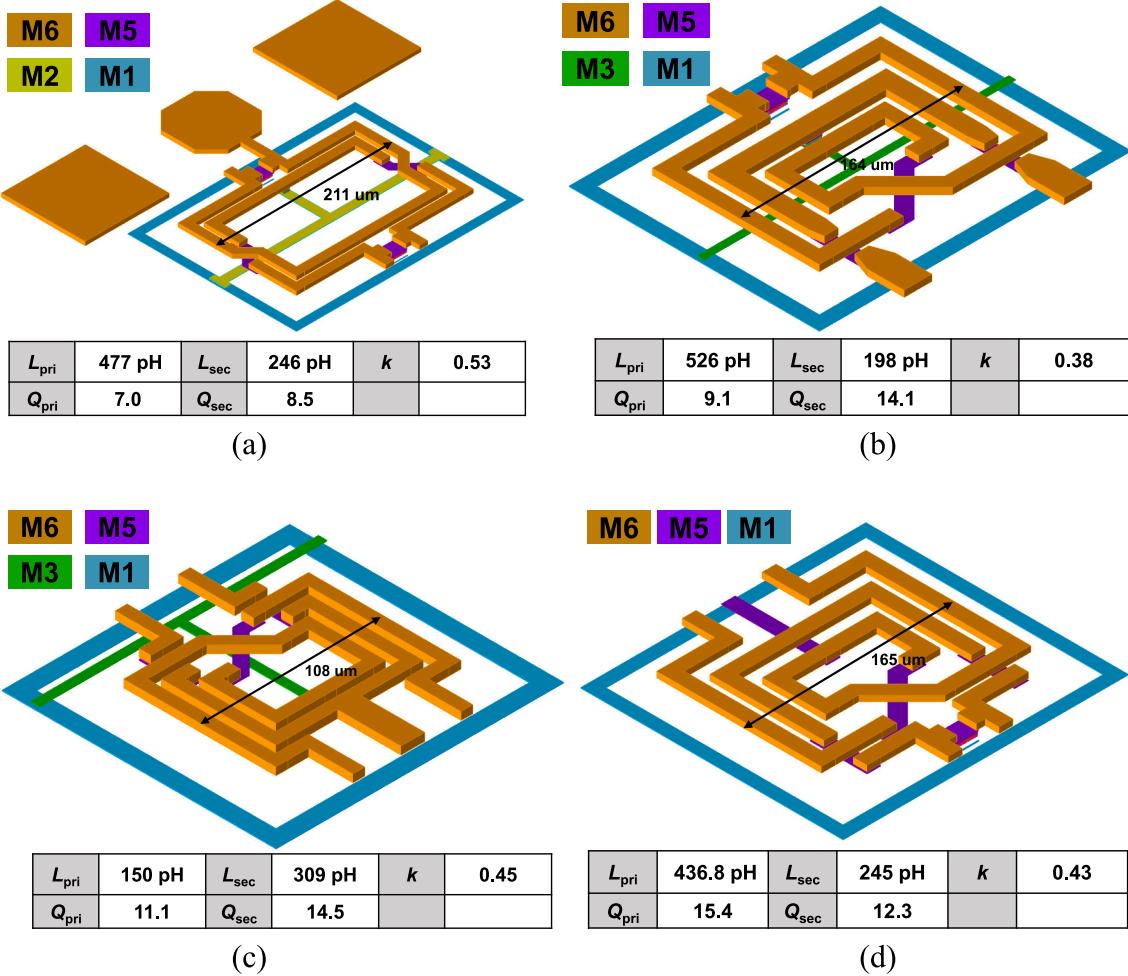
Furthermore, after cascading a  $5 \Omega$  resistor at each output end of the VGA core circuit, the simulated results of the real and imaginary parts of the output impedance and the output phase response for different gain states are shown in Fig. 5. At the center frequency of 24 GHz, the variation ranges of the absolute values of the real and imaginary parts of the output impedance are  $11.89\text{--}12.66 \Omega$  and  $32.06\text{--}32.9 \Omega$ , respectively. Within the 22–26 GHz, the fluctuation ranges of the real and imaginary parts of the output impedance are less than  $1.34 \Omega$  and  $6.29 \Omega$ , respectively. Additionally, at the center frequency of 24 GHz, the output phase response variation range at the output end is  $68.45\text{--}70.12^\circ$ , and

the fluctuation range of the output phase response is less than  $3.94^\circ$  across the 22–26 GHz. The relationship between the phase difference of different gain states and frequency variation is shown in Fig. 5(b). Within the 22–26 GHz, the phase difference is less than  $1.77^\circ$ . The relatively concentrated real and imaginary parts of the output impedance and the small fluctuation range of the output phase response within the operating band for different gain states indicate that the VGA core circuit with a symmetric topology has good output impedance and phase consistency.

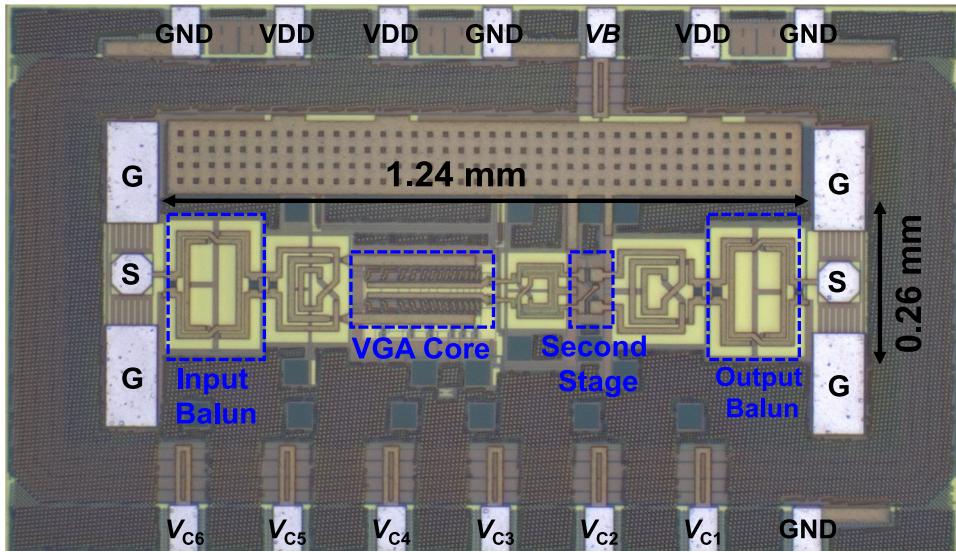
The  $G_{max}$  and phase variation response simulation results of the VGA core circuit are shown in Fig. 6. At the center frequency of 24 GHz, the  $G_{max}$  corresponding to the maximum and minimum gain states are 1.72 dB and  $-15$  dB, respectively, resulting in a gain control range of 16.72 dB. Taking the maximum gain state “111111” as the reference, the phase variation response within the 22–26 GHz is better than  $11.5^\circ$ .

#### 2.4. Transformer-based matching network

The proposed VGA incorporates a total of five transformer-based matching networks. The input and output ends utilize baluns with identical structure and parameters, as illustrated in Fig. 7(a). Notably, the GSG pad, which is an integral part of the balun, is designed and optimized in conjunction with the balun in the overall layout.



**Fig. 7.** The diagram of the 3D layout structure of the transformer-based (a)  $50 \Omega$  single-ended to  $100 \Omega$  differential balun, (b) input, (c) interstage, and (d) output matching networks for the VGA, and the values of  $L$ ,  $Q$ , and  $k$  at 24 GHz related to the transformer.



**Fig. 8.** Chip microphotograph of the 6-bit digitally controlled VGA.

Furthermore, the 3D layouts of the input matching, interstage matching, and output matching networks are depicted in Fig. 7(b), (c), and (d), respectively.

In the utilized process, only a single thick metal layer, M6, is available. To achieve the desired inductance while maintaining a high  $Q$  factor for both the primary and secondary coils, these coils are wound

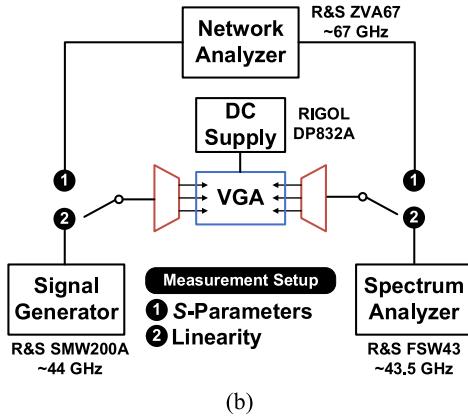
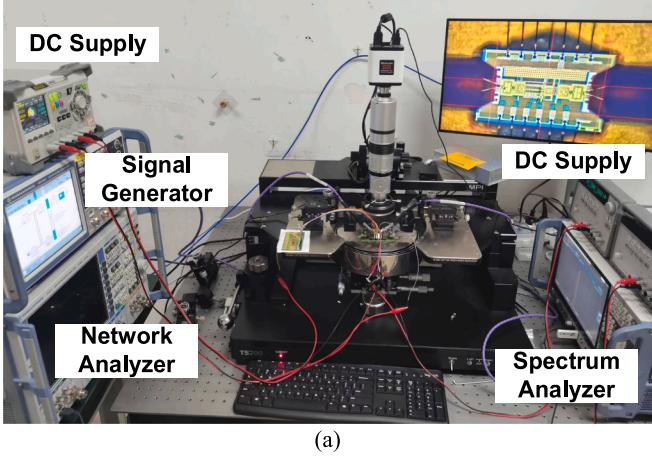


Fig. 9. Measurement (a) on-site environment and (b) setup diagram for the VGA.

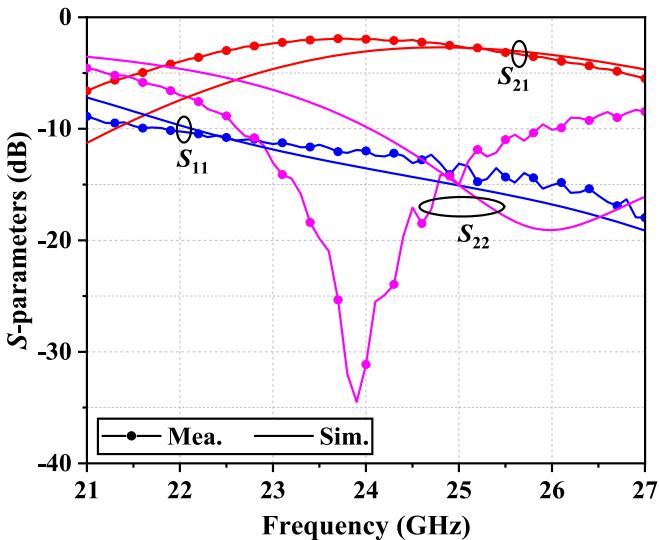


Fig. 10. Measured and simulated S-parameters at maximum gain state (111111).

using the M6 layer. The RF signal is magnetically coupled through side-by-side coupling. The crossovers of the same-layer metal are implemented using the M1-M5 metal layers. Additionally, the inductance  $L$ , quality factor  $Q$ , and coupling coefficient  $k$  of the primary and secondary coils of the four transformer-based matching networks at the center frequency of 24 GHz are indicated in Fig. 7.

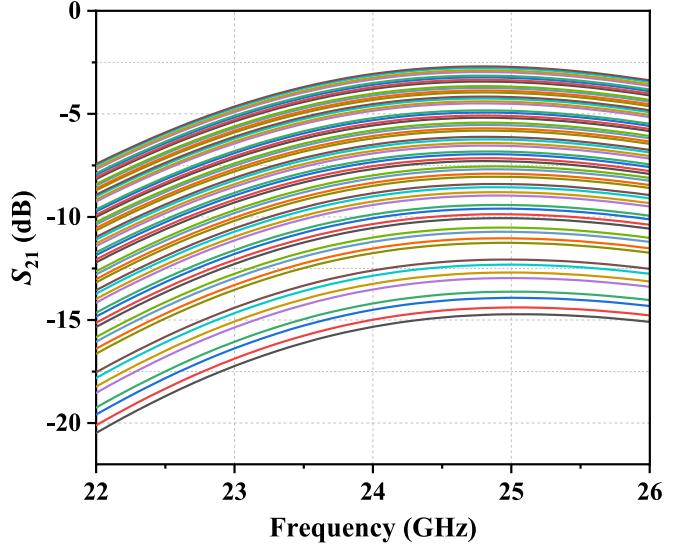


Fig. 11. Simulated  $S_{21}$  of different gain states.

### 3. Measurement results

The proposed VGA is fabricated using the 180-nm CMOS process. The microphotograph of the chip is shown in Fig. 8, with the core area of  $1.24 \times 0.26 \text{ mm}^2$  excluding the testing pad. The DC and RF pads are clearly labeled in the figure. The current consumption of the VGA is 19.27 mA from a 1.8 V supply. To characterize the VGA, S-parameter and linearity tests were conducted using a probe station equipped with MPI T26A probes. Fig. 9(a) presents the measurement on-site environment, and the instrument connections with different test configurations are illustrated in Fig. 9(b). Specifically, the S-parameter test was performed using the vector network analyzer R&S ZVA67, while the linearity test was carried out using the vector signal generator R&S SMW200A and spectrum analyzer FSW43.

The simulated and measured S-parameters for the maximum gain state "111111" are shown in Fig. 10. At the center frequency of 24 GHz, the gain control range across the 64 states is 21.47 dB, while the phase variation within the operating band of the VGA remains below  $35.24^\circ$ . However, the eight low-gain states, although contributing a gain control range of 6.1 dB, cause a phase variation degradation of  $18.76^\circ$ . This degradation significantly deteriorates the overall phase variation performance. Therefore, to strike a balance between gain control range and phase variation, the eight low-gain states ranging from "000111" to "000000" were discarded. The simulated results of  $S_{21}$  for the remaining 56 gain states are presented in Fig. 11, and the corresponding measured S-parameters are shown in Fig. 12. As illustrated in Fig. 12, at the center frequency of 24 GHz, the maximum gain for state "111111" is  $-1.97 \text{ dB}$ , and the minimum gain for state "001000" is  $-17.34 \text{ dB}$ . This results in a gain control range of 15.37 dB. The  $S_{11}$  for all 56 gain states remains below  $-10 \text{ dB}$  across the 22–26 GHz band, and the  $S_{22}$  is below  $-10 \text{ dB}$  across the 22.6–25.8 GHz band and better than  $-7 \text{ dB}$  over the entire 22–26 GHz band. It is important to note that, compared with the simulated  $S_{21}$  results shown in Fig. 11, the measured  $S_{21}$  results shown in Fig. 12(a) exhibit two distinct gain discontinuities. These discontinuities may be attributed to several factors, including the reduced accuracy of the active device models in the process library beyond 20 GHz, unavoidable process corner variations during fabrication, and the nonideal characteristics of the DC power supply.

Taking the maximum gain state "111111" of  $S_{21}$  as the reference, the measured phase variation across the 56 gain states is illustrated in Fig. 13. Within the 22–26 GHz, the phase variation remains below  $16.48^\circ$ . Moreover, the nonlinearity of VGA was evaluated by varying the input power applied to the VGA input port and measuring the output

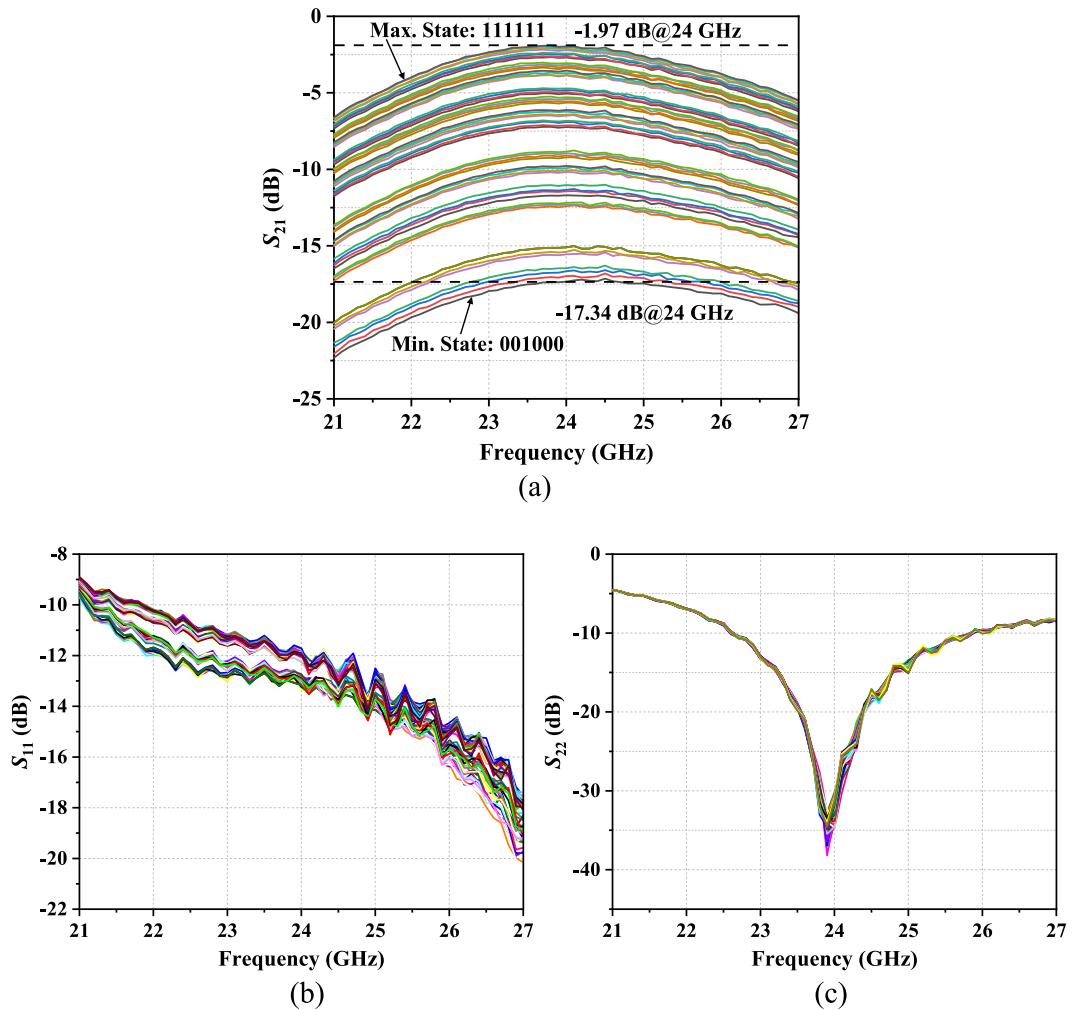


Fig. 12. Measured S-parameters of different gain states: (a)  $S_{21}$ , (b)  $S_{11}$ , and (c)  $S_{22}$ .

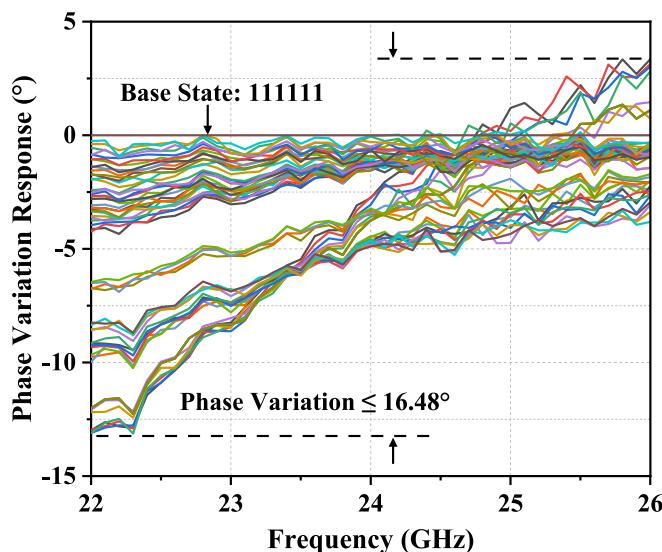


Fig. 13. Measured phase variation responses of different gain states.

power at the VGA output port using the spectrum analyzer. The input and output 1-dB compression points ( $IP_{1dB}$  and  $OP_{1dB}$ ) of the VGA in the maximum gain state are shown in Fig. 14. Within the 22–26 GHz, the

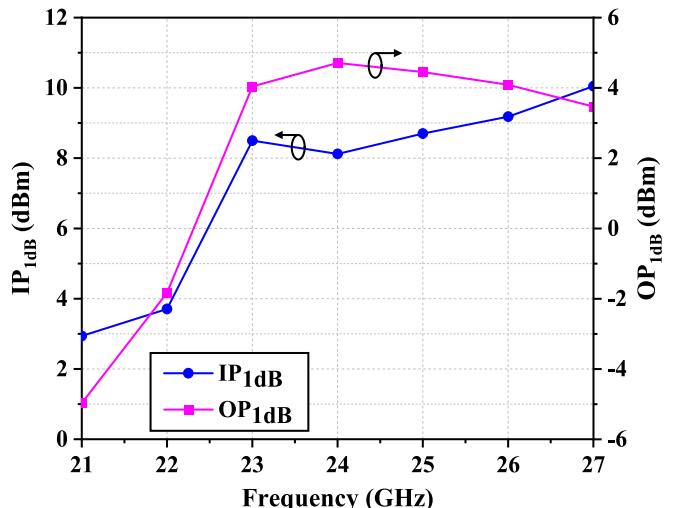


Fig. 14. Measured (a) input and (b) output 1-dB compression point versus frequency.

$IP_{1dB}$  is higher than 3.71 dBm, and the  $OP_{1dB}$  is higher than -1.83 dBm. Specifically, within the 23–26 GHz, the  $IP_{1dB}$  and  $OP_{1dB}$  are better than 8.1 dBm and 4 dBm, respectively. Additionally, the performance comparison between the proposed VGA and other VGAs is shown in Table 1.

**Table 1**

Performance comparison with previous VGAs.

Refs.	Tech.	Freq. (GHz)	Max. Gain (dB)	$\Delta$ Gain (dB)	$\Delta\varphi$ (°)	P <sub>DC</sub> (mW)	OP1dB* (dBm)	Chip size (mm <sup>2</sup> )	Structure (Single-ended/Diff.)
[15]	65-nm CMOS	38–40	22	16	3.18*	38	2.5	0.37	Single-ended
[18]	65-nm CMOS	27–43	16.3	8.4	< 5	27.6	N/A	0.25	Single-ended
[19]	40-nm CMOS	6–15.3	−1.7	15.5	< 9.5#	18.4–29.6	N/A	0.075	Single-ended
[21]	65-nm CMOS	27–42	9.6	7.8	< 3.5	15.6	2.5	0.08	Diff.
[23]	65-nm CMOS	30.5–39	−0.2**	16	< 4.9	15.6	−2.2	0.08	Diff.
This Work	180-nm CMOS	22–26	−1.97	15.37	≤16.48	34.7	4.71	0.32	Diff.

\* Measured at center frequency. \*\* : Except the loss of balun. #: Estimated from the figure.

The typical supply voltage for the 180-nm CMOS process used in this work is 1.8 V. This process has a limited cutoff frequency, and the intrinsic gain decreases at high frequency. To compensate for this and maintain the gain, the second-stage circuit is added and consumes an additional current of 6.16 mA. Compared with other VGAs in Table 1, these factors together contribute to the relatively high power consumption of the VGA in this paper.

#### 4. Conclusion

In this paper, a two-stage differential VGA operating in the 22–26 GHz is presented. A six-unit current-steering structure with progressively increasing transistor sizes is employed to achieve 6-bit digital gain control. Transformer-based matching networks are integrated into the VGA design to minimize the layout area while maintaining high performance. Moreover, the VGA was fabricated and measured for S-parameters and linearity. The measured results demonstrate that within the 22–26 GHz, the 56 gain states ranging from “001000” to “111111” achieve a gain control range of 15.37 dB.

#### CRediT authorship contribution statement

**Shuchen Zhen:** Writing – original draft, Conceptualization. **Yongle Wu:** Resources, Project administration, Funding acquisition. **Zhuoyin Chen:** Writing – review & editing, Data curation. **Xiaopan Chen:** Writing – review & editing, Validation. **Weimin Wang:** Resources, Funding acquisition.

#### Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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#### Data availability

The authors do not have permission to share data.

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