A Novel IPD-Based Dual-Band Filtering Power Divider Chip Across X-Band and K-Band

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***Abstract*—This letter presents a compact dual-band filtering power divider (DBFPD) based on a novel dual-π-type matching circuit (MC). The proposed dual-π-type MC achieves precise dual-band matching through analytical design, and integrated hybrid resonators (HRs) significantly enhance the bandwidth of passbands. Three independently controllable transmission zeros (TZs) of DBFPD improve stopband rejection and frequency selectivity. To validate the design, a DBFPD working at 8.9 and 21.6 GHz with a compact size of 1.9 $\times$ 3.1 mm^2 is fabricated and measured using integrated passive device (IPD). The design achieves low insertion loss (IL) and wide bandwidth, with minimum ILs of 0.43 and 0.47 dB and 3-dB bandwidths of 50% and 33.5%, respectively.**

***Index Terms*—Dual-π-type matching circuit (MC), dual-band filtering power divider (DBFPD), integrated passive device (IPD), low insertion loss (IL), wide bandwidth.**

I. Introduction

With the rapid development of wireless communication technologies, the space of radio frequency (RF) chips is being continuously shrinking. As key RF front-end components, filters select frequencies while power dividers (PDs) split power. To meet demands for high integration and performance, filtering PDs have become a research hot spot. In modern 5G networks and satellite communications, scarce spectrum resources and large frequency gaps between key bands impose rigorous requirements on dual-band filtering PDs (DBFPDs) working across common bands. The diagram of the DBFPD and the equivalent circuit structure is shown in Fig. 1.

At present, the implementation of PDs is primarily fabricated based on processes, such as printed circuit board (PCB) [1], [2], [3], [4], low-temperature co-fired ceramic (LTCC) [5], [6], [7], complementary metal-oxide–semiconductor (CMOS) [8], [9], [10], and integrated passive device (IPD) [11], [12], [13]. In [1] and [3], two types of DBFPD are designed based on coupled lines. However, they lack transmission zeros (TZs) between the two passbands, resulting in poor roll-off rates. Additionally, their working frequencies are below 10 GHz, and sizes are relatively large. In [4], a DBFPD based on a single substrate integrated waveguide cavity is proposed, but the insertion losses (ILs) require improvement. In [5], a miniaturized dual-band PD is realized by replacing distributed element with lumped element, making it more suitable for LTCC implementation. However, the bandwidths of the design remain relatively narrow. In [9], a wideband millimeter-wave dual-band PD is proposed using the inverted spiral-coupled line. In [12], a dual-band PD based on a novel bridged-T coil, which can be equivalent to two distinct transmission lines, is reported. Unfortunately, it is regrettable that the design of dual-band PDs with filtering function using chip fabrication processes is quite rare.

Fig. 1. Diagram of the DBFPD and the equivalent circuit structure.

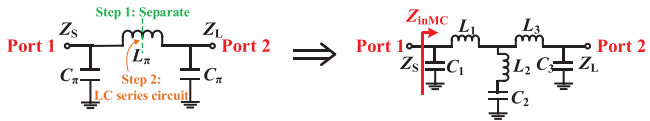

Fig. 2. Design procedure of the proposed dual-π-type MC. (a) Traditional π-type MC. (b) Dual-π-type MC.

In this letter, a novel dual-π-type matching circuit (MC) that achieves impedance matching at two defined frequencies in distinct bands is proposed. To expand bandwidths, hybrid resonators (HRs) are innovatively incorporated to introduce a transmission pole (TP) for each matched band. Simultaneously, three independently controllable TZs are realized, greatly improving frequency selectivity and stopband suppression. A high-performance DBFPD with tunable center frequencies (CFs) is designed. To the best of our knowledge, the DBFPD chip featuring low IL, wide bandwidth, and ultrawide stopband suppression across bands is proposed for the first time.

II. Design Theory

Fig. 2 illustrates the design procedure of the novel dual-π-type MC. Two independently tunable matching frequencies f_1 and f_2 are obtained, as shown in Fig. 3. For the MC, $Z_S = 2Z_L = 2Z_0$. The matching condition of dual-π-type MC is satisfied at f_1 and f_2 when the input impedance $Z_{\text{inMC}} = Z_S$.

Z_{inMC} is expressed as follows:

$$Z_{\text{inMC}} = \frac{j\left(M + 2\pi f_i L_1 N\right)}{-N + 2\pi f_i C_1 \left(M + 2\pi f_i L_1 N\right)} \left(f_i = f_1 \text{ or } f_2\right) \tag{1}$$

where

$$\begin{cases} M = \left(-1 + (2\pi f_i)^2 C_2 L_2\right)\left(-Z_L + 2\pi f_i L_3 P\right) \\ N = -P + 2\pi f_i C_2 \left(-Z_L + 2\pi f_i \left(L_2 + L_3\right) P\right) \\ P = -j + 2\pi f_i C_3 Z_L. \end{cases} \tag{2}$$

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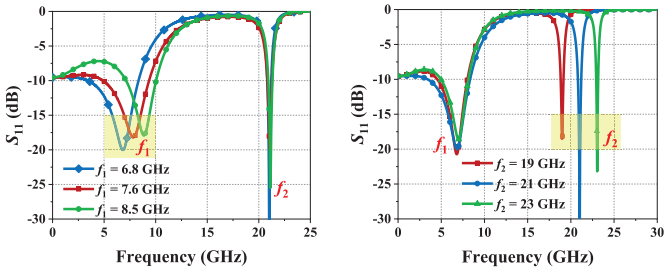

Fig. 3. Simulated results of independent tuning for matching frequencies (a) f_1 and (b) f_2.

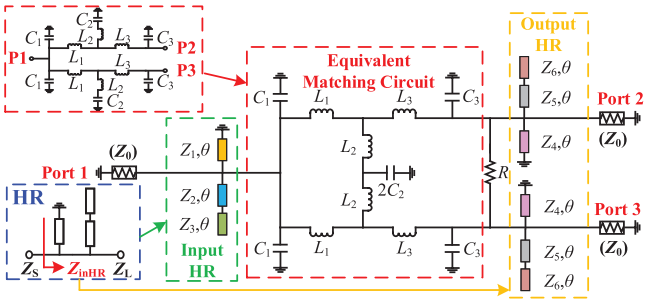

Fig. 4. Circuit schematic of the proposed DBFPD.

In addition, the S-parameters of the proposed MC are illustrated in (3) [14], [15]. When $Z_{\text{in}} = Z_{\text{inMC}}$ and $S_{21} = 0$, a TZ is calculated as (4). The TZ_{MC} is generated by the L_2C_2 series circuit

$$S_{11} = (Z_{\text{in}} - Z_S)/(Z_{\text{in}} + Z_S), \quad |S_{21}| = \sqrt{1 - |S_{11}|^2}. \tag{3}$$

$$f_{\text{TZMC}} = 1/\left(2\pi\sqrt{L_2C_2}\right). \tag{4}$$

To analytically design the dual-π-type MC, a critical constraint condition is presented in (5). Therefore, the parameters of components can be calculated by (1), (4), and (5) to achieve target f_1, f_2, and TZ_{MC}

$$\sqrt{1/(L_1C_1)} + \sqrt{1/(L_3C_3)} = 2\pi(f_1 + f_2). \tag{5}$$

The HR is implemented by a cascade connection of a shorted stub and a stepped-impedance stub, as shown in Fig. 4. For the HR, $Z_S = Z_L = Z_0$. The input impedances of HRs that connect the input and output port are presented as follows:

$$Z_{\text{inHR-In}} = 1 \Bigg/ \left(\frac{1}{Z_L} - \frac{j\cot\theta}{Z_1} - \frac{j\cot\theta\,(Z_2 + Z_3)}{Z_2\left(Z_2 - (\cot\theta)^2 Z_3\right)}\right) \tag{6a}$$

$$Z_{\text{inHR-Out}} = 1 \Bigg/ \left(\frac{1}{Z_L} - \frac{j\cot\theta}{Z_4} - \frac{j\cot\theta\,(Z_5 + Z_6)}{Z_5\left(Z_5 - (\cot\theta)^2 Z_6\right)}\right). \tag{6b}$$

The TZs are derived when $Z_{\text{inHR-In}} = 0$ or $Z_{\text{inHR-Out}} = 0$, with $f_{\text{TZHR1}} = 0$ and the remaining two TZs defined by (7). The result shows that TZ_{HR1} is generated by shorted stub, while TZ_{HR2} and TZ_{HR3} are related to stepped-impedance stubs

$$f_{\text{TZHR2}} = \frac{f_0 arc\cot\left(\sqrt{Z_2/Z_3}\right)}{\theta}$$

$$f_{\text{TZHR3}} = \frac{f_0 arc\cot\left(\sqrt{Z_5/Z_6}\right)}{\theta}. \tag{7}$$

To simplify the circuit, the dual-π-type MCs on two branches are equivalent to a combined structure. The circuit schematic of the designed DBFPD is presented in Fig. 4. It consists of an equivalent MC, the HRs connecting the input and output ports, and an isolation resistor R. As shown in Fig. 5, the MC creates dual-band matching, each containing one TP, but exhibits narrow bandwidth at high frequencies due to lumped-element limitations. The microstrip-based input and output HRs introduce an additional TP per band through coupling of the distributed element, significantly broadening the bandwidth of the second band, and the TZs enhance passband selectivity and stopband rejection. Finally, the design methodology of the DBFPD is summarized in Fig. 6.

Additionally, the tunable matching frequencies of MC and three independent TZs enable the DBFPD to achieve different CFs with excellent performance. The ideal simulated results of the two passbands changing independently are shown in Fig. 7.

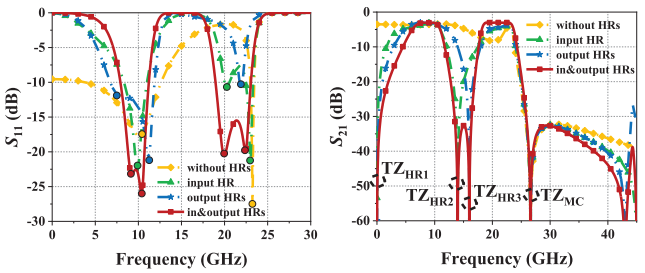

Fig. 5. Simulated comparison of (a) S_{11} and (b) S_{21} for: 1) MC only, 2) MC with input HR, 3) MC with output HR, and 4) MC with input and output HRs.

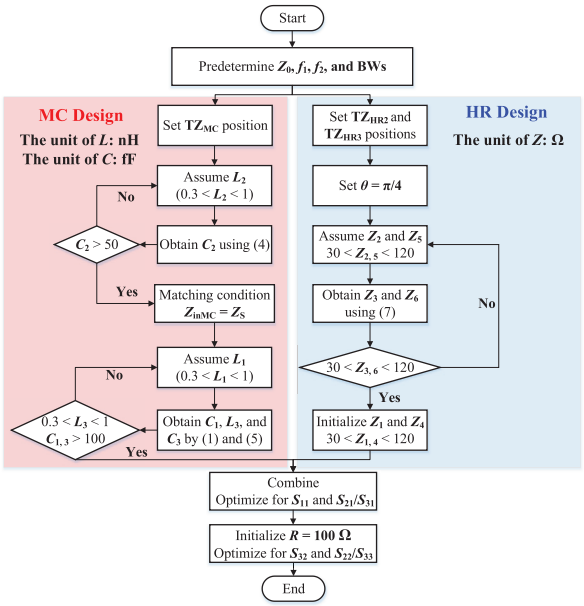

Fig. 6. Design flowchart of the proposed DBFPD.

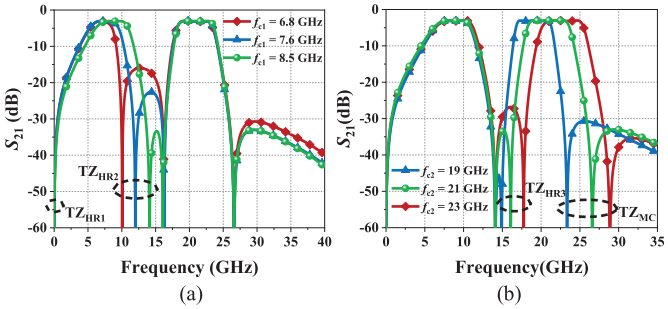

Fig. 7. Simulated results of independent tuning for (a) passband 1 and (b) passband 2.

TABLE I
PERFORMANCE COMPARISON FOR SOME DUAL-BAND PDS

Ref.	f_0 (GHz)	IL (dB)	RL (dB)	In-band Iso.	Filtering	15-dB FBW (%)	HS	Size (mm^2)	Process
[1]	4.1/6.6	0.80/1.80	> 17.3	> 17.0/26.0	Yes	1.2/0.9*	No	20.0 × 13.0	PCB Microstrip
[2]	2.6/5.7	0.60/1.20	> 16.0/16.0	> 21.0/17.0	Yes	7.3/4.9*	No	30.0 × 30.0	PCB Patch
[3]	2.4/3.8	1.23/0.94*	> 17.2	> 15.0	Yes	21.8/13.2*	No	34.4 × 34.9	PCB Microstrip
[4]	11.2/13.7	1.40/2.20	17.8/18.4	> 16.1	Yes	4.5/2.9*	No	23.2 × 20.9	PCB SIW
[5]	1.2/1.6	0.40/0.80	23.6/29.8	20.2/29.8	No	10.8/2.9*	No	6.2 × 3.9	LTCC
[12]	2.4/5.5	0.81/0.81	26.8/26.1	22.9/23.6	No	53.6/17.7	No	1.8 × 1.7	Silicon-based IPD
[13]	28.0/60.0	0.90/0.90	34.0/18.0	19.0/24.0	No	20.4/20.3	No	0.7 × 0.7	GaAs-based IPD
This work	**8.9/21.6**	**0.43/0.47**	**> 21.0/16.5**	**> 10.0**	**Yes**	**27.8/21.5**	**Yes**	**1.9 × 3.1**	**GaAs-based IPD**

***: Estimated value**

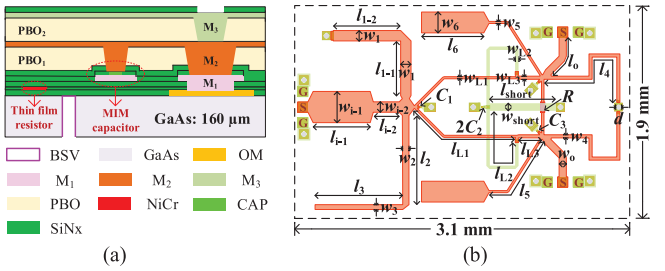

Fig. 8. (a) Layer structure of the used IPD technology. (b) Planar layout of the proposed DBFPD.

III. EXPERIMENTAL VALIDATION

To verify the validity of the designed DBFPD, the layout is simulated in ADS. The layer information of the IPD technology is shown in Fig. 8(a). The substrate uses 160-μm-thick GaAs with a dielectric constant of 12.9. Three metal layers (M_1–M_3) are made of gold with thicknesses of 1, 4, and 4 μm. Spiral inductors and transmission lines can be constructed on any metal layer. The MIM capacitors are formed by M_1, M_2, CAP, and the dielectric between them. The material of the thin-film resistance is NiCr in PDK.

The layout is presented in Fig. 8(b). M_1 serves as the main routing layer (orange) and M_3 serves as the overlap layer (green). Microstrip inductance is the most suitable implementation due to the small values of inductances in the circuit. The value of L_2 exceeds the theoretical value due to constraints of routing in layout, reducing the frequency of TZ_{MC} according to (4). The shorted stub between two L_2 provides equivalent negative inductance to compensate, preserving TZ_{MC} at the designated value. The size of the final layout is 1.9×3.1 mm^2 including pads, and the electrical size is $0.094 \times 0.153\ \lambda_0^2$. The specific dimensions are (units: μm): $w_{i-1} = 300$, $l_{i-1} = 550$, $w_{i-2} = 100$, $l_{i-2} = 250$, $w_1 = 100$, $l_{1-1} = 525$, $l_{1-2} = 650$, $w_2 = 60$, $l_2 = 858$, $w_3 = 46.5$, $l_3 = 845$, $w_4 = 30$, $l_4 = 1356.74$, $w_5 = 20$, $l_5 = 791.8$, $w_6 = 200$, $l_6 = 600$, $w_{L1} = 20$, $l_{L1} = 1090.4$, $w_{L2} = 30$, $l_{L2} = 1049.45$, $w_{L3} = 30$, $l_{L3} = 202.4$, $w_{\text{short}} = 70$, $l_{\text{short}} = 639$, $w_o = 70$, $l_o = 418.9$, and $d = 50$.

The proposed DBFPD is fabricated and measured, and the comparison between theoretical, simulated, and measured results is shown in Fig. 9, demonstrating excellent agreement. The measured results demonstrate that CFs of the passbands are 8.9 and 21.6 GHz. The 3-dB fractional bandwidths (FBWs) are 50% and 33.5%, and 15-dB FBWs are 27.8% and 21.5%. The minimum ILs are 0.43 and 0.47 dB (excluding the original 3 dB), and return losses (RLs) are better than 21 and 16.5 dB. The interpassband rejection is better than 22 dB, and the ultrawide out-of-band rejection is realized. The in-band isolation remains better than 10 dB. The measured amplitude/phase

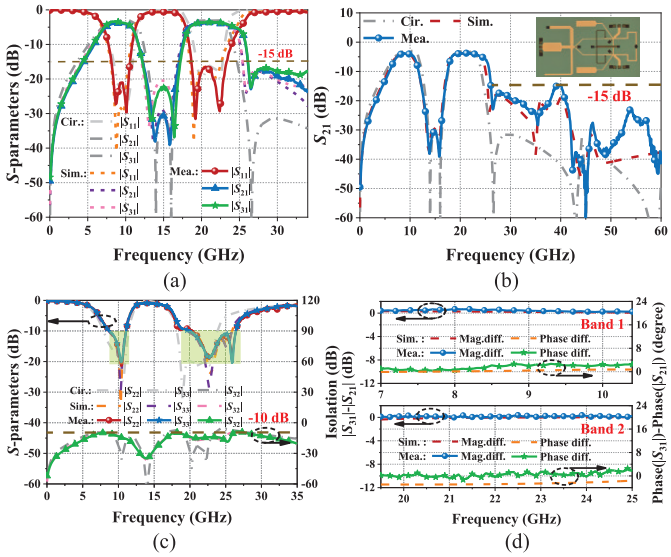

Fig. 9. Theoretical, simulated, and measured results of the proposed DBFPD (a) Input return loss and insertion losses. (b) Insertion loss from 0 to 60 GHz. (c) Output return losses and isolation. (d) Amplitude and phase imbalances. (L_1 = 0.64 nH, L_2 = 0.6 nH, L_3 = 0.5 nH, C_1 = 212.3 fF, C_2 = 60 fF, C_3 = 169.6 fF, Z_1 = 70 Ω, Z_2 = 60 Ω, Z_3 = 78.4 Ω, Z_4 = 100 Ω, Z_5 = 120 Ω, Z_6 = 102 Ω, Z_0 = 50 Ω, R = 100 Ω, θ = 45°, f_{c1} = 9.0 GHz, and f_{c2} = 21 GHz).

imbalances at CFs of the two passbands are 0.46 dB/2.463° and 0.29 dB/0.004°.

Table I shows the performance comparison between this design and previously reported dual-band PDs. Compared with PCB-based designs, our design is characterized by wideband and compact. Compared with PD chips, the proposed DBFPD integrates cross-band and filtering functions. Furthermore, the low ILs and ultrawide harmonic suppression (HS) enhance the competitive advantage.

IV. CONCLUSION

In this letter, a novel dual-π-type MC is proposed, and through co-design with HRs, a DBFPD operating across X-band and K-band is designed. The rigorous design methodology is presented. A prototype based on IPD working at 8.9 and 21.6 GHz is fabricated and measured. The results demonstrate the following advantages: 1) cross-band; 2) filtering response; 3) low ILs; 4) wideband; and 5) ultrawide out-of-band HS. The proposed DBFPD provides a pioneering IPD solution for multiband device in satellite communication systems.

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