Best Practices for PCB Design for World Skills Competitors

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Introduction:

There are many best practices that companies and individuals follow when designing PCBs (Printed Circuit Boards). We have researched best practices related to PCB layout and have compiled them here to help Experts train their competitors and during judging at the competition.

World Skills competitors are not considered to be experts in multi-layer high frequency PCB design and as such these guidelines will focus on best practices to minimize noise radiation and reception and ease manufacture of circuits.

These best practices apply to single- and two-layer PCB designs prototyped on a PCB Milling Machine. It is important to note that the techniques applied to PCBs manufactured by professional PCB factories may be very different from techniques needed when prototyping a milled board.

At the competition, if milled boards will be created, techniques that are used should favour creating milled boards. This means spacing between traces may be larger than spacing used for factory produced boards. PCBs may need keep out areas so that the likelihood of shorts will be minimized. And Competitors should try to minimize the amount of rubout areas needed

Otherwise, if possible, competitors should layout their boards as if they would be professionally manufactured. If there is a conflict choosing a technique that favours manufactured boards or milled prototype boards, the Competitor should choose the technique that favours milled prototype.

While we do not expect Competitors to know multi-layer high frequency layout and EMC reduction techniques, we do expect they will follow these guidelines that minimize EMC radiation.

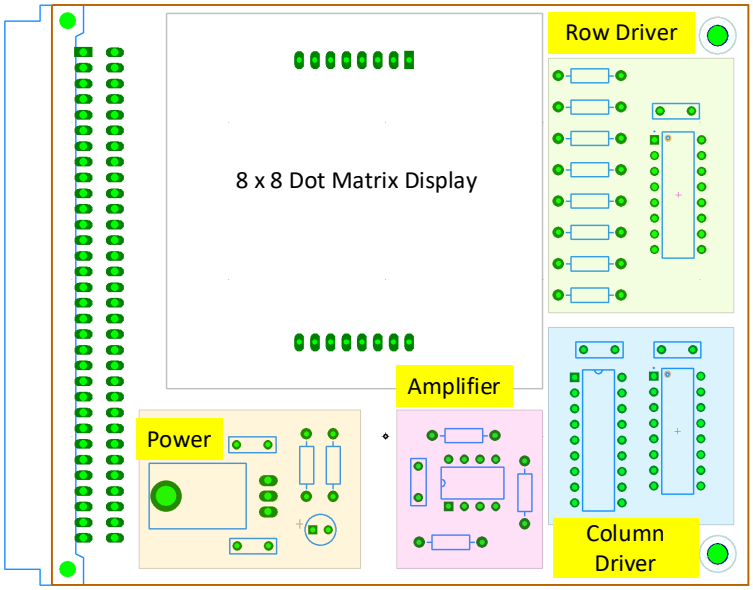
Best Practices

1. Ideally on mixed PCBs all SMD components should be placed on the Bottom layer and all TH components should be placed on the Top layer.

Power supply and other high current traces should be larger than signal traces. The rails should at a minimum be able to handle the current through them according to IPC-2152. A good guideline is:

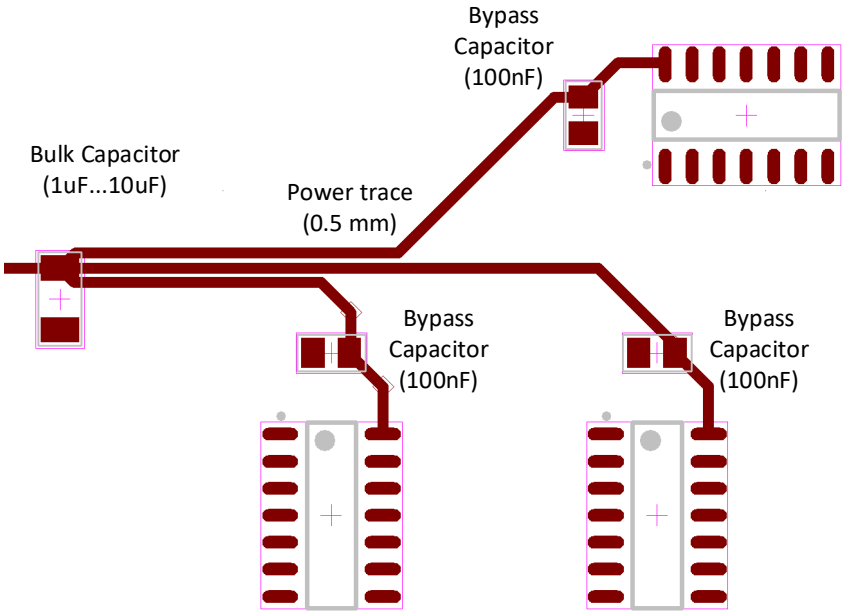
10 mils (about 0.25 mm)	0.3 Amps
16 mils (about 0.4 mm)	0.4 Amps
20 mils (about 0.5 mm)	0.7 Amps
24 mils (about 0.6 mm)	1.0 Amps
50 mils (about 1.3 mm)	2.0 Amps
100 mils (about 2.5 mm)	4.0 Amps
150 mils (about 4 mm)	6.0 Amps

2. Clearance between pads / traces ground planes must be at least 10 mils (about 0.25 mm)
3. Signal traces should be as short as possible.
4. When beginning any layout, the components that must be in a precise location have to be placed first. For example: mounting holes, switches, LEDs and displays.
5. Make sure that temperature sensitive devices (like Electrolytic caps, temperature sensors) are separated from heat producing components.
6. Next, components should be grouped together in a logical way by function. Poor grouping results in long traces, difficulty in routing and a poor PC board.



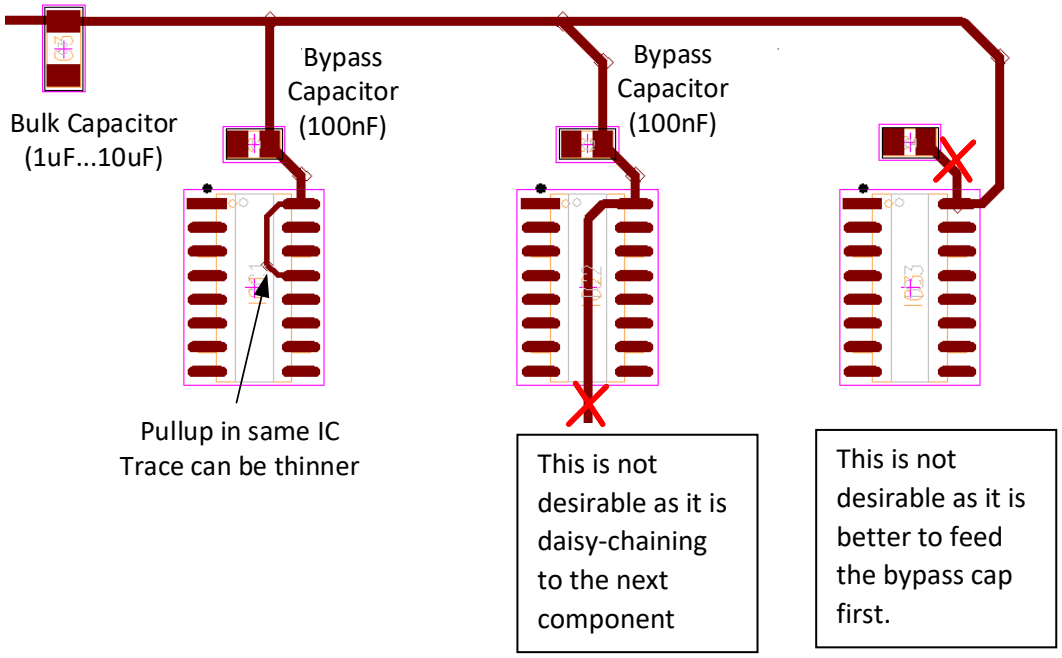
7. Try to separate areas that produce strong EM fields from circuits that may be sensitive to them.

8. Ideally, avoid daisy-chaining grounds and supply rails. Instead try to radiate power outwards from a central

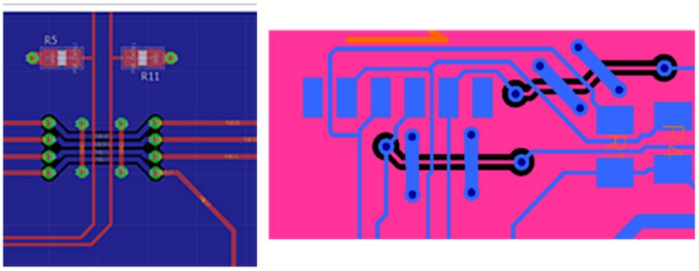


single point.

However, with single layer PCBs it isn't usually possible to do that way. We can accept stubs from a power rail.



9. Bypass capacitors need to be as close as possible to the corresponding power pins. (both power and ground)
10. Use a ground plane to minimize noise radiation.
11. If you have to make an opening in a ground plane make it as small as possible. If you need to route on the ground layer, add ground return paths over the gap beside the routed signals.



From: [Seven Habits of Successful 2-layer Board Designers | 2019-04-08 | Signal Integrity Journal]

12. Only route digital signals or less sensitive signals in ground plane gaps.
13. Filling layer 1 with ground plane pours only helps if you connect them to ground! Be careful floating islands of copper will radiate a lot of noise. This means competitors should use vias to ground stitch top and bottom ground planes.
14. Noisy, poorly designed ICs should have a ground plane underneath them to contain their fields.
15. Sometimes it is better to keep analog and digital grounds separate and connect them later at one point.

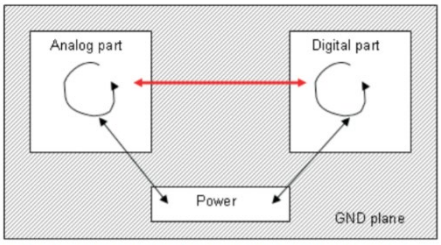
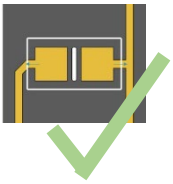
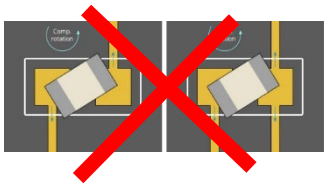


Figure 9. Good Placement of Different Functional Blocks Without the Need of a Split Ground Plane

16. Above 20 kHz, it is not necessary to isolate analog and digital grounds **IF** the respective signals are separated by a distance > 20H where H is the the height (or thickness) of the PCB.
17. Below 20kHz, grounds can be isolated to separate analog and digital sections if desired.
18. Strive to give both side of component pads the same thermal load to minimize tombstoning and misaligned components.





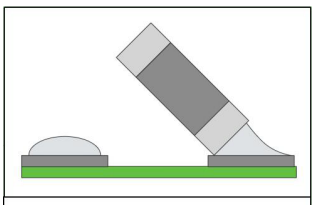
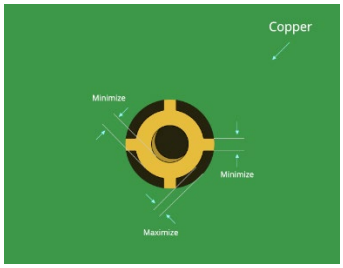


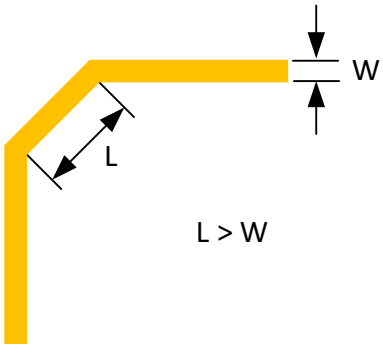
Figure 4 – Tombstoning

19. Use thermal reliefs for connections to large copper areas.

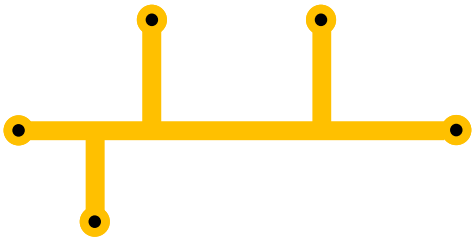


20. Use mitred or rounded corners so noise is minimized. (Does not apply to T intersections).

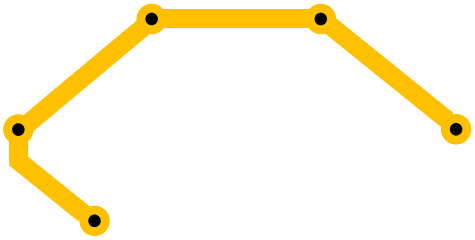
Sharp angle can cause noise injection into other tracks on the PCB. Therefore, all corners should be rounded or mitred (angled) by 45 deg.



Avoid stubs with tracks carrying high frequency and sensitive signals (low voltage) because stubs produce reflections. Power lines stub are OK.

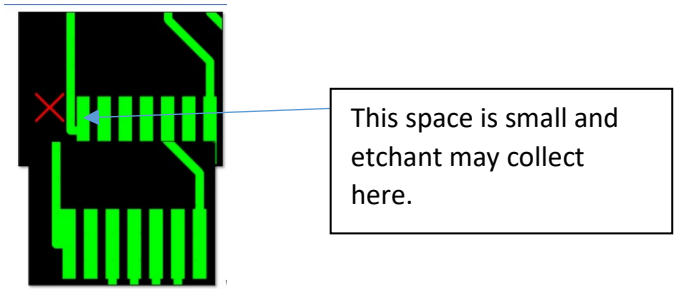


Connection via stub lines



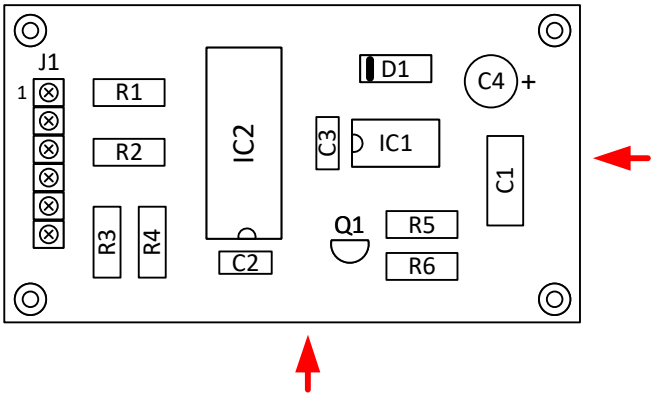
Connection via continuous trace

21. Avoid acid traps

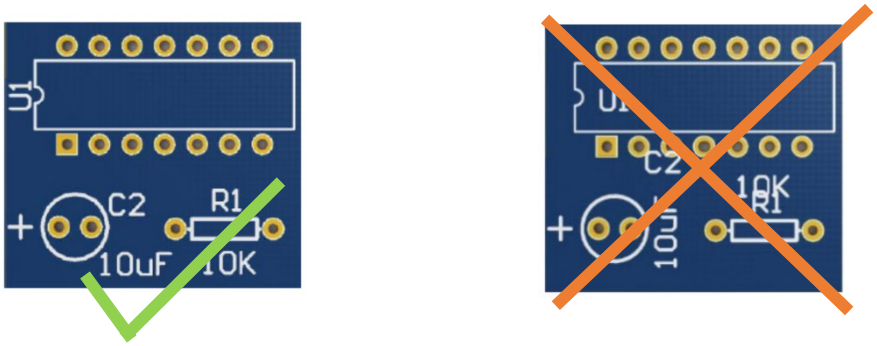


22. Run traces vertically on one layer and horizontally on the other.
23. While we cannot produce a silk screen layer on our milled boards, Competitors should ensure reference designators and other needed information is present in the assembly documentation. All text should be in the same direction, ideally. There may be times where space does not permit this, and in this case the competitor should place the designation in a location that most clearly identifies where the component is located, or other important information related to the component.

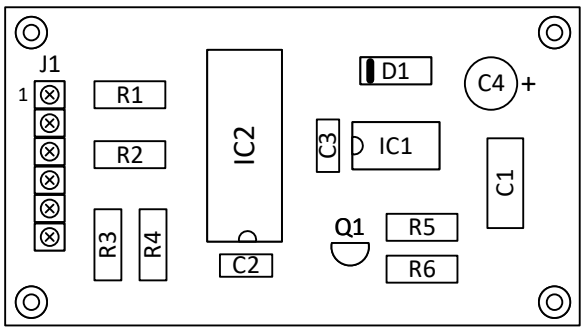
Text should be readable in two directions only.



24. There should be no overlap of text onto other text or outlines.



25. Polarized or Orientation Component Marking
Components that have a polarity should be marked on the assembly documentation. Non-polarized components should also be indicated through markings on the assembly.



Notice that D1 and C4 show markings that indicate polarization. ICs show markings indicating orientation.

Resistors have no marking indicating orientation or polarization.

26. Do not place jumpers under components.
27. Route signals and power on layer 1 and keep layer 2 ground.

References:

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EMC at component and PCB level, Martin O'Hara
Seven Habits of Successful 2-layer Board Designers | 2019-04-08 | Signal Integrity Journal