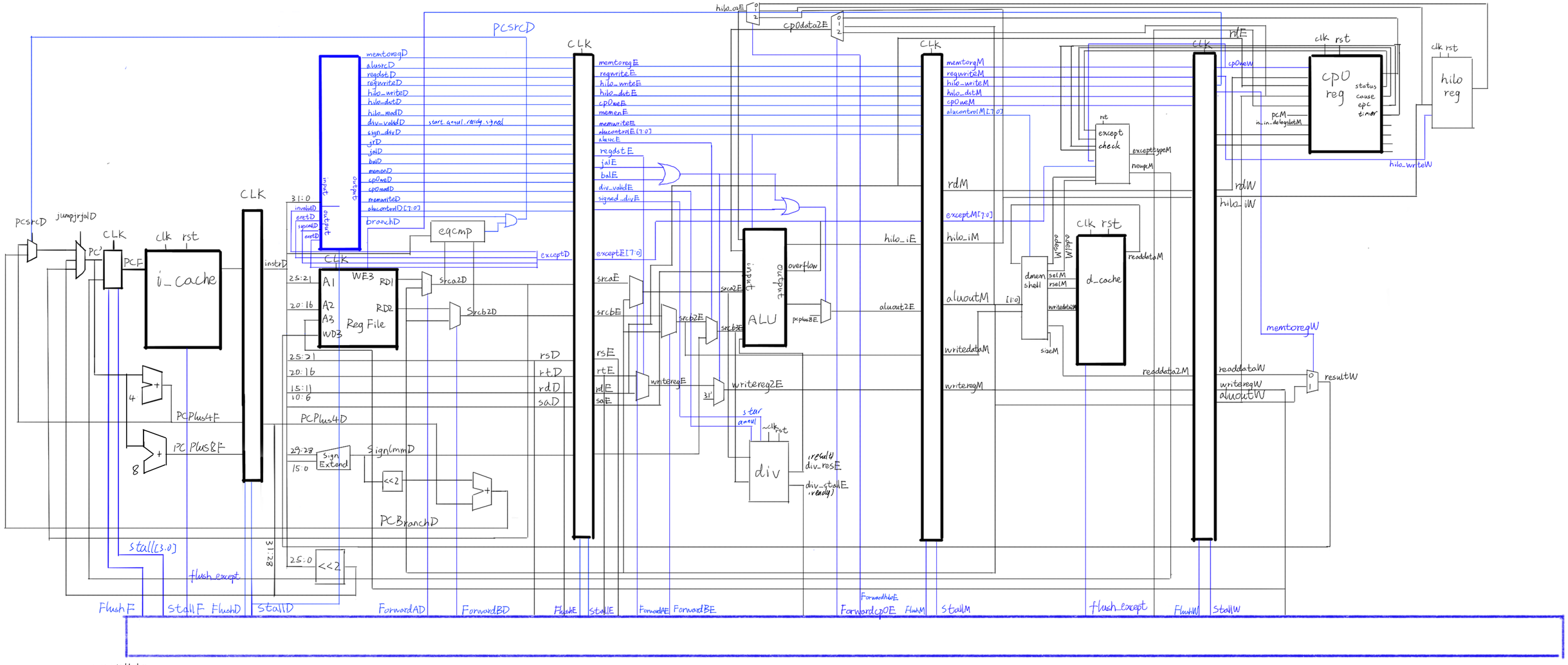
pcsrcD
jumpjrjalD
PC'
PCF
CLK
clk rst
i_cache
instrD
PCPlus4F
PCPlus8F
4
8
stall[3:0]
flush_except
FlushF
StallF
FlushD
StallD
31:0
invalidD
eretD
syscallD
eretD
instr
output
opcode
memtoregD
alusrcD
regdstD
regwriteD
hilo_writeD
hilo_dstD
hilo_readD
div_validD
sign_divD
jrD
jalD
balD
memenD
cp0weD
cp0readD
memwriteD
alucontrolD[7:0]
branchD
start, annul, ready, signed
eqcmp
exceptD
A1
A2
A3
WD3
WE3
RD1
RD2
Reg File
srcaD
srcbD
25:21
20:16
15:11
10:6
rsD
rtD
rdD
saD
PCPlus4D
29:28
15:0
Sign Extend
signImmD
<<2
PCBranchD
31:28
25:0
memtoregE
regwriteE
hilo_writeE
hilo_dstE
cp0weE
memenE
memwriteE
alucontrolE[7:0]
alusrcE
regdstE
jalE
balE
div_validE
signed_divE
exceptE[7:0]
srcaE
srcbE
rsE
rtE
rdE
saE
writeregE
srcaE
srcbE
srcbE
writeregE
31'
writeregE
hilo_oE
cp0dataE
overflow
input
output
ALU
pcplus8E
star
annul
~clk rst
div
result
div_resE
div_stallE
ready
memtoregM
regwriteM
hilo_writeM
hilo_dstM
cp0weM
alucontrolM[7:0]
rdM
exceptM[7:0]
hilo_iM
aluoutM
writedataM
writeregM
hilo_iE
aluout2E
rst
except check
exceptypeM
newpcM
pcM
in_in_delayslotM
cp0weM
rdE
clk rst
cpU reg
status
cause
epc
timer
hilo_writeW
clk rst
hilo reg
rdW
hilo_iW
clk rst
d_cache
readdataM
readdata2M
dmem shell
selM
rselM
writedata2M
sizeM
opcodeM
WMopcodeM
[1:0]
memtoregW
readdataW
writeregW
aluoutW
resultW
ForwardAD
ForwardBD
FlushE
StallE
ForwardAE
ForwardBE
ForwardhioE
ForwardcpOE
FlushM
StallM
flush_except
FlushW
StallW

注:信号结构体定义