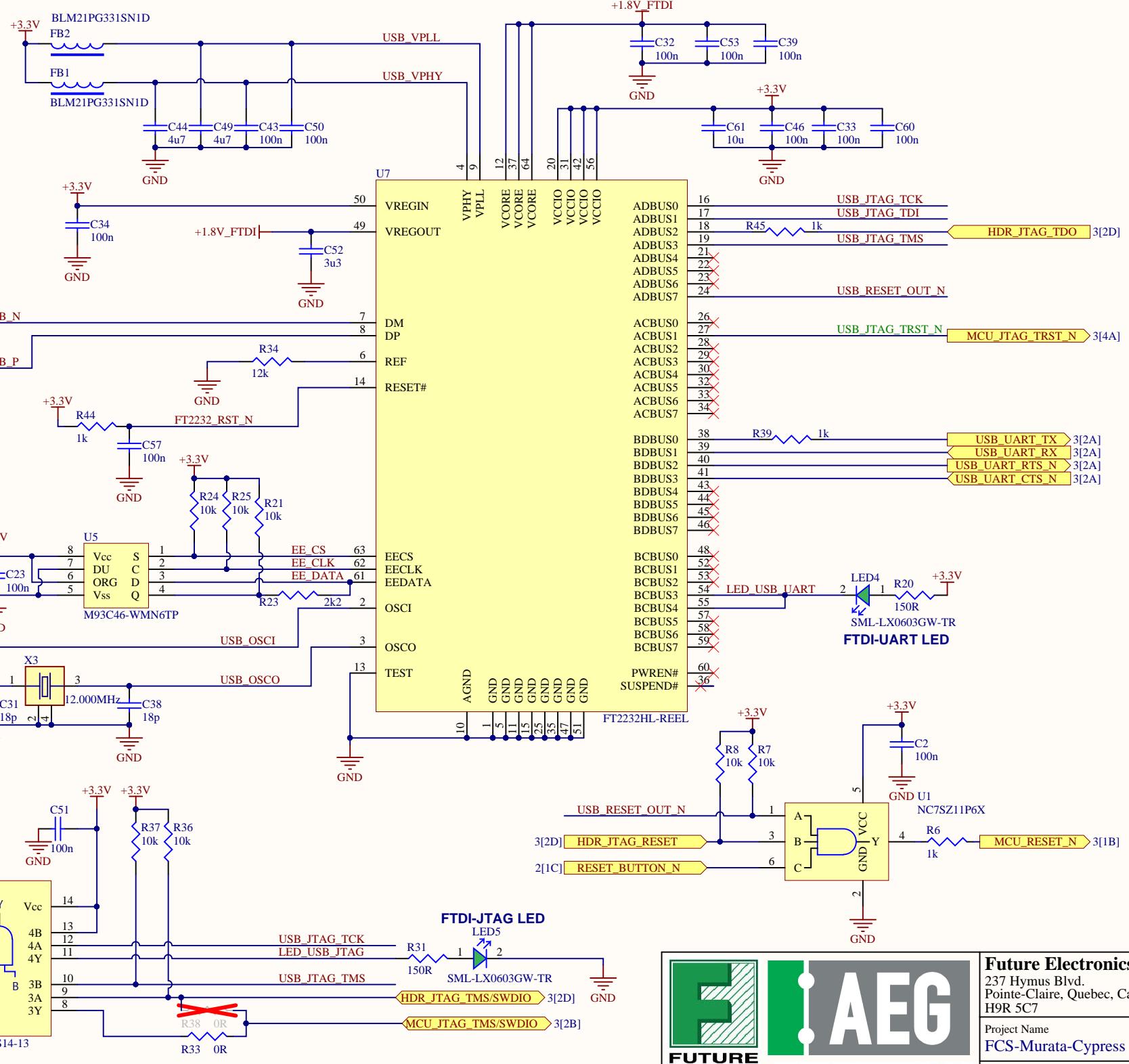


FTDI USB-JTAG



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7 Hymus Blvd.
Pointe-Claire, Quebec, Canada
H9R 5C7

ject Name
CS-Murata-Cypress Dev kit Rev 2

|e

TDI

Page B Dwg No. FEN-413458-SCH-1

1/10/2018 Sheet 1 of 4 Variant: Nebula Dev kit

1

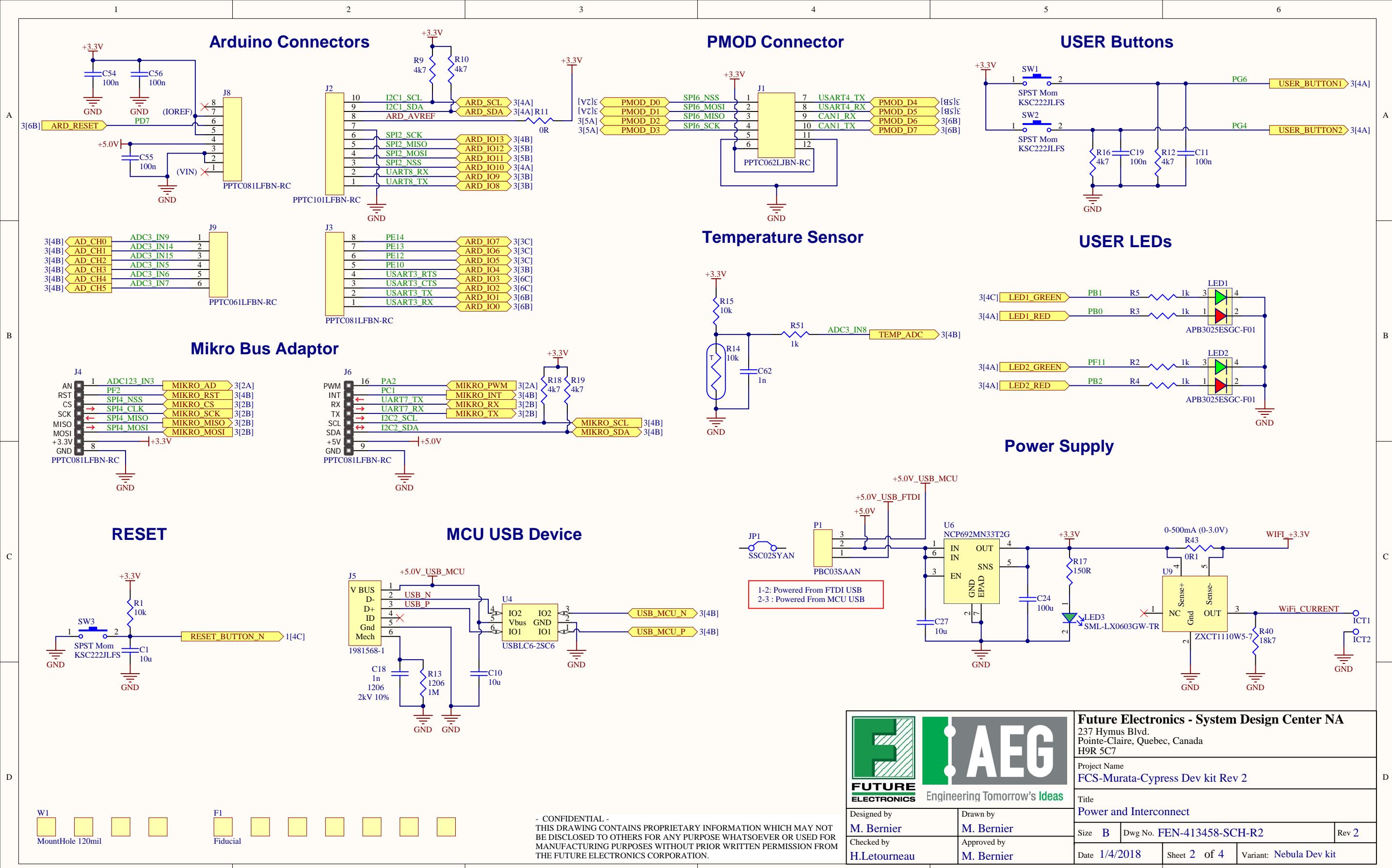
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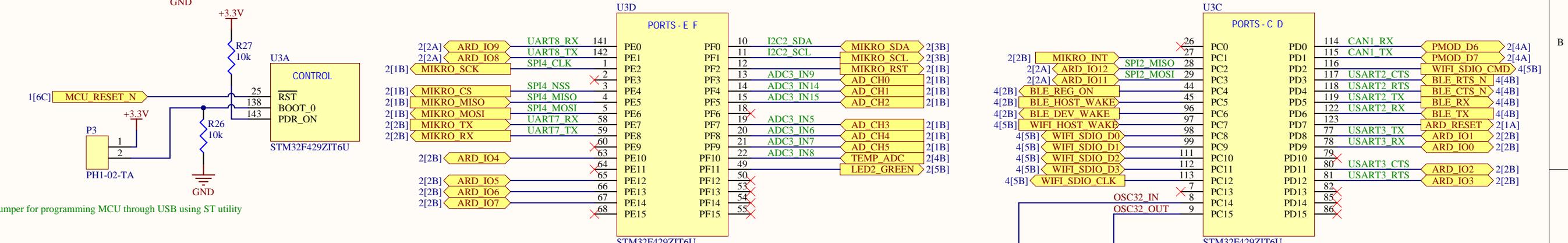
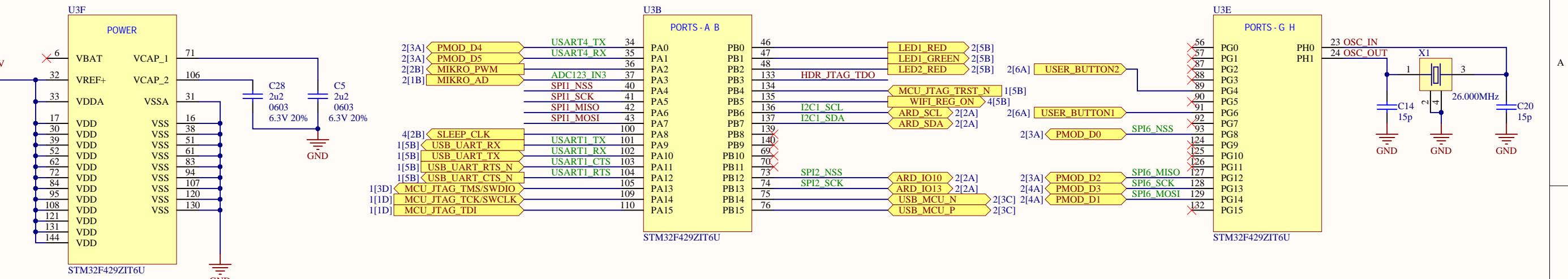
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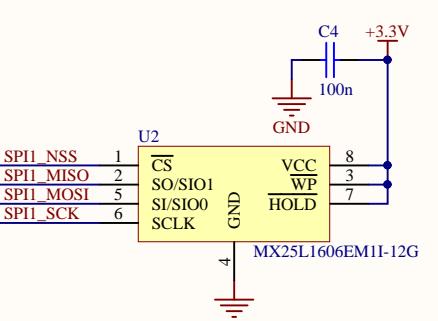
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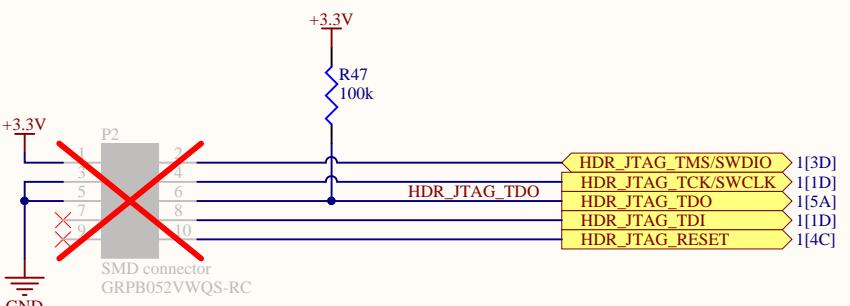
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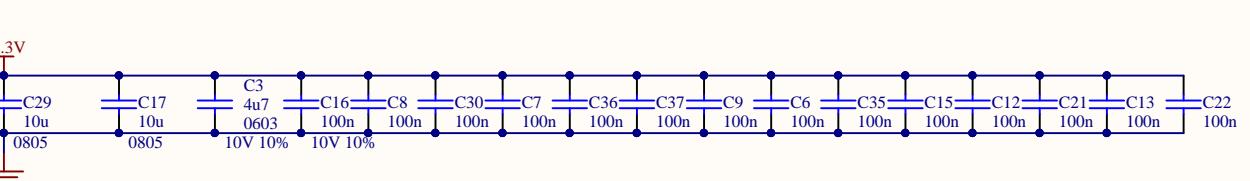
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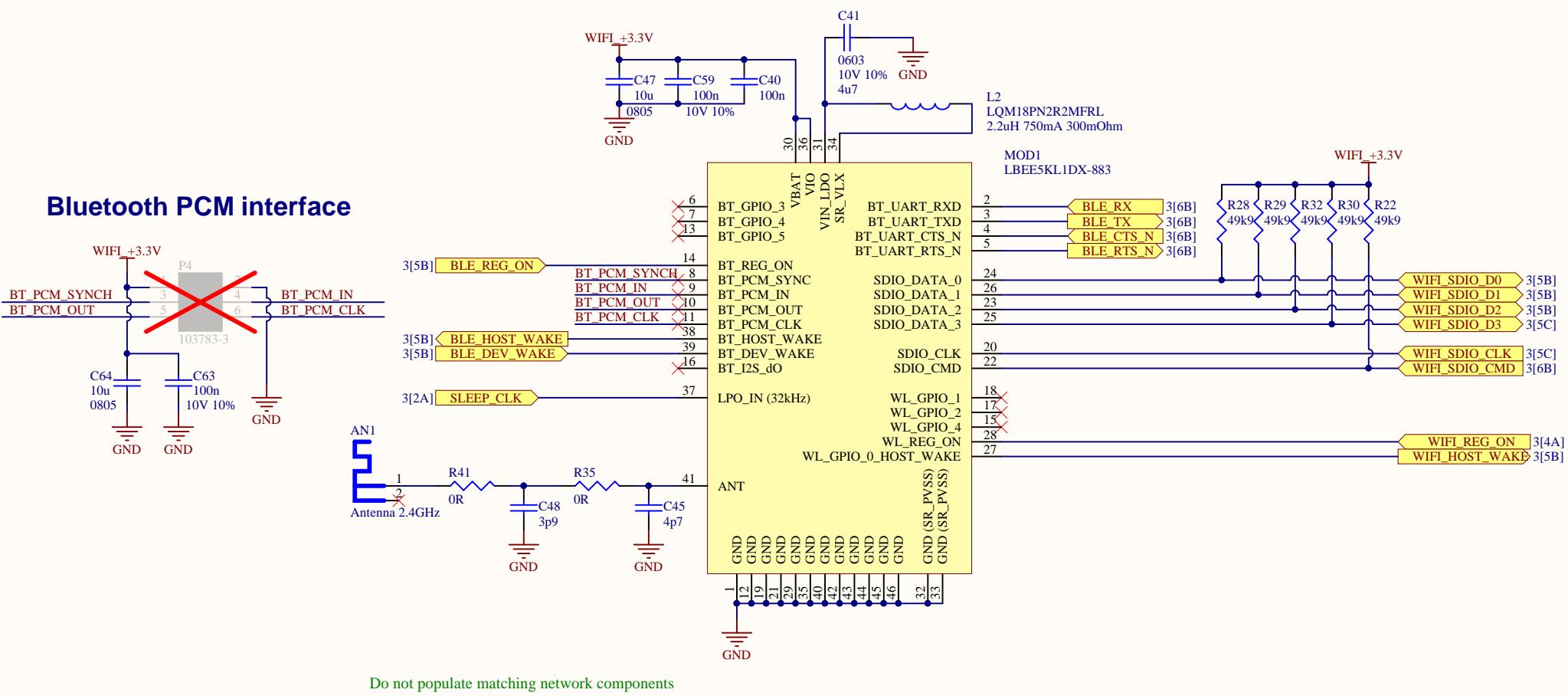
Cortex-M Debug Connector (SWD)



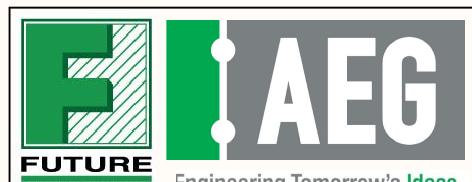
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WiFi and Bluetooth Module



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Engineering Tomorrow's Ideas

Future Electronics - System Design Center NA	
237 Hymus Blvd. Pointe-Claire, Quebec, Canada H9R 5C7	
Project Name FCS-Murata-Cypress Dev kit Rev 2	
Title WIFI	
Size B Dwg No. FEN-413458-SCH-R2 Rev 2	
Designed by M. Bernier Drawn by M. Bernier	
Checked by H.Letourneau Approved by M. Bernier	
Date 2/15/2018 Sheet 4 of 4 Variant: Nebula Dev kit	

1	2	3	4	5	6	7	8
Layers	Top Layer				Instructions (GM16) Top Overlay		

Impedance Requirements					
Layer	Impedance 50 Ohms	Impedance 90 Ohms (Diff)	Co-planar Waveguide : 50 Ohms		
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
Bottom Layer	9 mils	8 mils	9 mils	10 mils	30 mils

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top Layer	Copper	2,10mil		
4	Dielectric1	FR-4 HTg	6,00mil	4,5	
5	GND	Copper	1,40mil		
6	Dielectric3	FR-4 HTg	45,00mil	4,5	
7	Power	Copper	1,40mil		
8	Dielectric2	FR-4 HTg	6,00mil	4,5	
9	Bottom Layer	Copper	2,10mil		
10	Bottom Solder	Solder Resist	0,40mil	3,5	
11	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

1. BOARD SPECS - BOARD SHALL BE MANUFACTURED TO MEET
ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

2. BASE MATERIAL - FR4 High Tg Metal Core Other
- Tg for LAMINATE AND PREPREG SHALL BE GREATER THAN OR EQUAL
TO 170°C

3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL

4. PLATING - 0.5oz 0.75oz 1oz Other

5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other

8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

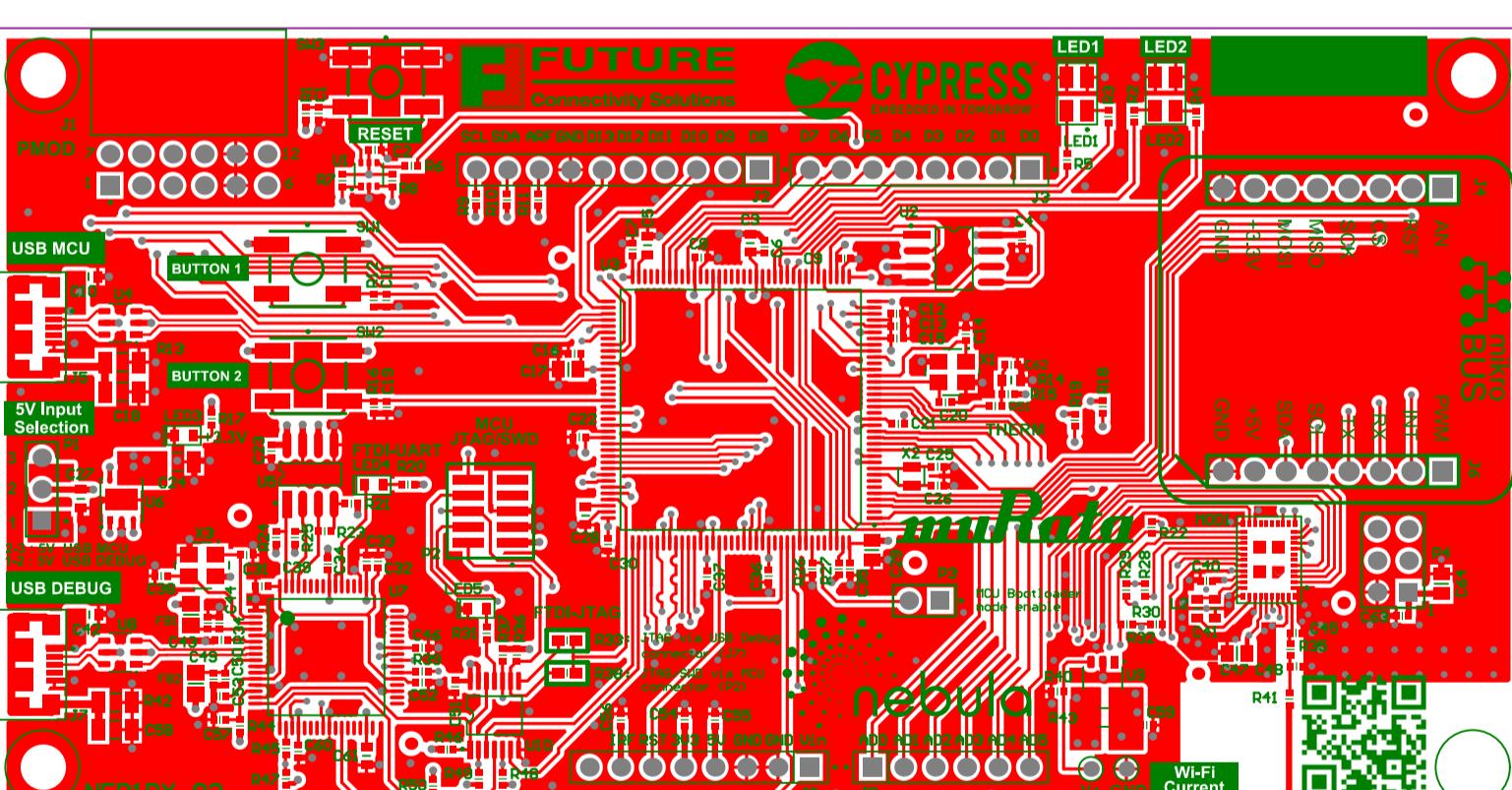
10. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP
- ALL HOLES LOCATION TOLERANCES ARE TO BE +/- .002 IN REFERENCE TO THE PRIMARY DATUM

11. GERBER FILES - SUPPLIED GERBER FILES MUST NOT BE MODIFIED WITHOUT PRIOR PERMISSION FROM THE CLIENT

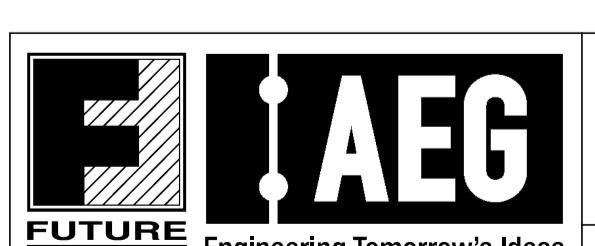
12. LOGO - ONLY LOGOS SUPPLIED IN GERBER FILES WILL BE ACCEPTED ON PCB

13. TOOLING HOLES - NO HOLES SHALL BE PERMITTED WITHIN THE BOARD AREA, EXCEPT THOSE INDICATED
IN THE DRILL LEGEND

14. REGISTRATION - REGISTRATION OF PATTERNS TO BE WITHIN +/- .005 LOCATION OF PATTERN ON BOARD
TO DIMENSION SHOWN



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Future Electronics – System Design Center NA	
237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7	
<input checked="" type="checkbox"/>	
Project #	FCS-Murata-Cypress Dev kit
Designed by:	M. Bernier
Drawn by:	M. Bernier
Title:	FCS-Murata-Cypress Dev kit
Checked by:	H.Letourneau
Approved by:	M. Bernier
Date:	2/16/2018
Size: B	DWG NO: FEN-413458-PCB-R2
REV: 2	
Sheet	1 of 1

Layers

GND

Instructions (GM16)

Impedance Requirements					
Layer	Impedance 50 Ohms	Impedance 90 Ohms (Diff)	Co-planar Waveguide : 50 Ohms		
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
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10	Bottom Solder	Solder Resist	0,40mil	3,5	
11	Bottom Overlay				

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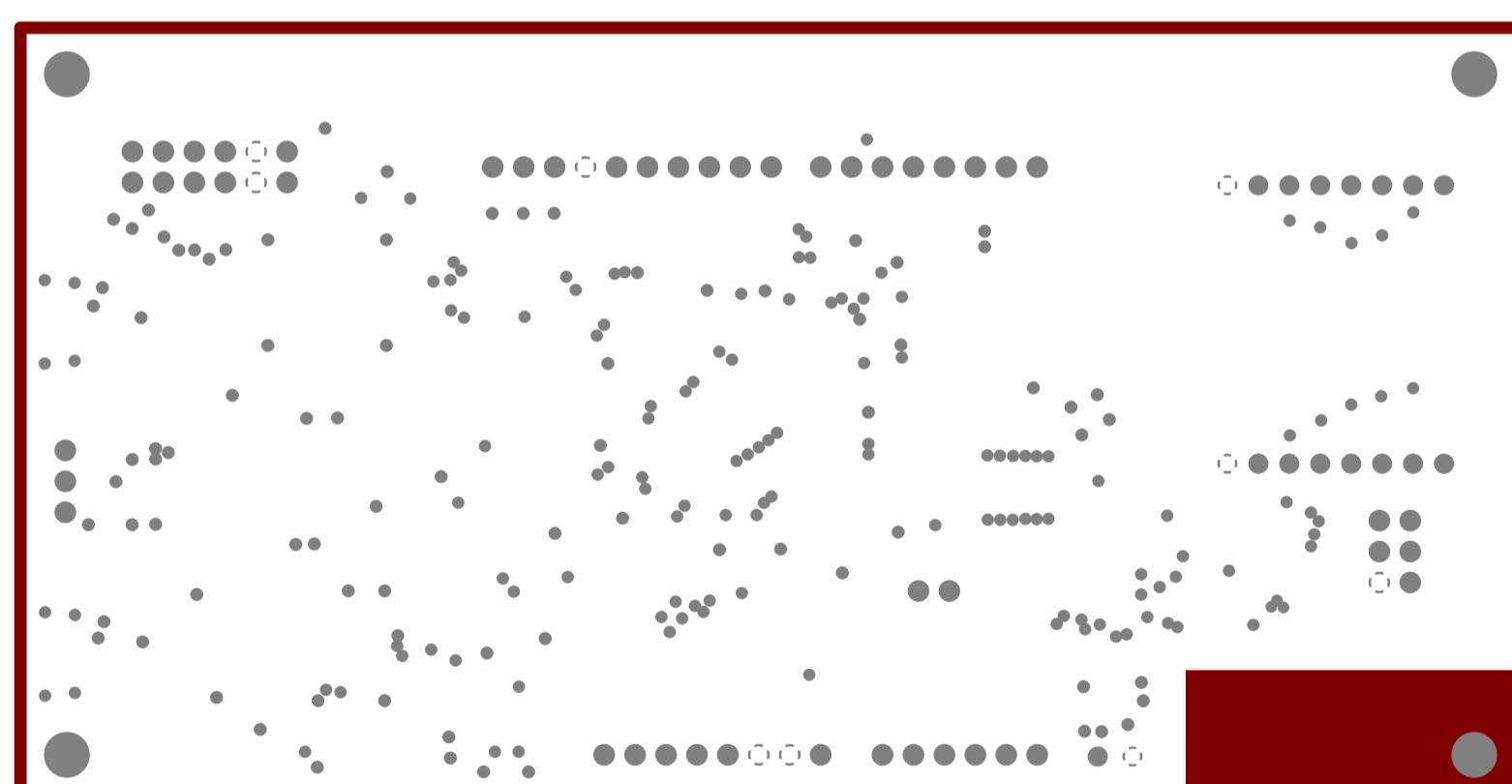
4. PLATING - 0.5oz 0.75oz 1oz Other 5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other 6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other 7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other 8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

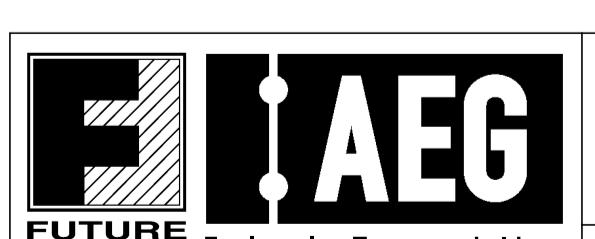
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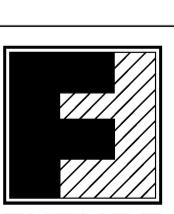
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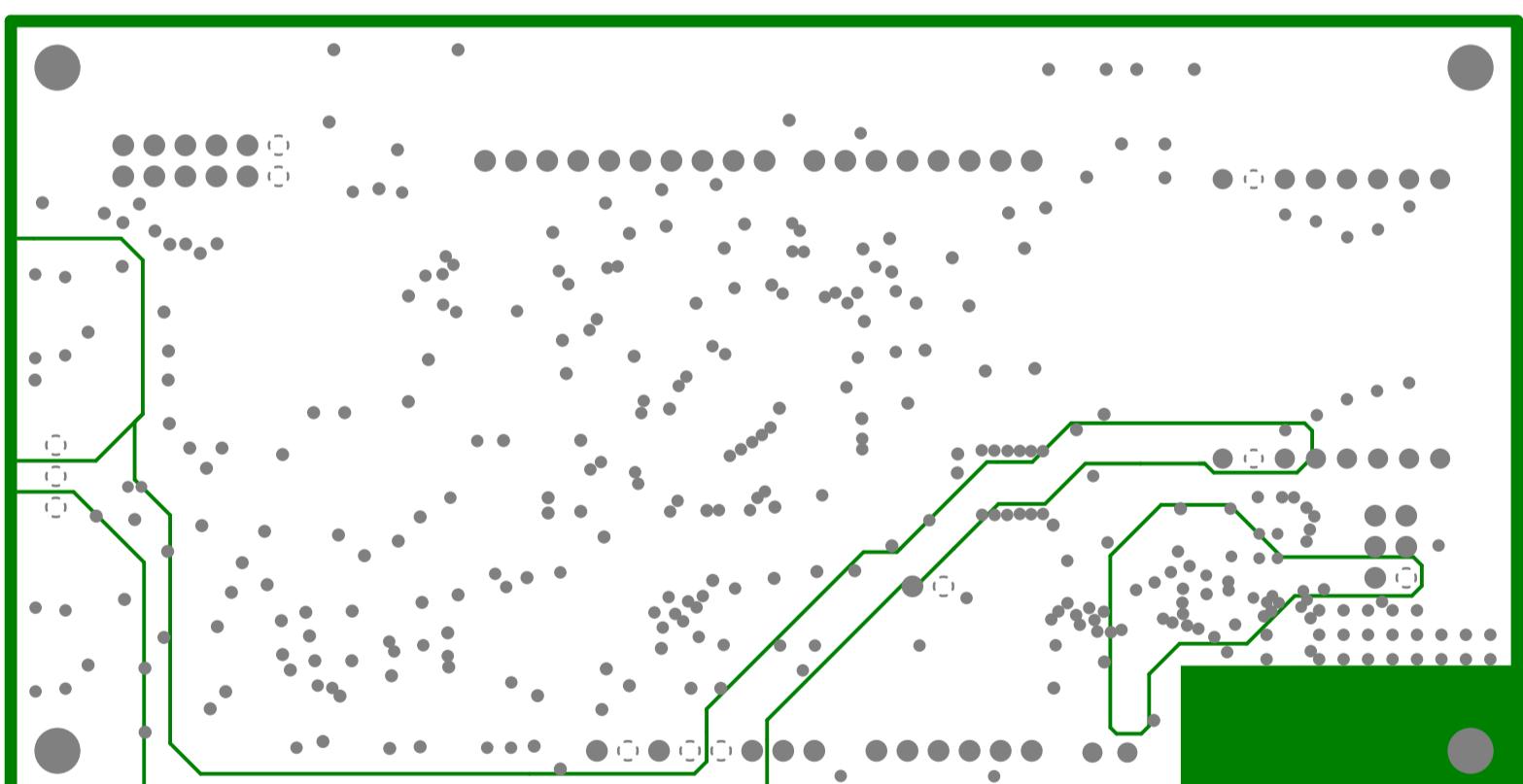


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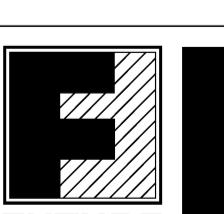
Project #	FCS-Murata-Cypress Dev kit
Title:	FCS-Murata-Cypress Dev kit
Size:	B DWG NO: FEN-413458-PCB-R2
Date:	2/16/2018
Sheet	1 of 1



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<small>4. PLATING - 0.5oz <input type="checkbox"/> 0.75oz <input type="checkbox"/> 1oz <input checked="" type="checkbox"/> Other <input type="checkbox"/></small>																																																																															
<small>5. FINISH - HASL RoHS <input checked="" type="checkbox"/> HASL <input type="checkbox"/> Immersion Silver <input type="checkbox"/> Immersion Tin <input type="checkbox"/> ENIG <input type="checkbox"/> Other <input type="checkbox"/></small>																																																																															
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<small>7. SILKSCREEN - LPI - APPLY EPOXY BASED INK - TOP/BOTTOM <input type="checkbox"/> TOP ONLY <input checked="" type="checkbox"/> BOTTOM ONLY <input type="checkbox"/> NONE <input type="checkbox"/> - WHITE <input checked="" type="checkbox"/> BLACK <input type="checkbox"/> Other <input type="checkbox"/></small>																																																																															
<small>8. IMPEDANCE CONTROL - NO <input type="checkbox"/> YES <input checked="" type="checkbox"/> SEE TABLE FOR DETAIL</small>																																																																															
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<small>Project # FCS-Murata-Cypress Dev kit</small>				<small>Drawn by: M. Bernier</small>																																																																											
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<small>Checked by: H.Letourneau</small>				<small>Approved by: M. Bernier</small>																																																																											
<small>Date: 2/16/2018</small>				<small>Sheet 1 of 1</small>																																																																											

1	2	3	4	5	6	7	8
Layers	Top Layer			Instructions (GM16) Board Outline (GM14)	Top Overlay Bottom Overlay		
		Bottom Layer					

Impedance Requirements					
Layer	Impedance 50 Ohms	Impedance 90 Ohms (Diff)	Co-planar Waveguide : 50 Ohms		
	Trace Width (mils)	Trace Width (mils)	Trace Spacing (mils)	Trace Width (mils)	Trace Spacing (mils)
Top Layer	9 mils	8 mils	9 mils	10 mils	30 mils
Bottom Layer	9 mils	8 mils	9 mils	10 mils	30 mils

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0,40mil	3,5	
3	Top Layer	Copper	2,10mil		
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7	Power	Copper	1,40mil		
8	Dielectric2	FR-4 HTg	6,00mil	4,5	
9	Bottom Layer	Copper	2,10mil		
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11	Bottom Overlay				

NOTES: < UNLESS OTHERWISE SPECIFIED >

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ALL SPECS DEFINED UNDER IPC-A-600 (LATEST REVISION)

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3. COPPER FOIL WEIGHT - SEE TABLE FOR FINISHED STACK-UP DETAIL

4. PLATING - 0.5oz 0.75oz 1oz Other

5. FINISH - HASL RoHS HASL Immersion Silver Immersion Tin ENIG
Other

6. SOLDER MASK - APPLY SOLDER MASK AS PER SPECIFIED IPC-SM-840 ON PCB OVER BARE COPPER
- GREEN WHITE BLUE Other

7. SILKSCREEN - LPI - APPLY EPOXY BASED INK
- TOP/BOTTOM TOP ONLY BOTTOM ONLY NONE
- WHITE BLACK Other

8. IMPEDANCE CONTROL - NO YES SEE TABLE FOR DETAIL

9. ELECTRICAL TEST - 100% IPC-D-356B

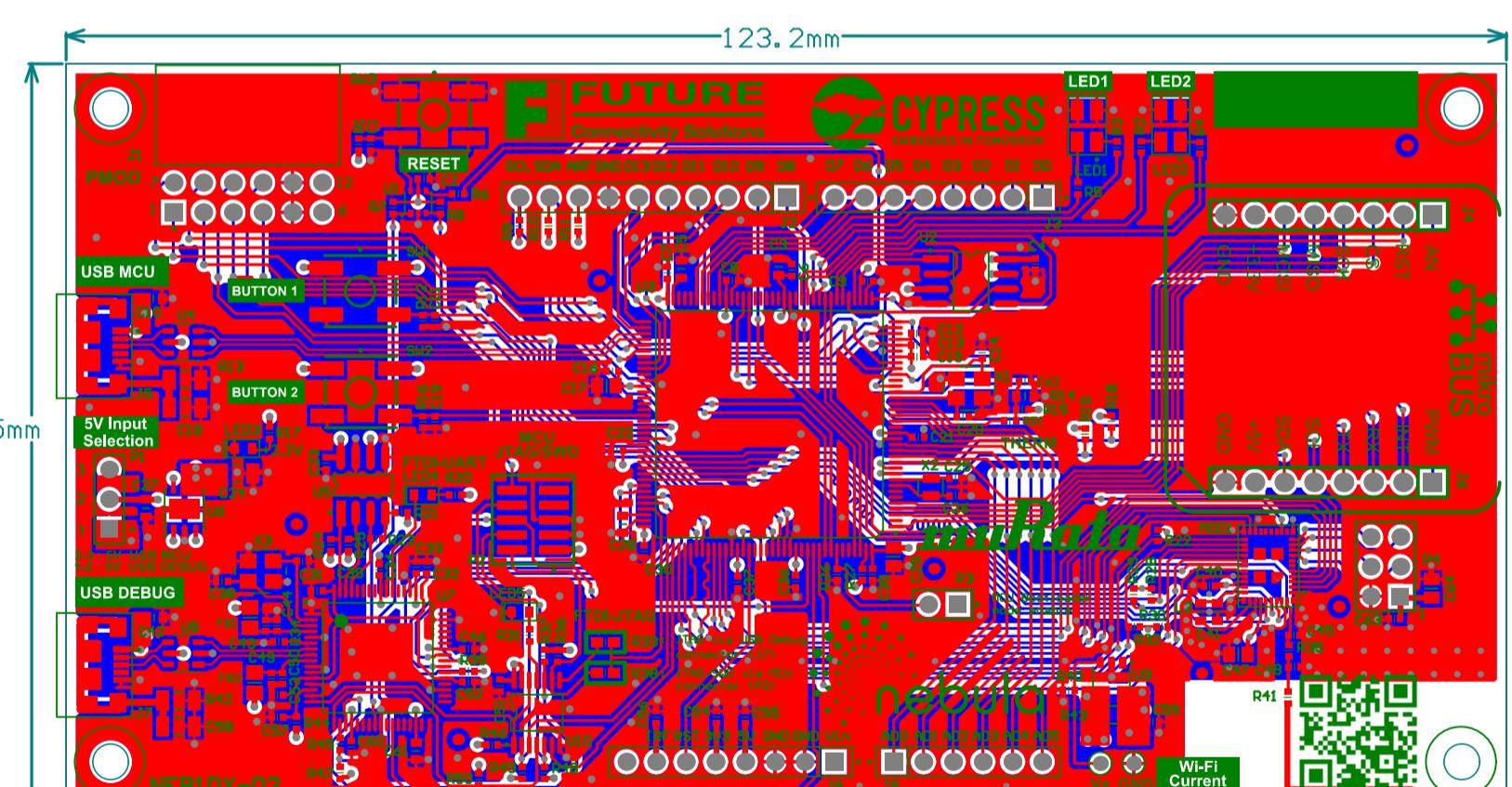
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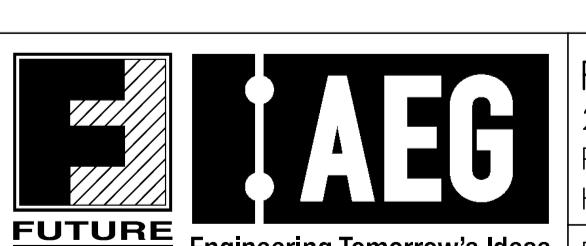
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Future Electronics – System Design Center NA	
237 Hymus Blvd Pointe-Claire, Quebec, Canada H9R 5C7	
<input checked="" type="checkbox"/>	
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Sheet	1 of 1

