



# AK4961

## Low-Power CODEC with Audio/Voice DSP

### 1. General Description

The AK4961 is four channels 24-bit ADC, stereo advanced 32-bit high sound quality audio DAC and stereo 24-bit DAC with a built-in microphone amplifier, mono receiver amplifier, ground-referenced headphone amplifier, lineout, and a high feature Audio/Voice DSP. The AK4961 features AKM's DSP core that enables various kinds of voice processing such as voice wakeup, dual mic Tx noise suppression, Rx noise suppression, echo cancellation, and hands free functions. The AK4961 has five audio I/F and SLIMbus I/F to communicate with an Application processor, up to two Baseband processors, a Bluetooth module and a digital input class-D amplifier simultaneously, and mixes asynchronous signal with built-in SRCs.

### 2. Features

#### 1. Recording Function

- 4ch Low Power 24-bit ADC
  - 3-types Digital Filter for Sound Color Selection
- 3 Stereo Input Selectors
- 3 Stereo Inputs (Single-ended) or 6 Mono Inputs (Full-differential)
- MIC-Amp Gain: +30dB ~ 0dB, 3dB step
- 4 MIC Power Supplies: 2.8 / 2.5 / 1.8V Selectable
- ADC Characteristics:
  - Single-ended Mode
    - S/(N+D): 88dB, DR, S/N: 95dB (MIC-Amp=+18dB)
    - S/(N+D): 84dB, DR, S/N: 100dB (MIC-Amp=+6dB)
  - Full-Differential Mode:
    - S/(N+D): 90dB, DR, S/N: 95dB (MIC-Amp=+18dB)
    - S/(N+D): 90dB, DR, S/N: 102dB (MIC-Amp=0dB)

#### • 4-Channel Digital MIC Interface

#### 2. Playback Function

- Stereo High Sound Quality Low Power Advanced 32-bit DAC for Headphone
  - 4 types of Digital Filter for Sound Color Selection
- Low Power 24-bit Stereo DAC for LINEOUT/ Receiver / External Speaker Amp
- Ground-referenced Class-G Stereo Headphone-Amp
  - Output Power: 25mW @ 32Ω, 40mW @ 16Ω, THD+N = 0.1%
  - S/(N+D): 99dB
  - S/N: 110dB
  - Output Noise Level: -119dBV (Analog Volume ≤ -14dB)
  - Analog Volume: +6 ~ -40dB & Mute, 2dB Step
  - Ground Loop Noise Cancellation
- Ground-referenced Stereo Line Outputs
  - S/(N+D): 86dB, DR, S/N: 100dB
  - Analog Volume: +3 ~ -7.5dB, 1.5dB Step
- Mono Receiver-Amp
  - BTL Output
  - Output Power: 100mW @ 32Ω, THD+N = 1%
  - S/(N+D): 87dB @ 32Ω, Po=30mW
  - S/N: 100dB @ Po = 30mW
  - Analog Volume: + 3 ~ -7.5dB, 1.5dB Step

- **Ground-referenced stereo Line Outputs for External Speaker-Amp**
  - 2ch Single-ended or Full Differential Outputs
  - S/(N+D): 86dB, DR, S/N: 100dB
  - Analog Volume: +3 ~ -7.5B, 1.5dB Step

### 3. Five Digital Audio interface

- Master/Slave mode
- Sampling Frequency (ADC):
  - 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k
- Sampling Frequency (DAC):
  - 8k, 11.025k, 12k, 16k, 22.05k, 24k, 32k, 44.1k, 48k, 64k, 88.2k, 96k, 128k, 176.4k, 192kHz
- Interface Format
  - SDTOx: 24/16-bit I<sup>2</sup>S/MSB justified, 16-bit PCM Short/Long Frame
  - SDTIX: 32/24/16-bit I<sup>2</sup>S/MSB justified, 16-bit PCM Short/Long Frame

### 4. SLIMbus Interface

### 5. Five Asynchronous Sample Rate Converters:

- Up sample: up to x6
- Down sample: down to x1/6
- 4 types of Digital Filter for Sound Color Selection (Only SRCE)

### 6. Power Management

### 7. Dual PLL

### 8. X'tal Oscillator

### 9. Jitter Cleaner with a built-in SRC

### 10. Accessories

- Jack Detection
- Headset Detection
- Button Detection

### 11. Embedded Audio/ Hands Free DSP

- Flexible programming with built-in program and data memories
- Pre-processing for Voice Wakeup
- Hardware accelerator
- Processing features (example)

- Single/Dual Microphone Noise suppression
- Echo cancellation
- Rx Voice Clarity Enhancement
- 5-Band Parametric EQ, Dynamic Range Control

### 12. μP I/F: SPI / I<sup>2</sup>C(1MHz) and SLIMbus

### 13. Operation Temperature Range: Ta = -40 ~ 85°C

### 14. Power Supply:

- |   |                               |
|---|-------------------------------|
| • AVDD1, 2 (CODEC, MIC, PLL):           | 1.7 to 1.9V                   |
| • CVDD (HP/LINE/RCV-Amps, Charge Pump): | 1.7 to 1.9V                   |
| • LVDD (LDO2 for Digital Core):         | 1.7 to 1.9V (built-in LDO)    |
| • VDD12 (Digital Core):                 | 1.14 to 1.26V (direct supply) |
| • TVDD1, 2, 3(Host & Audio I/F):        | 1.65 to 3.6V                  |

### 15. Package: 116 pin CSP (4.522 x 4.774mm, 0.4mm pitch)

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#### 4. Block Diagram and Functions

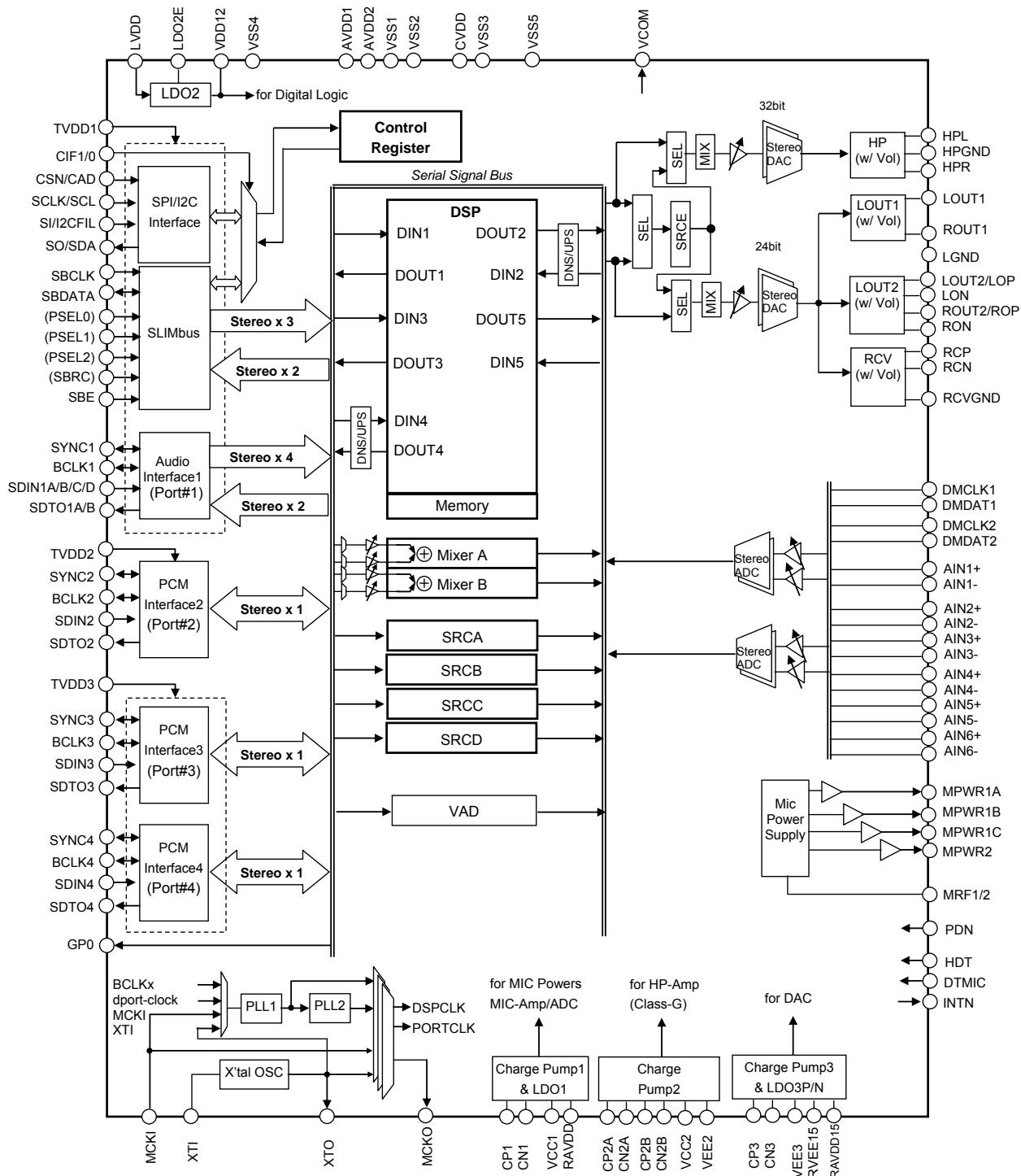


Figure 1. Block Diagram

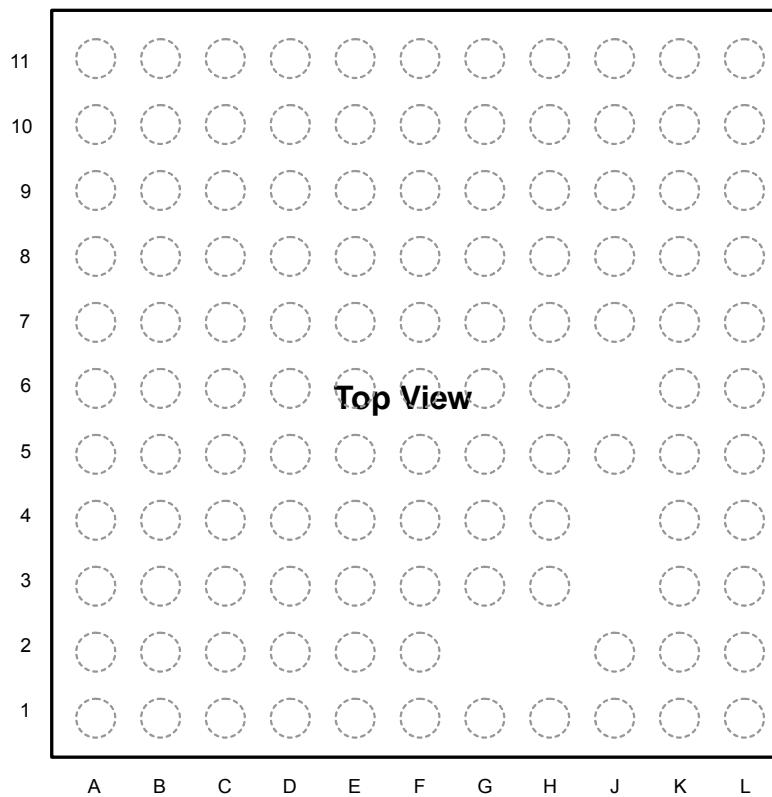
## 5. Pin Configurations and Functions

### ■ Ordering Guide

**AK4961ECB** -40 to 85°C 116 pin CSP (0.4mm pitch)  
AKD4961 Evaluation board for AK4961

### ■ Pin Configurations

CSP 116 pin (4.522 x 4.774mm, 0.4mm pitch)



<b>11</b>	VDD12	LVDD	DMCLK2	XTO	XTI	DMCLK1	VSS1	AVDD1	MPWR2	MPWR1A	AIN1-
<b>10</b>	VSS4	SDTI4	SDTI3	TVDD3	DMDAT1	TESTO2	MRF2	MPWR1C	MRF1	AIN2+	AIN1+
<b>9</b>	SDTO4/ GPI	SDTO3	BCLK4	SYNC4	VSS5	MPWR1B	HDETGND	AIN3-	AIN2-	AIN4+	AIN4-
<b>8</b>	BCLK3	SYNC3	SDTI2	DMDAT2	VSS5	AIN5+	AIN5-	AIN3+	AIN6-	AIN6+	VCOM
<b>7</b>	TVDD2	SDTO2	BCLK2	SYNC2	VSS5	DTMIC	RON	ROP/ ROUT2	LON	LOP/ LOUT2	LGND
<b>6</b>	PDN	LDO2E	TESTI	SDTI1D	VSS5	RAVDD	CN3	CP3	-	CVDD	CN2B
<b>5</b>	SDTI1C/ PSEL2	SDTI1B/ CODECCSDTI2/ PSEL1	SDTI1A/ CODECCSDTI1/ PSEL0	SI/ I2CFIL	VCC1	LOUT1	ROUT1	VEE3	VSS3	CP2B	CN2A
<b>4</b>	CSN/ CAD	SBE	CIF1	MCKI/ CODECMCLK	VSS5	VSS5	CN1	CP1	-	CP2A	VEE2
<b>3</b>	INTN	TESTO1	GP0	VSS4	CIF0	VSS5	RVEE15	VCC2	-	RCP	RCVGND
<b>2</b>	TVDD1	SYNC1/ CODECSYNC	SBDATA	SO/ SDA	SBCLK	VSS5	-	-	HPR	HPL	RCN
<b>1</b>	SDTO1B/ CODECSDTO2	SDTO1A/ CODECSDTO1/ SBRC	BCLK1/ CODECBCLK	MCKO	SCLK/ SCL	VSS5	RAVDD15	VSS2	AVDD2	HPGND	HDT
	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>E</b>	<b>F</b>	<b>G</b>	<b>H</b>	<b>J</b>	<b>K</b>	<b>L</b>

Top View

## ■ Pin Functions

No.	Pin Name	I/O	Function	Protection Diode	Power Domain	Clock Domain
<b>Power Supply</b>						
H11	AVDD1	-	Analog Power Supply 1 Pin		AVDD1	
J1	AVDD2	-	Analog Power Supply 2 Pin		AVDD2	
G11	VSS1	-	Ground 1 Pin			
H1	VSS2	-	Ground 2 Pin			
K6	CVDD	-	HP-Amp/Charge Pump Power Supply Pin		CVDD	
J5	VSS3	-	Ground 3 Pin			
B11	LVDD	-	Digital Core & LDO2 Power Supply Pin		LVDD	
A10, D3	VSS4	-	Ground 4 Pin			
E4, E6-9, F1-4	VSS5	-	Ground 5 Pin			
A2	TVDD1	-	Digital I/F(SLIMbus, Port #1, SPI) Power Supply Pin		TVDD1	
A7	TVDD2	-	Digital I/F(Port #2) Power Supply Pin		TVDD2	
D10	TVDD3	-	Digital I/F(Port #3) Power Supply Pin		TVDD3	
L8	VCOM	O	Common Voltage Output Pin This pin must be connected to VSS1 pin with 2.2μF ± 50% Ceramic capacitor in series.	AVDD1/ VSS1		DC
A11	VDD12	-	LDO2 (1.2V) Output/1.2V Power Supply Pin LDO2E pin = “L”: 1.2V External Power Supply LDO2E pin = “H”: LDO2 output This pin must be connected to VSS4 pin with 2.2μF ± 50% capacitor in series.	LVDD/ VSS1	LVDD	
B6	LDO2E	I	LDO2 Enable Pin “L”: LDO2 Disable, “H”: LDO2 Enable	TVDD1/ VSS4	TVDD1	DC

No.	Pin Name	I/O	Function	Protection Diode	Power Domain	Clock Domain
<b>Charge Pump &amp; LDO</b>						
F6	RAVDD	O	LDO1(3.3V) Output Pin This pin must be connected to VSS1 pin with 2.2μF ± 50% capacitor in series.	VSS1		
H4	CP1	O	Positive Charge Pump Capacitor Terminal 1 Pin This pin must be connected to CN1 pin with 2.2μF ± 50% capacitor in series.	VSS3	CVDD	CODEC Clock
G4	CN1	I	Negative Charge Pump Capacitor Terminal 1 Pin This pin must be connected to CP1 pin with 2.2μF ± 50% capacitor in series.	CVDD/ VSS3	CVDD	CODEC Clock
E5	VCC1	O	Charge Pump Circuit Positive Voltage Output Pin (CVDD x 2) This pin must be connected to VSS3 pin with 2.2μF ± 50% capacitor in series.	VSS3	CVDD	
H3	VCC2	O	Charge Pump Circuit Positive Voltage Output Pin (CVDD or 1/2*CVDD) This pin must be connected to VSS3 pin with 2.2μF ± 50% capacitor in series.	CVDD/ VSS3	CVDD	
K4	CP2A	O	Positive Charge-Pump Capacitor Terminal 2A Pin This pin must be connected to CN2A pin with 2.2μF ± 50% capacitor in series.	CVDD/ VSS3	CVDD	CODEC Clock
L5	CN2A	I	Negative Charge Pump Capacitor Terminal 2A Pin This pin must be connected to CP2A pin with 2.2μF ± 50% capacitor in series.	CVDD	CVDD	CODEC Clock
K5	CP2B	O	Positive Charge Pump Capacitor Terminal 2B Pin This pin must be connected to CN2B pin with 2.2μF ± 50% capacitor in series.	CVDD/ VSS3	CVDD	CODEC Clock
L6	CN2B	I	Negative Charge Pump Capacitor Terminal 2B Pin This pin must be connected to CP2B pin with 2.2μF ± 50% capacitor in series.	CVDD	CVDD	CODEC Clock
L4	VEE2	O	Charge Pump Circuit Negative Voltage (-CVDD or -1/2*CVDD) Output 2 Pin This pin must be connected to VSS3 pin with 2.2μF ± 50% capacitor in series.	CVDD/ VSS3		

No.	Pin Name	I/O	Function	Protection Diode	Power Domain	Clock Domain
<b>Charge Pump &amp; LDO</b>						
H6	CP3	O	Positive Charge Pump Capacitor Terminal 3 Pin This pin must be connected to CN3 pin with $2.2\mu F \pm 50\%$ capacitor in series.	CVDD/ VSS3	CVDD	CODEC Clock
G6	CN3	I	Negative Charge Pump Capacitor Terminal 3 Pin This pin must be connected to CP3 pin with $2.2\mu F \pm 50\%$ capacitor in series.	CVDD	CVDD	CODEC Clock
H5	VEE3	O	Charge Pump Circuit Negative Voltage (-CVDD) Output 3 Pin This pin must be connected to VSS3 pin with $2.2\mu F \pm 50\%$ capacitor in series.	CVDD/ VSS3		
G1	RAVDD15	O	LDO3P (1.5V) Output 1 Pin This pin must be connected to VSS2 pin with $2.2\mu F \pm 50\%$ capacitor in series.	AVDD2/ VSS2		DC
G3	RVEE15	O	LDO3N (-1.5V) Output 1 Pin This pin must be connected to VSS2 pin with $2.2\mu F \pm 50\%$ capacitor in series.	AVDD2/ VSS2		DC
<b>MIC Power Supplies</b>						
K11	MPWR1A	O	MIC Power Supply 1A Pin	AVDD1/ VSS1	RAVDD	DC
F9	MPWR1B	O	MIC Power Supply 1B Pin	AVDD1/ VSS1	RAVDD	DC
H10	MPWR1C	O	MIC Power Supply 1C Pin	AVDD1/ VSS1	RAVDD	DC
J10	MRF1	O	MIC Power Ripple Filter Pin for MPWR1A/B/C pins This pin must be connected to VSS1 pin with $2.2\mu F \pm 50\%$ Ceramic capacitor in series.	None/ VSS1	RAVDD	DC
J11	MPWR2	O	MIC Power Supply 2 Pin	AVDD1/ VSS1	RAVDD	DC
G10	MRF2	O	MIC Power Ripple Filter Pin for MPWR2 pin This pin must be connected to VSS1 pin with $2.2\mu F \pm 50\%$ Ceramic capacitor in series.	None/ VSS1	RAVDD	DC

No.	Pin Name	I/O	Function	Protection Diode	Power Domain	Clock Domain
<b>Control Interface</b>						
A4	CSN	I	Serial Data Chip Select Pin (CIF1 pin = "L", CIF0 pin = "L")	TVDD1/ VSS4	TVDD1	SCLK
	CAD	I	I <sup>2</sup> C Chip Address Pin (CIF1 pin = "L", CIF0 pin = "H")			
E1	SCLK	I	SPI Serial Data Clock Pin (CIF1 pin = "L", CIF0 pin = "L")	TVDD1/ VSS4	TVDD1	SCLK
	SCL	I	I <sup>2</sup> C Serial Data Clock Pin (CIF1 pin = "L", CIF0 pin = "H")			
D5	SI	I	SPI Serial Data Input Pin (CIF1 pin = "L", CIF0 pin = "L")	TVDD1/ VSS4	TVDD1	SCLK
	I2CFIL	I	I <sup>2</sup> C Filter Select Pin (CIF1 pin = "L", CIF0 pin = "H") "L": 400kHz Mode, "H": 1MHz Mode			
D2	SO	O	Serial Data Output Pin (CIF1 pin = "L", CIF0 pin = "L")	TVDD1/ VSS4	TVDD1	SCLK
	SDA	I/O	I <sup>2</sup> C Serial Data Input/Output Pin (CIF1 pin = "L", CIF0 pin = "H")			
E3	CIF0	I	Microcontroller Mode Select 0 Pin	TVDD1/ VSS4	TVDD1	DC
C4	CIF1	I	Microcontroller Mode Select 1 Pin	TVDD1/ VSS4	TVDD1	DC
<b>SLIMbus Interface</b>						
E2	SBCLK	I	SLIMbus Clock Pin (SBE pin = "H")	TVDD1/ VSS4	TVDD1	SBCLK
C2	SBDATA	I/O	SLIMbus Input/Output Data Pin (SBE pin = "H")	TVDD1/ VSS4	TVDD1	SBCLK
B4	SBE	I	SLIMbus Enable Pin "L": Disable, "H" : Enable	TVDD1/ VSS4	TVDD1	DC

No.	Pin Name	I/O	Function	Protection Diode	Power Domain	Clock Domain
<b>Audio Interface</b>						
D4	MCKI	I	External Master Clock Input Pin (EXIF bit = "0")	TVDD1/ VSS4	TVDD1	CODEC Clock
	CODECMCLK	I	CODEC Master Clock Input Pin (EXIF bit = "1")			
E11	XTI	I	X'tal Oscillator Input Pin	AVDD1/ VSS1	AVDD1	
D11	XTO	O	X'tal Oscillator Output Pin	AVDD1/ VSS1	AVDD1	
D1	MCKO	O	Master Clock Output Pin	TVDD1/ VSS4	TVDD1	
C1	BCLK1	I/O	Audio Serial Data Clock 1 Pin (EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
	CODECBCLK	I	CODEC Audio Serial Data Clock Pin (EXIF bit = "1")			
B2	SYNC1	I/O	Frame Sync Clock 1 Pin (EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
	CODECSYNC	I	CODEC Frame Sync Clock Pin (EXIF bit = "1")			CODEC Clock
C5	SDTI1A	I	Audio Serial Data Input 1A Pin (SBE pin = "L", EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
	CODECSDTI1	I	CODEC Audio Serial Data Input 1 Pin (SBE pin = "L", EXIF bit = "1")			CODEC Clock
	PSEL0	I	SLIMbus Data Drivability Select 0 Pin (SBE pin = "H")			DC
B5	SDTI1B	I	Audio Serial Data Input 1B Pin (SBE pin = "L", EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
	CODECSDTI2	I	CODEC Audio Serial Data Input 2 Pin (SBE pin = "L", EXIF bit = "1")			CODEC Clock
	PSEL1	I	SLIMbus Data Drivability Select 1 Pin (SBE pin = "H")			DC
A5	SDTI1C	I	Audio Serial Data Input 1C Pin (SBE pin = "L", EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
	PSEL2	I	SLIMbus Data Drivability Select 2 Pin			DC
D6	SDTI1D	I	Audio Serial Data Input 1D Pin (EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
B1	SDTO1A	O	Audio Serial Data Output1A Pin (SBE pin = "L", EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
	CODECSDTO1	O	CODEC Audio Serial Data Direct Output 1 Pin (SBE pin = "L", EXIF bit = "1")			CODEC Clock
	SBRC	I	SLIMbus Reset Counter Enable Pin (SBE pin = "H")			DC
A1	SDTO1B	O	Audio Serial Data Output 1A Pin (EXIF bit = "0")	TVDD1/ VSS4	TVDD1	BCLK1
	CODECSDTO2	O	CODEC Audio Serial Data Direct Output 2 Pin (EXIF bit = "1")			CODEC Clock

No.	Pin Name	I/O	Function	Protection Diode	Power Domain	Clock Domain
<b>Audio Interface</b>						
C7	BCLK2	I/O	Audio Serial Data Clock 2 Pin	TVDD2/ VSS4	TVDD2	BCLK2
D7	SYNC2	I/O	Frame Sync Clock 2 Pin	TVDD2/ VSS4	TVDD2	BCLK2
C8	SDTI2	I	Audio Serial Data Input 2 Pin	TVDD2/ VSS4	TVDD2	BCLK2
B7	SDTO2	O	Audio Serial Data Output 2 Pin	TVDD2/ VSS4	TVDD2	BCLK2
A8	BCLK3	I/O	Audio Serial Data Clock 3 Pin	TVDD3/ VSS4	TVDD3	BCLK3
B8	SYNC3	I/O	Input/Output Channel Clock 3 Pin	TVDD3/ VSS4	TVDD3	BCLK3
C10	SDTI3	I	Audio Serial Data Input 3 Pin	TVDD3/ VSS4	TVDD3	BCLK3
B9	SDTO3	O	Audio Serial Data Output 3 Pin	TVDD3/ VSS4	TVDD3	BCLK3
C9	BCLK4	I/O	Audio Serial Data Clock 4 Pin	TVDD3/ VSS4	TVDD3	BCLK4
D9	SYNC4	I/O	Input/Output Channel Clock 4 Pin	TVDD3/ VSS4	TVDD3	BCLK4
B10	SDTI4	I	Audio Serial Data Input 4 Pin	TVDD3/ VSS4	TVDD3	BCLK4
A9	SDTO4	O	Audio Serial Data Output 4 Pin (GP1E bit = "0")	TVDD3/ VSS4	TVDD3	BCLK4
	GP1	O	DSP Programmable Output 1 Pin (GP1E bit = "1")			DC
C3	GP0	O	DSP Programmable Output 0 Pin	TVDD1/ VSS4	TVDD1	DC

No.	Pin Name	I/O	Function	Protection Diode	Power Domain	Clock Domain
<b>Analog Input</b>						
L10	AIN1+	I	Positive Analog Input 1 Pin	None/ VSS1	RAVDD	
L11	AIN1-	I	Negative Analog Input 1 Pin	None/ VSS1	RAVDD	
K10	AIN2+	I	Positive Analog Input 2 Pin	None/ VSS1	RAVDD	
J9	AIN2-	I	Negative Analog Input 2 Pin	None/ VSS1	RAVDD	
H8	AIN3+	I	Positive Analog Input 3 Pin	None/ VSS1	RAVDD	
H9	AIN3-	I	Negative Analog Input 3 Pin	None/ VSS1	RAVDD	
K9	AIN4+	I	Positive Analog Input 4 Pin	None/ VSS1	RAVDD	
L9	AIN4-	I	Negative Analog Input 4 Pin	None/ VSS1	RAVDD	
F8	AIN5+	I	Positive Analog Input 5 Pin	None/ VSS1	RAVDD	
G8	AIN5-	I	Negative Analog Input 5 Pin	None/ VSS1	RAVDD	
K8	AIN6+	I	Positive Analog Input 6 Pin	None/ VSS1	RAVDD	
J8	AIN6-	I	Negative Analog Input 6 Pin	None/ VSS1	RAVDD	
F11	DMCLK1	O	Digital Microphone Clock Output 1 Pin (DMIC1 bit = “1”)	AVDD1/ VSS1	AVDD1	CODEC Clock
E10	DMDAT1	I	Digital Microphone Data Input 1 Pin (DMIC1 bit = “1”)	AVDD1 / VSS1	AVDD1	CODEC Clock
C11	DMCLK2	O	Digital Microphone Clock Output 2 Pin (DMIC2 bit = “1”)	AVDD1 / VSS1	AVDD1	CODEC Clock
D8	DMDAT2	I	Digital Microphone Data Input 2 Pin (DMIC2 bit = “1”)	AVDD1 / VSS1	AVDD1	CODEC Clock

No.	Pin Name	I/O	Pin Power down	Protection Diode	Power Domain	Clock Domain
<b>Analog Output</b>						
K2	HPL	O	Lch Headphone-Amp Output Pin	CVDD/ VEE2	CVDD/ VEE2	
J2	HPR	O	Rch Headphone-Amp Output Pin	CVDD/ VEE2	CVDD/ VEE2	
K1	HPGND	I	Headphone-Amp Ground Loop Noise Cancellation Pin	-	-	
F5	LOUT1	O	Lch Lineout-Amp 1 Output Pin	AVDD1/ VEE3	AVDD1/ VEE3	
G5	ROUT1	O	Rch Lineout-Amp 1 Output Pin	AVDD1/ VEE3	AVDD1/ VEE3	
L7	LGND	I	Lineout 1/2 Ground Pin			
K7	LOUT2	O	Lch Lineout-Amp 2 Pin (LO2DIF bit = "0")	AVDD1/ VEE3	AVDD1/ VEE3	
	LOP	O	Lch Lineout-Amp 2 Positive Output Pin (LO2DIF bit = "1")			
J7	LON	O	Lch Lineout-Amp 2 Negative Output Pin (LO2DIF bit = "1")	AVDD1/ VEE3	AVDD1/ VEE3	
H7	ROUT2	O	Rch Lineout-Amp 2 Pin (LO2DIF bit = "0")	AVDD1/ VEE3	AVDD1/ VEE3	
	ROP	O	Rch Lineout-Amp 2 Positive Output Pin (LO2DIF bit = "1")			
G7	RON	O	Rch Lineout-Amp 2 Negative Output Pin (LO2DIF bit = "1")	AVDD1/ VEE3	AVDD1/ VEE3	
K3	RCP	O	Receiver-Amp Positive Output Pin	AVDD2/ VEE2	AVDD2/ VEE2	
L2	RCN	O	Receiver-Amp Negative Output Pin	AVDD2/ VEE2	AVDD2/ VEE2	
L3	RCVGND	I	Receiver-Amp Ground Pin	-	-	
<b>Others</b>						
A6	PDN	I	Power down Pin “L”: Power-down, “H”: Power-Up	TVDD1/ VSS4	TVDD1	Async
C6	TESTI	I	Test Input Pin It must be tied “L”	TVDD1 VSS4	TVDD1	
B3	TESTO1	O	Test Output 1 Pin	TVDD1 VSS4	TVDD1	
A3	INTN	O	Interrupt Pin	TVDD1/ VSS4	TVDD1	Async
L1	HDT	I	Jack Detection Input Pin	AVDD2/ None	AVDD2	Async
F7	DTMIC	I	MIC Detection Input Pin	None/ VSS1	AVDD1	Async
G9	HDETGND	I	Detection Circuit Analog Ground Pin	-	-	-
F10	TESTO2	O	TEST Output 2 Pin	-	-	-

Note 1. All digital input pins except analog input/output pins should not be left floating. I/O pins should be processed appropriately.

## ■ Handing of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR1A/B/C, MPWR2, MRF1/2, AIN1+/-, AIN2+/-, AIN3+/-, AIN4+/-, AIN5+/-, AIN6+/-, HPL/R, LOUT1/ROUT1, XTI, XTO, LOUT2/ROUT2, LOP/N, ROP/N, RCP/N, CP/Nx, VCC1, VCC2, VEE2, VEE3, RVEE15, RAVDD15, RAVDD	These pins should be open.
Digital	Outputs Pins	These pins should be open.
	I/O Pins	Connected to VSS4 via pull-down resistor and these pins are set to slave mode.
	Input Pins	These pins should be connected to VSS4.

### 6. Absolute Maximum Ratings

(VSS1=VSS2=VSS3=VSS4=VSS5=0V; [Note 2](#), [Note 3](#))

Parameter		Symbol	min	max	Unit
Power Supplies:	Analog 1 (Rec, Play, etc)	AVDD1	-0.3	4.3	V
	Analog 2 (Play)	AVDD2	-0.3	4.3	V
	HP-Amp/Charge Pump	CVDD	-0.3	4.3	V
	Digital LDO	LVDD	-0.3	4.3	V
	Digital Core	VDD12	-0.3	1.6	V
	Digital I/F	TVDD	-0.3	4.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage ( <a href="#">Note 4</a> ) ( <a href="#">Note 5</a> ) ( <a href="#">Note 6</a> )		VINA1 VINA2 VINA3	-0.3 -CVDD -0.3	4.3 AVDD1+0.3 AVDD2+0.3	V V V
Digital Input Voltage ( <a href="#">Note 7</a> ) ( <a href="#">Note 8</a> ) ( <a href="#">Note 9</a> )		VIND1 VIND2 VIND3	-0.3 -0.3 -0.3	TVDD1+0.3 TVDD2+0.3 TVDD3+0.3	V V V
Ambient Temperature (powered applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 2. All voltages with respect to ground.

**Note 3. VSS1 to 5 must be connected to the same analog ground plane.**

Note 4. AIN1+/-, AIN2+/-, AIN3+/-, AIN4+/-, AIN5+/-, AIN6+/- pins

Note 5. HDT pin

Note 6. XTI, DTMIC pins

Note 7. MCKI, BCLK1, SYNC1, SDTI1A, SDTI1B, SDTI1C, SDTI1D, SBCLK, SBDATA, CSN/CAD, SCLK/SCK, SI/I2CFIL, PDN, CIF0-1, SBE, PSEL0-2, SBRC, TESTI pins

Note 8. BCLK2, SYNC2, SDTI2 pins

Note 9. BCLK3, SYNC3, SDTI3, BCLK4, SYNC4, SDTI4 pins

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device. Normal Operation is not guaranteed at these extremes.

## 7. Recommended Operating Conditions

(VSS1=VSS2=VSS3=VSS4=VSS5=0V; ([Note 2](#))

Parameter	Symbol	min	typ	max	Unit
Power Supplies <a href="#">(Note 13)</a>	Analog 1 (Rec, Play, etc.)	AVDD1	1.7	1.8	V
	Analog 2 (Play)	AVDD2	1.7	1.8	V
	HP-Amp / Charge Pump	CVDD	1.7	1.8	V
	Digital LDO ( <a href="#">Note 10</a> )	LVDD	1.7	1.8	V
	Digital Core (LDO2E pin="L", <a href="#">Note 11</a> )	VDD12	1.14	1.2	V
	Digital I/F 1 ( <a href="#">Note 12</a> )	TVDD1	1.65	1.8	V
	Digital I/F 2	TVDD2	1.65	1.8	V
	Digital I/F 3	TVDD3	1.65	1.8	V

Note 2. All voltages with respect to ground.

Note 10. 1.8V (typ) power supply should be supplied to the LVDD pin even if not using the LDO2 (LDO2E pin = "L").

Note 11. External 1.2V power supply is not necessary when using the LDO2 (LDO2E pin = "H").

**Note 12. When using SLIMbus interface, power supply range of TVDD1 is 1.65 to 1.95V.**

Note 13. Each power-up/down sequence is shown below.

<Power-Up>

1. PDN pin = "L"
2. TVDD1/2/3, AVDD1/2, LVDD, CVDD  
(The power-up sequence between TVDD1/2/3, AVDD1/2, LVDD and CVDD is not critical.)
3. VDD12(@ LDO2E pin = "L")
4. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

<Power-down>

1. PDN pin = "L"
2. VDD12 (@ LDO2E pin = "L")
3. TVDD1/2/3, AVDD1/2, LVDD, CVDD  
(The power-up sequence between TVDD1/2/3, AVDD1/2, LVDD and CVDD is not critical.)

## 8. Electrical Characteristics

### ■ Microphone & ADC Analog Characteristics

(Ta=25°C; AVDD1=AVDD2=CVDD=LVDD=TVDD1=TVDD2=TVDD3=1.8V;  
 VSS1-5=LGND=HPGND=RCVGND= 0V; Signal Frequency=1kHz; 24bit Data; fs=44.1kHz, BICK=64fs;  
 Measurement Bandwidth=20Hz ~ 20kHz; unless otherwise specified)

Parameter		min	typ	max	Unit
<b>MIC Amplifier:</b> AINn+/AINn- pins					
Input Resistance		140	200	260	kΩ
<b>MIC-Amp Gain</b>					
Gain Setting		0		+30	dB
Step Width		2	3	4	dB
<b>MIC Power Supply:</b> MPWR1A/1B/1C, MPWR2 pins					
Output Voltage (Note 14)	“00”	2.6	2.8	3.0	V
	“01”	2.3	2.5	2.7	
	“10”	1.7	1.8	1.9	
Load Resistance		2.0	-	-	kΩ
Load Capacitance		-	-	30	pF
Output Noise Level (A-weighted)	“00”	-	-114	-	dBV
	“01”	-	-114	-	
	“10”	-	-114	-	
<b>PSRR</b> (Note 15)					
217Hz		-	115	-	dB
1kHz		-	100	-	dB

Note 14. Microphone power output voltage of MPWR1A, MPWR1B and MPWR1C is common settings.  
 Microphone power output voltage of MPWR2 is independent setting. Output voltage is proportional to AVDD voltage. MICLx[1:0] bits = “00”: typ. 2.8 x AVDD/1.8V, “01”: typ. 2.5 x AVDD/1.8V, “10”: typ. 1.8 x AVDD/1.8V. When MICL1[1:0] bits is “11”, MPWR1A/B/C output AVDD1 via internal switch (Switch ON resistance: typ. 90Ω, max. 140Ω). When MICL2[1:0] bits is “11”, MPWR2 outputs the same voltage (typ. 1.8V) as MICL2[1:0] bits = “10”.

Note 15. PSRR is referred to all power supplies with 100mVpp sine wave.

Parameter		min	typ	max	Unit	
<b>ADC1 Lch/Rch, ADC2 Lch Analog Input Characteristics:</b>						
AINn+/AINn- pins(Differential Input) → ADC1/2 → SDTO1/2						
Resolution		-	-	24	Bits	
Input Full Scale Voltage(P-N)		0dB	1.85	2.02	Vpp	
		+18dB	0.235	0.255	Vpp	
S/(N+D)	-1dBFS	fs=44.1kHz BW=20kHz	0dB +18dB	85 93 82 90	- dB - dB	
		fs=96kHz BW=40kHz	0dB +18dB	- 86 - 84	- dB - dB	
		fs=44.1kHz BW=20kHz	0dB +18dB	- 39 - 32	- dB - dB	
		fs=96kHz BW=40kHz	0dB +18dB	- 36 - 29	- dB - dB	
D-Range (-60dBFS, A-weighted)		0dB +18dB	94 87	102 95	- dB	
S/N (A-weighted)		0dB +18dB	94 87	102 95	- dB	
Interchannel Isolation		0dB +18dB	- 80	110 100	- dB	
Interchannel Gain Mismatch			-	0	0.8	
PSRR (217Hz) (Note 16)		0dB +18dB	- -	90 80	- dB	

Note 16. PSRR is referred to all supplies with 100mVpp sine wave (ADC output data is -26.1dBFS).

typ. 90dB @ 0dB = -116.1dBFS, typ. 80dB @ +18dB = -106.1dBFS.

Parameter		min	typ	max	Unit		
<b>ADC1 Lch/Rch, ADC2 Lch Analog Input Characteristics:</b>							
AINn+ pins(Single-ended Input) → ADC1/2 → SDTO1/2							
Resolution		-	-	24	Bits		
Input Full Scale Voltage			0dB	-	2.02		
+6dB			0.92	1.01	1.09		
+18dB			0.235	0.255	0.275		
S/(N+D)	-1dBFS	fs=44.1kHz BW=20kHz	0dB	-	73		
			+6dB	-	84		
			+18dB	80	88		
		fs=96kHz BW=40kHz	0dB	-	70		
			+6dB	-	81		
			+18dB	-	83		
	-60dBFS	fs=44.1kHz BW=20kHz	0dB	-	39		
			+6dB	-	37		
			+18dB	-	32		
		fs=96kHz BW=40kHz	0dB	-	37		
			+6dB	-	35		
			+18dB	-	29		
Dynamic Range (-60dBFS, A-weighted)			0dB	-	102		
+6dB			-	-	dB		
+18dB			89	95	-		
S/N (A-weighted)			0dB	-	102		
+6dB			-	-	dB		
+18dB			89	95	-		
Interchannel Isolation			0dB	-	100		
+6dB			-	-	dB		
+18dB			80	100	-		
Interchannel Gain Mismatch			-	0	0.8		
PSRR (217Hz) (Note 17)			0dB	-	90		
			+6dB	-	90		
			+18dB	-	80		

Note 17. PSRR is referred to all supplies with 100mVpp sine wave (ADC output data is -26.1dBFS).  
 typ. 90dB @ 0dB, +6dB =-116.1dBFS, typ. 80dB @ +18dB = -106.1dBFS

Parameter		min	typ	max	Unit	
<b>ADC2 Rch Analog Input Characteristics:</b>						
AINn+/AINn- pins(Differential Input) → ADC2 Rch→ SDTO2						
Resolution		-	-	24	Bits	
Input Full Scale Voltage(P-N)		0dB	1.85	2.02	Vpp	
		+18dB	0.235	0.255	Vpp	
S/(N+D)	-1dBFS	fs=16kHz	0dB	82	90	
		BW=8kHz	+18dB	80	88	
		fs=44.1kHz	0dB	-	83	
		BW=20kHz	+18dB	-	80	
	-60dBFS	fs=16kHz	0dB	-	39	
		BW=8kHz	+18dB	-	31	
		fs=44.1kHz	0dB	-	35	
		BW=20kHz	+18dB	-	27	
D-Range (fs=44.1kHz, -60dBFS, A-weighted)		0dB	-	98	-	
		+18dB	82	90	-	
S/N (fs=44.1kHz ,A-weighted)		0dB	-	98	-	
		+18dB	82	90	-	
Interchannel Isolation (to ADC2 Lch)		0dB	-	110	-	
		+18dB	80	100	-	
Interchannel Gain Mismatch			-	0	0.8	
PSRR (217Hz) (Note 16)		0dB	-	90	-	
		+18dB	-	80	-	

Note 18. PSRR is referred to all supplies with 100mVpp sine wave (ADC output data is -26.1dBFS).

typ. 90dB @ 0dB =-116.1dBFS, typ. 80dB @ +18dB = -106.1dBFS

Parameter		min	Typ	max	Unit
<b>ADC2 Rch Analog Input Characteristics:</b>					
AINn+ pins(Single-ended Input) → ADC2 Rch → SDTO2					
Resolution		-	-	24	Bits
Input Full Scale Voltage(P-N)		0dB	-	2.02	-
		+6dB	0.92	1.01	1.09
		+18dB	0.235	0.255	0.275
S/(N+D)	-1dBFS	fs=16kHz BW=8kHz	0dB +6dB +18dB	85 92 88	- - -
		fs=44.1kHz BW=20kHz	0dB +6dB +18dB	87 87 80	- - -
		fs=16kHz BW=8kHz	0dB +6dB +18dB	39 37 31	- - -
		fs=44.1kHz BW=20kHz	0dB +6dB +18dB	35 34 29	- - -
		D-Range (fs=44.1kHz, -60dBFS, A-weighted)	0dB +6dB +18dB	98 96 80	- - -
		S/N (fs=44.1kHz, A-weighted)	0dB +6dB +18dB	98 96 80	- - -
	Interchannel Isolation (to ADC2 Lch)	0dB +6dB +18dB	-	110 110 100	- - -
		Interchannel Gain Mismatch	-	0	0.8
		PSRR (217Hz) (Note 16)	0dB +6dB +18dB	80 70 80	- - -

Note 19. PSRR is referred to all supplies with 100mVpp sine wave (ADC output data is -26.1dBFS).  
typ. 80dB @ 0dB, +18dB = -106.1dBFS, typ. 70dB @ +6dB = -96.1dBFS

## ■ DAC Analog Characteristics

(Ta=25°C; AVDD1=AVDD2=CVDD=LVDD=TVDD1=TVDD2=TVDD3=1.8V;  
 VSS1-5=LGND=HPGND=RCVGND=0V; Signal Frequency=1kHz; 24bit Data; fs=44.1kHz, BICK=64fs;  
 Measurement Bandwidth=20Hz ~ 20kHz; Rs = 0Ω; unless otherwise specified)

Parameter	min	Typ	max	Unit	
<b>Stereo DAC1 Characteristics:</b>					
Resolution	-	-	32	Bits	
<b>Headphone-Amp Characteristics:</b> DAC(Stereo) → HPL/HPR pins, OVL/R=0dB, HPG=0dB, RL=32Ω					
Output Power					
0dBFS, RL = 32Ω, HPG =0dB, THD+N < 0.1%	-	25	-	mW	
0dBFS, RL = 32Ω, HPG=-4dB	-	10	-	mW	
0dBFS, RL = 16Ω, HPG =0dB, THD+N < 0.1%	-	40	-	mW	
-1.5dBFS, RL = 16Ω, HPG =+2dB, THD+N < 10%	-	56	-	mW	
Output Level (0dBFS, RL = 32Ω, HPG=-4dB)	0.52	0.57	0.61	Vrms	
S/(N+D)					
0dBFS, Rs = 20Ω, RL = 32Ω, HPG=-4dB (Figure 2)	fs=44.1kHz BW=20kHz	-	99	-	dB
0dBFS, RL = 32Ω, HPG=-4dB (Po=10mW)	fs=44.1kHz BW=20kHz	87	97	-	dB
	fs=96kHz BW=40kHz	-	96	-	dB
	fs=192kHz BW=40kHz	-	96	-	dB
-60dBFS, RL = 32Ω, HPG=-4dB	fs=44.1kHz BW=20kHz	38	46	-	dB
	fs=96kHz BW=40kHz	35	43	-	dB
	fs=192kHz BW=40kHz	-	43	-	dB
Dynamic Range (-60dBFS, A-weighted, HPG=-4dB )		101	109		dB
S/N (A-weighted) Po=25mW, HPG=0dB (Data=0dBFS/ "0" Data) Po=10mW, HPG=-4dB (Data=0dBFS/ "0" Data)	-	110	-	dB	
Output Noise Level (A-weighted , HPG≤ -14dB)		101	109	-	dB
		-	-119	-111	dBV

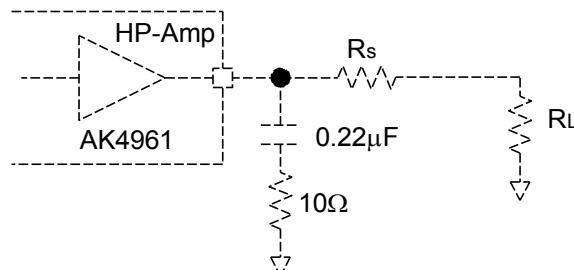


Figure 2. External Circuit for HP-Amp

Parameter	min	Typ	max	Unit
Interchannel Isolation 0dBFS, HPG=-4dB( $P_o = 10\text{mW}$ ) External Impedance = $0.03\Omega$ ( <a href="#">Note 21</a> ) External Impedance = $0.1\Omega$ ( <a href="#">Note 21</a> )	80 -	100 92	- -	dB dB
Interchannel Gain Mismatch	-	0	0.8	dB
Load Resistance	16	32	-	$\Omega$
Load Capacitance	-	-	300	pF
PSRR (HPG=-4dB) ( <a href="#">Note 20</a> )				
217Hz	-	85	-	dB
1kHz	-	85	-	dB
DC-offset ( <a href="#">Note 22</a> )				
HPG = 0dB	-0.15	0	+0.15	mV
HPG = All gain	-0.2	0	+0.2	mV
<b>Headphone Output Volume Characteristics:</b>				
Gain Setting	-40	-	+6	dB
Step Width	Gain: +6 ~ -40dB	1	2	3

Note 20. PSRR is referred to all power supply voltages with  $100\text{mVpp}$  sine wave.

Note 21. External impedance between the HPGND pin and the system ground.

Note 22. When there is no gain change and temperature drift after HP-Amp is powered-up.

Parameter	min	typ	max	Unit	
<b>Stereo DAC2 Characteristics:</b>					
Resolution	-	-	24	Bits	
<b>Lineout-Amp 1 Characteristics:</b> DAC2(Stereo) → LOUT1/ROUT1 pins, OVL/R=0dB, LO1G=0dB, $R_L=10\text{k}\Omega$					
Output Full Scale Level	2.10	2.32	2.57	Vpp	
S/(N+D)					
0dBFS (Vo=0.82Vrms)	fs=44.1kHz BW=20kHz	76	86	- dB	
	fs=96kHz BW=40kHz	-	86	- dB	
	fs=192kHz BW=40kHz	-	86	- dB	
-60dBFS	fs=44.1kHz BW=20kHz	30	38	- dB	
	fs=96kHz BW=40kHz	28	36	- dB	
	fs=192kHz BW=40kHz	-	36	- dB	
Dynamic Range (-60dBFS, A-weighted)	92	100		dB	
S/N (A-weighted)	92	100	-	dB	
Interchannel Isolation	80	100	-	dB	
Interchannel Gain Mismatch	-	0	0.8	dB	
Load Resistance	10		-	$\text{k}\Omega$	
Load Capacitance	-	-	30	pF	
PSRR (Note 23)					
217Hz	-	80	-	dB	
1kHz	-	80	-	dB	
DC Offset (LO1G = 0dB)	-8	0	+8	mV	
<b>Lineout 1 Volume Characteristics:</b>					
Gain Setting	-7.5	-	+3	dB	
Step Width	Gain: +3 ~ -7.5dB	1	1.5	2	dB

Note 23. PSRR is referred to all power supply voltages with 100mVpp sine wave.

Parameter		min	typ	max	Unit
<b>Stereo DAC2 Characteristics:</b>					
Resolution		-	-	24	Bits
<b>Lineout-Amp 2 Characteristics:</b>					
DAC2(Stereo) → LOUT2/ROUT2 pins, OVL/R=0dB, LO2G=0dB, $R_L=10\text{k}\Omega$					
Output Full Scale Level		2.10	2.32	2.57	Vpp
S/(N+D)					
0dBFS (Vo=0.82Vrms)	fs=44.1kHz BW=20kHz	76	86	-	dB
	fs=96kHz BW=40kHz	-	86	-	dB
	fs=192kHz BW=40kHz	-	86	-	dB
-60dBFS	fs=44.1kHz BW=20kHz	30	38	-	dB
	fs=96kHz BW=40kHz	28	36	-	dB
	fs=192kHz BW=40kHz	-	36	-	dB
Dynamic Range (-60dBFS, A-weighted)		92	100		dB
S/N (A-weighted)		92	100	-	dB
Interchannel Isolation		80	100	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance		10		-	$\text{k}\Omega$
Load Capacitance		-	-	30	pF
PSRR (Note 24)					
217Hz		-	80	-	dB
	1kHz	-	80	-	dB
DC Offset (LO2G = 0dB)		-8	0	+8	mV
<b>Lineout 2 Volume Characteristics:</b>					
Gain Setting		-7.5	-	+3	dB
Step Width	Gain: +3 ~ -7.5dB	1	1.5	2	dB

Note 24. PSRR is referred to all power supply voltages with 100mVpp sine wave.

Parameter		min	typ	max	Unit
<b>Lineout-Amp 2 Characteristics:</b>					
DAC2(Stereo) → LOP/N, ROP/N pins, OVL/R=0dB, LO2G=0dB, $R_L=20\text{k}\Omega$					
Output Full Scale Level		2.10	2.32	2.57	Vpp
S/(N+D)					
0dBFS ( $V_o=0.82\text{Vrms}$ )	fs=44.1kHz BW=20kHz	78	88	-	dB
	fs=96kHz BW=40kHz	-	88	-	dB
	fs=192kHz BW=40kHz	-	88	-	dB
-60dBFS	fs=44.1kHz BW=20kHz	30	38	-	dB
	fs=96kHz BW=40kHz	26	34	-	dB
	fs=192kHz BW=40kHz	-	36	-	dB
Dynamic Range (-60dBFS, A-weighted)		92	100		dB
S/N (A-weighted)		92	100	-	dB
Interchannel Isolation		80	100	-	dB
Interchannel Gain Mismatch		-	0	0.8	dB
Load Resistance (Pout – Nout)		20		-	$\text{k}\Omega$
Load Capacitance (for GND)		-	-	30	pF
PSRR (Note 25)					
217Hz		-	80	-	dB
		-	80	-	dB
DC Offset (LO2G = 0dB, Pout-Nout)		-8	0	+8	mV
<b>Lineout 2 Volume Characteristics:</b>					
Gain Setting		-7.5	-	+3	dB
Step Width	Gain: +3~ -7.5dB	1	1.5	2	dB

Note 25. PSRR is referred to all power supply voltages with 100mVpp sine wave.

Parameter		min	Typ	max	Unit
<b>Receiver-Amp Characteristics:</b> DAC2(Mono) → RCP/RCN pins, OVL/R=0dB, RCVG=0dB, $R_L=32\Omega$					
Output Power					
0dBFS, RCVG =+1.5dB, THD+N = 1%		75	100	-	mW
Output Level (0dBFS, $R_L=32\Omega$ , RCVG=-4.5dB)		2.44	2.7	2.98	Vpp
S/(N+D)					
0dBFS, RCVG=-4.5dB (Po=30mW)	fs=44.1kHz BW=20kHz	72	87	-	dB
	fs=96kHz BW=40kHz	-	86	-	dB
-60dBFS, RCVG=-4.5dB	fs=44.1kHz BW=20kHz	30	38	-	dB
	fs=96kHz BW=40kHz	27	35	-	dB
Dynamic Range (-60dBFS, A-weighted, RCVG=-4.5dB)		92	100		dB
S/N (A-weighted, Po=30mW, RCVG=-4.5dB Data = 0dBFS/0 Data)		92	100	-	dB
Load Resistance (Pout-Nout)		32	-	-	$\Omega$
Load Capacitance (for GND)		-	-	30	pF
PSRR (RCVG=-4.5dB) (Note 26)					
217Hz		-	80	-	dB
	1kHz	-	80	-	dB
DC-offset (Note 27) RCVG = All gain		-0.5	0	+0.5	mV
<b>Receiver Output Volume Characteristics:</b>					
Gain Setting		-7.5	-	+3	dB
Step Width	Gain: +3 ~ -7.5dB	1	1.5	2	dB

Note 26. PSRR is referred to all power supply voltages with 100mVpp sine wave.

Note 27. When there is no gain change and temperature drift after RCV-Amp is powered-up.

## ■ Power Supply Current

(Ta=25°C; AVDD1=AVDD2=CVDD=LVDD=TVDD1=TVDD2=TVDD3=1.8V;  
VSS1-5=LGND=HPGND=RCVGND=0V; unless otherwise specified)

Parameter	min	typ	max	Unit
<b>Power Supply Current:</b>				
Power Up (PDN pin = “H”, LDO2 Enable, PMSW bit = “0”, Other Circuits Power-down)				
AVDD1 + AVDD2 + CVDD + LVDD + TVDD1+ TVDD2 + TVDD3	-	0.5	1.6	mA
Power Up (PDN pin = “H”, LDO2 Enable, PMSW bit = “1”, Other Circuits Power-down)				
AVDD1 + AVDD2 + CVDD + LVDD + TVDD1+ TVDD2 + TVDD3	-	0.8	8.6	mA
Power Up (PDN pin = “L”, LDO2 Disable) ( <a href="#">Note 28</a> )				
AVDD1 + AVDD2 + CVDD + LVDD + TVDD1+ TVDD2 + TVDD3	-	50	300	μA
Power Down (PDN pin = “L”, LDO2 Enable) ( <a href="#">Note 28</a> )				
AVDD1 + AVDD2 + CVDD + LVDD + TVDD1+ TVDD2 + TVDD3	-	0	20	μA

Note 28. All digital input pins are fixed to each supply pin TVDD1-3 or VSS4.

Maximum value of each power supply line is as follows.

AVDD1+AVDD2: 20mA

CVDD: 100mA @ Po=40mW, 16Ω, Stereo

LVDD: 50mA @ LDO2 Enable, 1mA @ LDO2 Disable

VDD12= 0mA @ LDO2 Disable, 50mA @ LDO2 Enable

TVDD1: 6mA @ SBE pin = “H”, 2mA @ SBE pin = “L”

TVDD2: 2mA,

TVDD3: 2mA

## ■Power Consumption for Each Operation Mode

Conditions:

T<sub>a</sub>=25°C; AVDD1=AVDD2=CVDD=LVDD=TVDD1=TVDD2=TVDD3=1.8V; LDO2 Enable  
VSS1-5=0V; External Slave Mode, MCKI=256fs, BICK=64fs; Direct Interface Mode. No data input,  
No Load. MPWR OFF (CKSELCP1[1:0] bits = “11”; CP1 switching Frequency =62.5kHz)

Mode	AVDD1-2 [mA]	CVDD [mA]	LVDD [mA]	TVDD1-3 [mA]	Total Power [mW]
Voice Wakeup (MIC Power: Direct Mode, ADC fs=16kHz)	0.43	0.66	0.34	0.02	2.6
Jack Detection	0.12	0	0.26	0.01	0.7
AIN1/AIN2(Stereo) → ADC (fs=44.1kHz)	0.68	2.42	0.71	0.03	6.9
AIN1/AIN2(stereo) → ADC(fs=96kHz)	1.71	2.90	1.32	0.04	10.8
DAC → HP (fs=44.1kHz)	1.98	2.91	0.39	0.01	9.5
DAC → HP (fs=96kHz)	1.98	2.96	0.51	0.01	9.8
DAC → HP (fs=192kHz)	1.98	2.96	0.57	0.01	9.9
DAC → RCV (fs=44.1kHz)	1.61	1.04	0.42	0.01	5.5
DAC → LINEOUT1 (fs=44.1kHz)	1.83	0.60	0.42	0.01	5.1
DAC → LINEOUT1 (fs=192kHz)	2.13	0.88	0.58	0.09	6.6
DAC → LINEOUT2 (fs=44.1kHz)					
Mono Single-ended	1.12	0.44	0.42	0.01	3.6
Mono Differential	1.26	0.60	0.42	0.01	4.1
Stereo Single-ended	1.83	0.60	0.42	0.01	5.1
Stereo Differential	2.11	0.92	0.42	0.01	6.2

Table 1. Power Consumption for Each Operation Mode (typ)

## ■ SRCA/B/C/D Characteristics

(Ta=-40~85 °C; AVDD1 =AVDD2 =CVDD =LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V;  
Signal Frequency = 1kHz; 24bit Data, Measurement Bandwidth = 20Hz ~ FSO/2; Unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Resolution				24	Bits
Input Sample Rate	FSI	8		192	kHz
Output Sample Rate	FSO	8		192	kHz
THD+N (Input= 1kHz, 0dBFS) FSO/FSI=192kHz/48kHz FSO/FSI=192kHz/44.1kHz FSO/FSI=44.1kHz/48kHz FSO/FSI=44.1kHz/96kHz FSO/FSI=48kHz/44.1kHz FSO/FSI=48kHz/96kHz FSO/FSI=48kHz/8kHz FSO/FSI=16kHz/48kHz FSO/FSI=16kHz/44.1kHz FSO/FSI=8kHz/48kHz FSO/FSI=8kHz/44.1kHz FSO/FSI=48kHz/192kHz FSO/FSI=44.1kHz/192kHz		-	-113	-	dB
Dynamic Range (Input= 1kHz, -60dBFS) FSO/FSI=192kHz/48kHz FSO/FSI=192kHz/44.1kHz FSO/FSI=44.1kHz/48kHz FSO/FSI=44.1kHz/96kHz FSO/FSI=48kHz/44.1kHz FSO/FSI=48kHz/96kHz FSO/FSI=48kHz/8kHz FSO/FSI=16kHz/48kHz FSO/FSI=16kHz/44.1kHz FSO/FSI=8kHz/48kHz FSO/FSI=8kHz/44.1kHz FSO/FSI=48kHz/192kHz FSO/FSI=44.1kHz/192kHz		-	113	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted, FSO/FSI=44.1kHz/48kHz)		108	113	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

## ■ SRCE Characteristics

(Ta=-40~85 °C; AVDD1 =AVDD2 =CVDD =LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V;  
Signal Frequency = 1kHz; 24bit Data, Measurement Bandwidth = 20Hz ~ FSO/2; Unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Resolution				32	Bits
Input Sample Rate	FSI	8		192	kHz
Output Sample Rate	FSO	8		192	kHz
THD+N (Input= 1kHz, 0dBFS) FSO/FSI=192kHz/48kHz FSO/FSI=192kHz/44.1kHz FSO/FSI=44.1kHz/48kHz FSO/FSI=44.1kHz/96kHz FSO/FSI=48kHz/44.1kHz FSO/FSI=48kHz/96kHz FSO/FSI=48kHz/8kHz FSO/FSI=16kHz/48kHz FSO/FSI=16kHz/44.1kHz FSO/FSI=8kHz/48kHz FSO/FSI=8kHz/44.1kHz FSO/FSI=48kHz/192kHz FSO/FSI=44.1kHz/192kHz		-	-120	-	dB
Dynamic Range (Input= 1kHz, -60dBFS) FSO/FSI=192kHz/48kHz FSO/FSI=192kHz/44.1kHz FSO/FSI=44.1kHz/48kHz FSO/FSI=44.1kHz/96kHz FSO/FSI=48kHz/44.1kHz FSO/FSI=48kHz/96kHz FSO/FSI=48kHz/8kHz FSO/FSI=16kHz/48kHz FSO/FSI=16kHz/44.1kHz FSO/FSI=8kHz/48kHz FSO/FSI=8kHz/44.1kHz FSO/FSI=48kHz/192kHz FSO/FSI=44.1kHz/192kHz		-	140	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted, FSO/FSI=44.1kHz/48kHz)		135	140	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

## ■ ADC Sharp Roll-Off Filter 1 (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; ADxSD[1:0] bits = “00”)

Parameter	Symbol	min	typ	max	Unit
<b>ADC Digital Filter (Decimation LPF):</b>					
Passband (Note 29)	PB	0	-	19.1	kHz
-0.87dB		-	19.9	-	kHz
-3.0dB		-	20.9	-	kHz
-6.0dB			21.8	-	kHz
-7.0dB		-	22.05	-	kHz
Stopband (Note 29)	SB	26.1	-	-	kHz
Passband Ripple	PR	-0.09	-	+0.16	dB
Stopband Attenuation	SA	65	-	-	dB
Group Delay (Note 30)	GD	-	12.1	-	1/fs
Group Delay Distortion	ΔGD	-	0	-	μs
<b>ADC Digital Filter (HPF): HPFC1-0 bits = “00”</b>					
Frequency Response (Note 29)	FR	-	3.4	-	Hz
-3.0dB		-	10	-	Hz
-0.5dB		-	22	-	Hz
-0.1dB					

Note 29. The passband and stopband frequencies scale with fs (system sampling rate).

For example, ADC is PB=0.433 x fs (@-0.09/+0.16dB). Each response refers to that of 1kHz.

Note 30. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 24-bit data of both channels from the input register to the output register of the ADC. This time includes group delay of the HPF.

## ■ ADC Sharp Roll-Off Filter 2 (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; ADxSD[1:0] bits = “01”)

Parameter	Symbol	min	typ	max	Unit
<b>ADC Digital Filter (Decimation LPF):</b>					
Passband (Note 31)	PB	0	-	19.4	kHz
-0.163dB		-	19.9	-	kHz
-3.0dB		-	21.69	-	kHz
-4.25dB			22.05	-	kHz
-6.0dB		-	22.46	-	kHz
Stopband (Note 31)	SB	26.1	-	-	kHz
Passband Ripple	PR	-0.02	-	+0.05	dB
Stopband Attenuation	SA	65	-	-	dB
Group Delay (Note 32)	GD	-	14.1	-	1/fs
Group Delay Distortion	ΔGD	-	0	-	μs
<b>ADC Digital Filter (HPF): HPFC1-0 bits = “00”</b>					
Frequency Response (Note 31)	FR	-	3.4	-	Hz
-3.0dB		-	10	-	Hz
-0.5dB		-	22	-	Hz
-0.1dB					

Note 31. The passband and stopband frequencies scale with fs (system sampling rate).

For example, ADC is PB=0.44 x fs (@-0.02/+0.05dB). Each response refers to that of 1kHz.

Note 32. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 24-bit data of both channels from the input register to the output register of the ADC. This time includes group delay of the HPF.

## ■ ADC Short Delay Sharp Roll-Off Filter (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; ADxSD[1:0] bits = “10”)

Parameter	Symbol	min	typ	max	Unit
<b>ADC Digital Filter (Decimation LPF):</b>					
Passband (Note 33)	+0.16dB ~ -0.11dB	PB	0	-	19.1 kHz
	-0.87dB		-	19.9	- kHz
	-3.0dB		-	20.9	- kHz
	-6.0dB		-	21.8	- kHz
	-7.0dB		-	22.05	- kHz
Stopband (Note 33)	SB	26.1	-	-	kHz
Passband Ripple	PR	-0.11	-	+0.16	dB
Stopband Attenuation	SA	64	-	-	dB
Group Delay (Note 34)	GD	-	4.7	-	1/fs
Group Delay Distortion	ΔGD	-	-	±1.94	1/fs
<b>ADC Digital Filter (HPF): HPFC1-0 bits = “00”</b>					
Frequency Response (Note 33)	-3.0dB	FR	-	3.4	- Hz
	-0.5dB		-	10	- Hz
	-0.1dB		-	22	- Hz

Note 33. The passband and stopband frequencies scale with fs (system sampling rate).

For example, ADC is PB=0.433 x fs (@-0.11/+0.16dB). Each response refers to that of 1kHz.

Note 34. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 24-bit data of both channels from the input register to the output register of the ADC. This time includes group delay of the HPF.

### ■ DAC1 Sharp Roll-Off Filter (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; DFTHR1 bit = “0”, DA1SD bit = “0”, DA1SL bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 35)	-0.006dB ~+0.23dB -6.0dB	PB	0 -	- 22.07	20.6 - kHz kHz
Stopband (Note 35)	SB	24.1	-	-	kHz
Passband Ripple	PR	-0.006	-	+0.23	dB
Stopband Attenuation	SA	69.8	-	-	dB
Group Delay (Note 36)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 20.0kHz	FR	-0.12	-	+0.1	dB

Note 35. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.467 \times fs(@-0.006/+ 0.23dB)$ , SB =  $0.5465 \times fs$ . Each frequency response refers to that of 1kHz.

Note 36. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Sharp Roll-Off Filter (fs=96kHz)

(Ta=-40~85 °C; AVDD = CVDD1=CVDD2=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=96kHz; DFTHR1 bit = “0”, DA1SD bit = “0”, DA1SL bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 37)	-0.003dB ~ +0.24dB -6.0dB	PB	0 -	- 48.04	44.85 - kHz kHz
Stopband (Note 37)	SB	52.5	-	-	kHz
Passband Ripple	PR	-0.003	-	+0.24	dB
Stopband Attenuation	SA	69.8	-	-	dB
Group Delay (Note 38)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 40.0kHz	FR	-0.72	-	+0.11	dB

Note 37. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.4672 \times fs(@-0.003/+0.24dB)$ , SB =  $0.547 \times fs$ . Each frequency response refers to that of 1kHz.

Note 38. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Sharp Roll-Off Filter (fs=192kHz)

(Ta=-40~85 °C; AVDD1= AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V;  
fs=192kHz; DFTHR1 bit = “0”, DA1D bit = “0”, DA1SL bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 39)	PB	0 -6.0dB	-	96.08	kHz kHz
Stopband (Note 39)	SB	104.9	-	-	kHz
Passband Ripple	PR	-0.002	-	+0.24	dB
Stopband Attenuation	SA	69.8	-	-	dB
Group Delay (Note 40)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 80.0kHz	FR	-3.00	-	+0.35	dB

Note 39. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.4674 \times fs(@-0.002/+0.24dB)$ , SB =  $0.5465 \times fs$ . Each frequency response refers to that of 1kHz.

Note 40. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Slow Roll-Off Filter (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1 = AVDD2 = CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; DFTHR1 bit = “0”, DA1SD bit = “0”, DA1SL bit = “1”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 41)	PB	0 -3.0dB	-	18.51	7.8 kHz kHz
Stopband (Note 41)	SB	39.11	-	-	kHz
Passband Ripple	PR	-0.07	-	+0.005	dB
Stopband Attenuation	SA	72.8	-	-	dB
Group Delay (Note 42)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 20.0kHz	FR	-4.34	-	+0.03	dB

Note 41. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.1769 \times fs(@-0.07/+0.005dB)$ , SB =  $0.887 \times fs$ . Each frequency response refers to that of 1kHz.

Note 42. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Slow Roll-Off Filter (fs=96kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=96kHz; DFTHR1 bit = “0”, DA1SD bit = “0”, DA1SL bit = “1”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 43)	PB	0 -3.0dB	-	40.3	17.02 kHz kHz
Stopband (Note 43)	SB	85.2	-	-	kHz
Passband Ripple	PR	-0.07	-	+0.006	dB
Stopband Attenuation	SA	72.8	-	-	dB
Group Delay (Note 44)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 40.0kHz	FR	-4.00	-	+0.1	dB

Note 43. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.1773 \times fs(@-0.07/+0.006dB)$ , SB =  $0.887 \times fs$ . Each frequency response refers to that of 1kHz.

Note 44. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

## ■ DAC1 Slow Roll-Off Filter (fs=192kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=192kHz; DFTHR1 bit = “0”, DA1SD bit = “0”, DA1SL bit = “1”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband <a href="#">(Note 45)</a>	PB	0	-	34.17	kHz
-3.0dB		-	80.65	-	kHz
Stopband <a href="#">(Note 45)</a>	SB	170.3	-	-	kHz
Passband Ripple	PR	-0.07	-	+0.006	dB
Stopband Attenuation	SA	72.8	-	-	dB
Group Delay <a href="#">(Note 46)</a>	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 80.0kHz	FR	-6.10	-	+0.35	dB

Note 45. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.178 \times fs(@-0.07/+0.006dB)$ , SB =  $0.887 \times fs$ . Each frequency response refers to that of 1kHz.

Note 46. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Short Delay Sharp Roll-Off Filter (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; DFTHR1 bit = “0”, DA1SD bit = “1”, DA1SL bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 47)	PB	0 -6.0dB	-	22.19	20.59 kHz kHz
Stopband (Note 47)	SB	24.1	-	-	kHz
Passband Ripple	PR	-0.009	-	+0.232	dB
Stopband Attenuation	SA	56.2	-	-	dB
Group Delay (Note 48)	GD	-	5.5	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 20.0kHz	FR	-0.12	-	+0.1	dB

Note 47. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.4669 \times fs(@-0.009/+0.232dB)$ , SB =  $0.5465 \times fs$ . Each frequency response refers to that of 1kHz.

Note 48. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Short Delay Sharp Roll-Off Filter (fs=96kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=96kHz; DFTHR1 bit = “0”, DA1SD bit = “1”, DA1SL bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 49)	PB	0 -6.0dB	- 48.32	44.82	kHz kHz
Stopband (Note 49)	SB	52.5	-	-	kHz
Passband Ripple	PR	-0.004	-	+0.238	dB
Stopband Attenuation	SA	56.2	-	-	dB
Group Delay (Note 50)	GD	-	5.5	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 40.0kHz	FR	-0.90	-	+0.11	dB

Note 49. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.4669 \times fs(@-0.004/+0.238dB)$ , SB =  $0.5465 \times fs$ . Each frequency response refers to that of 1kHz.

Note 50. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

## ■ DAC1 Short Delay Sharp Roll-Off Filter (fs=192kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=192kHz; DFTHR1 bit = “0”, DA1SD bit = “1”, DA1SL bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband <a href="#">(Note 51)</a>	PB	0 -	- 96.64	89.68 -	kHz kHz
Stopband <a href="#">(Note 51)</a>	SB	104.9	-	-	kHz
Passband Ripple	PR	-0.002	-	+0.247	dB
Stopband Attenuation	SA	56.2	-	-	dB
Group Delay <a href="#">(Note 52)</a>	GD	-	5.5	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 80.0kHz	FR	-3.10	-	+0.36	dB

Note 51. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.4671 \times fs(@-0.002/+0.247dB)$ , SB =  $0.5464 \times fs$ . Each frequency response refers to that of 1kHz.

Note 52. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Short Delay Slow Roll-Off Filter (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; DFTHR<sub>x</sub> bit = “0”, DA1SD bit = “1”, DA1SL bit = “1”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 53)	PB	0 -3.0dB	-	18.9	kHz kHz
Stopband (Note 53)	SB	39.49	-	-	kHz
Passband Ripple	PR	-0.07	-	+0.025	dB
Stopband Attenuation	SA	75.1	-	-	dB
Group Delay (Note 54)	GD	-	4.7	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 20.0kHz	FR	-4.06	-	+0.04	dB

Note 53. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.2045 \times fs(@-0.07/+0.025dB)$ , SB =  $0.8955 \times fs$ . Each frequency response refers to that of 1kHz.

Note 54. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ DAC1 Short Delay Slow Roll-Off Filter (fs=96kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=96kHz; DFTHR<sub>1</sub> bit = “0”, DA1SD bit = “1”, DA1SL bit = “1”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 55)	PB	0 -3.0dB	-	19.7 41.16	kHz kHz
Stopband (Note 55)	SB	85.97	-	-	kHz
Passband Ripple	PR	-0.07	-	+0.027	dB
Stopband Attenuation	SA	75.1	-	-	dB
Group Delay (Note 56)	GD	-	4.7	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 40.0kHz	FR	-3.80	-	+0.1	dB

Note 55. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.2052 \times fs(@-0.07/+0.027dB)$ , SB =  $0.8955 \times fs$ . Each frequency response refers to that of 1kHz.

Note 56. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

## ■ DAC1 Short Delay Slow Roll-Off Filter (fs=192kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=192kHz; DFTHR1 bit = “0”, DA1SD bit = “1”, DA1SL bit = “1”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband <a href="#">(Note 57)</a>	PB	0 -	- 82.37	39.54 -	kHz kHz
Stopband <a href="#">(Note 57)</a>	SB	172	-	-	kHz
Passband Ripple	PR	-0.07	-	+0.028	dB
Stopband Attenuation	SA	75.1	-	-	dB
Group Delay <a href="#">(Note 58)</a>	GD	-	4.7	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Headphone-Amp):</b>					
Frequency Response: 0 ~ 80.0kHz	FR	-6.00	-	+0.35	dB

Note 57. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.2059 \times fs(@-0.07/+0.028dB)$ , SB =  $0.8958 \times fs$ . Each frequency response refers to that of 1kHz.

Note 58. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

## ■ DAC2 Sharp Roll-Off Filter (fs=44.1kHz)

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=44.1kHz; DITHER2 bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 59)	PB	0 -6.0dB	- 22.04	20.13 -	kHz kHz
Stopband (Note 59)	SB	24.1	-	-	kHz
Passband Ripple	PR	-0.05	-	+0.06	dB
Stopband Attenuation	SA	69.9	-	-	dB
Group Delay (Note 60)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Lineout1-Amp, Lineout2 –Amp: Single-ended Mode):</b>					
Frequency Response: 0 ~ 20.0kHz	FR	-0.18	-	+0.12	dB
<b>DAC Digital Filter (LPF) + DACANA(Lineout2-Amp, Differential Mode):</b>					
Frequency Response: 0 ~ 20.0kHz	FR	-0.18	-	+0.12	dB
<b>DAC Digital Filter (LPF) + DACANA(Receiver-Amp):</b>					
Frequency Response: 0 ~ 20.0kHz	FR	-0.18	-	+0.12	dB

Note 59. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.4565 \times fs$ (@-0.05/+ 0.06dB), SB =  $0.5469 \times fs$ . Each frequency response refers to that of 1kHz.

Note 60. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

## ■ DAC2 Sharp Roll-Off Filter (fs=96kHz)

(Ta=-40~85 °C; AVDD = CVDD1=CVDD2=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V; fs=96kHz; DITHER2 bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 61)	PB	0 -6.0dB	- 47.79	43.87 -	kHz kHz
Stopband (Note 61)	SB	52.5	-	-	kHz
Passband Ripple	PR	-0.05	-	+0.06	dB
Stopband Attenuation	SA	69.9	-	-	dB
Group Delay (Note 62)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Lineout1-Amp, Lineout2 –Amp: Single-ended Mode):</b>					
Frequency Response: 0 ~ 40.0kHz	FR	-0.36	-	+0.04	dB
<b>DAC Digital Filter (LPF) + DACANA(Lineout2-Amp, Differential Mode):</b>					
Frequency Response: 0 ~ 40.0kHz	FR	-0.36	-	+0.04	dB
<b>DAC Digital Filter (LPF) + DACANA(Receiver-Amp):</b>					
Frequency Response: 0 ~ 40.0kHz	FR	-0.36	-	+0.24	dB

Note 61. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.457 \times fs$ (@-0.05/+ 0.06dB), SB =  $0.5469 \times fs$ . Each frequency response refers to that of 1kHz.

Note 62. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

## ■ DAC2 Sharp Roll-Off Filter (fs=192kHz)

(Ta=-40~85 °C; AVDD1= AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V;  
fs=192kHz; DITHER2 bit = “0”)

Parameter	Symbol	min	typ	max	Unit
<b>DAC Digital Filter (LPF):</b>					
Passband (Note 63)	PB	0 -6.0dB	-	95.94	87.82 kHz kHz
Stopband (Note 63)	SB	104.9	-	-	kHz
Passband Ripple	PR	-0.05	-	+0.06	dB
Stopband Attenuation	SA	69.9	-	-	dB
Group Delay (Note 64)	GD	-	26	-	1/fs
<b>DAC Digital Filter (LPF) + DACANA(Lineout1-Amp, Lineout2 -Amp: Single-ended Mode):</b>					
Frequency Response: 0 ~ 80.0kHz	FR	-1.10	-	+0.10	dB
<b>DAC Digital Filter (LPF) + DACANA(Lineout2-Amp, Differential Mode):</b>					
Frequency Response: 0 ~ 80.0kHz	FR	-1.10	-	+0.10	dB

Note 63. The passband and stopband frequencies scale with fs(system sampling rate).

DAC is PB =  $0.4574 \times fs(@-0.05/+ 0.06dB)$ , SB =  $0.5464 \times fs$ . Each frequency response refers to that of 1kHz.

Note 64. The calculated delay time caused by digital filtering. This time is from setting the 16/24/32-bit impulse data of both channels from the input register to the output of analog peak signal.

### ■ SRCA/B/C/D Filter Characteristics

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V)

Parameter		Symbol	min	typ	max	Unit
Passband	-0.01dB	0.980≤FSO/FSI≤6.000	PB	0	-	0.4583FSI kHz
	-0.01dB	0.900≤FSO/FSI<0.990	PB	0	-	0.4167FSI kHz
	-0.01dB	0.533≤FSO/FSI<0.909	PB	0	-	0.2182FSI kHz
	-0.01dB	0.490≤FSO/FSI<0.539	PB	0	-	0.2177FSI kHz
	-0.01dB	0.450≤FSO/FSI<0.495	PB	0	-	0.1948FSI kHz
	-0.01dB	0.225≤FSO/FSI<0.455	PB	0	-	0.1312FSI kHz
	-0.50dB	0.167≤FSO/FSI<0.227	PB	0	-	0.0658FSI kHz
Stopband	0.980≤FSO/FSI≤6.000	SB	0.5417FSI	-	-	kHz
	0.900≤FSO/FSI<0.990	SB	0.5021FSI	-	-	kHz
	0.533≤FSO/FSI<0.909	SB	0.2974FSI	-	-	kHz
	0.490≤FSO/FSI<0.539	SB	0.2812FSI	-	-	kHz
	0.450≤FSO/FSI<0.495	SB	0.2604FSI	-	-	kHz
	0.225≤FSO/FSI<0.455	SB	0.1802FSI	-	-	kHz
	0.167≤FSO/FSI<0.227	SB	0.0970FSI	-	-	kHz
Passband Ripple	0.225≤FSO/FSI≤6.000	PR	-	-	±0.01	dB
	0.167≤FSO/FSI<0.227	PR	-	-	±0.50	dB
Stopband Attenuation	0.450≤FSO/FSI≤6.000	SA	95.2	-	-	dB
	0.167≤FSO/FSI<0.455	SA	90.0	-	-	dB
Group Delay <a href="#">(Note 65)</a>		GD	-	61 (54/FSI + 7/FSO)	-	1/fs

Note 65. This value is SRC block only. It is the time from a rising edge of SYNC after data is input to a rising edge of SYNC just before the data is output when there is no phase difference between input and output.

## ■ SRCE Filter Characteristics

(Ta=-40~85 °C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V; TVDD1=TVDD2=TVDD3=1.65 ~ 3.6V)

<Sharp Roll-Off Filter>

Parameter			Symbol	min	typ	max	Unit
Passband	-0.01dB	0.980≤FSO/FSI≤6.000	PB	0	-	0.4583FSI	kHz
	-0.01dB	0.711≤FSO/FSI<0.990	PB	0	-	0.4167FSI	kHz
	-0.01dB	0.533≤FSO/FSI<0.718	PB	0	-	0.2183FSI	kHz
	-0.01dB	0.490≤FSO/FSI<0.539	PB	0	-	0.2177FSI	kHz
	-0.01dB	0.356≤FSO/FSI<0.495	PB	0	-	0.1948FSI	kHz
	-0.01dB	0.225≤FSO/FSI<0.359	PB	0	-	0.0917FSI	kHz
	-0.01dB	0.167≤FSO/FSI<0.248	PB	0	-	0.0826FSI	kHz
Stopband		0.980≤FSO/FSI≤6.000	SB	0.5417FSI	-	-	kHz
		0.711≤FSO/FSI<0.990	SB	0.5021FSI	-	-	kHz
		0.533≤FSO/FSI<0.718	SB	0.2974FSI	-	-	kHz
		0.490≤FSO/FSI<0.539	SB	0.2813FSI	-	-	kHz
		0.356≤FSO/FSI<0.495	SB	0.2604FSI	-	-	kHz
		0.225≤FSO/FSI<0.359	SB	0.1573FSI	-	-	kHz
		0.167≤FSO/FSI<0.248	SB	0.1471FSI	-	-	kHz
Passband Ripple		0.167≤FSO/FSI≤6.000	PR	-	-	±0.01	kHz
Stopband Attenuation		0.980≤FSO/FSI≤6.000	SB	-121.2	-	-	kHz
		0.711≤FSO/FSI<0.990	SB	-121.4	-	-	kHz
		0.533≤FSO/FSI<0.718	SB	-114.6	-	-	kHz
		0.490≤FSO/FSI<0.539	SB	-100.2	-	-	kHz
		0.356≤FSO/FSI<0.495	SB	-103.3	-	-	kHz
		0.225≤FSO/FSI<0.359	SB	-104.0	-	-	kHz
		0.167≤FSO/FSI<0.248	SB	-103.3	-	-	kHz
Group Delay <a href="#">(Note 66)</a>			GD	-	62 (54/FSI + 8/FSO)	-	1/fs

Note 66. This value is SRC block only. It is the time from a rising edge of SYNC after data is input to a rising edge of SYNC just before the data is output when there is no phase difference between input and output.

## &lt;Slow Roll-Off Filter&gt;

<b>Parameter</b>		<b>Symbol</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Passband	-0.01dB	0.356≤FSO/FSI≤6.000	PB	0	-	0.1853FSI kHz
	-0.01dB	0.167≤FSO/FSI<0.359	PB	0	-	0.0583FSI kHz
Stopband		0.356≤FSO/FSI≤6.000	SB	0.8313FSI	-	- kHz
		0.167≤FSO/FSI<0.359	SB	0.7063FSI	-	- kHz
Passband Ripple		0.167≤FSO/FSI≤6.000	PR	-	-	±0.01 kHz
Stopband Attenuation		0.356≤FSO/FSI≤6.000	SB	-128.4	-	- kHz
		0.167≤FSO/FSI<0.359	SB	-131.9	-	- kHz
Group Delay <a href="#">(Note 67)</a>		GD	-	62 (54/FSI + 8/FSO)	-	1/fs

Note 67. This value is SRC block only. It is the time from a rising edge of SYNC after data is input to a rising edge of SYNC just before the data is output when there is no phase difference between input and output.

## &lt;Short Delay Sharp Roll-Off Filter&gt;

Parameter		Symbol	min	typ	max	Unit
Passband	-0.01dB	0.980≤FSO/FSI≤6.000	PB	0	-	0.4583FSI kHz
	-0.01dB	0.711≤FSO/FSI<0.990	PB	0	-	0.4167FSI kHz
	-0.03dB	0.533≤FSO/FSI<0.718	PB	0	-	0.2183FSI kHz
	-0.01dB	0.490≤FSO/FSI<0.539	PB	0	-	0.2177FSI kHz
	-0.01dB	0.356≤FSO/FSI<0.495	PB	0	-	0.1948FSI kHz
	-0.01dB	0.225≤FSO/FSI<0.359	PB	0	-	0.0917FSI kHz
	-0.01dB	0.167≤FSO/FSI<0.248	PB	0	-	0.0826FSI kHz
Stopband	0.980≤FSO/FSI≤6.000	SB	0.5417FSI	-	-	kHz
	0.711≤FSO/FSI<0.990	SB	0.5021FSI	-	-	kHz
	0.533≤FSO/FSI<0.718	SB	0.2974FSI	-	-	kHz
	0.490≤FSO/FSI<0.539	SB	0.2813FSI	-	-	kHz
	0.356≤FSO/FSI<0.495	SB	0.2604FSI	-	-	kHz
	0.225≤FSO/FSI<0.359	SB	0.1573FSI	-	-	kHz
	0.167≤FSO/FSI<0.248	SB	0.1471FSI	-	-	kHz
Passband Ripple	0.167≤FSO/FSI≤6.000	PR	-	-	±0.01	kHz
Stopband Attenuation	0.980≤FSO/FSI≤6.000	SB	-121.2	-	-	kHz
	0.711≤FSO/FSI<0.990	SB	-121.4	-	-	kHz
	0.533≤FSO/FSI<0.718	SB	-114.6	-	-	kHz
	0.490≤FSO/FSI<0.539	SB	-100.2	-	-	kHz
	0.356≤FSO/FSI<0.495	SB	-103.3	-	-	kHz
	0.225≤FSO/FSI<0.359	SB	-104.0	-	-	kHz
	0.167≤FSO/FSI<0.248	SB	-103.3	-	-	kHz
Group Delay <a href="#">(Note 68)</a>	0.711≤FSO/FSI≤6.000	GD	-	18 (10/FSI +8/FSO)	-	1/fs
	0.533≤FSO/FSI<0.718	GD	-	21 (13/FSI +8/FSO)	-	1/fs
	0.490≤FSO/FSI<0.539	GD	-	20 (12/FSI +8/FSO)	-	1/fs
	0.356≤FSO/FSI<0.495	GD	-	21 (13/FSI +8/FSO)	-	1/fs
	0.225≤FSO/FSI<0.359	GD	-	25 (17/FSI +8/FSO)	-	1/fs
	0.167≤FSO/FSI<0.248	GD	-	26 (18/FSI +8/FSO)	-	1/fs

Note 68. This vale is SRC block only. It is the time from a rising edge of SYNC after data is input to a rising edge of SYNC just before the data is output when there is no phase difference between input and output.

## &lt;Short Delay Slow Roll-Off Filter&gt;

<b>Parameter</b>		<b>Symbol</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Passband	-0.01dB	0.356≤FSO/FSI≤6.000	PB	0	-	0.1853FSI kHz
	-0.01dB	0.167≤FSO/FSI<0.359	PB	0	-	0.0583FSI kHz
Stopband		0.356≤FSO/FSI≤6.000	SB	0.8313FSI	-	- kHz
		0.167≤FSO/FSI<0.359	SB	0.7063FSI	-	- kHz
Passband Ripple		0.167≤FSO/FSI≤6.000	PR	-	-	±0.01 kHz
Stopband Attenuation		0.356≤FSO/FSI≤6.000	SB	-128.4	-	- kHz
		0.167≤FSO/FSI<0.359	SB	-131.9	-	- kHz
Group Delay <a href="#">(Note 69)</a>		0.356≤FSO/FSI<6.00	GD	-	18 (10/FSI +8/FSO)	- 1/fs
		0.167≤FSO/FSI<0.359	GD	-	26 (18/FSI +8/FSO)	- 1/fs

Note 69. This value is SRC block only. It is the time from a rising edge of SYNC after data is input to a rising edge of SYNC just before the data is output when there is no phase difference between input and output.

## ■ DC Characteristics

(Ta=-40 ~ 85°C; AVDD1=AVDD2=CVDD=LVDD=1.7 ~ 1.9V, TVDD1 = TVDD2 = TVDD3 =1.65 ~ 3.6V)

Parameter	Symbol	min	typ	max	Unit
<b>Normal Pin (Except for SBDATA and SBCLK pins) (Note 70)</b>					
High-Level Input Voltage Except for XTI pin XTI pin	VIH VIH	70%TVDD 70%AVDD1	- -	- -	V V
Low-Level Input Voltage Except for XTI pin XTI pin	VIL VIL	- -	- -	30%TVDD 30%AVDD1	V V
High-Level Output Voltage (Iout=-200μA)	VOH	TVDD-0.2	-	-	V
Low-Level Output Voltage Except for SDA, XTO pin, Iout= 200μA SDA pin(Fast Mode) 2V < TVDD1 ≤ 3.6V (Iout=3mA) 1.65V≤ TVDD1 ≤ 2V(Iout=2mA)	VOL VOL VOL	- - -	- - -	0.2 0.4 20%TVDD1	V V V
SDA pin(Fast Mode Plus) 1.65V < TVDD1 ≤ 3.6V (Iout=20mA) 1.65V≤ TVDD1 ≤ 2V (Iout=2mA)	VOL VOL	- -	- -	0.4 20%TVDD1	V V
Input Leakage Current (Note 71)	Iin	-5	-	+5	μA
<b>SLIMbus (SBDATA and SBCLK pins); TVDD1 = 1.65 ~ 1.95V</b>					
High-Level Input Voltage	VIH1	65%TVDD1	-	-	V
Low-Level Input Voltage	VIL1	-	-	35%TVDD1	V
High-Level Output Voltage (Iout=-1mA)	VOH	90%TVDD1	-	TVDD1	V
Low-Level Output Voltage (Iout= 1mA)	VOL	-	-	10%TVDD1	V
Bus Holder Output Impedance	R <sub>DATAS</sub>	10	-	50	kΩ
I/O Capacitance	CIO	-	-	5	pF
Input Leakage Current (Note 72) VI = 10% * TVDD1 VI = 90% * TVDD1	IL	-5	-	5	μA
Short Circuit Output Current Tied to opposite rail	I <sub>SHORT</sub>	-100	-	100	mA

Note 70. Relationship between the TVDD power supply for interface and pin is as follows.

TVDD1:MCKI, MCKO, BCLK1, SYNC1, SDTI1A, SDTI1B, SDTI1C, SDTI1D, SDTO1A, SDTO1B, INTN, GP0, SBCLK, SBDATA, PSEL0-2, SBRC, CSN/CAD, SCLK/SCL, SI/I2CFIL, SO/SDA, PDN, SPIE, TESTI, TESTO1, TESTO2 pins

TVDD2: BCLK2, SYNC2, SDTI2, SDTO2 pins

TVDD3: BCLK3, SYNC3, SDTI3, SDTO3, BCLK4, SYNC4 SDTI4, SDTO4, GP1 pins

Note 71. PSW4N = PSW3N = PSW2N = PSW1N bits = “1”

Note 72. LDO2E pin = “H”

### ■ DC Characteristics (Digital Microphone)

(Ta=-40 ~ 85°C; AVDD1=AVDD2= CVDD= LVDD=1.7 ~ 1.9V, TVDD1 = TVDD2 = TVDD3 =1.65 ~ 3.6V)

Parameter	Symbol	min	typ	max	Unit
<b>Digital MIC Interface (DMDAT1/2 pin Input ; DMIC1/2 bit = “1”)</b>					
High-Level Input Voltage	VIH2	65%AVDD1	-	-	V
Low-Level Input Voltage	VIL2	-	-	35%AVDD1	V
<b>Digital MIC Interface (DMCLK1/2 pin Output; DMIC1/2 bit = “1”)</b>					
High-Level Output Voltage (Iout=-80μA)	VOH2	AVDD1-0.4	-	-	V
Low-Level Output Voltage (Iout= 80μA)	VOL2	-	-	0.4	V
Input Leakage Current	Iin	-5	-	+5	μA

## ■ Switching Characteristics

(Ta=-40 ~ 85°C; AVDD1=AVDD2=CVDD=LVDD==1.7 ~ 1.9V, TVDD1=TVDD2=TVDD3 =1.65 ~ 3.6V; C<sub>L</sub>=80pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
<b>MCKI</b>					
Input Frequency	fMCK	0.256	-	28.8	MHz
Pulse Width Low	tMCKL	0.4/fMCK	-	-	ns
Pulse Width High	tMCKH	0.4/fMCK	-	-	ns
<b>X'tal Oscillator (XTI pin)</b>					
Input Frequency	fMCK	11.2896	-	24.576	MHz
<b>MCKO</b>					
Output Frequency	fMCK	-	-	18.432	MHz
Duty Cycle (Note 73)	dMCK	-	50	-	%
<b>PLLCLK1/PLLCLK2</b>					
Output Frequency 44.1kHz * 256fs * 9	fPLL	-	101.606	-	MHz
48.0kHz * 256fs * 9	fPLL	-	110.592	-	MHz
44.1kHz * 256fs * 10	fPLL	-	112.896	-	MHz
48.0kHz * 256fs * 10	fPLL	-	122.880	-	MHz
Reference Clock	rPLL	256		3072	kHz
Duty	Duty	-	50	-	%
Long Term Jitter (10,000 Period)	Pjt	-	200	-	ps
Lock Time (Note 74)	PLT	-	-	2	ms
<b>Master Mode</b>					
SYNCx Output Timing Input Frequency (Note 75)	fs	8	-	192	kHz
Pulse Width High PCM Mode Except PCM Mode (Note 73)	tLRCKH	-	tBCK 50	-	ns %
BCLKx Output Timing Period (Note 77) Duty (Note 73)	tBCK tBCKL	0.256 -	- 50	12.288 or 512fs -	MHz %
<b>Slave Mode</b>					
SYNCx Input Timing Frequency (Note 75) Pulse Width High PCM Mode Except PCM Mode	fs tLRCKH	8 0.8 x tBCK 45	- 50	192 1/fs-0.8xtBCK 55	kHz ns %
BCLKx Input Timing Period (Note 77) Pulse Width Low Pulse Width High	tBCK tBCKL tBCKH	0.256 0.4 x tBCK 0.4 x tBCK	- -	12.288 or 512fs -	MHz ns ns

Note 73. Divided by even number

Note 74. Lock time is PLL1 and PLL2, respectively. PLL2 needs to be powered-up after PLL1 is locked.

Therefore, it takes maximum 4ms to lock PLL2.

Note 75. Sampling frequency of ADC1 L/Rch and ADC2 Lch is max. 96kHz. Sampling frequency of ADC2 Rch is max. 48kHz (In case of Digital MIC, it is max. .96kHz).

Note 76. SYNCx and BCLKx should be synchronized and their sampling rates(fs) should be stable for each port.

Note 77. Required to meet the following expression: fBCLK ≥ 2 x (Data Length by setting DLCx bits).  
The maximum value is shorter period between “12.288MHz” and “256fs”.

Parameter	Symbol	min	typ	max	Unit
<b>Serial Audio I/F (SYNCx, BCLKx, SDTlx, SDOUTx pins)</b>					
Delay Time from SYNCx to BCLKx “↑” (Note 78)	tBSYD	20	-	-	ns
Delay Time from BCLKx “↑” to SYNCx (Note 78)	tSYBD	20	-	-	ns
Serial Data Input Setup Time	tBIDS	10	-	-	ns
Serial Data Input Hold Time	tBIDH	10	-	-	ns
Delay Time from SYNCx to Serial Data	tSYOD	-	-	40	ns
Delay Time from BCLKx “↓” to Serial Data (Note 79)	tBOD	-	-	40	ns

Note 78. When the polarity of BCLKx is inverted, delay time is from BCLKx “↓”.

Note 79. When the polarity of BCLKx is inverted, delay time is from BCLKx “↑”.

#### <Direct Interface Mode; Slave Mode>

Parameter	Symbol	min	typ	max	Unit
<b>CODECMCKI</b>					
Input Frequency	fMCK	2.048	-	24.576	MHz
Pulse Width Low	tMCKL	0.4/fMCK	-	-	ns
Pulse Width High	tMCKH	0.4/fMCK	-	-	ns
<b>CODECSYNC</b>					
Frequency (Note 80)	fs	8	-	192	kHz
Pulse Width High	tLRCKH	45	50	55	%
<b>CODECBCLK</b>					
Period	tBCK	-	1/(64fs)	-	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
<b>Serial Audio I/F</b>					
Delay Time from CODEBCLK “↑” to COCECSYNC	tBSYD	20	-	-	ns
Delay Time from CODECSYNC to CODECBCLK “↑”	tSYBD	20	-	-	ns
Serial Data Input Setup Time	tBIDS	10	-	-	ns
Serial Data Input Hold Time	tBIDH	10	-	-	ns
Delay Time from CODECBCLK “↓” to Serial Data	tBOD	-	-	40	ns

Note 80. Sampling frequency of ADC1 L/Rch and ADC2 Lch is max. 96kHz. Sampling frequency of ADC2 Rch is max. 48kHz (In case of Digital MIC, it is max. .96kHz).

Parameter	Symbol	min	typ	max	Unit
<b>SPI Interface</b>					
SCLK					
Frequency	fSCLK	-	-	26	MHz
Duty Cycle	dSCLK	45	50	55	%
CSN					
High Level Width	tWRQH	80	-	-	ns
From PDN “↑” to CSN “↓”	tIRRQ	2.5	-	-	ms
From CSN “↓” to SCLK “↑”	tWSC	80	-	-	ns
From SCLK “↑” to CSN “↑”	tSCW	80	-	-	ns
SI					
Latch Setup Time	tSIS	12	-	-	ns
Latch Hold Time	tSIH	16	-	-	ns
SO					
Delay Time from SCLK “↓” to SO	tSOS	-	-	14	ns
Hold Time from SCLK “↑” to SO (Note 81)	tSOH	16	-	-	ns
CSN “↓” to SO(“L”) (SOCFG bit = “1”)	tDCD	-	-	70	ns
CSN “↑” to SO(Hi-z) (SOCFG bit = “1”)	tCCZ	-	-	70	ns

Note 81. Except when input the eighth bit of a command code.

Parameter	Symbol	min	typ	max	Unit
<b>Digital Audio Interface Timing: <math>C_L = 100\text{pF}</math></b>					
DMCLK Output Timing					
Period	tSCK	-	1/(64fs)	-	ns
Rising Time	tSRise	-	-	10	ns
Falling Time	tSFall	-	-	10	ns
Duty Cycle	dSCK	45	50	55	%
Audio Interface Timing					
DMDAT Setup Time	tDMS	50	-	-	ns
DMDAT Hold Time	tDMH	0	-	-	ns

<I<sup>2</sup>C: Fast Mode>

Parameter	Symbol	min	typ	max	Unit
<b>Control Interface Timing (I<sup>2</sup>C Bus mode): (Note 82)</b>					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 83)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive Load on Bus	C <sub>b</sub>	-	-	400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

<I<sup>2</sup>C: Fast Mode Plus>

Parameter	Symbol	min	typ	max	Unit
<b>Control Interface Timing (I<sup>2</sup>C Bus mode): (Note 82)</b>					
SCL Clock Frequency	fSCL	-	-	1	MHz
Bus Free Time Between Transmissions	tBUF	0.5	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.26	-	-	μs
Clock Low Time	tLOW	0.5	-	-	μs
Clock High Time	tHIGH	0.26	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.26	-	-	μs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.05	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.12	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.12	μs
Setup Time for Stop Condition	tSU:STO	0.26	-	-	μs
Capacitive Load on Bus	C <sub>b</sub>	-	-	550	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 82. I<sup>2</sup>C-bus is a registered trademark of NXP B.V.

Note 83. Data must be held long enough to bridge the 300ns-transition time of SCL.

Parameter	Symbol	min	typ	max	Unit
<b>Power-down &amp; Reset Timing</b>					
PDN accept pulse width ( <a href="#">Note 84</a> ) LDO2E pin = "L" LDO2E pin = "H"	tPDN tPDN tRPD	1 1 -	- - -	- - 50	μs ms ns
PDN Reject Pulse Width ( <a href="#">Note 84</a> )  TESTI, LDO2E, CIF1, CIF0, SBE pins Reject Pulse Width ( <a href="#">Note 85</a> )	tRPD	-	-	50	ns
PMADx bit = "1" to SDTOx valid ( <a href="#">Note 86</a> ) ADRST1-0 bits = "00" ADRST1-0 bits = "01" ADRST1-0 bits = "10" ADRST1-0 bits = "11"	tPDV tPDV tPDV tPDV	- - - -	1059 267 2115 531	- - - -	1/fs 1/fs 1/fs 1/fs
PMDMX bit = "1" to SDTOx valid ( <a href="#">Note 87</a> ) ADRST1-0 bits = "00" ADRST1-0 bits = "01" ADRST1-0 bits = "10" ADRST1-0 bits = "11"	tPDV tPDV tPDV tPDV	- - - -	1059 267 2115 531	- - - -	1/fs 1/fs 1/fs 1/fs

Note 84. The AK4961 will be reset by bringing the PDN pin = "L". The PDN pin must hold "L" for longer period than or equal to tRPD period. The AK4961 will not be reset by the "L" pulse shorter than or equal to tRPD.

Note 85. The logic of the TESTI, LDO2E, CIF1, CIF0 and SBE pins will not be changed by a pulse less than 50ns.

Note 86. This is the count of SYNCx "↑" from PMADx bit = "1".

Note 87. This is the count of SYNCx "↑" from PMDMX bit = "1".

## ■ Switching Characteristics (SLIMbus)

(Ta=-40 ~ 85°C; AVDD1=AVDD2=CVDD=LVDD==1.7 ~ 1.9V, TVDD1=TVDD2=TVDD3 =1.65 ~ 1.95V; C<sub>L</sub>=15pF/75pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
<b>SLIMbus Clock (Input)</b>					
Frequency	f <sub>SBCLK</sub>	-	-	28.8	MHz
Clock Input High Time	T <sub>CLKIH</sub>	12	-		ns
Clock Input Low Time	T <sub>CLKIL</sub>	12	-	-	ns
Clock Input Slew Rate 20% < VI < 80% ( <a href="#">Note 88</a> )	SR <sub>CLKI</sub>	2%TVDD1	-	-	V/ns
Clock Input Hysteresis ( <a href="#">Note 88</a> )	H <sub>CLKI</sub>	50	-	-	mV
<b>SLIMbus Data</b>					
Data Output Slew Rate 20% < VO < 80% ( <a href="#">Note 88</a> )	SR <sub>DATA</sub>	-	-	50% TVDD1	V/ns
Time for Data Output Valid	T <sub>DV</sub>		-	12	ns
Data Input Hold Time	T <sub>HOLD</sub>	2	-	-	ns
Data Input Setup Time	T <sub>SETUP</sub>	3.5	-	-	ns
Driver Disable Time	T <sub>DD</sub>	-	-	10	ns

Note 88. Guaranteed by design

### ■ Timing Diagram (System Clock)

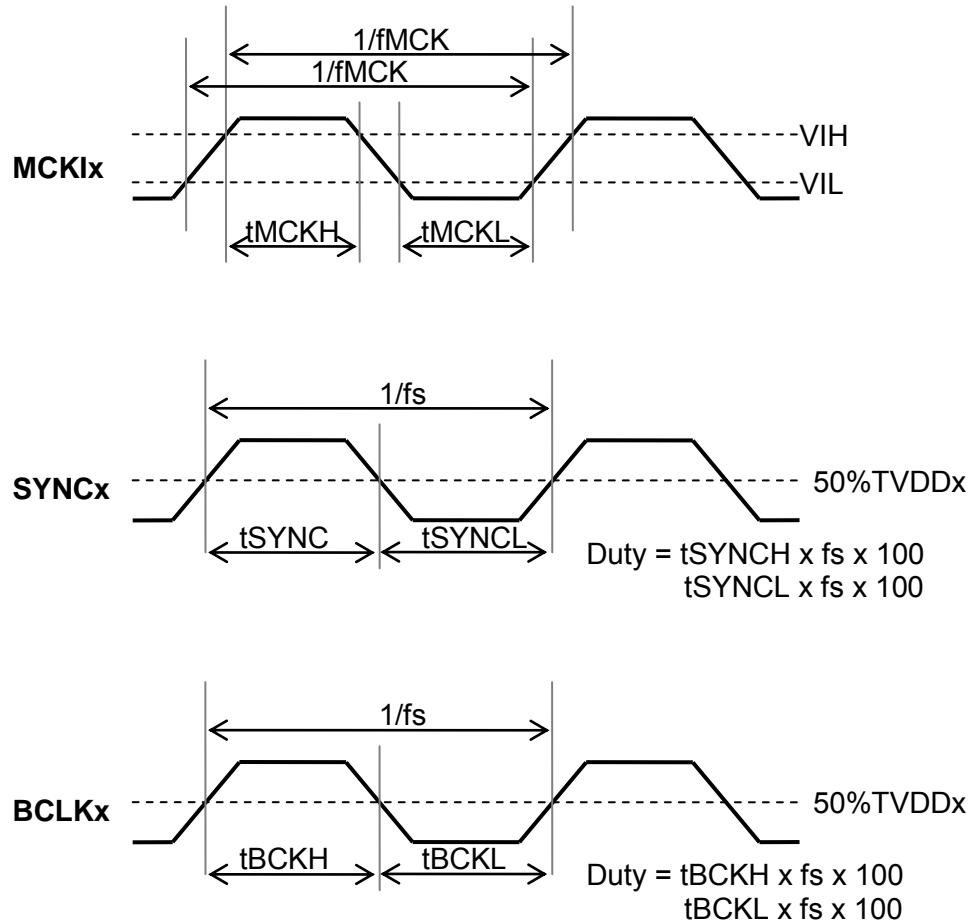


Figure 3. System Clock (Master Mode)

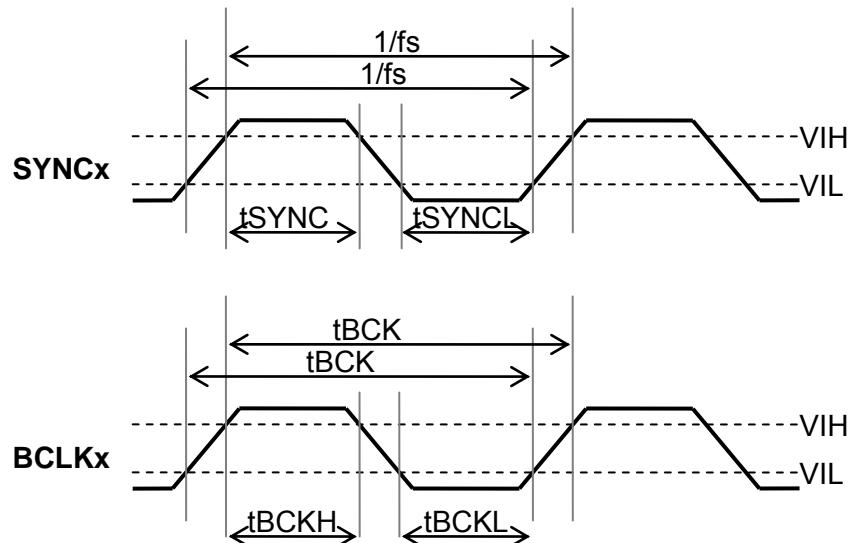


Figure 4. System Clock (Slave Mode)

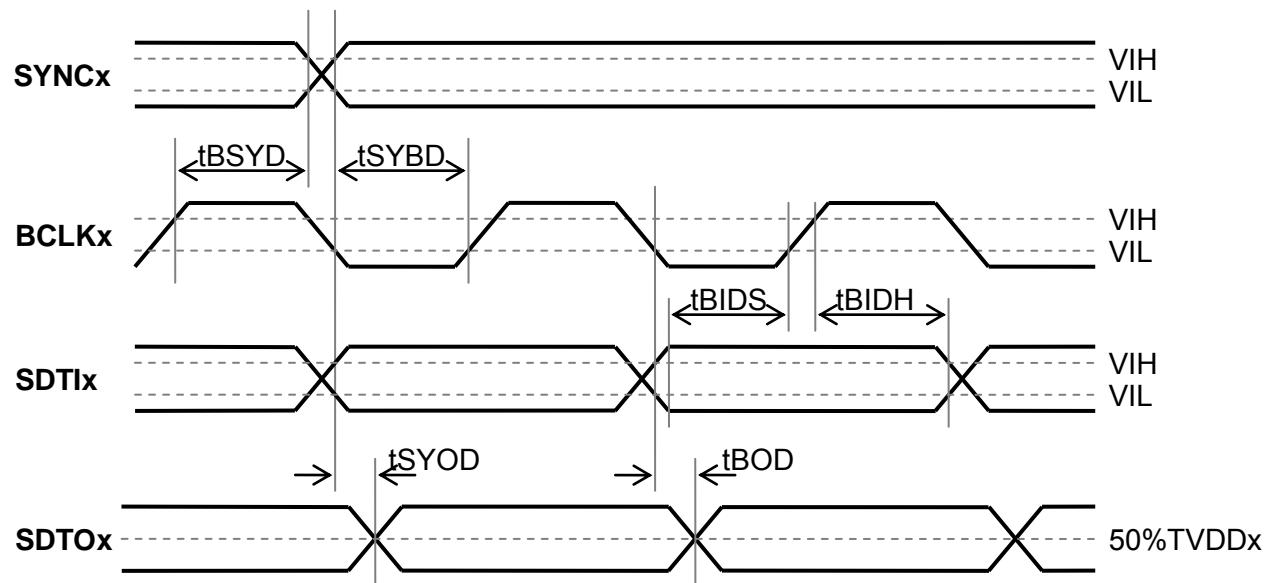
**■ Timing Diagram (Serial Audio I/F)**

Figure 5. Serial Audio Interface (Slave Mode)

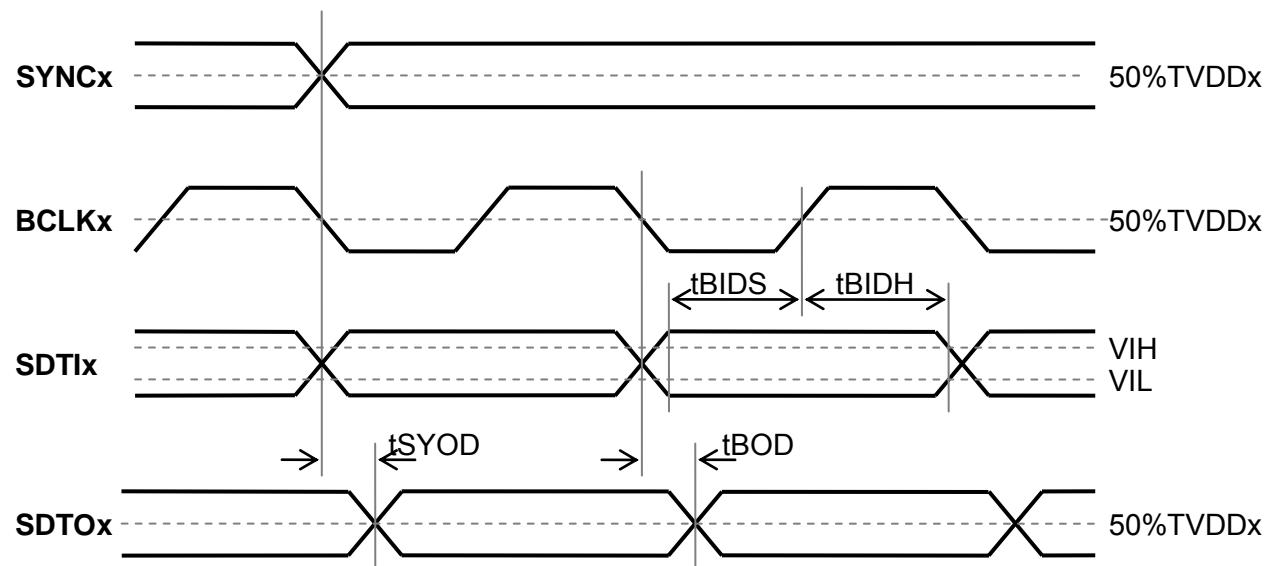


Figure 6. Serial Audio Interface (Master Mode)

### ■ Timing Diagram (SPI Interface)

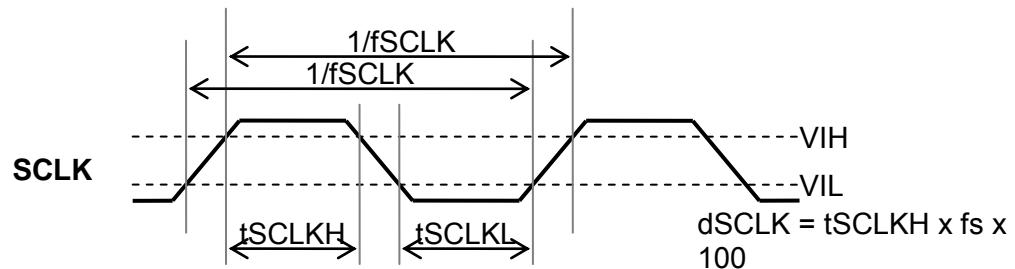


Figure 7. SPI Interface SCLK

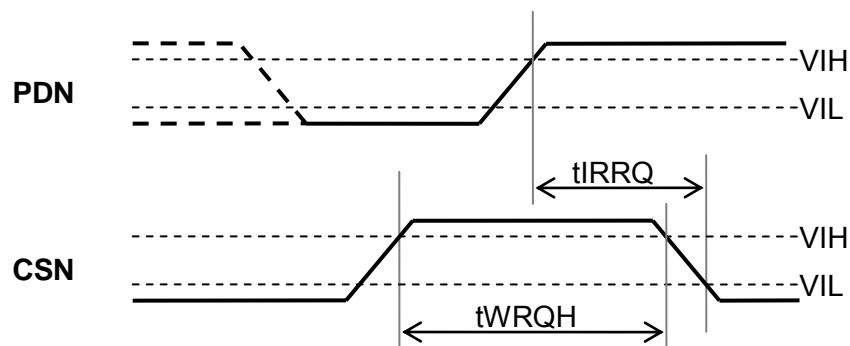


Figure 8. SPI Interface CSN/PDN

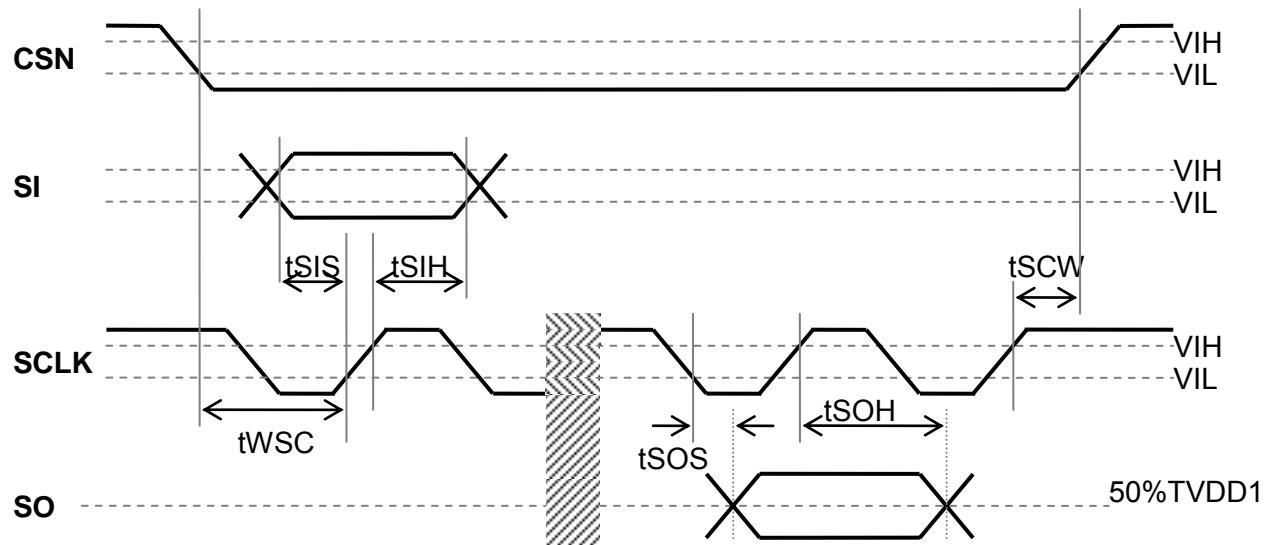


Figure 9. SPI Interface 1(SI/SO)

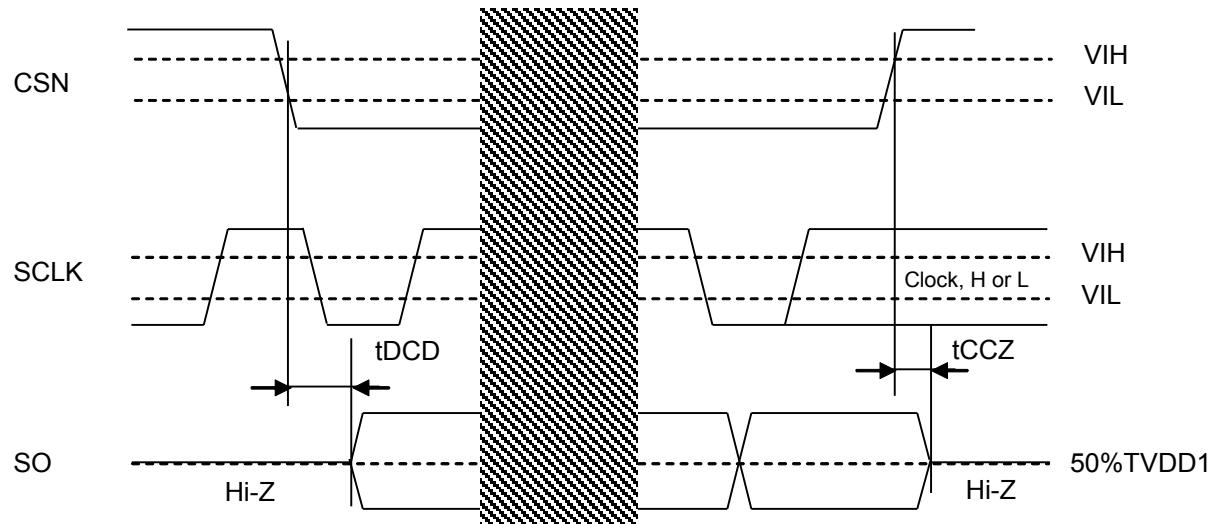
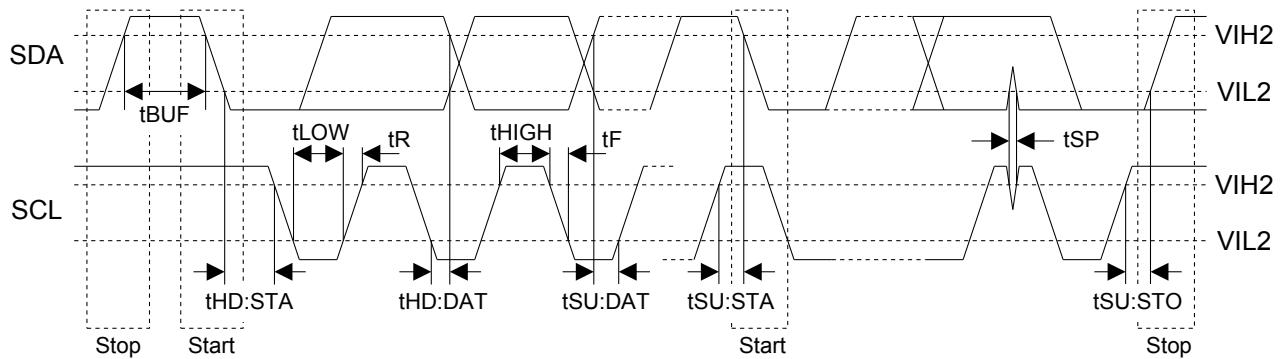


Figure 10. SPI Interface (SO) @ SOCFG bit = “1”

### ■ Timing Diagram (I<sup>2</sup>C Interface)

Figure 11. I<sup>2</sup>C Bus Mode Timing

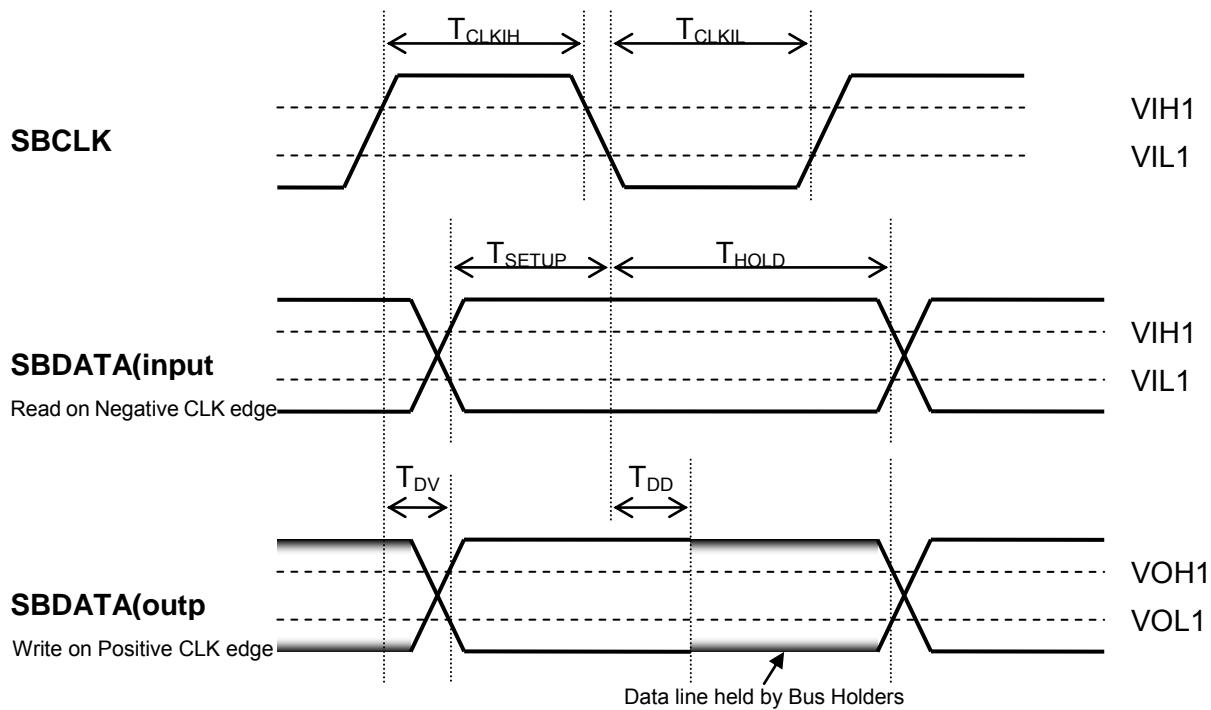
**■ Timing Diagram (SLIMbus)**

Figure 12. SLIMbus Interface

### ■ Timing Diagram (Digital MIC)

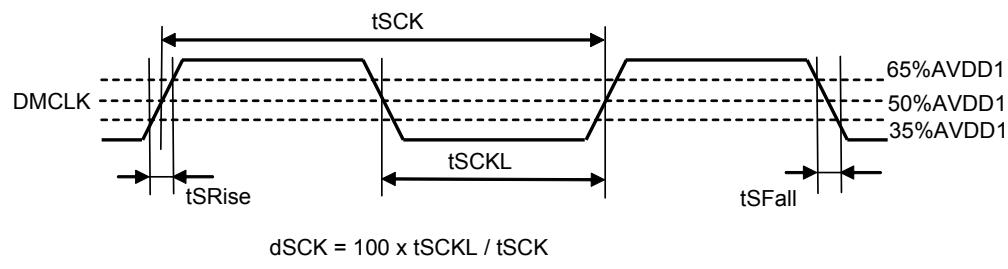


Figure 13. DMCLK Clock Timing

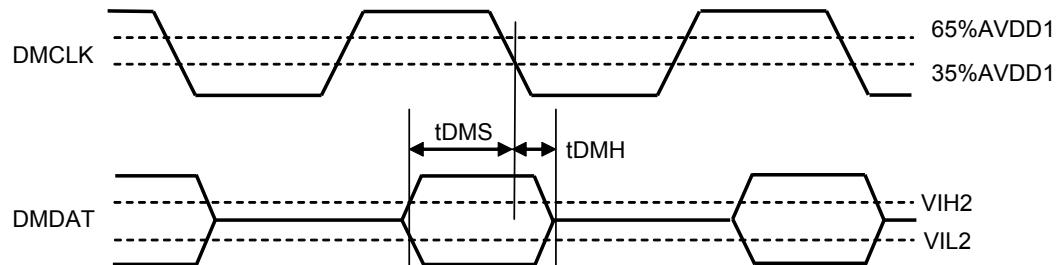


Figure 14. Audio Interface Timing (DCLKP bit = "1")

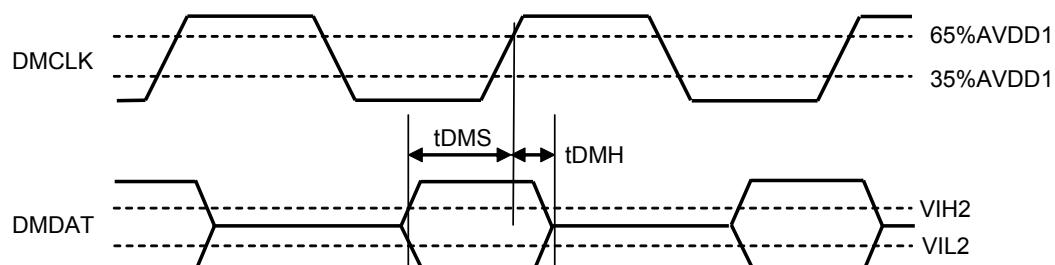


Figure 15. Audio Interface Timing (DCLKP bit = "0")

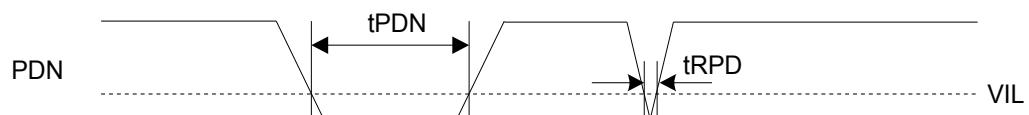
**■ Timing Diagram (Reset)**

Figure 16. Power down

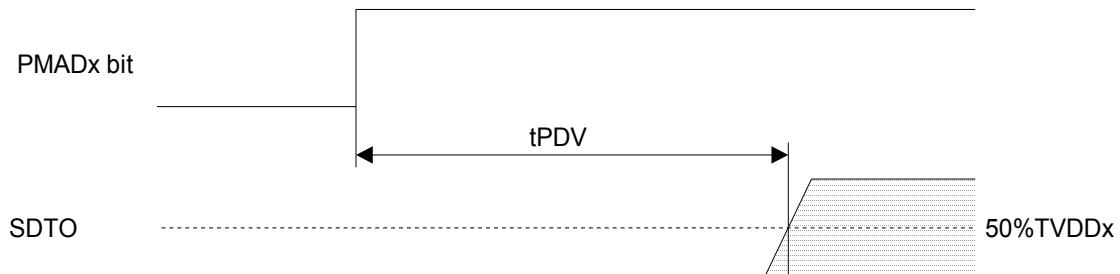


Figure 17. ADC Power Up Timing

## 9. Functional Descriptions

### ■ Internal Pull-down Pin

When the PDN pin = “H”, digital pins shown in [Table 2](#) can set internal pull-down resistor to ON/OFF by PSW1N, PSW2N, PSW3N and PSW4N bits. Default is pull-down resistor ON and the control register is “0”. The pull-down setting should be properly selected in external condition.

Pin Name	I/O	Power Domain	Control bit
LDO2E	I	TVDD1	-
CSN	I	TVDD1	-
SCLK	I	TVDD1	-
SI	I	TVDD1	-
SO	O	TVDD1	-
CIF0	I	TVDD1	-
CIF1	I	TVDD1	-
SBE	I	TVDD1	-
SBCLK	I	TVDD1	-
SBDATA	I/O	TVDD1	-
MCKI1	I	TVDD1	-
MCKO	O	TVDD1	PSW1N
BCLK1	I/O	TVDD1	-
SYNC1	I/O	TVDD1	-
SDTI1A	I	TVDD1	-
SDTI1B	I	TVDD1	-
SDTI1C	I	TVDD1	-
SDTI1D	I	TVDD1	-
SDTO1A	O	TVDD1	PSW1N
SDTO1B	O	TVDD1	PSW1N
GP0	O	TVDD1	PSW1N
PDN	I	TVDD1	-
TESTI	I	TVDD1	-
TESTO	O	TVDD1	-
INTN	O	TVDD1	-
XTI	I	TVDD1	-
XTO	O	TVDD1	-

Pin Name	I/O	Power Domain	Control bit
BCLK2	I/O	TVDD2	PSW2N
SYNC2	I/O	TVDD2	PSW2N
SDTI2	I	TVDD2	PSW2N
SDTO2	O	TVDD2	PSW2N
BCLK3	I/O	TVDD3	PSW3N
SYNC3	I/O	TVDD3	PSW3N
SDTI3	I	TVDD3	PSW3N
SDTO3	O	TVDD3	PSW3N
BCLK4	I/O	TVDD3	PSW4N
SYNC4	I/O	TVDD3	PSW4N
SDTI4	I	TVDD3	PSW4N
SDTO4	O	TVDD3	PSW4N
DMCLK1	O	AVDD1	-
DMDAT1	I	AVDD1	-
DMCLK2	O	AVDD1	-
DMDAT2	I	AVDD1	-

Table 2. Internal Pull-down Pin

## ■ CODEC System Clock

CODEC block is operated by a clock generated by PLL1/2, CODECMCLK or X'tal. CODECMCLK selects 128fs, 256fs, 512fs or 1024fs. The master clock is set by CM[1:0] bits ([Table 4](#)) and the sampling frequency is set by FS[4:0] bits ([Table 5](#)). When using the data via SRCE, the master clock is set by CM2[1:0] bits ([Table 6](#)) and the sampling frequency is set by FS2[4:0] bits ([Table 7](#)).

CODEC Block		Clock Source	Master Clock	Sampling Frequency
ADC		CODECMCLK	CM[1:0] bits	FS[4:0] bits ( <a href="#">Note 89</a> )
DAC1 (32bit DAC)	SRCE Bypass (SELDA1N bit = "0")	CODECMCLK	CM[1:0] bits	FS[4:0] bits
	SRCE Through (SELDA1N bit = "1")	X'tal (XCKSEL bit = "1")	CM2[1:0] bits	FS2[4:0]bits
DAC2 (24bit DAC)	SRCE Bypass (SELDA2N bit = "0")	CODECMCLK	CM[1:0] bits	FS[4:0] bits
	SRCE Through (SELDA2N bit = "1")	X'tal (XCKSEL bit = "1")	CM2[1:0] bits	FS2[4:0]bits
SRCE	FSI	CODECMCLK	CM[1:0] bits ( <a href="#">Note 90</a> )	FS[4:0] bits ( <a href="#">Note 90</a> )
	FSO	X'tal (XCKSEL bit = "1")	CM2[1:0] bits	FS2[4:0]bits
CP1/2/3	SRCE Through	CODECMCLK (XCKCPSEL bit = "0")	CM[1:0] bits	FS[4:0] bits
	SRCE Enable	X'tal (XCKCPSEL bit = "1")	CM2[1:0] bits	FS2[4:0]bits

Note 89. Maximum sampling frequency of ADC1 Lch/Rch and ADC2 Lch is 96kHz and maximum sampling frequency of ADC2 Rch is 48kHz (In case of digital microphone, it is max. 96kHz). When ADC is operated by more than maximum sampling frequency, ADC (including digital microphone) should be powered-down. If the ADC is not powered-down, ADC may output abnormal data.

Note 90. Master clock of FSI of SRCE should be equal or more than 256fs.

Table 3. CODEC System Clock

## &lt;ADC&gt;

CM1 bit	CM0 bit	Master Clock Frequency	Sampling Frequency Range
0	0	256fs	8 ~ 96kHz
0	1	512fs	8 ~ 48kHz
1	0	1024fs	8 ~ 24kHz
1	1	128fs	N/A

(default)

## &lt;DAC1&gt;

DSMLP1 bit	CM1 bit	CM0 bit	Master Clock Frequency	Sampling Frequency Range
1	0	0	256fs	8 ~ 12kHz
0	0	0	256fs	16 ~ 96kHz
0	0	1	512fs	8 ~ 48kHz
0	1	0	1024fs	8 ~ 24kHz
0	1	1	128fs	128 ~ 192kHz

(default)

## &lt;DAC2&gt;

DSMLP2 bit	CM1 bit	CM0 bit	Master Clock Frequency	Sampling Frequency Range
1	0	0	256fs	16 ~ 24kHz
0				32 ~ 96kHz
1	0	1	512fs	8 ~ 12kHz
0				16 ~ 48kHz
0	1	0	1024fs	8 ~ 24kHz
0	1	1	128fs	128 ~ 192kHz

(default)

Table 4. Setting of Master Clock Frequency 1 (N/A: Not available)

FS4 bit	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency
0	0	0	0	0	8kHz
0	0	0	0	1	11.025kHz
0	0	0	1	0	12kHz
0	0	1	0	0	16kHz
0	0	1	0	1	22.05kHz
0	0	1	1	0	24kHz
0	1	0	0	0	32kHz
0	1	0	0	1	44.1kHz
0	1	0	1	0	48kHz
0	1	1	0	0	64kHz
0	1	1	0	1	88.2kHz
0	1	1	1	0	96kHz
1	0	0	0	0	128kHz
1	0	0	0	1	176.4kHz
1	0	0	1	0	192kHz
Others				N/A	

(default)

Table 5. Setting of Sampling Frequency 1 (N/A: Not available)

\* Depending on setting of PLL's divider, the sampling frequency may differ. Please set PLD1[15:0], PLM1[15:0], PLD2[15:0] and PLM2[15:0] bits precisely.

&lt;DAC1/2&gt;

DSMLP1 bit DSMLP2 bit	CM21 bit	CM20 bit	Master Clock Frequency	Sampling Frequency Range	
0	0	0	256fs	44.1 ~ 96kHz	
0	0	1	512fs	22.05 ~ 48kHz	
0	1	0	1024fs	11.025 ~ 24kHz	
0	1	1	128fs	128 ~ 192kHz	

Table 6. Setting of Master Clock Frequency 2

FS24 bit	FS23 bit	FS22 bit	FS21 bit	FS20 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
0	0	0	0	1	11.025kHz	
0	0	0	1	0	12kHz	
0	0	1	0	0	16kHz	
0	0	1	0	1	22.05kHz	
0	0	1	1	0	24kHz	
0	1	0	0	0	32kHz	
0	1	0	0	1	44.1kHz	
0	1	0	1	0	48kHz	
0	1	1	0	0	64kHz	
0	1	1	0	1	88.2kHz	
0	1	1	1	0	96kHz	
1	0	0	0	0	128kHz	
1	0	0	0	1	176.4kHz	
1	0	0	1	0	192kHz	
Others					N/A	

(default)

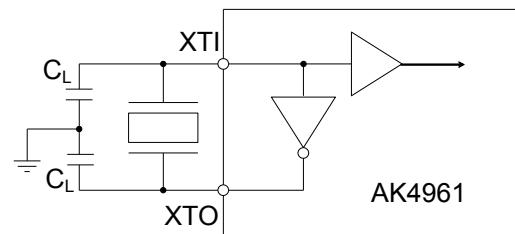
\* Depending on setting of PLL's divider, the sampling frequency may differ. Please set PLD1[15:0], PLM1[15:0], PLD2[15:0] and PLM2[15:0] bits precisely.

Table 7. Setting of Sampling Frequency 2 (N/A: Not available)

## ■ X'tal Circuit

The clock for the XTI pin can be generated by the following methods. When using X'tal circuit, PMOSC bit should be set to "1".

1) X'tal Mode (PMOSC bit = "1")



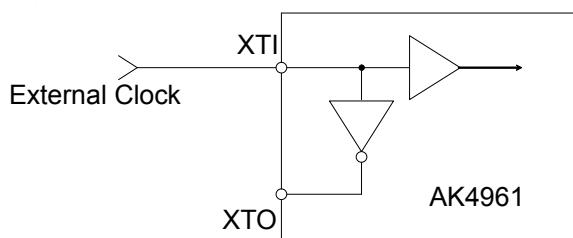
Note 91. External capacitance depends on the crystal oscillator.

$C_L=21.5\text{pF}(\text{max})$ ,  $R_L(\text{Equivalent Series Resistance}) = 80\Omega(\text{max})$  @ 24.576MHz

$C_L=30.6\text{pF}(\text{max})$ ,  $R_L(\text{Equivalent Series Resistance}) = 200\Omega(\text{max})$  @ 11.2896MHz

Figure 18. X'tal Mode

2) External Clock Mode(PMOSC bit = "0")



Note: Input clock must not exceed AVDD1.

Figure 19. External Clock Mode

3) OFF Mode (Not using X'tal circuit; PMOSC bit = "0")

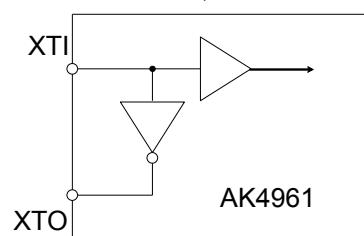


Figure 20. OFF Mode

## ■ ADC Initialization Cycle

The ADC enters an initialization cycle when PMAD1L, PMAD1R, PMAD2M or PMAD2V bit is changed from PMAD1L = PMAD1R = PMAD2V = PMAD2M bits = “0” to “1”. The initialization cycle time is set by ADRST1-0 bits ([Table 8](#)) During the initialization cycle, the ADC digital data output of both channels are forced to a 2’s complement, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete. When using a digital microphone, the initialization cycle is the same as ADC’s.

Note 92. The initial data of ADC has offset data that depends on the condition of the microphone and the cut-off frequency of HPF. If this offset is not small, make initialization cycle longer or do not use the initial data of ADC.

ADC Initialization Cycle					
ADRST1 bit	ADRST0 bit	Cycle	fs = 8kHz	fs = 44.1kHz	fs = 96kHz
0	0	1059/fs	132.4ms	24ms	11ms
0	1	267/fs	33.4ms	6.1ms	2.8ms
1	0	2115/fs	264.4ms	48ms	22ms
1	1	531/fs	66.4ms	12ms	5.5ms

(default)

Table 8. ADC Initialization Cycle

## ■ Analog Input Start-Up Time

Microphone input circuit can be powered-up/down by PMAIN1-6 bits. When PMAINx bit is “1”, the initialization cycle starts. The initialization cycle can be set by ADRST[1:0] bits and this setting is common for all channels.

Although it depends on the condition of microphone characteristic and external circuit, the initialization cycle should be set to longer than 13.7ms when a capacitor for AC-coupling is  $1\mu\text{F} \pm 50\%$ . The initialization cycle should be set to longer than 6.8ms when a capacitor for AC-coupling is  $0.47\mu\text{F} \pm 50\%$ .

AINx Start-Up Time					
ADRST1 bit	ADRST0 bit	Cycle	fs = 8kHz	fs = 44.1kHz	fs = 96kHz
0	0	656/fs	82.0ms	14.9ms	6.8ms
0	1	164/fs	20.5ms	3.7ms	1.7ms
1	0	1312/fs	164.0ms	29.8ms	13.7ms
1	1	328/fs	41.0ms	7.4ms	3.4ms

(default)

Table 9. AINx Start-Up Time

## ■ Mono/Stereo Mode

PMAD1L/R bits set mono/stereo ADC operation. PMAD2M and PMAD2V bits set ADC2 output data. When changing ADC operation and analog/digital microphone, PMAD1L/R (PMAD2V/M) and PMDM1L/R (PMDM2L/R) bits must be set “0” at first. When DMIC1 bit is = “1”, PMAD1L/R bit settings are ignored. When DMIC2 bit = “1”, PMAD2M and PMAD2V bits setting are ignored.

PMAD1R bit	PMAD1L bit	ADC1 Lch data	ADC1 Rch data
0	0	All “0”	All “0”
0	1	MIC1 Lch Input Signal	MIC1 Lch Input Signal
1	0	MIC1 Rch Input Signal	MIC1 Rch Input Signal
1	1	MIC1 Lch Input Signal	MIC1 Rch Input Signal

Table 10. ADC1 Mono/Stereo Select (Analog Microphone)

PMAD2V bit	PMAD2M bit	ADC2 Lch data	ADC2 Rch data
0	0	All “0”	All “0”
0	1	MIC2 Input Signal	MIC2 Input Signal
1	0	MIC3 Input Signal	MIC3 Input Signal
1	1	MIC3 Input Signal	MIC2 Input Signal

Table 11. ADC2 Output Data (Analog Microphone)

PMDM1R bit	PMDM1L bit	ADC1 Lch data	ADC1 Rch data
0	0	All “0”	All “0”
0	1	DMIC1 Lch Input Signal	DMIC1 Lch Input Signal
1	0	DMIC1 Rch Input Signal	DMIC1 Rch Input Signal
1	1	DMIC1 Lch Input Signal	DMIC1 Rch Input Signal

Table 12. ADC1 Mono/Stereo Select (Digital Microphone)

PMDM2R bit	PMDM2L bit	ADC2 Lch data	ADC2 Rch data
0	0	All “0”	All “0”
0	1	DMIC2 Lch Input Signal	DMIC2 Lch Input Signal
1	0	DMIC2 Rch Input Signal	DMIC2 Rch Input Signal
1	1	DMIC2 Lch Input Signal	DMIC2 Rch Input Signal

Table 13. ADC2 Mono/Stereo Select (Digital Microphone)

## ■ MIC/LINE Selector

The AK4961 has input selectors. Input signal from the AIN1-6 pins to a microphone amplifier is selected by INS1L[2:0], INS1R[2:0], INS2M[2:0] and INS2V[2:0] bits. The AK4961 supports both full-differential and single-ended modes. In single-ended mode, the signal is input to AINx+ pin and AINx- pin is connected with a capacitor in series. When DMIC1(DMIC2) bit is “1”, digital microphone input is selected.

Do not select the same signal input pin for a microphone amplifier except for MIC-Amp 3. For example, AIN1+/- is selected to MIC-Amp 1 Lch and MIC-Amp 2 Lch at the same time.

MIC-Amp 3 is for Voice Wakeup. The input path is set by INS2V[2:0] bits and the gain is set by MG2V[3:0] bits. Output data selects ADC2 Rch.

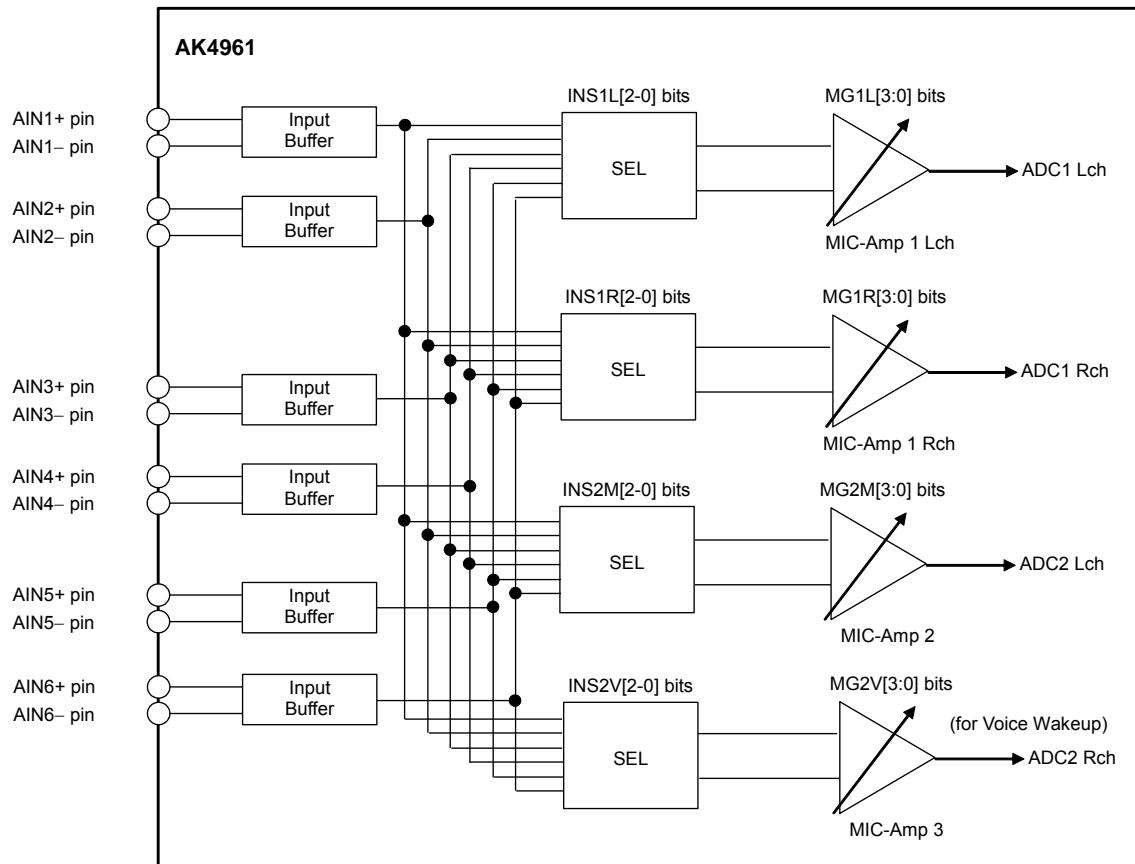


Figure 21. Setting of Microphone Input Selector & Volume

DMIC1 bit	INS1L2 bit	INS1L1 bit	INS1L0 bit	ADC1 Lch
0	0	0	0	AIN1
0	0	0	1	AIN2
0	0	1	0	AIN3
0	0	1	1	AIN4
0	1	0	0	AIN5
0	1	0	1	AIN6
0	1	1	x	MUTE
1	x	x	x	Digital MIC

(default)

Table 14. MIC-Amp 1 Lch Input Signal Select (x: Do not care)

DMIC1 bit	INS2R2 bit	INS2R1 bit	INS2R0 bit	ADC1 Rch
0	0	0	0	AIN1
0	0	0	1	AIN2
0	0	1	0	AIN3
0	0	1	1	AIN4
0	1	0	0	AIN5
0	1	0	1	AIN6
0	1	1	x	MUTE
1	x	x	x	Digital MIC

(default)

Table 15. MIC-Amp 1 Rch Input Signal Select (x: Do not care)

DMIC2 bit	INS2M2 bit	INS2M1 bit	INS2M0 bit	ADC2 Lch
0	0	0	0	AIN1
0	0	0	1	AIN2
0	0	1	0	AIN3
0	0	1	1	AIN4
0	1	0	0	AIN5
0	1	0	1	AIN6
0	1	1	x	MUTE
1	x	x	x	Digital MIC

(default)

Table 16. MIC-Amp 2 Input Signal Select (x: Do not care)

DMIC2 bit	INS2V2 bit	INS2V1 bit	INS2V0 bit	ADC2 Rch
0	0	0	0	AIN1
0	0	0	1	AIN2
0	0	1	0	AIN3
0	0	1	1	AIN4
0	1	0	0	AIN5
0	1	0	1	AIN6
0	1	1	x	MUTE
1	x	x	x	Digital MIC

(default)

Table 17. MIC-Amp 3 Input Signal Select (x: Do not care)

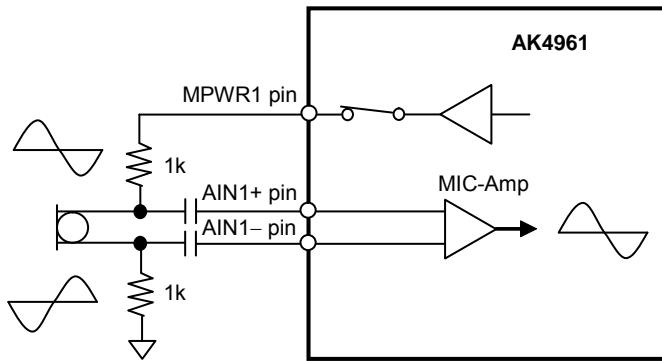


Figure 22. Connection Example for Full-differential Microphone Input

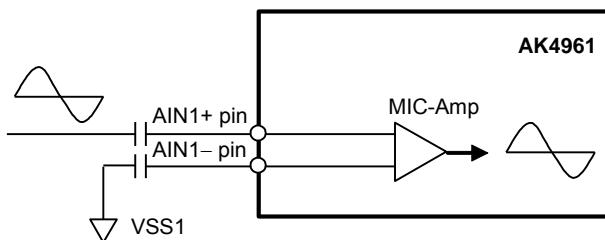


Figure 23. Connection Example for Single-ended Microphone Input

### ■ Microphone Amplifier Gain

The AK4961 has gain amplifiers for microphone input. The gain of four microphone amplifiers can be independently selected by MG1L[3:0], MG1R[3:0], MG2M[3:0] and MG2V[3:0] bits. The volume is changed immediately by setting these bits.

MG1L3 bit	MG1L2 bit	MG1L1 bit	MG1L0 bit	Gain
MG1R3 bit	MG1R2 bit	MG1R1 bit	MG1R0 bit	(default)
MG2M3 bit	MG2M2 bit	MG2M1 bit	MG2M0 bit	
MG2V3 bit	MG2V2 bit	MG2V1 bit		
0	0	0	0	0dB
0	0	0	1	+3dB
0	0	1	0	+6dB
0	0	1	1	+9dB
0	1	0	0	+12dB
0	1	0	1	+15dB
0	1	1	0	+18dB
0	1	1	1	+21dB
1	0	0	0	+24dB
1	0	0	1	+27dB
1	0	1	0	+30dB
Others				N/A

Table 18. MIC-Amp Gain (N/A: Not available)

## ■ Microphone Power

The AK4961 has four microphone power supplies. They can be powered up at the same time. Output voltage of MPWR1A/B/C and MPWR2 is set by MICL1[1:0] and MICL2[1:0] bits, respectively. Control of output is set by PMMPx bit. When PMMPx bit is “1”, microphone power is output. When PMMPx bit is “0”, MPWRx pin becomes power-down state (Hi-z). The load resistance is minimum 2kΩ for each MPWR1A/B/C and MPWR2 pin. Any capacitor must not be connected directly to the MPWR1A/B/C and MPWR2. The AK4961 has a MIC power direct mode for the MPWR1A/B/C pins. In this mode, the AVDD1 voltage is directly output from the MPWR1A/B/C pin via the internal switch (ON resistance: typ. 90Ω, max. 140Ω).

Both MRFx pins are powered up with an acceleration circuit when one of PMMPx bit is set to “1” from “0”. This power up time is set by FS4-0 bits. In MIC power direct mode (MICL[1:0] bits = “11”), PMMP1A/B/C bit controls ON/OFF of the internal switch. This power-up timer will not work in MIC power direct mode.

Set MICLx bit before power-on of the corresponding MPWR pin (there is no time limitation). When a MPWR pin is ON, the setting of corresponding MICLx bit should not be changed.

FS4 bit	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency(fs)	MIC Power Power-Up Time	
0	0	0	0	0	8kHz	20ms	160/fs
0	0	0	0	1	11.025kHz	14.5ms	160/fs
0	0	0	1	0	12kHz	13.3ms	160/fs
0	0	1	0	0	16kHz	20ms	320/fs
0	0	1	0	1	22.05kHz	14.5ms	320/fs
0	0	1	1	0	24kHz	13.3ms	320/fs
0	1	0	0	0	32kHz	20ms	640/fs
0	1	0	0	1	44.1kHz	14.5ms	640/fs
0	1	0	1	0	48kHz	13.3ms	640/fs
0	1	1	0	0	64kHz	20ms	1280/fs
0	1	1	0	1	88.2kHz	14.5ms	1280/fs
0	1	1	1	0	96kHz	13.3ms	1280/fs
Others					-	-	N/A

Table 19. MIC Power Power-Up Time (N/A: Not available)

When using a microphone power, the power-up sequence below should be followed to reduce DC offset (pop noise).

1. MIC Power ON
2. MIC-Amp ON
3. ADC ON

MICL11 bit	MICL10 bit	MPWR1A/B/C Output Level (typ)	
0	0	2.8V	(default)
0	1	2.5V	
1	0	1.8V	
1	1	Direct Mode (AVDD1)	

Table 20. Microphone Power Output Voltage (MPWR1A/B/C)

MICL21 bit	MICL20 bit	MPWR2 Output Level (typ)	
0	0	2.8V	(default)
0	1	2.5V	
1	0	1.8V	
1	1	N/A	

Table 21. Microphone Power Output Voltage (MPWR2), (N/A: Not available)

PMMP1A/B/C bits PMMP2 bit	MPWR1A/B/C pins MPWR2 pin		
0	Hi-Z		(default)
1	Output		

Table 22. Microphone Power Output State

## ■ Digital Microphone

### 1. Connection to Digital Microphone

When DMIC1 bit is set to “1”, DMDAT1 (digital microphone data input) and DMCLK1 (digital microphone clock supply) pins are enabled. When DMIC2 bit is set to “1”, DMDAT2 (digital microphone data input) and DMCLK2 (digital microphone clock supply) pins are enabled. DMCLK2 is the same clock (64fs) as DMCLK1.

The same power supply as AVDD1 must be provided to the digital microphone. The [Figure 24](#) and [Figure 25](#) show mono/stereo connection examples. The DMCLK1 (DMCLK2) signal is output from the AK4961, and the digital microphone outputs 1bit data, which generated by  $\Delta\Sigma$ Modulator, from DMDAT1 (DMDAT2). PMDM1L/R (PMMD2L/R) bits control power up/down of the digital block (Decimation Filter and HPF). PMAD1L/R (PMMD2L/R) bits settings do not affect the digital microphone power management. The DCLKE1 (DCLKE2) bit controls ON/OFF of the output clock from the DMCLK1 (DMCLK2) pin. When the AK4961 is powered-up (PDN pin = “H”), external pull-down resistor(R) should be connected to the DMDAT1 (DMDAT2) pin to avoid floating state.

**Maximum sampling frequency of Digital Microphone is 96kHz. The AK4961 does not work normally at higher sample rate.**

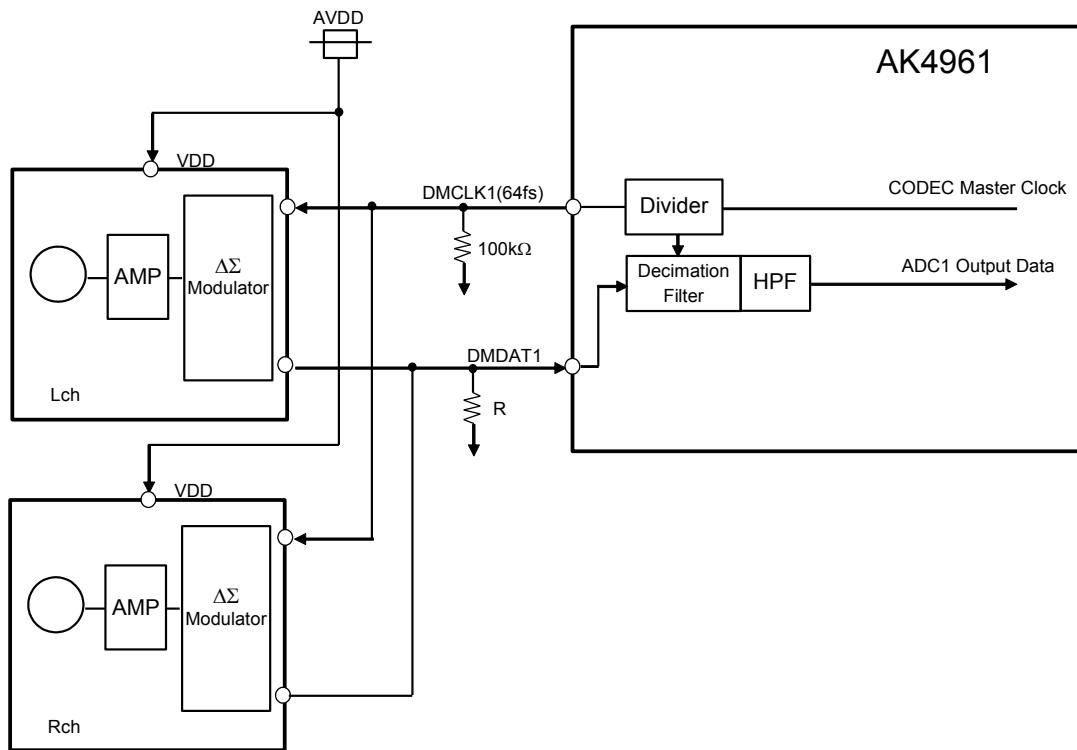


Figure 24. Connection Example of Stereo Digital Microphone (DMIC1 bit = “1”)

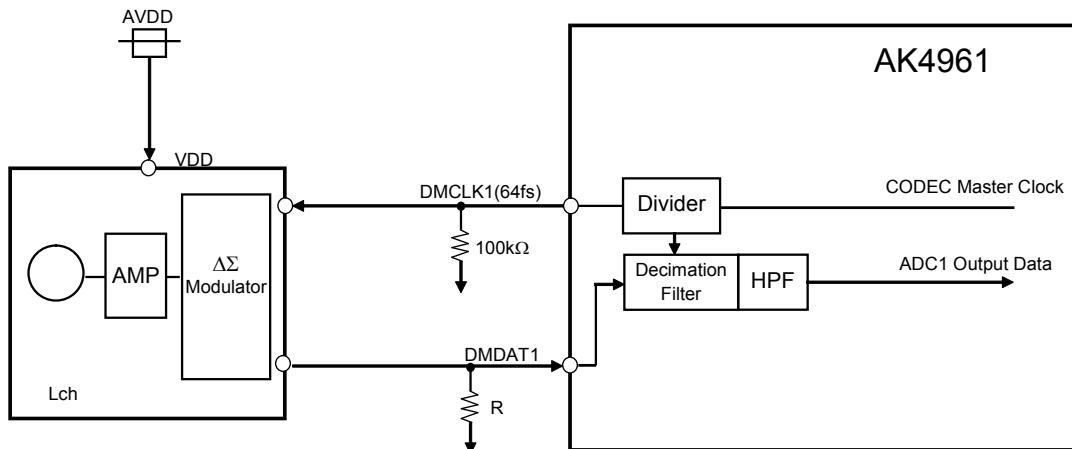


Figure 25. Connection Example of Mono Digital Microphone (DMIC1 bit = “1”)

## 2. Interface

The input data channel of the DMDAT1 (DMDAT2) pin is set by DCLKP1 (DCLKP2) bit. When DCLKP1 (DCLKP2) bit = “1”, Lch data is input to the Decimation Filter if DMCLK1 (DMCLK2) = “H”, Rch data is input if DMCLK1 (DMCLK2) = “L”. When DCLKP1 (DCLKP2) bit = “0”, Rch data is input to the Decimation Filter if DMCLK1 (DMCLK2) = “H”, Lch data is input if DMCLK1 (DMCLK2) = “L”. The DMCLK1 (DMCLK2) pin outputs “L” when DCLKE1 (DCLKE2) bit = “0”, and only supports 64fs. In this case, necessary clocks must be supplied to the AK4961 for ADC operation. The output data through “the Decimation and Digital Filters” is the negative full-scale with 0% 1’s density of 1bit output data and positive full-scale with the 100% 1’s density of 1bit output data.

DCLKP1/2 bit	DMCLK1/2 pin= “H”	DMCLK1/2 pin= “L”	(default)
0	Rch	Lch	
1	Lch	Rch	

Table 23. Data In/Output Timing with Digital Microphone

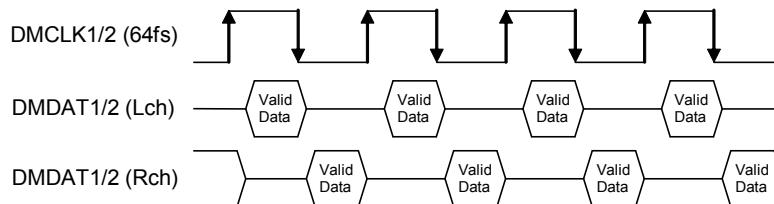


Figure 26. Data In/Output Timing with Digital Microphone (DCLKP1/2 bit = “1”)

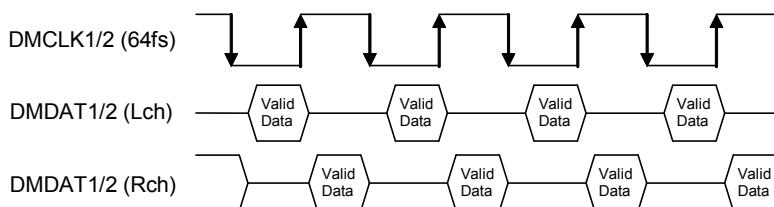


Figure 27. Data In/Output Timing with Digital Microphone (DCLKP1/2 bit = “0”)

## ■ Digital HPF

A digital High Pass Filter (HPF) is integrated for DC offset cancellation of the ADC input. The cut-off frequencies are set by HPFC1[1:0] bits for ADC1, HPFC2[1:0] bits for ADC2 ([Table 24](#)). It is proportional to the sampling frequency (fs) and default is 3.4Hz (@fs = 44.1kHz). HPFAD1N and HPFAD2N bits control the ON/OFF of the HPF (Recommend HPF enable).

HPFC11 bit HPFC21 bit	HPFC10 bit HPFC20 bit	Cut-off Frequency			(default)
		fs=8kHz	fs=44.1kHz	fs=96kHz	
0	0	0.62Hz	3.4Hz	7.4Hz	
0	1	2.47Hz	13.6Hz	29.6Hz	
1	0	19.7Hz	108.8Hz	236.4Hz	
1	1	39.5Hz	217.6Hz	474Hz	

Table 24. ADC1/2 HPF Cut-off Frequency

## ■ ADC Digital Filter Setting

ADC has three types of digital filter. The filter mode can be selected by AD1SD[1:0] bits (ADC1) and AD2SD[1:0] bits (ADC2). Default is Sharp Roll-Off Filter 1(AD1SD[1:0] = AD2SD[1:0] bits =“00”).

AD1SD1 bit AD2SD1 bit	AD1SD0 bit AD2SD0 bit	ADC1/2 Filter Mode Setting	(default)
0	0	Sharp Roll-Off Filter 1	
0	1	Sharp Roll-Off Filter 2	
1	0	Short Delay Sharp Roll-Off Filter	
1	1	N/A	

Table 25. ADC Digital Filter Setting (N/A: Not available)

## ■ DAC Digital Filter Setting

DAC1 has five types of digital filter. The filter mode of DAC1 can be selected by DA1SD, DA1SL and DFTHR1 bits. When DFTHR1 bit is “1”, the setting of DA1SD and DA1SL bits is ignored. Default is Sharp Roll-Off Filter (DFTHR1 = DA1SD = DA1SL bits = “0”).

The filter mode of DAC2 can select Sharp Roll-Off Filter and Decimation Filter Bypass Mode.

When DFTHR1 bit is “1”, level detection of Class-G, DVOL/Mixing functions of DAC1 and analog volume zero crossing detection of HP-Amp cannot be used. When DFTHR2 bit is “1”, DVOL/Mixing functions of DAC2 cannot be used.

When SRCE output mode is 8fs, DFTHR1(DFTHR2) bit should be set to “1”.

DFTHR1 bit	DA1SD bit	DA1SL bit	DAC1 Filter Mode Setting
0	0	0	Sharp Roll-Off Filter
0	0	1	Slow Roll-Off Filter
0	1	0	Short Delay Sharp Roll-Off Filter
0	1	1	Short Delay Slow Roll-Off Filter
1	x	x	Decimation Filter Bypass Mode

Table 26. DAC1 Digital Filter Setting (x: Do not Care)

DFTHR2 bit	DAC2 Filter Mode Setting
0	Sharp Roll-Off Filter
1	Decimation Filter Bypass Mode

Table 27. DAC2 Digital Filter Setting

## ■ Direct Interface Mode

When EXIF bit is set to “1”, the AK4961 becomes “Direct Interface Mode”. In this mode, the clock and data are directly applied to CODEC without “Serial Audio Data Bus”.

EXIF bit	Normal Mode			Direct I/F Mode		
	0		1			
	Pin Name	Pin Name	Pin Name	Clock & Format		
MCKI pin	MCKI	CODECMCLK	CODECMCLK	256fs/512fs/1024fs		
SYNC1 pin	SYNC1	CODECSYNC	CODECSYNC	1fs		
BCLK1 pin	BCLK1	CODECBCLK	CODECBCLK	64fs		
SDTI1A pin	SDTI1A	CODECSDTI1	CODECSDTI1	16-32bit I <sup>2</sup> S		
SDTI1B pin	SDTI1B	CODECSDTI2	CODECSDTI2	16-32bit I <sup>2</sup> S		
SDTO1A pin	SDTO1A	CODECSDTO1	CODECSDTO1	16-24bit I <sup>2</sup> S		
SDTO1B pin	SDTO1B	CODECSDTO2	CODECSDTO2	16-24bit I <sup>2</sup> S		

Table 28. Direct Interface Mode

## ■ Digital Mixing 1/2

The AK4961 has digital mixing circuits for Lch and Rch of both DAC1 and DAC2. They can mix the data digitally and convert the polarity. The inverted data by this polarity conversion is calculated in 2's complement format.

MDAC1L bit MDAC1R bit	RDAC1L bit RDAC1R bit	LDAC1L bit LDAC1R bit	DAC1 Lch Input Data DAC1 Rch Input Data	(default)
0	0	0	MUTE	
0	0	1	Lch	
0	1	0	Rch	
0	1	1	Lch + Rch	
1	0	0	MUTE	
1	0	1	Lch/2	
1	1	0	Rch/2	
1	1	1	(Lch + Rch)/2	

Table 29. DAC1 L/Rch Input Signal Select

MDAC2L bit MDAC2R bit	RDAC2L bit RDAC2R bit	LDAC2L bit LDAC2R bit	DAC2 Lch Input Data DAC2 Rch Input Data	(default)
0	0	0	MUTE	
0	0	1	Lch	
0	1	0	Rch	
0	1	1	Lch + Rch	
1	0	0	MUTE	
1	0	1	Lch/2	
1	1	0	Rch/2	
1	1	1	(Lch + Rch)/2	

Table 30. DAC2 L/Rch Input Signal Select

INV1L bit INV1R bit INV2L bit INV2R bit	Output Data	(default)
0	Normal	
1	Inverting	

Table 31. DAC1/2 L/Rch Input Signal Polarity Select

## ■ Digital Volume 1/2

The AK4961 has 32-level digital volume in front of DAC1 and DAC2. The volume is changed from +3dB to -12dB in 0.5dB step including Mute. The volume change is executed immediately by setting registers.

When OVOLC1N (OVOLC2N) bit is “1”, the OVL1[4:0] (OVL2[4:0]) bits control Lch level and OVR1[4:0] (OVR2[4:0]) bits control Rch level. When OVOLC1N (OVOLC2N) bit = “0”, the OVL1[4:0] (OVL2[4:0]) bits control both Lch and Rch attenuation levels. In this case, OVR1[4:0] (OVR2[4:0]) bits are ignored.

OVL1[4:0] bits OVR1[4:0] bits OVL2[4:0] bits OVR2[4:0] bits	Volume (dB)
1FH	+3
1EH	+2.5
1DH	+2
1CH	+1.5
1BH	+1
1AH	+0.5
19H	0
18H	-0.5
17H	-1
16H	-1.5
15H	-2
14H	-2.5
13H	-3
12H	-3.5
11H	-4
10H	-4.5
0FH	-5
0EH	-5.5
0DH	-6
0CH	-6.5
0BH	-7
0AH	-7.5
09H	-8
08H	-8.5
07H	-9
06H	-9.5
05H	-10
04H	-10.5
03H	-11
02H	-11.5
01H	-12
00H	MUTE

Table 32. Setting of Digital Volume 1/2

## ■ Headphone-Amplifier (HPL/HPR pins)

Headphone amplifiers are operated by positive and negative power that is supplied from internal charge pump circuit. The VEE2 pin output the negative voltage generated by the internal charge pump circuit from CVDD. This charge pump circuit is switched between VDD mode, 1/2VDD mode and WAIT mode by the output level of the headphone amplifiers. The headphone amplifier output is single-ended and centered on HPGND (0V). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is  $16\Omega$ . The output power is 10mW (@0dBFS,  $R_L = 32\Omega$ , AVDD1=AVDD2=CVDD=1.8V, HPG = -4dB) and 25mW (@0dBFS,  $R_L = 32\Omega$ , AVDD1=AVDD2=CVDD=1.8V, HPG=0dB). Ground loop noise cancelling function for headphone amplifier is available by connecting the HPGND pin to the ground of the jack.

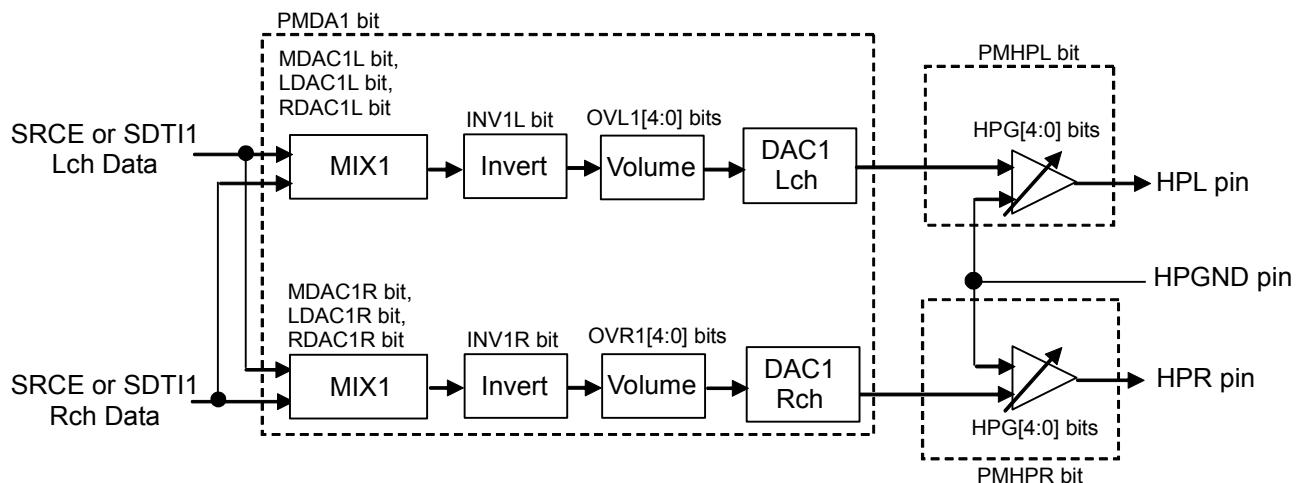


Figure 28. DAC1 & Headphone-Amp Block Diagram

CPMODE1 bit	CPMODE0 bit	Mode	Operation Voltage	
0	0	Class-G Operation Mode	Automatic Switching	(default)
0	1	$\pm$ VDD Operation Mode	$\pm$ VDD	
1	0	$\pm$ 1/2 VDD Operation Mode	$\pm$ 1/2 VDD	
1	1	N/A	N/A	

Table 33. Charge Pump Mode Setting (N/A: Not available)

### <Class-G Mode Switching Level>

VDD → 1/2VDD: < 1.05mW at both channels (@CVDD=1.8V,  $R_L=32\Omega$ )  
 1/2VDD → VDD:  $\geq$  1.05mW at either channel (@CVDD=1.8V,  $R_L=32\Omega$ )

When the charge pump operation mode is changed to VDD mode from 1/2VDD mode, an internal counter for holding VDD mode starts (Table 34). The charge pump changes to 1/2VDD mode if the output signal level is lower than the switching level and 1/2VDD mode detection time that is set by LVDTM[2:0] is passed after VDD mode hold time is finished.

VDDTM[3:0] bits		VDD Mode Holding Period			
		8kHz	44.1kHz	96kHz	192kHz
0000	1024/fs	128ms	23.2ms	10.7ms	5.3ms
0001	2048/fs	256ms	46.4ms	21.3ms	10.7ms
0010	4096/fs	512ms	92.9ms	42.7ms	21.3ms
0011	8192/fs	1024ms	186ms	85.3ms	42.7ms
0100	16384/fs	2048ms	372ms	170.7ms	85.3ms
0101	32768/fs	4096ms	743ms	341.3ms	170.7ms
0110	65536/fs	8192ms	1486ms	682.7ms	341.3ms
0111	131072/fs	16384ms	2972ms	1365.3ms	682.7ms
1xxx	262144/fs	32768ms	5944ms	2730.7ms	1365.3ms

(default)

Table 34. VDD Mode Holding Period Setting (x: Do not care)

When the output voltage becomes less than class-G mode switching level, the internal detection counter for 1/2VDD mode which is set by LVTDM[2:0] bits starts. This counter is reset when the output voltage exceeds class-G mode switching level. The charge pump operation mode is changed to VDD from 1/2 VDD if the detection counter of 1/2VDD mode is finished and also the 1/2VDD mode hold period is passed.

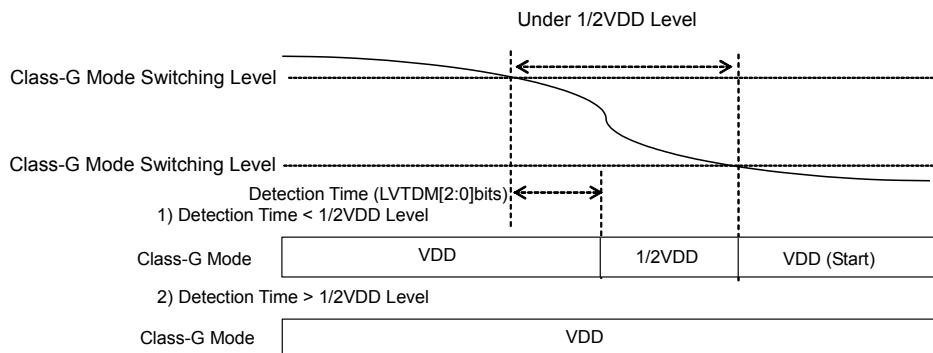


Figure 35. Transition to 1/2VDD Mode from VDD Mode

LVDTM[2:0] bits		1/2VDD Mode Detection Time/ Minimum Frequency That Is Not Detected			
		8kHz	44.1kHz	96kHz	192kHz
000	64/fs	8ms	1.5ms	0.67ms	0.33ms
		62.5Hz	344.5Hz	750Hz	1500Hz
001	128/fs	16ms	2.9ms	1.3ms	0.67ms
		31.3Hz	172.3Hz	375Hz	750Hz
010	256/fs	32ms	5.8ms	2.7ms	1.3ms
		15.6Hz	86.1Hz	187.5Hz	375Hz
011	512/fs	64ms	11.6ms	5.3ms	2.7ms
		7.8Hz	43.1Hz	93.8Hz	187.5Hz
100	1024/fs	128ms	23.2ms	10.7ms	5.3ms
		3.9Hz	21.5Hz	46.9Hz	93.8Hz
101	2048/fs	256ms	46.4ms	21.3ms	10.7ms
		2.0Hz	10.8Hz	23.4Hz	46.9Hz
110	4096/fs	512ms	92.9ms	42.7ms	21.3ms
		1.0Hz	5.4Hz	11.7Hz	23.4Hz
111	8192/fs	1024ms	185.8ms	92.9ms	42.7ms
		0.5Hz	2.7Hz	5.9Hz	11.7Hz

Table 35. 1/2VDD Detection Period (Minimum frequency that is not detected)

### <Headphone Amplifier Volume Circuit>

The output level of headphone amplifier can be controlled by HPG[4:0] bits. This volume is in common for L/R channels and can attenuate/gain from +6dB to -40dB in 2dB steps ([Table 36](#)). When the volume is changed, zero cross detection is executed independently on L and R channels. Zero crossing timeout period is set by HPTM2-0 bits ([Table 37](#)).

HPG[4-0] bits	Volume (dB)
19H ~ 1FH	N/A
18H	+6
17H	+4
16H	+2
15H	<b>0</b>
14H	-2
13H	-4
12H	-6
11H	-8
10H	-10
0FH	-12
0EH	-14
0DH	-16
0CH	-18
0BH	-20
0AH	-22
09H	-24
08H	-26
07H	-28
06H	-30
05H	-32
04H	-34
03H	-36
02H	-38
01H	-40
00H	MUTE

Table 36. Headphone Amplifier Volume Setting (N/A: Not available)

HPTM2 bit	HPTM1 bit	HPTM0 bit	Zero Crossing Timeout Period			
			8kHz	44.1kHz	96kHz	192kHz
0	0	0	128/fs	16ms	2.9ms	1.3ms
0	0	1	256/fs	32ms	5.8ms	2.7ms
0	1	0	512/fs	64ms	11.6ms	5.3ms
0	1	1	1024/fs	128ms	23.2ms	10.7ms
1	x	x	2048/fs	256ms	46.4ms	21.4ms

(default)

Table 37. Headphone Amplifier Volume Setting (x: Do not care)

### <Headphone-Amp External Circuit>

It is necessary to put an oscillation prevention circuit ( $0.22\mu\text{F}\pm20\%$  capacitor and  $10\Omega\pm20\%$  resistor) because there is a possibility that the Headphone-Amp oscillates.

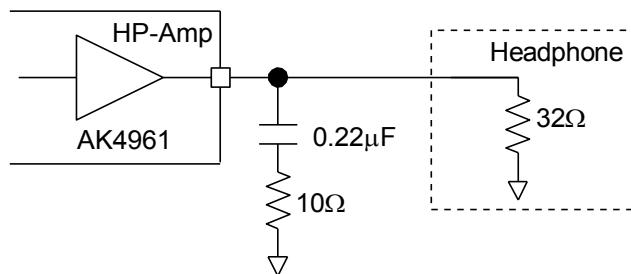


Figure 29. Headphone-Amp Oscillation Prevention Circuit Example

### <Power-Up/down Sequence of Headphone Amplifier>

After releasing DAC1 power-down state by PMDA1 bit, the headphone amplifier should be powered-up by PMHPL/R bits. A wait time from DAC1 power-up to headphone power-up is not necessary. PMDA1 bit releases a power-down of the digital block of the DAC1, PMHPL or PMHPR bit powers up the analog block of the DAC1 and the headphone amplifier. The gain setting (HPG[4:0] bits) should be made before PMDA1 bit is set to “1”. A wait time from the gain setting to PMDA1 bit = “1” is not necessary.

The headphone amplifier should be powered down first and the DAC1 should be powered down next. (There is no time limitation for this sequence.) When the headphone amplifier is powered-down, HPL and HPR pins are pulled down to HPGND via the internal pull-down resistor. The pulled-down resistor is  $9\Omega$ (typ). When the headphone amplifier is power down and HPLHZ and HPRHZ bits are set to “1”, the HPL and HPR pins are pull down to HPGND via the internal pull-down resistor.

PMHPL bit PMHPR bit	HPLHZ bit HPRHZ bit	HP-Amp Status
0	0	Pull-down by $9\Omega$ (typ)
0	1	Pull-down by $200\text{k}\Omega$ (typ)
1	x	Normal Operation

Table 38. State of Headphone Amplifier (x: Do not care)

If the pop noise at power-down exceeds an acceptable range, headphone amplifier should be powered down after attenuating the headphone volume gradually until mute.

The power-up time of headphone amplifier is shown in [Table 39](#). The HPL and HPR pins output 0V (HPGND) during power-up time. After that, they are in normal operation state. The power-down is executed immediately.

Sampling Frequency[kHz]	Power-Up Time(max)
8/12/16/24/32/48/64/96/128/192	23.9ms
11.025/22.05/44.1/88.2/176.4	25.9ms

Table 39. Headphone-Amp Power-up Time

## &lt;Example of Power-up sequence&gt;

1. Path, Digital Volume, Analog Volume Setting
2. CP3 Power-Up (PMCP3 bit: “0” → “1”)
3. Wait 6.5ms
4. LDO3P& LDO3N Power-Up (PMLDO3P & PMLDO3N bits: “0” → “1”)
5. Wait 1ms
6. DAC1 Power-Up (PMDAC1 bit: “0” → “1”)
7. CP2 Power-Up (PMCP2 bit: “0” → “1”)
8. Wait 4.5ms
9. Headphone-Amp Power-Up (PMHPL/R bits: “0” → “1”)
10. Wait 25.9ms (@ fs=44.1kHz)
11. Playback

## &lt;Example of Power-down sequence&gt;

1. Headphone-Amp Power-down (PMHPL/R bits: “1” → “0”)
2. CP2 Power-down (PMCP2 bit: “1” → “0”)
3. DAC1 Power-down (PMDAC1 bit: “1” → “0”)
4. LDO3P & LDO3N Power-Down (PMLDO3P & PMLDO3N bits: “1” → “0”)
5. CP3 Power-down (PMCP3 bit: “1” → “0”)
6. Stop

**<Simultaneous Use of Headphone-Amp, Receiver-Amp and Lineout 1/2>**

When using the headphone and Lineout 1/2 amplifiers at the same time, power up Lineout 1/2 amplifier after the headphone is powered up. Do not power Lineout 1/2 and Receiver amplifiers Up/Down during power-up sequence of the headphone. The headphone amplifier and the receiver amplifier cannot be used together.

**<Over Current protection Circuit>**

If the headphone amplifier is in an overcurrent state, such as when output pins are shorted, the headphone amplifier limits the operation current. The headphone amplifier returns to a normal operation state if all causes are cleared.

## ■ 24-bit DAC2 Path

The 24-bit DAC2 outputs the data to Single-ended Lineout1, Single-ended/Differential Lineout 2 and Mono Receiver-Amp. Although the digital block is in common for these outputs, the output channels can be powered up/down independently.

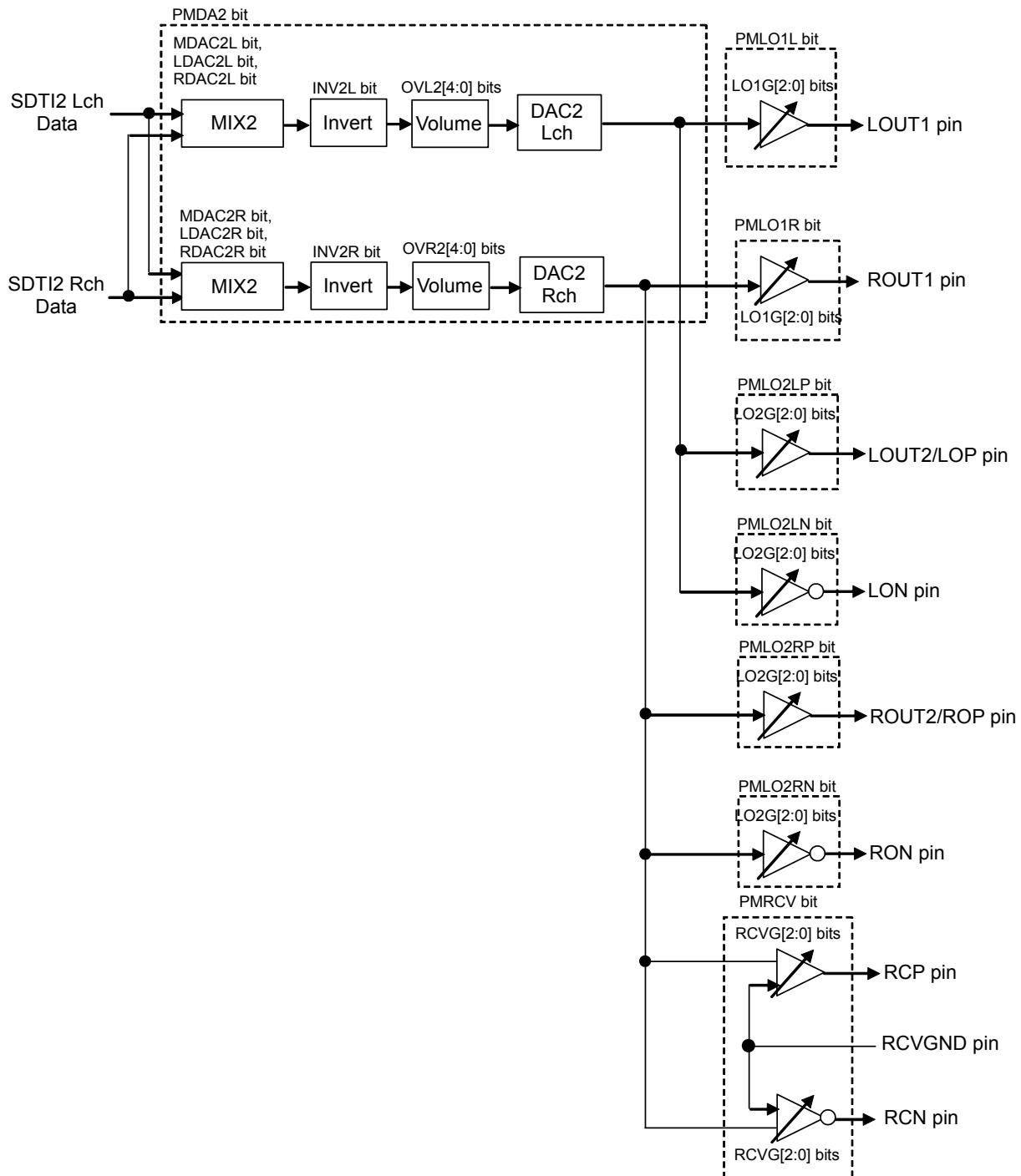


Figure 30. DAC2 & Lineout1/2 & Receiver-Amp Block Diagram

## ■ Lineout 1

L and R channel signals of the 24-bit DAC2 are output from the LOUT1 and ROUT1 pins. The output signal of the DAC2 is single-ended and centered on 0V (LGND). Therefore, the capacitor for AC-coupling can be removed. The load resistance is minimum 10kΩ. LO1G[2:0] bits control the output level of Lineout 1 (Table 40). The volume of L and R channels are controlled together, ranging from +3dB to -7.5dB in +1.5dB steps. The volume value is changed immediately by setting LO1G[2:0] bits. Set IBIAS bit to “1” when operating the Lineout 1 in quad speed mode ( $fs \geq 128\text{kHz}$ ).

LO1G[2-0] bits	Volume (dB)	
7H	+3	
6H	+1.5	
5H	0	(default)
4H	-1.5	
3H	-3	
2H	-4.5	
1H	-6	
0H	-7.5	

Table 40. Lineout 1 Amplifier Volume Setting

### <Lineout 1 Power Up/Down Sequence>

Release the power down state of the Lineout 1 by PMLO1L/R bits after power up the DAC2 by PMDA2 bit. (A wait time from DAC power-up to headphone power-up is not necessary.)

The Lineout 1 amplifier should be powered down first and the DAC2 should be powered down next. (There is no time limitation for this sequence.) When the Lineout 1 amplifier is powered down, LOUT1 and ROUR1 pins are pulled down to LGND via the internal pull-down resistor. The pulled-down resistor is 8Ω(typ).

PMLO1L bit PMRO1R bit	LINEOUT1-Amp Status
0	Pull-down by 8Ω (typ)
1	Normal Operation

Table 41. Lineout 1 Output Status (x: Do not care)

The power-up time of Lineout 1 amplifier block is shown in Table 42. The LOUT1 pin and ROUT1 pin output 0V (LGND) during a power-up sequence of the Lineout 1. The Lineout 1 is in normal operation after finishing a power-up sequence. Power-down of the Lineout 1 block is executed immediately.

Sampling Frequency[kHz]	Power-Up Time(max)
8/12/16/24/32/48/64/96/128/192	4.2ms
11.025/22.05/44.1/88.2/176.4	4.4ms

Table 42. Lineout 1 Power-up Time

<Example of Power-up Sequence>

1. Path, Digital Volume, Analog Volume Setting
2. CP3 Power-Up (PMCP3 bit: “0” → “1”)
3. Wait 6.5ms
4. LDO3P& LDO3N Power-Up (PMLDO3P & PMLDO3N bits: “0” → “1”)
5. Wait 1ms
6. DAC2 Power-Up (PMDAC2 bit: “0” → “1”)
7. Lineout 1 Power-Up (PMLO1L/R bits: “0” → “1”)
8. Wait 4.4ms (@ fs=44.1kHz)
9. Playback

<Example of Power-down Sequence>

1. Lineout 1 Power-down (PMLO1/L/R bits: “1” → “0”)
2. DAC2 Power-down (PMDAC2 bit: “1” → “0”)
3. LDO3P & LDO3N Power-Down (PMLDO3P & PMLDO3N bits: “1” → “0”)
4. Stop

#### <Power up Lineout 1 while Lineout 2 is in operation>

When power up the Lineout 1 while the Lineout 2 is in operation, 0V is output from the Lineout 1 and the common voltage is output from the DAC2 even if a data is input to the DAC2. This is to prevent a pop noise at the Lineout 1. Therefore, the Lineout 2 output will be interrupted for a period shown in [Table 42](#).

## ■ Lineout 2

The Lineout 2 supports both single-ended and differential output modes. LO2DIF bit selects these modes. The Lineout 2 output is centered on 0V (LGND). Therefore, the capacitor for AC-coupling can be removed. The load resistance is minimum 10kΩ in single-ended mode, and minimum 20kΩ between Positive and Negative pins in differential mode. Set IBIAS bit to “1” when operating the Lineout 2 in quad speed mode ( $f_s \geq 128\text{kHz}$ ).

LO2DIF bit	Mode	Output Pin		(default)
		Lch	Rch	
0	Single-ended Mode	LOUT pin	ROUT pin	
1	Differential Mode	LOP/LON pins	ROP/RON pins	

Table 43. Lineout 2 Output Mode Setting

The output level of the Lineout 2 is controlled by LO2G[2:0] bits (Table 44). The volume of L and R channels are controlled together, ranging from +3dB to -7.5dB in +1.5dB steps. The volume value is changed immediately by setting LO2G[2:0] bits.

LO2G[2-0] bits	Volume (dB)
7H	+3
6H	+1.5
5H	0
4H	-1.5
3H	-3
2H	-4.5
1H	-6
0H	-7.5

(default)

Table 44. Lineout 2 Amplifier Volume Setting

### <Lineout 2 Power Up/Down Sequence>

Release the power down state of the Lineout 2 by PMLO2L/R bits after power up the DAC2 by PMDA2 bit. (A wait time from DAC power-up to Lineout 2 power-up is not necessary.) It is not necessary to set PMLO2LN and PMRO2RN bits to “1” in single-ended mode. Independent power management of L and R channels is available.

The Lineout 2 amplifier should be powered down first and the DAC2 should be powered down next. (There is no time limitation for this sequence.) When the Lineout 2 amplifier is powered down, LOUT2 and ROUT2 pins (in Single-ended Mode, LOP/N and ROP/N pins in Differential Mode) are pulled down to LGND via the internal pull-down resistor. The pulled-down resistor is 8Ω(typ).

PMLO2LP bit PMRO2LNbit PMLO2RP bit PMRO2LN bit	LINEOUT2-Amp Status
0	Pull-down by 8Ω (typ)
1	Normal Operation

Table 45. Lineout 2 Output Status (x: Do not care)

The power-up time of Lineout 2 amplifier block is shown in [Table 46](#). The LOUT2 (LOP/LON) pin and ROUT2 (ROP/RON) pin output 0V (LGND) during a power-up sequence of the Lineout 2. The Lineout2 is in normal operation after finishing the power-up sequence. Power-down of the Lineout 2 block is executed immediately

Sampling Frequency[kHz]	Power-Up Time (max)
8/12/16/24/32/48/64/96/128/192	4.2ms
11.025/22.05/44.1/88.2/176.4	4.4ms

Table 46. Lineout 2 Power-Up Time

In differential mode, PMLO2LP and PMLO2LN bits should be powered up/down simultaneously. A pop noise may occur if these bits are set to “1” separately since the Lineout 2 is powered up immediately before the power-up time shown in [Table 46](#).

## &lt;Example of Power-up Sequence&gt;

1. Path, Digital Volume, Analog Volume Setting
2. CP3 Power-Up (PMCP3 bit: “0” → “1”)
3. Wait 6.5ms
4. LDO3P & LDO3N Power-Up (PMLDO3P & PMLDO3N bits: “0” → “1”)
5. Wait 1ms
6. DAC2 Power-Up (PMDAC2 bit: “0” → “1”)
7. Lineout 2 Power-Up (PMLO2LP/N = PMLO2RP/N bits: “0” → “1” @ Stereo Differential Mode)
8. Wait 4.4ms (@ fs=44.1kHz)
9. Playback

## &lt;Example of Power-down Sequence&gt;

1. Lineout 2 Power-down (PMLO2LP/N = PMLO2RP/N bits: “1” → “0” @ Stereo Differential Mode)
2. DAC2 Power-down (PMDAC2 bit: “1” → “0”)
3. LDO3P & LDO3N Power-Down (PMLDO3P & PMLDO3N bits: “1” → “0”)
4. Stop

**< Power up Lineout 2 while Lineout 1 is in operation >**

When power up the Lineout 2 while the Lineout 1 is in operation, 0V is output from the Lineout 2 and the common voltage is output from the DAC2 even if a data is input to the DAC2. This is to prevent a pop noise at the Lineout 2. Therefore, the Lineout 1 output will be interrupted for a period shown in [Table 46](#).

## ■ Receiver Amplifier

The R channel signal of the 24-bit DAC2 is output from the RCP and RCN pins. The receiver amplifier outputs are differential and centered on 0V (RCVGND). The load resistance is minimum  $32\Omega$ . RCVG[2:0] bits control the output level of the receiver amplifier (Table 47). The volume ranges from +3dB to -7.5dB in +1.5dB steps. It is changed immediately by setting RCVG[2:0] bits. The power supply of the receiver amplifier is supplied by the Charge Pump 2 (Class-G) that is common in the headphone amplifier. Therefore, when the receiver amplifier is powered up, the Charge Pump 2 enters VDD fixed mode automatically. **The Receiver-Amp does not support quad speed mode ( $fs \geq 128\text{kHz}$ ).**

RCVG[2-0] bits	Volume (dB)	
7H	+3	
6H	+1.5	
5H	0	(default)
4H	-1.5	
3H	-3	
2H	-4.5	
1H	-6	
0H	-7.5	

Table 47. Receiver-Amp Volume Setting

### <Receiver-Amp Power Up/Down Sequence>

Release the power down state of the Receiver amplifier by PMRCV bit after power up the DAC2 by PMDA2 bit. (A wait time from DAC2 power-up to Receiver amplifier power-up is not necessary.) The gain setting (RCVG[2:0] bits) should be made before setting PMDA2 bit = "1". There is no time limitation from gain setting to PMDA2 bit = "1". Do not power the Lineout 1 and Lineout 2 ON/OFF while the Receiver amplifier is in power-up sequence.

The Receiver amplifier should be powered down first and the DAC2 should be powered down next. (There is no time limitation for this sequence.) When the Receiver amplifier is powered down, RCP and RCN pins are pulled down to RCVGND via the internal pull-down resistor. The pulled-down resistor is  $5\Omega$ (typ).

PMRCV bit	Receiver-Amp Status
0	Pull-down by $5\Omega$ (typ)
1	Normal Operation

Table 48. Receiver-Amp Output Status

The power-up time of the Receiver amplifier is shown in Table 49. The RCP pin and RNC pin output 0V (RCVGND) during a power-up sequence of the Receiver amplifier. Power-down of the Receiver amplifier block is executed immediately.

Sampling Frequency[kHz]	Power-Up Time(max)
8/12/16/24/32/48/64/96	15.2ms
11.025/22.05/44.1/88.2	16.4ms

Table 49. Receiver-Amp Power-up Time

<Example of Power-up sequence>

1. Path, Digital Volume, Analog Volume Setting
2. CP3 Power-Up (PMCP3 bit: “0” → “1”)
3. Wait 6.5ms
4. LDO3P& LDO3N Power-Up (PMLDO3P & PMLDO3N bits: “0” → “1”)
5. Wait 1ms
6. DAC2 Power-Up (PMDAC2 bit: “0” → “1”)
7. CP2 Power-Up (PMCP2 bit: “0” → “1”)
8. Wait 4.5ms
9. Receiver-Amp Power-Up (PMRCV bit: “0” → “1”)
10. Wait 16.4ms (@ fs=44.1kHz)
11. Playback

<Example of Power-down sequence>

1. Receiver-Amp Power-down (PMHPL/R bits: “1” → “0”)
2. CP2 Power-down (PMCP2 bit: “1” → “0”)
3. DAC2 Power-down (PMDAC2 bit: “1” → “0”)
4. LDO3P & LDO3N Power-Down (PMLDO3P & PMLDO3N bits: “1” → “0”)
5. CP3 Power-down (PMCP3 bit: “1” → “0”)
6. Stop

### <Over Current protection Circuit>

When the receiver amplifier enters an irregular state and is in an over current state (e.g. output pins are shortened), it limits the current. When the causes are cleared, the receiver amplifier returns to a normal operation state.

## ■ Charge Pump & LDO Circuits

CVDD is used to generate negative and positive voltage. The power-up/down sequence of charge pump and LDO circuits is as follows. CP1 and CP3 should be powered up before LDO1 and LDO3N are powered up. CP2 should be powered up after LDO3P and LDO3N are powered up.

**Power-up sequence: CP1, CP3 → LDO1, LDO3P, LDO3N → CP2**

**Power-down sequence: CP2 → LDO3P, LDO3N, LDO1 → CP1, CP3**

Each power-up time is shown in [Table 50](#). The charge pump and the LDO1 circuits, except for the LDO2, can be powered up again while they are in power-down state.

Block	Power-up Time (max)
CP1	6.5ms
CP2	4.5ms
CP3	6.5ms
LDO1	0.3ms
LDO2	1ms
LDO3P/N	1ms

Table 50. Charge Pump & LDO Power-up Time

LDO3P and LDO3N have an over current protection circuit. When over current flows in a normal operation, the LDO3P and LDO3N circuits limit the operation current. If the over current state is cleared, the over current protection will be off and the LDO3P and LDO3N circuits will return to normal operation.

LDO2 has an overvoltage protection circuit. This overvoltage protection circuit powers the LDO2 down when the power supply becomes unstable by an instantaneous power failure, etc. during operation. The LDO2 circuit will not return to normal operation until being reset by the PDN pin ("L" → "H") after removing the problems.

Charge Pump	Power Management bit	Power Supply	Output Voltage (typ)	Use Block
CP1	PMCP1	CVDD	3.6V	LDO1
CP2(Class-G)	PMCP2	CVDD	±1.8V/±0.9V	HP/RCV
CP3	PMCP3	CVDD	-1.8V	LDO3N DAC1 Lineout 1/2 RCV

Table 51. Power supply voltage, Output Voltage, Control Register and use block of Charge Pump

LDO	Power Management bit	Power Supply	Output Voltage (typ)	Use Block
LDO1	PMLDO1	CP1/ VSS1	+3.3V	MIC Power, MIC-Amp, ADC
LDO2	(Controlled by LDO2E pin)	LVDD or VCC12/ VSS1	+1.2V	Digital Core, SLIMbus, SRAM, SPI
LDO3P	PMLDO3P	AVDD2/VSS2	+1.5V	VREF+ for DAC1/2, HP, RCV, Lineout 1/2
LDO3N	PMLDO3N	VSS2/CP3 Output	-1.5V	VREF- for DAC1, HP, RCV, Lineout 1/2

Table 52. Power supply voltage, Output Voltage, Control Register and use block of LDO

## ■ Accessory Detection

The AK4961 has JACK Detection, Microphone Detection and Remote Control (Button Press) functions. When the INTN pin is “L”, a microcontroller reads Event bit and Status bit. After that, the microcontroller sets the control registers corresponding to the Event/Status.

Event bit: Register of error handling of the INTN pin

When Event bit is changed from “0” to “1”, the INTN pin is changed from “H” to “L”. Event of accessory detection is shown in [Table 53](#)

Status bit: Status registers for each function:

The status of jack detection is shown in [Table 55](#).

Event	JACK Insertion	JACK Removal	Button Press	Button Release
Event bit	<b>JDE (JACK Detection Event) bit</b>		<b>RCE (Remote Control Event) bit</b>	
Status bit	<b>JDS (JACK Detection Status) bit</b>		<b>RCS (Remote Control Status) bit</b>	

Note 93. When jack detection function is not used and mask bit (MJDE bit) is set to “1”, the INTN pin holds “H” even if JDE bit (Event bit) becomes “1”. When remote control function is not used and mask bit (MRCE bit) is set to “1”, the INTN pin holds “H” even if RCE bit (Event bit) becomes “1”

Table 53. Accessory Detection Event(Event bit, Status bit)

## ■ JACK Detection Function

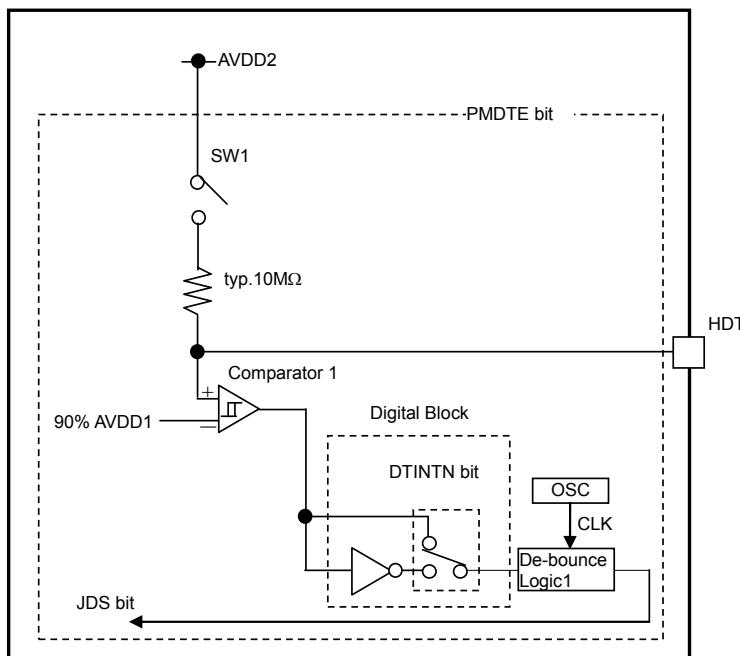


Figure 31. Jack Detection Circuit

PMDTE bit	JACK Detection Circuit	
0	Power Down	(default)
1	Power Up	

Table 54. Jack Detection Circuit Power Management

JDS bit	JACK Detection Status	
0	Removal	(default)
1	Insertion	

Table 55. Jack Detection Status

JDT bit	De-bounce Time 1(typ.)	
0	20ms	(default)
1	50ms	

Table 56. De-bounce Time1 (Tolerance: typ. ±50%)

DTINTN bit	HDT pin	Comparator1 Output	JDS bit (JACK Detection Status)
0	< 90% AVDD1	L	1
	≥ 90% AVDD1	H	0
1	≥ 90% AVDD1	H	1
	< 90% AVDD1	L	0

Note 94. If output level of HP-Amp is over 90% AVDD1, the jack detection circuit may not work correctly.

For example, when a signal of 0dBFS is input to the DAC, the gain of the headphone amplifier needs to be set to 0dB or less.

Table 57. HDT pin and JDS bit

## &lt;Example of connecting a Plug to the AK4961&gt;

**Case 1: In case of connecting the Lch of HP-Amp to the HDT pin when a jack is inserted.  
(DTINTN bit = “0”)**

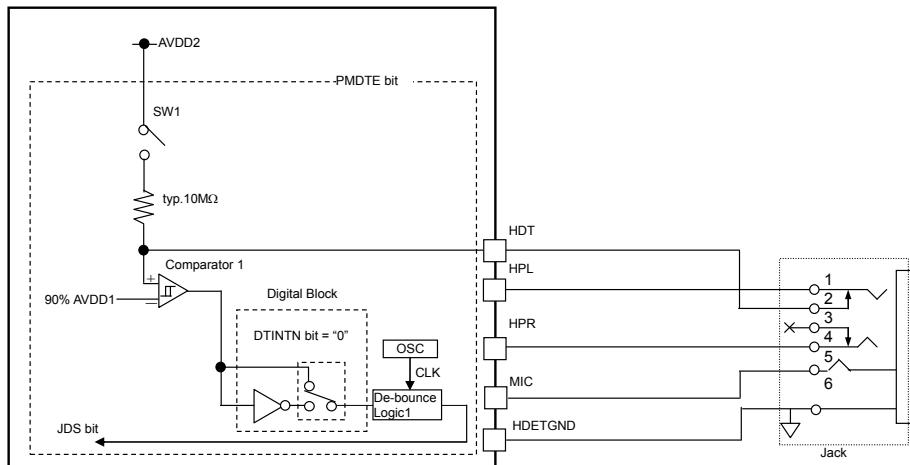


Figure 32. Example of connecting a plug and the AK4961 (DTINTN bit = “0”)

Jack Plug (Pin1-Pin2)	JACK	HDT pin	Comparator1 Output	JDS bit (JACK Detection Status)
Short	Insertion	L / HPL pin	L	1
Open	Removal	H	H	0

Table 58. Jack Detection (DTINTN bit = “0”)

**Case 2: In case of connecting HPGND and HDT pins when a jack is inserted.  
(DTINTN bit = “1”)**

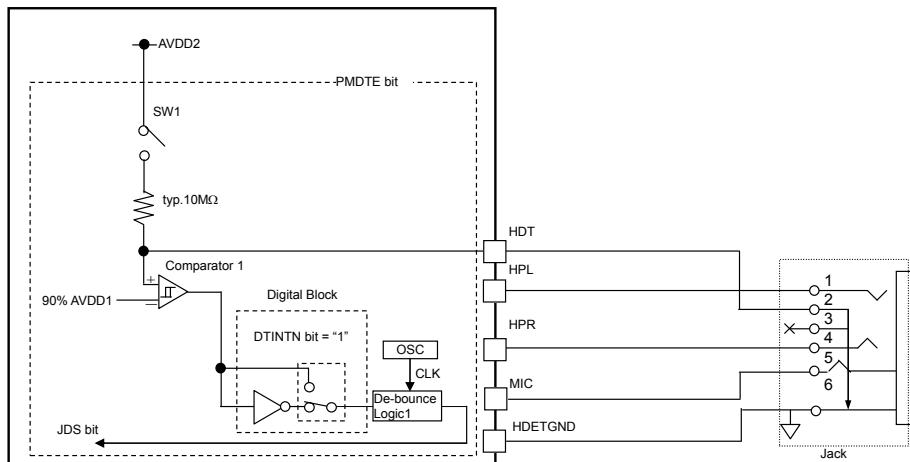


Figure 33. Example of connecting a plug and the AK4961 (DTINTN bit = “1”)

Jack Plug (Pin2-Pin6)	JACK	HDT pin	Comparator1 Output	JDS bit (JACK Detection Status)
Open	Insertion	H	H	1
Short	Removal	L / HPGND	L	0

Table 59. Jack Detection (DTINTN bit = “1”)

## ■ Microphone/Remote Control Button Detection circuit

The jack detection circuit includes detections of microphones and remote control buttons.

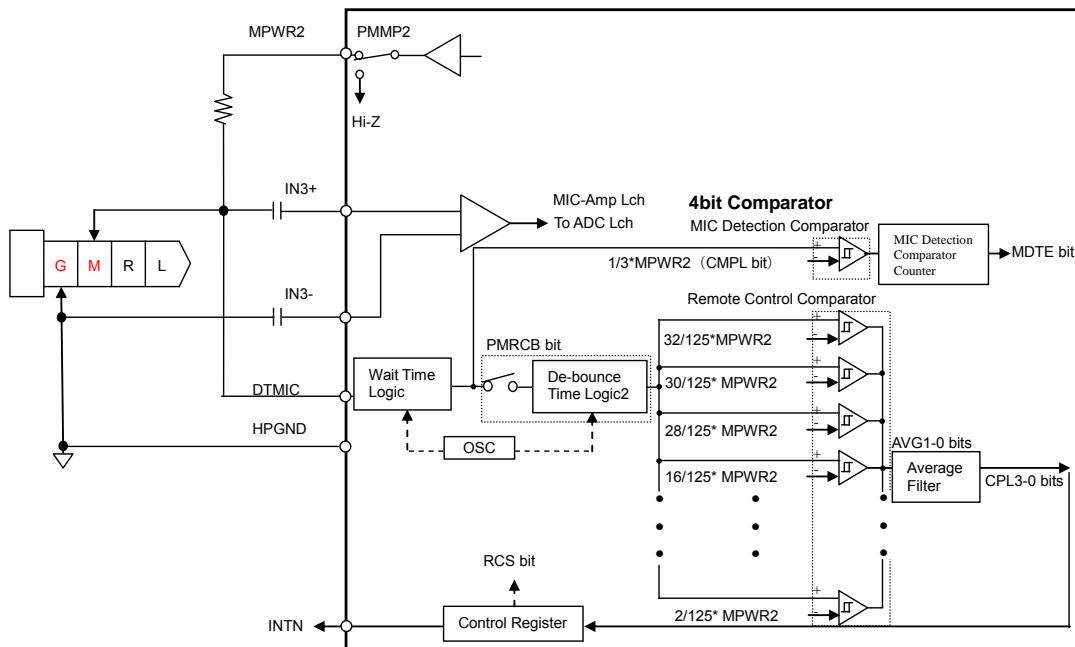


Figure 34. MIC Detection/ Remote Control Button Detection Circuit

### <MIC Detection>

MPWT2-0 bits	Wait Time(typ.)	
000	50ms	(default)
001	100ms	
010	200ms	
011	500ms	
100	1000ms	
101	1500ms	
110	N/A	
111	N/A	

Table 60. Wait Time Setting (Tolerance: typ.  $\pm 50\%$ , N/A: Not available)

CMPL bit	Reference Level of Comparator	
0	1/3 x MPWR2	(default)
1	4/9 x MPWR2	

Table 61. Setting of Comparator Reference Level

MDTE bit	Status	
0	No MIC (Headphone)	(default)
1	MIC (Headset)	

Note 95. During the jack detection sequence, the status of MDTE bit is changed once depending on output signal of comparator for microphone detection. The MDTE bit maintains the updated status regardless of the output level of comparator for microphone detection.

Table 62. Microphone Detection Status

PMRCB bit	Remote Control Circuit	
0	Disable	(default)
1	Enable	

Table 63. Remote Control Circuit Enable

CLR bit	Event Status	
0	Not Clear	(default)
1	Event Clear	

Table 64. Setting of Event Clear

MDDIF bit	Mode Select	
0	$\mu$ P Mode	(default)
1	Automatic Mode	

Table 65. Microphone Detection Mode Setting

Remote Control Button	DTMIC pin	RCS bit
ON	$\leq$ Reference Level of Comparator	1
OFF	$>$ Reference Level of Comparator	0

Table 66. Status of RCS bit when remote control button is pressed.

RCS bit	Remote Control Status	
0	Release	(default)
1	Press	

Table 67. Remote Control Status

## ■ 4bit Comparator

The AK4961 has a 4-bit comparator to detect microphones and remote control buttons. The comparator is automatically powered-up/down by internal status.

De-bounce Time 2 is time from “Button Press” to “Remote Control Comparator Power-up”. The De-bounce Time 2 can be set by CMPWT1-0 bits.

The number of sampling can be selected among 1, 6 and 10 times. When the number of sampling data selects 6 or 10 times, the AK4961 calculates the average value, discarding the minimum and maximum values by a median averaging filter, and stores the results to CPL[3:0] bits. If another event (e.g. Button press → Button Release) occurs while a median filter is processed, data of comparator output is not stored in CPL[3:0] bits. After reading CPL[3:0] bits, the data stored in CPL[3:0] bits can be reset or kept depending on the setting of CMRST bit.

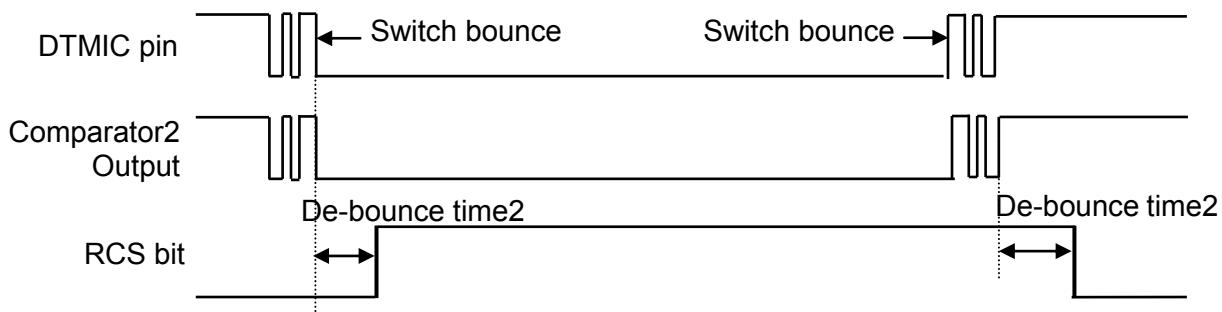


Figure 35. Sequence of Remote Control Detection

MIC Level of DTMIC pin		CPL[3:0] bits
30/125 x MPWR2	~	32/125 x MPWR2
28/125 x MPWR2	~	30/125 x MPWR2
26/125 x MPWR2	~	28/125 x MPWR2
24/125 x MPWR2	~	26/125 x MPWR2
22/125 x MPWR2	~	24/125 x MPWR2
20/125 x MPWR2	~	22/125 x MPWR2
18/125 x MPWR2	~	20/125 x MPWR2
16/125 x MPWR2	~	18/125 x MPWR2
14/125 x MPWR2	~	16/125 x MPWR2
12/125 x MPWR2	~	14/125 x MPWR2
10/125 x MPWR2	~	12/125 x MPWR2
8/125 x MPWR2	~	10/125 x MPWR2
6/125 x MPWR2	~	8/125 x MPWR2
4/125 x MPWR2	~	6/125 x MPWR2
2/125 x MPWR2	~	4/125 x MPWR2
0	~	2/125 x MPWR2
		0000

Table 68. Microphone Level of the DTMIC pin

AVG1 bit	AVG0 bit	Sampling Count	
0	0	10	(default)
0	1	6	
1	0	1	
1	1	N/A	

Table 69. Number of Sampling Data (N/A: Not available)

CMPRST bit	Sampling Data	
0	Reset	(default)
1	Hold	

Table 70. Sampling Data State When Reading Control Register

CMPWT1 bit	CMPWT0 bit	De-Bounce Time 2 (typ.)	
0	0	3ms	(default)
0	1	8ms	
1	0	20ms	
1	1	50ms	

Table 71. De-Bounce Time 2 Setting (Tolerance: typ.  $\pm 50\%$ )

**Jack Insertion Timing Chart 1:**  
**DTMIC pin=MIC Level,  $\mu$ P Operation Mode (MDDIF = DTINTN bits="0")**

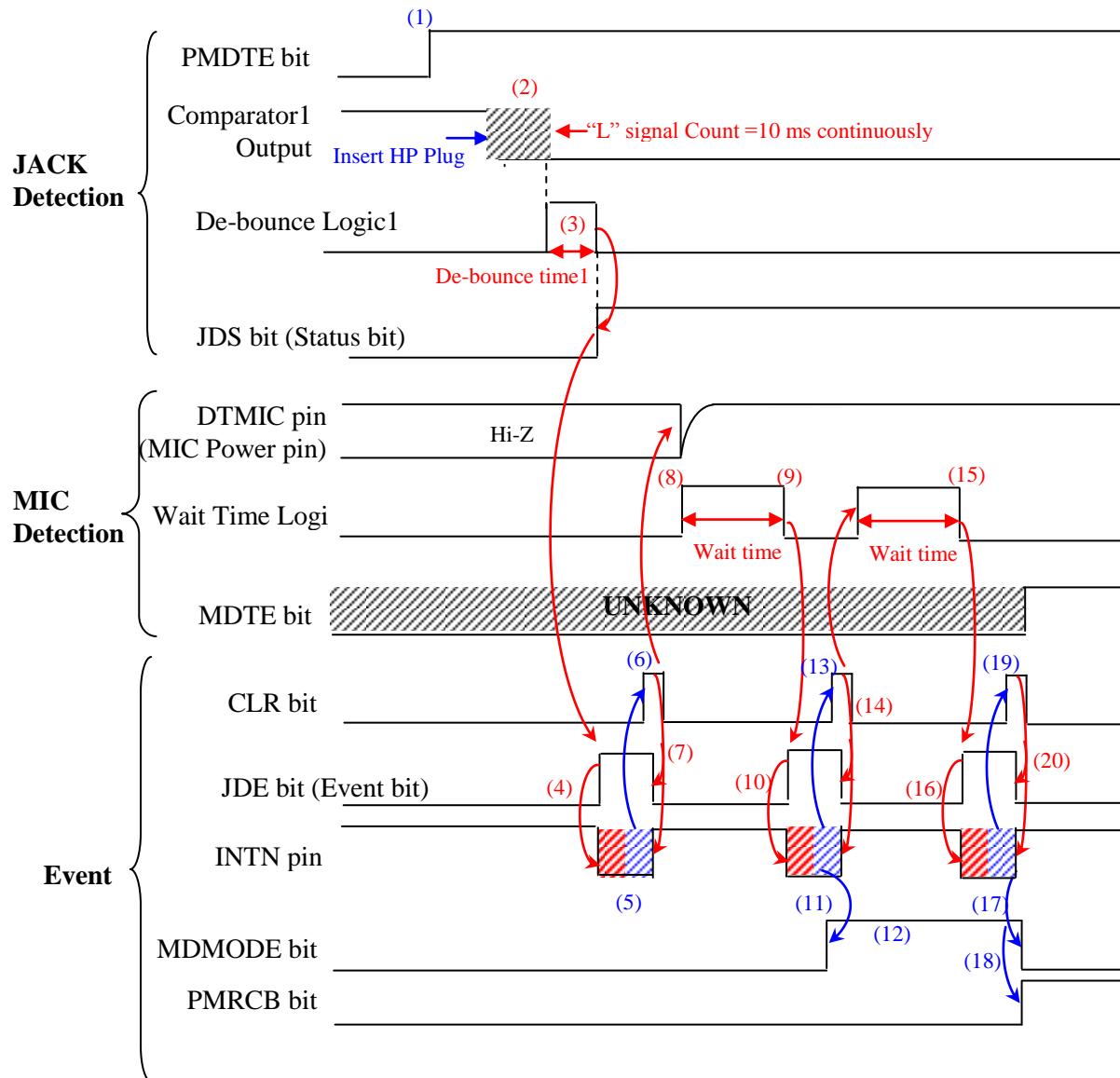


Figure 36. Jack Insertion Timing Chart 1 (DTMIC pin=MIC Level, DTINTN bit = "0")

- (1) When PMDTE bit is changed to “1” by a microcontroller, the jack detection circuit is powered-up. Then SW1 is ON and the HDT pin is pulled up by an internal  $10M\Omega$ (typ.) resistor to AVDD2.
- (2) The internal comparator compares the HDT pin signal to 90% of AVDD1 (reference level) when a jack is inserted. The comparator outputs “L” when the input signal is 90% AVDD1 or higher. The de-bounce timer 1 starts automatically if the comparator output level is “L” for 10ms (typ.).
- (3) The AK4961 sets JDS bit (Status bit) = “1” after the De-bounce Time1 period. And the AK4961 sets JDE bit = “1” by a change of JDS bit status.
- (4) The output of the INTN pin changes to “L” from “H” when JDE bit (Event bit) = “0”  $\rightarrow$  “1” by an internal operation.
- (5) A microcontroller reads the JDE bit and JDS bit to confirm the Jack status.
- (6) A microcontroller writes CLR bit = “1”.
- (7) JDE bit (Event bit) returns to “0” and the INTN pin output returns to “H” after writing CLR bit = “1” by a microcontroller. When the Event completes, CLR bit returns to “0” automatically.
- (8) After MDMODE bit = “0” and CLR bit returns to “0”, the CP1, LDO1 and MPWR2 blocks are automatically powered up. This wait time is set by the Wait Timer (MPWT2-0 bits ([Table 60](#))).
- (9) After the wait time, the output signal of Microphone detection comparator is automatically monitored by the internal counter.
- (10) If the counter detects “L” signal continuously during the wait time, MDTE bit turns to “1”. If not, MDTE bit remains “0”. When MDTE bit is updated internally, JDE bit (Event bit) automatically changes to “1” from “0” if PMRCB bit = “0”.
- (11) A microcontroller monitors a microphone jack existence on the plug by reading JDE bit, JDS bit and MDTE bit.
- (12) When repeating MIC Detection sequence, MDMODE bit is set to “1” by a microcontroller.
- (13) Set CLR bit = “0”  $\rightarrow$  “1” by a microcontroller.
- (14) When CLR bit becomes “1”, the AK4961 sets JDE bit (Event bit) = “1”  $\rightarrow$  “0” and the INTN pin = “L”  $\rightarrow$  “H”. CLR bit automatically returns to “0” after the event is completed. When MDMODE bit = “1”, Wait time Logic (MPWT2-0 bits) automatically restarts by edge trigger of CLR bit = “1”  $\rightarrow$  “0”.
- (15) After the wait time, the output signal of Microphone detection comparator is automatically monitored by the internal counter.
- (16) If the counter detects “L” signal continuously during the wait time, MDTE bit turns to “1”. If not, MDTE bit remains “0”. When MDTE bit is updated internally, JDE bit (Event bit) automatically changes to “1” from “0” if PMRCB bit = “0”.
- (17) A microcontroller monitors a microphone jack existence on the plug by reading JDE bit, JDS bit, and MDTE bit.

(18) If MIC Detection is finished, MDMODE bit sets “1” to “0” by a microcontroller. And, when MDMODE bit = “0” and MDTE bit = “1”, PMRCB bit sets “0” to “1” by a microcontroller. In this case, the AK4961 is in Remote control detection sequence.

\* When MDMODE bit= “1”, the AK4961 is not in Remote control detection sequence unless PMRCB bit is set to “1” even if MDTE bit = “1”.

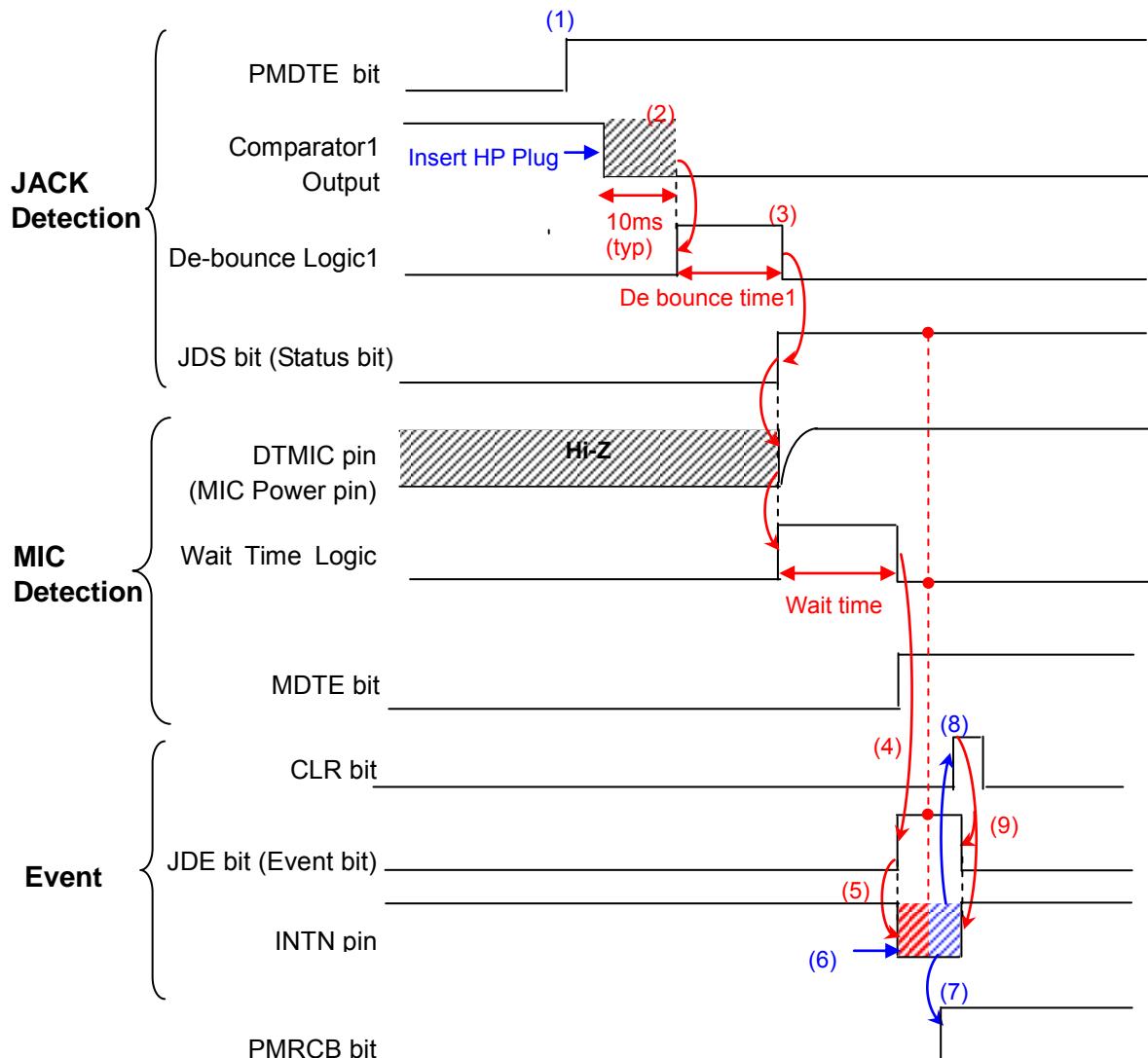
(19) Set CLR bit = “0” → “1” by a microcontroller.

(20) When CLR bit becomes “1”, the AK4961 sets JDE bit (Event bit) = “1” → “0” and the INTN pin = “L” → “H”. CLR bit automatically returns to “0” after the event is completed. When MDMODE bit = “0”, MIC Detection sequence is automatically finished by edge trigger of CLR bit = “1” → “0”.

<when the DTMIC pin = GND without microphone>

When CLR bit becomes “0” from “1”, MPWR2, LDO1 and CP1 in this order and Microphone detection comparator blocks are automatically powered down (if MDMODE = MDTE bits = “0”).

**Jack Insertion Timing Chart 2:**  
**DTMIC pin= Microphone Level, Automatic Mode (MDDIF bit = “1”, DTINTN bit = “0”)**

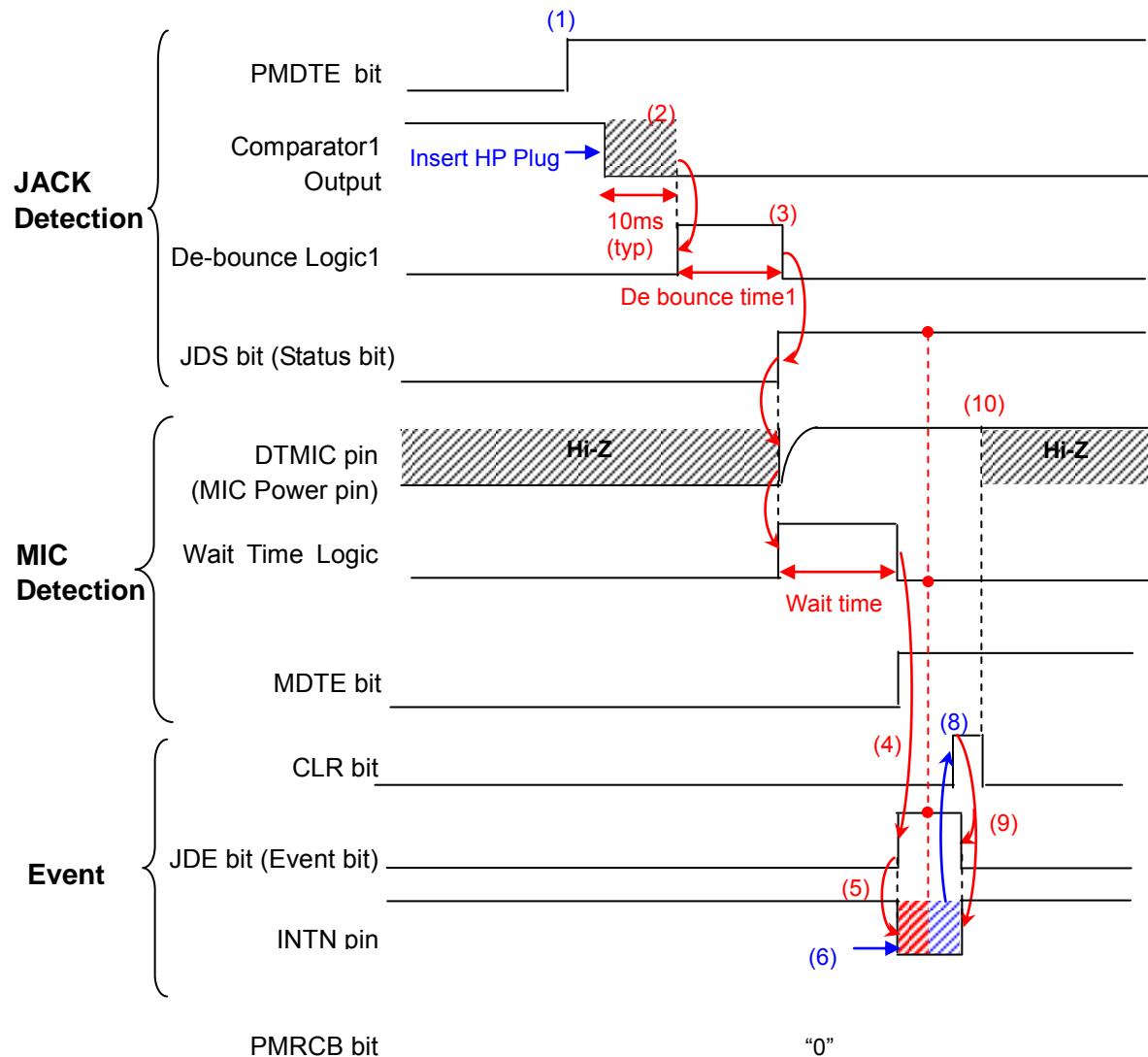


Red: Operated by the AK4961 automatically, Blue: External operation or operated by a microcontroller

Figure 37. Jack Insertion Timing Chart 2  
(Automatic mode, DTMIC pin= Microphone Level, DTINTN bit = “0”)

**Jack Insertion Timing Chart 3:**

**DTMIC pin=GND or Remote control is unused. Microphone Level, Automatic Mode  
(MDDIF bit = “1”, DTINTN bit = “0”)**



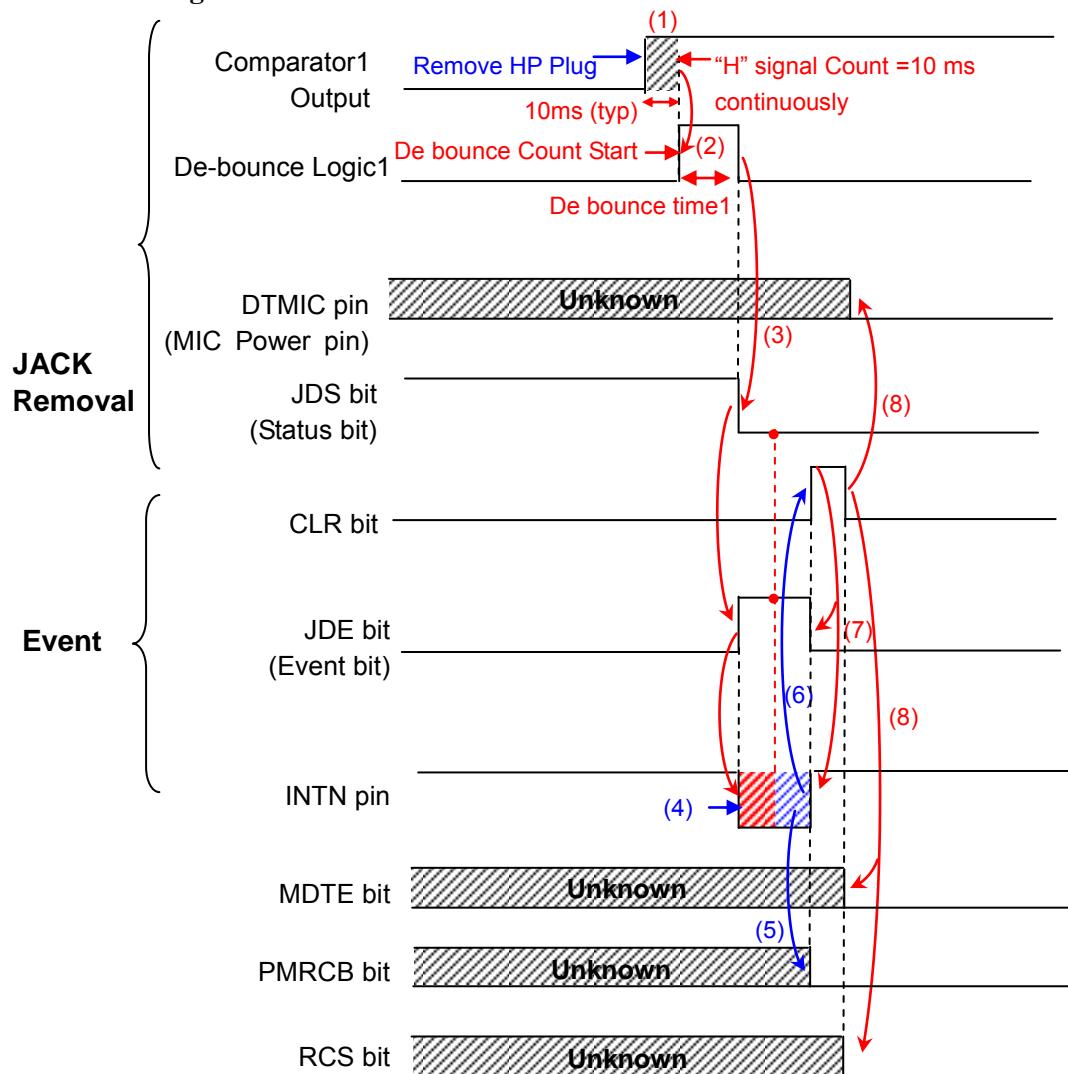
Red: Operated by the AK4961 automatically, Blue: External operation or operated by a microcontroller

Figure 38. Jack Insertion Timing Chart 3  
(Automatic mode, DTMIC pin= GND Level, DTINTN bit = “0”)

- (1) When PMDTE bit is changed to “1” by a microcontroller, the jack detection circuit is powered-up. Then SW1 is ON and HDT pin is pulled-up by an internal  $10M\Omega$ (typ.) resistor to AVDD2.
- (2) The internal comparator compares the HDT pin signal to 90% of AVDD1 (reference level) after a jack is inserted. The comparator outputs “L” when the input signal is 90% AVDD1 or higher. The de-bounce timer 1 starts automatically if the comparator output level is “L” for 10ms (typ.).
- (3) After the De-bounce Time1, the AK4961 sets JDS bit (Status bit) = “1” and CP1, LDO1 and MPWR2 blocks are automatically powered up (when PMMP2 = PMLDO1=PMCP1 bit = “0”).
- (4) Wait until the output voltage of the MPWR2 pin is stabilized. This wait time is set by the Wait Timer (MPWT2-0 bits ([Table 60](#))). After the wait time, the output signal of Microphone detection comparator is automatically monitored by the internal counter. If the counter detects “L” signal continuously during the wait time, MDTE bit turns to “1”. If not, MDTE bit remains “0”. When MDTE bit is updated internally, JDE bit (Event bit) automatically changes to “1” from “0” if PMRCB bit = “0”.  
\* The reference level of the Microphone detection comparator can be set by CMPL bit.
- (5) The INTN pin signal automatically changes to “L” from “H” when JDE bit (Event bit) becomes “0” → “1” by internal operation.
- (6) A microcontroller monitors a microphone jack existence on the plug by reading JDE bit, JDS bit, and MDTE bit.
- (7) A microcontroller sets PMRCB bit to “1” if a microphone is detected, and a microcontroller sets PMRCB bit to “0” if a microphone is not detected terminal.
- (8) Set CLR bit = “0” → “1” by a microcontroller.
- (9) When CLR bit becomes “1”, the AK4961 sets JDE bit (Event bit) = “1” → “0” and the INTN pin = “L” → “H”. CLR bit automatically returns to “0” after the event is completed.
- (10) When CLR bit becomes “0” from “1”, MPWR2, LDO1 CP1 and Microphone detection comparator blocks are automatically powered down (if PMMP2 = PMLDO1 = PMCP1 bits = “0”).

## &lt;Jack Removal&gt;

Jack Removal Timing Chart



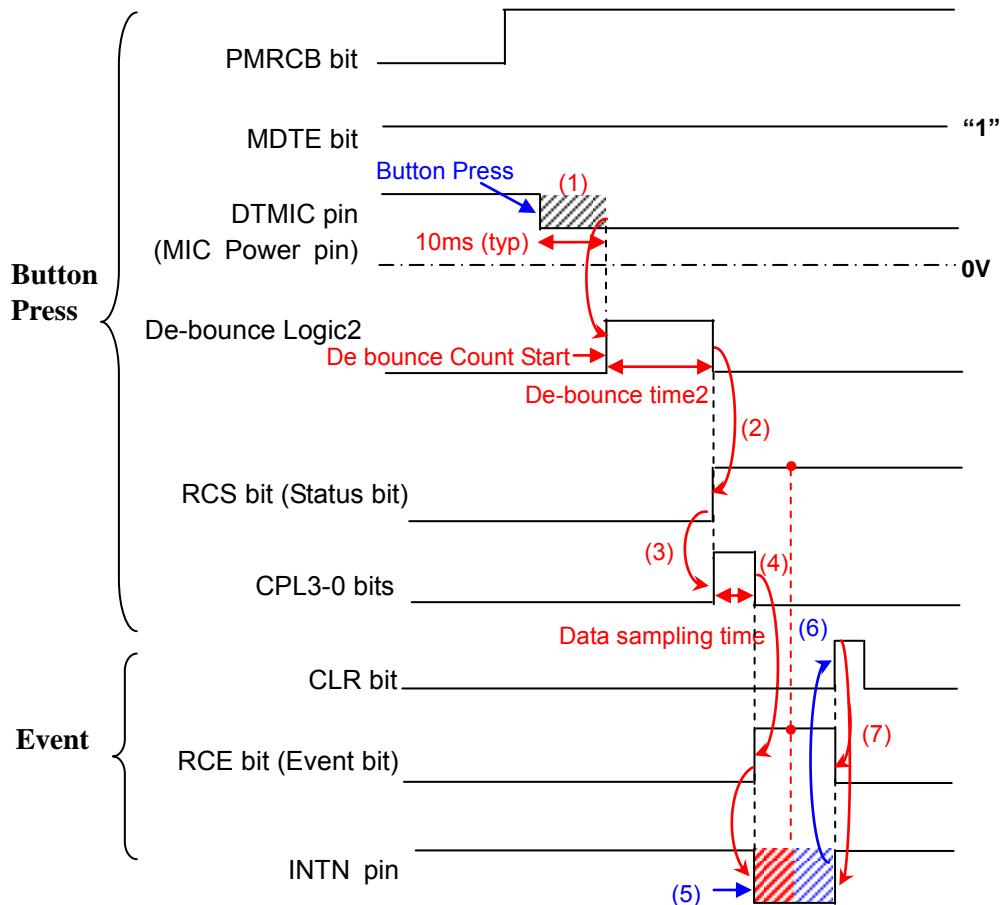
Red: Operated by the AK4961 automatically, Blue: External operation or operated by a microcontroller

Figure 39. Jack Removal Timing Chart

- (1) The HDT and HPL pins are shorted, and the analog output signal of the HPL pin or “L” signal is input to the HDT pin.
- (2) The de-bounce timer 1 starts automatically if “H” level is output for 10ms (typ.).
- (3) The AK4961 sets JDS bit (Status bit) = “0” after the De-bounce Time1 period. At the same time JDE bit becomes “1”, and the INTN pin goes to “L” from “H” by internal operation.
- (4) A microcontroller monitors a microphone jack existence on the plug by reading JDE bit and JDS bit.
- (5) Set PMRCB bit = “0” by a microcontroller.
- (6) Set CLR bit = “1” by a microcontroller.
- (7) When CLR bit becomes “1”, the AK4961 sets JDE bit (Event bit) = “1” → “0” and INTN pin = “L” → “H”. CLR bit returns to “0” automatically after the event is completed.
- (8) When CLR bit becomes “0” from “1”, MPWR2, LDO1 and CP1 blocks are automatically powered down (if PMMP2 = PMLDO1 = PMCP1 bits = “0”). In this case, RCS and MDTE bits are also changed to “0”.

## &lt;Remote Control Detection&gt;

## Button Press Timing Chart

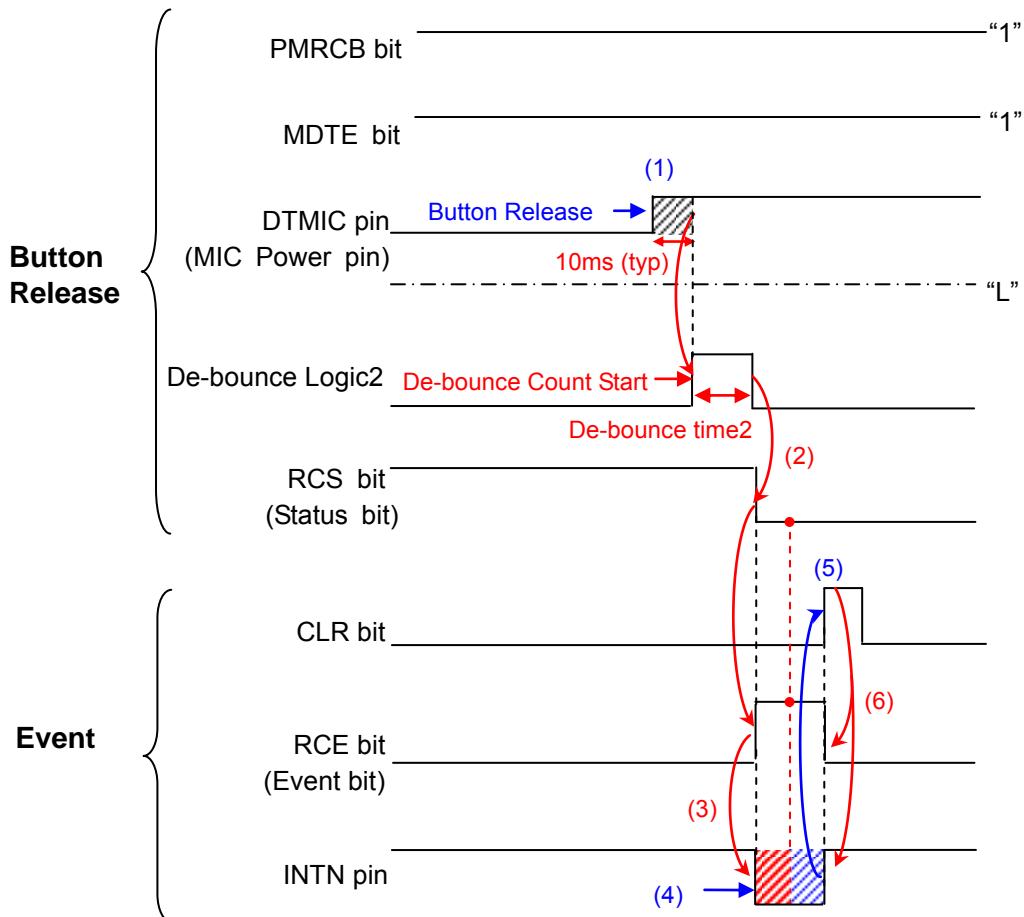


Red: Operated by the AK4961 automatically, Blue: External operation or operated by a microcontroller

Figure 40. Button Press Timing Chart

- (1) When PMRCB bit=“1” and the control button of an external headset is pushed, the voltage of the microphone terminal (DTMIC pin) becomes lower than the reference level of the microphone detection comparator and the microphone detection comparator outputs “L”. De-bounce timer 2 starts automatically if the “L” level output continues for 10ms (typ.). The reference level of the comparator for microphone detection can be set by CMPL bit. ([Table 61](#))
- (2) The AK4961 sets RCS bit (Status bit) = “1” and the comparator operation for remote controller starts automatically after the De-bounce Time 2 period.
- (3) The comparator for remote controller compares the input signal to seven reference levels and the result is automatically stored to CPL[3:0] bits.
- (4) When the data is stored, the AK4961 sets RCE bit (Event bit) = “1” and the INTN pin output becomes “L” from “H”.
- (5) A microcontroller monitors Button Press status by reading RCE, RCS, and CPL[3:0] bits.
- (6) Set CLR bit to “1” by a microcontroller.
- (7) When CLR bit becomes “1”, the AK4961 sets REC bit = “1” → “0” and the INTN pin = “L” → “H”. CLR bit returns to “0” automatically after the event is completed.

## Button Release Timing Chart



Red: Operated by the AK4961 automatically, Blue: External operation or operated by a microcontroller

Figure 41. Button Release Timing Chart

- (1) The voltage of the DTMIC pin rises by releasing the Remote Control Button of an external headset from pushed state when PMRCB bit = "1". The microphone terminal (DTMIC pin) voltage becomes higher than the reference level of a microphone detection comparator and the microphone detection comparator outputs "H". De-bounce Timer 2 starts automatically if the "H" level output continues for 10ms (typ.). The reference level of the Microphone detection comparator can be set by CMPL bit. (Table 61)
- (2) After the De-bounce time 2 period, RCS bit (Status bit) becomes "1" from "0" and RCE bit (Event bit) becomes "1" from "0" by internal operation.
- (3) The INTN pin output automatically changes to "L" from "H" when RCE bit (Event bit) becomes "1" from "0".
- (4) A microcontroller detects Button Release event by reading RCE bit = "1" and RCS bit = "0".
- (5) Set CLR bit to "1" by a microcontroller.
- (6) When CLR bit becomes "1", the AK4961 sets RCE bit (Event bit) = "1" → "0" and the INTN pin = "L" → "H". CLR bit returns to "0" automatically after the event is completed.

## ■ Voice Wakeup Function

The AK4961 has a Voice Wakeup function. The system diagram of the function is shown in [Figure 42](#). This function sends a wakeup flag (GPO) and input signal from microphones ( $I^2S$  or SLIMbus I/F) in response to a microphone input to an external ACPU by using MCLK.

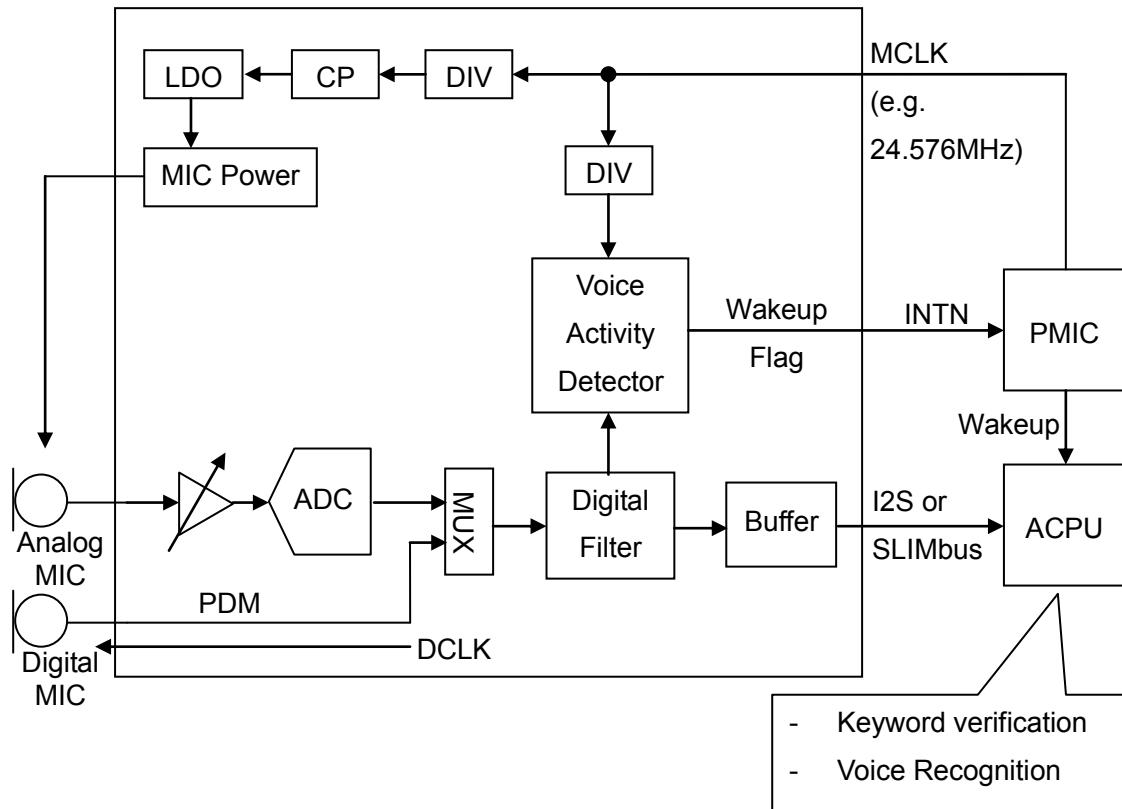


Figure 42. Voice Wakeup System Block Diagram

\* Refer to the application note for details.

## ■ Asynchronous Sampling Rate Converter (SRCA/B/C/D)

The AK4961 has four stereo asynchronous SRCs. The SRCs support an 8kHz to 192kHz audio source (FSI) and an 8kHz to 192kHz sampling rate output (FSO). Available sample rate ratio (FSO/FSI) is 0167 to 6.0. When operating the SRCA, SRCB, SRCC or/and SRCD, SRCCLK[1:0] bits should be set to “01”, “10” or “11”. When the SRCA/B/C/D is powered-up at the same time, the sum of FSI is less than [Table 72](#).

When using multiple SRCs with the same sync domain of input/output, there is a possibility the group delay of all SRCs is not exactly the same (1/fs shifted). To match SRCs group delay, PMSRCx bits should be set to “1” at the same time (In this case, the priority is in descending order. SRCD has the highest priority. For example, if SRCA and SRCC are powered up together, the group delay of SRCA matches that of SRCC). However, the group delay does not match by just switching SRC power-down and up. PMSRCx bit must be set to “1” after setting SWRSTN bit to “1” → “0” → “1” while all SRCs are powered down.

SRCCLK[1:0] bits	FSI max(Sum of SRCA,B,C,D)				
	DSPMCLK(MHz)				
	122.8800	112.8960	110.5920	101.6064	
00	N/A				
01	240.0kHz	220.5kHz	216.0kHz	198.5kHz	(default)
10	160.0kHz	147.0kHz	144.0kHz	132.3kHz	
11	120.0kHz	110.3kHz	108.0kHz	99.2kHz	

Table 72. SRCMCLK Setting (N/A: Not available)

### 1. Up Sampling ( $0.98 \leq \text{FSO}/\text{FSI} \leq 6.00$ )

Example of supported sampling rate is as follows.

FSO	FSI	FSO/FSI	Passband	Stopband	S.A.(dB)
192kHz	48kHz	4.00	22.00kHz	26.00kHz	-102.2
48kHz	48kHz	1.00	22.00kHz	26.00kHz	-102.2
48kHz	44.1kHz	1.09	20.21kHz	23.89kHz	-102.2
48kHz	32kHz	1.50	14.67kHz	17.33kHz	-102.2
48kHz	24kHz	2.00	11.00kHz	13.00kHz	-102.2
48kHz	16kHz	3.00	7.33kHz	8.67kHz	-102.2
48kHz	12kHz	4.00	5.50kHz	6.50kHz	-102.2
48kHz	8kHz	6.00	3.67kHz	4.33kHz	-102.2
192kHz	44.1kHz	4.35	20.21kHz	23.89kHz	-102.2
44.1kHz	44.1kHz	1.00	20.21kHz	23.89kHz	-102.2
44.1kHz	32kHz	1.38	14.67kHz	17.33kHz	-102.2
44.1kHz	24kHz	1.84	11.00kHz	13.00kHz	-102.2
44.1kHz	16kHz	2.76	7.33kHz	8.67kHz	-102.2
44.1kHz	12kHz	3.68	5.50kHz	6.50kHz	-102.2
44.1kHz	8kHz	5.51	3.67kHz	4.33kHz	-102.2
16kHz	16kHz	1.00	7.33kHz	8.67kHz	-102.2
16kHz	8kHz	2.00	3.67kHz	4.33kHz	-102.2
8kHz	8kHz	1.00	3.67kHz	4.33kHz	-102.2

Table 73. Example of Up-Sampling

2. Down-Sampling ( $0.167 \leq \text{FSO}/\text{FSI} < 0.99$ )

6 values of ratio in sampling rate (FSO/FSI) are supported.

FSO	FSI	FSO/FSI	Passband	Stopband	S.A.(dB)
44.1kHz	48kHz	0.919	20.00kHz	24.10kHz	-121.4
48kHz	88.2kHz	0.544	19.25kHz	26.23kHz	-100.2
48kHz	96kHz	0.50	20.90kHz	27.00kHz	-95.2
44.1kHz	88.2kHz	0.50	19.20kHz	24.81kHz	-95.2
16kHz	32kHz	0.50	6.97kHz	9.00kHz	-95.2
8kHz	16kHz	0.50	3.48kHz	4.50kHz	-95.2
44.1kHz	96kHz	0.459	18.70kHz	25.00kHz	-96.6
16kHz	44.1kHz	0.363	5.79kHz	7.95kHz	-96.0
16kHz	48kHz	0.333	6.30kHz	8.65kHz	-96.0
48kHz	192kHz	0.25	25.19kHz	34.60kHz	-96.0
44.1kHz	192kHz	0.229	25.19kHz	34.60kHz	-96.0
8kHz	48kHz	0.167	3.16kHz	4.66kHz	-90.0
8kHz	44.1kHz	0.181	2.90kHz	4.28kHz	-90.0

Table 74. Example of Down-Sampling

## ■ Soft Mute (SRCA/B/C/D)

Soft mute operation is performed in the SRC block. This function can be independently operated in SRCA, SRCB, SRCC and SRCD.

### 1. Manual Mode

When SMUTEx bit (x=A, B, C, D) is changed to “1”, the output signal is attenuated to  $-\infty$  (“0”) during 1024/FSO cycle. When the SMUTEx bit is returned to “0”, the mute is cancelled and the output attenuation level gradually changes to 0dB during 1024/FSO cycle. If the soft mute is cancelled within 1024/FSO, the attenuation is discontinued and the attenuation level returns to 0dB by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

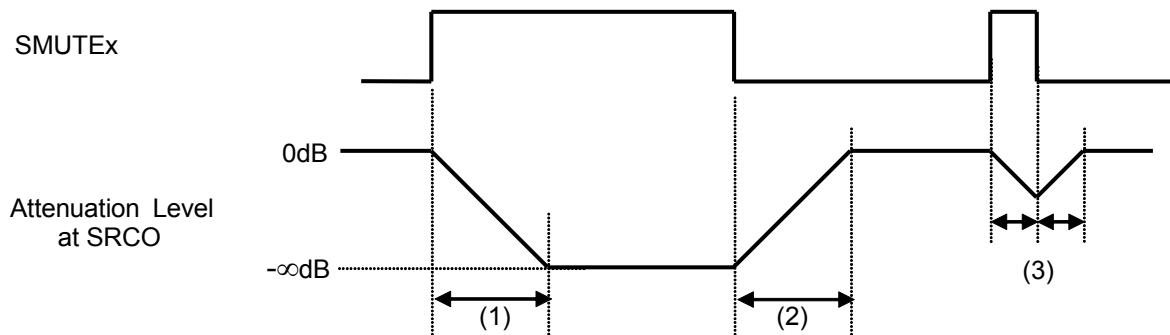


Figure 43. Soft Mute (Manual Mode)

- (1) The output signal is attenuated until  $-\infty$  (“0”) in 1024/FSO cycle.
- (2) The output signal returns to 0dB in 1024/FSO cycle.
- (3) If the soft mute is cancelled within the 1024/FSO cycle, the attenuation is discontinued and the attenuation level returns to 0dB in the same cycle.

## 2. Semi-Auto Mode

The AK4961 enters Semi-Auto mode by setting SAUTOx bit ( $x = A, B, C, D$ ) to “1”. In this mode, the soft mute is cancelled automatically in 20.5ms (longer time between  $128/f_{si}$  and  $\text{Max}(8/f_{si}, 8f_{so}) + 154/f_{so}$  cycles) after setting PMSRCx bit to “1” and the AK4961 will be able to output the data. When power-down state is released (PMSRCx bit = “0” → “1”), the soft mute function is ON if the SMUTE x ( $x=A, B, C, D$ ) bit is “1”.

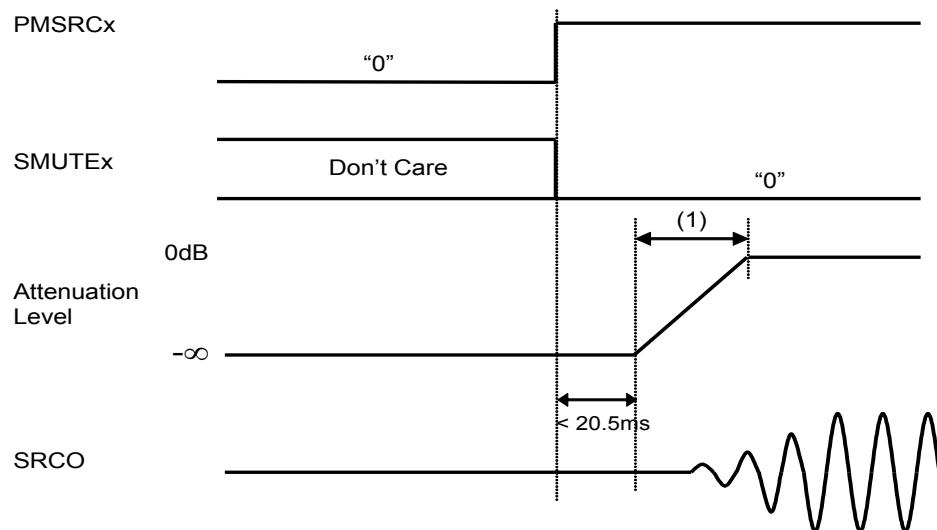


Figure 44. Soft Mute Semi-Auto Mode

(1) The attenuation level returns to 0dB in 1024/f<sub>so</sub> cycle.

## ■ SRC System Reset (SRCA/B/C/D)

SRC is reset by setting PMSRCx bit ( $x=A, B, C, D$ ) to “0”, and the digital filter of the SRC is reset at the same time. The SRC output is “L” when PMSRCx bit = “0”. A data output becomes available in 20.5ms (longer time between 128/fsi and Max(8/fsi, 8fso) + 154/fso cycles) and until then the AK4961 outputs “L”. SRC settings should be finished before the PMSRC bit is set to “1”.

There is a possibility that the SRCA/B/C/D is not powered-up when PMSRCx bit is set to “1”. In order to operate the SRC properly, use one of the following methods.

### 1. In case of using SWRSTN bit

Each SRC can be powered-up just one-time by setting SWRSTN bit to “1”. Note that SRAM (downloaded program) are reset by setting SWRSTN bit to “0”.

#### <Power-up Sequence>

- (1) SWRSTN bit = “0” → “1”: Release reset state of digital blocks (SRC, DSP, SRAM)
- (2) PMSRCx bit = “0” → “1”: SRC Power-up

#### <Power-down Sequence>

- (1) PMSRCx bit = “1” → “0”
- (2) SWRSTN bit = “1” → “0”: Reset Digital blocks (SRC, DSP, SRAM)

### 2. In case of controlling PMSRCx by reading SRC Status

- (1) PMSRCx bit = “0” → “1”
- (2) Wait (4/fsi)
- (3) Read “SRCSTx bit” ( $x = A, B, C, D$ )
- (4) SRCSTx bit = “0”: SRC is in normal operation

SRCSTx bit = “1”: SRC is in error status. In this case, PMSRCx bit should be set to “0”, and then set back PMSRCx bit to “1”. (PMSRCx bit = “1” → “0” → “1”; Repeat this until SRCSTx bit becomes “0”).

#### Case 1

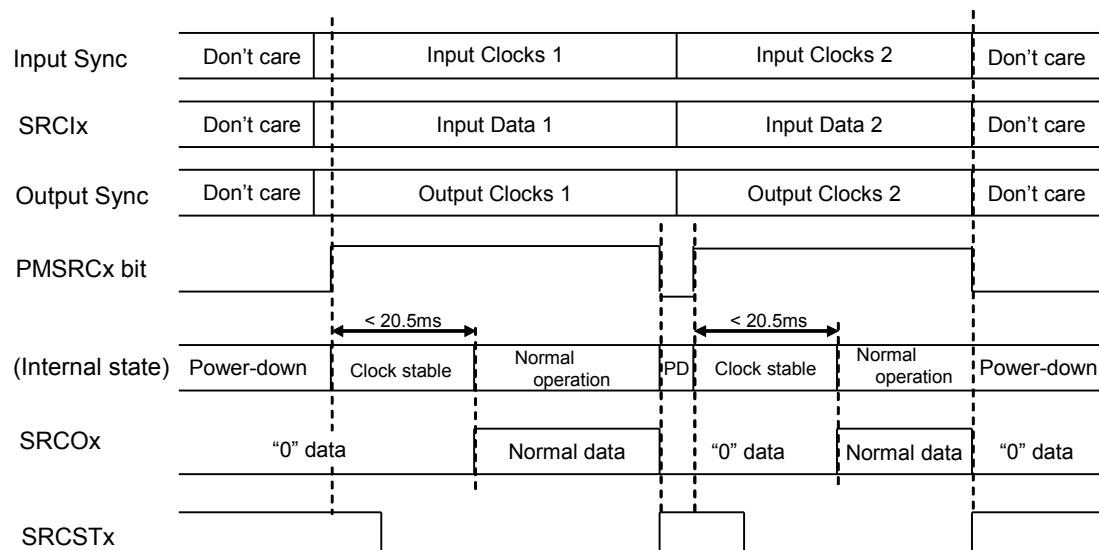


Figure 45. SRC System Reset 1

## Case 2

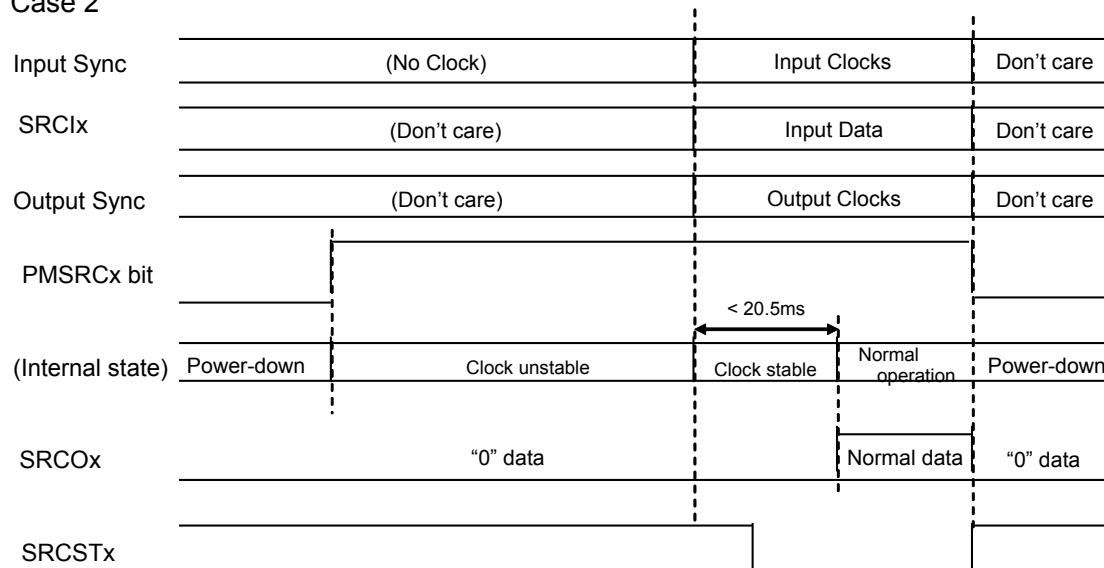


Figure 46. SRC System Reset 2

## ■ SRC Clock (SRCA/B/C/D)

### 1. Internal Reset for Clock Changing

The AK4961 is internally reset when input or output clock of SRC is stopped. In this case, the AK4961 outputs a normal data in 20.5ms (longer time between 128/fsi and Max(8/fsi, 8/fs0) + 154/fs0 cycles) after restarting the clock.

### 2. Clock Change Sequence

[Figure 47](#) shows a clock change sequence for SRC.

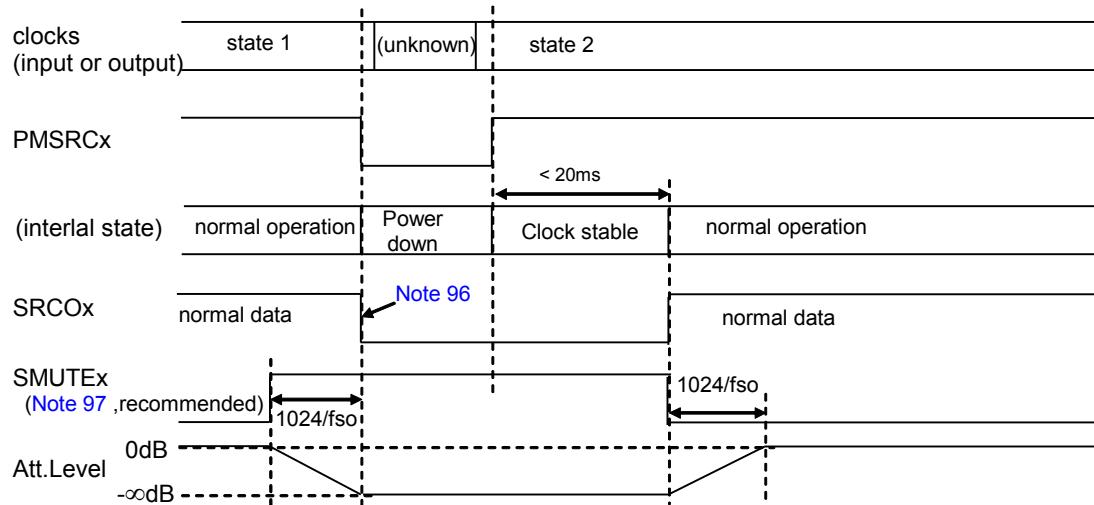


Figure 47. ASRC Clock Change Sequence

Note 96. The data on SRCOx may cause a clicking noise. To prevent the noise, set “0” to the input data of SRC before PMSRCx ( $x=A, B, C, D$ ) bit is set to “1”. It makes the data on SRCOx remain as “0”.

Note 97. This clicking noise (Note 96) can also be removed by setting SMUTEx bit to “1” even if the input data is not “0”.

## ■ Asynchronous Sampling Rate Converter (SRCE)

The AK4961 has high performance stereo asynchronous SRC in front of DAC1. The SRC supports an 8kHz to 192kHz audio source (FSI) and an 8kHz to 192kHz sampling rate output (FSO). Available sample rate ratio (FSO/FSI) is 0.167 to 6.0. Power management is controlled by SRCE bit.

### 1. Up-Sampling ( $0.98 \leq FSO/FSI \leq 6.00$ )

Example of supported sampling rate is as follows. The values of Passband, Stopband and S.A.(Stopband Attenuation) in [Table 75](#) are for Sharp Roll-Off filter.

FSO	FSI	FSO/FSI	Passband	Stopband	S.A.(dB)
192kHz	48kHz	4.00	22.00kHz	26.00kHz	-121.2
48kHz	48kHz	1.00	22.00kHz	26.00kHz	-121.2
48kHz	44.1kHz	1.09	20.21kHz	23.89kHz	-121.2
48kHz	32kHz	1.50	14.67kHz	17.33kHz	-121.2
48kHz	24kHz	2.00	11.00kHz	13.00kHz	-121.2
48kHz	16kHz	3.00	7.33kHz	8.67kHz	-121.2
48kHz	12kHz	4.00	5.50kHz	6.50kHz	-121.2
48kHz	8kHz	6.00	3.67kHz	4.33kHz	-121.2
192kHz	44.1kHz	4.35	20.21kHz	23.89kHz	-121.2
44.1kHz	44.1kHz	1.00	20.21kHz	23.89kHz	-121.2
44.1kHz	32kHz	1.38	14.67kHz	17.33kHz	-121.2
44.1kHz	24kHz	1.84	11.00kHz	13.00kHz	-121.2
44.1kHz	16kHz	2.76	7.33kHz	8.67kHz	-121.2
44.1kHz	12kHz	3.68	5.50kHz	6.50kHz	-121.2
44.1kHz	8kHz	5.51	3.67kHz	4.33kHz	-121.2
16kHz	16kHz	1.00	7.33kHz	8.67kHz	-121.2
16kHz	8kHz	2.00	3.67kHz	4.33kHz	-121.2
8kHz	8kHz	1.00	3.67kHz	4.33kHz	-121.2

Table 75. Example of Up-Sampling

### 2. Down-Sampling ( $0.167 \leq FSO/FSI < 0.99$ )

6 values of ratio in sampling rate (FSO/FSI) are supported.

FSO	FSI	FSO/FSI	Passband	Stopband	S.A.(dB)
44.1kHz	48kHz	0.919	20.00kHz	24.10kHz	-121.4
48kHz	88.2kHz	0.544	19.25kHz	26.23kHz	-114.6
48kHz	96kHz	0.50	20.90kHz	27.00kHz	-100.2
44.1kHz	88.2kHz	0.50	19.20kHz	24.81kHz	-100.2
16kHz	32kHz	0.50	6.97kHz	9.00kHz	-100.2
8kHz	16kHz	0.50	3.48kHz	4.50kHz	-100.2
44.1kHz	96kHz	0.459	18.70kHz	25.00kHz	-103.3
16kHz	44.1kHz	0.363	4.40kHz	6.94kHz	-104.0
16kHz	48kHz	0.333	4.40kHz	7.55kHz	-104.0
48kHz	192kHz	0.25	17.61kHz	30.20kHz	-104.0
44.1kHz	192kHz	0.229	17.61kHz	30.20kHz	-104.0
8kHz	48kHz	0.167	3.96kHz	7.06kHz	-103.3
8kHz	44.1kHz	0.181	3.64kHz	6.49kHz	-103.3

Table 76. Example of Down-Sampling

SRCE input clock (CODECMCLK) is fixed to 256fs (Note 98). XCKSEL bit selects output clock of SRC between CODECMCLK and X'tal. The charge pump clock is selected by XCKCPSEL bit. The SRC has digital filters that provide four kinds of sound color and these filters can be selected by SRCESD and SRCESL bits. These digital filters in DAC block can be bypassed by setting SRCO8FS bit = DFTHR<sub>x</sub> bit = “1” and 8fs rate data can be directly input to the DAC. With this bypass function, high quality sound can be achieved without filtering the sound source twice.

PMSRCE bit	SRCE Status	
0	Power Down	(default)
1	Power Up	

Table 77. SRCE Power Management

SRCO8FS bit	SRCE Output Mode	
0	1fs	(default)
1	8fs	

Table 78. SRCE Output Mode Setting

SRCESD bit	SRCESL bit	SRCE Digital Filtered Mode	
0	0	Sharp Roll-Off Filter	(default)
0	1	Slow Roll-Off Filter	
1	0	Short Delay Sharp Roll-Off Filter	
1	1	Short Delay Slow Roll-Off Filter	

Table 79. SRCE Digital Filter Setting

XCKSEL bit	SRCE/DAC Clock Mode	
0	CODECMCLK	(default)
1	X'tal	

Table 80. SRCE/DAC Clock Mode Setting

XCKCPSEL bit	Charge Pump Clock Mode	
0	CODECMCLK	(default)
1	X'tal	

Table 81. Charge Pump Clock Mode Setting

DIV bit	Divide by	
0	1	(default)
1	2.5	

Note 98. Set clock source frequency of CODECMCLK to 256fs,MDIV2[7:0]bits = “4”(divided by 5) and DIV bit = “1” to generate a256fs clock in quad speed mode(fs≥128kHz)

Table 82. CODECMCLK Divider

## &lt;Jitter Cleaner&gt;

The sound quality and characteristics may degrade if a clock with large jitter is input to the DAC from the host processor. The AK4961 maximizes DAC performance and the sound quality by the internal SRC with an external low jitter crystal oscillator. When the AK4961 is operated by a clock from the external crystal oscillator, the master clock is set by CM2[1:0] bits and the sampling frequency is set by FS2[4:0] bits.

**■ SRCE Dither**

The SRCE block has a dither circuit. It adds a dither to the second least bit by setting DITHERE bit to “1”.

DITHERE bit	Dither
0	OFF
1	ON

(default)

Table 83. SRCE Dither Setting

## ■ SRCE Selector

The input data to SRCE via Audio Sink Port for DAC1 and DAC2 is controlled by SELSRCIN bit. The input data to DAC1 (32-bit) and DAC2 (24-bit) are selected by SELDA1IN bit and SELDA2IN bit, respectively. The SRCE can be bypassed by setting SELDA1IN and SELDA2IN bits.

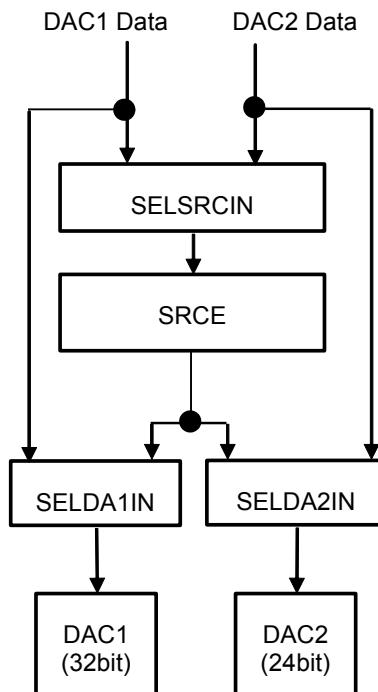


Figure 48. Input Selector for SRCE/DAC1/DAC2

SELSRCIN bit	Data
0	DAC1 (default)
1	DAC2

Table 84. SRCE Input Data Setting

SELD A1IN bit	SELD A2IN bit	SELSRCIN bit	DAC1 (32bit)	DAC2 (24bit)	
0	0	0/1	Bypass	Bypass	(default)
1	1	0	SRC (DAC1 Data)	SRC (DAC1 Data)	
1	1	1	SRC (DAC2 Data)	SRC (DAC2 Data)	
1	0	0	SRC (DAC1 Data)	Bypass	
0	1	1	Bypass	SRC (DAC2 Data)	

Table 85. SRCE Path Setting

## ■ Soft Mute (SRCE)

Soft mute operation is performed in the SRCE block

### 1. Manual Mode

When SMUTEE bit is changed to “1”, the output signal is attenuated to  $-\infty$  (“0”) during 1024/FSO cycle. When the SMUTEE bit is returned to “0”, the mute is cancelled and the output attenuation level gradually changes to 0dB during 1024/FSO cycle (@ SMT1-0 bits = “00”). If the soft mute is cancelled within 1024/FSO(@ SMT1-0 bits = “00”), the attenuation is discontinued and the attenuation level returns to 0dB by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

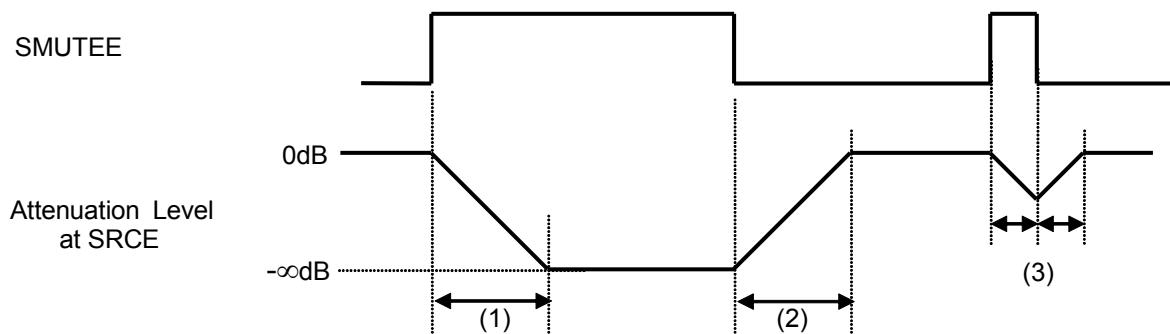


Figure 49. Soft Mute (Manual Mode)

- (1) SMUTEE bit = “0” → “1”: The output signal is attenuated until  $-\infty$  (“0”) in 1024/FSO cycle (@ SMT1-0 bits = “00”).
- (2) SMUTEE bit = “1” → “0”: The output signal returns to 0dB in 1024/FSO cycle (@ SMT1-0 bits = “00”).
- (3) If the soft mute is cancelled within the 1024/FSO cycle (@ SMT1-0 bits = “00”), the attenuation is discontinued and the attenuation level returns to 0dB by the same cycle.

SMT1 bit	SMT0 bit	Period	FSO=48kHz	FSO=96kHz	FSO=192kHz
0	0	1024/FSO	21.3ms	10.7ms	5.3ms
0	1	2048/FSO	42.7ms	21.3ms	10.7ms
1	0	4096/FSO	85.3ms	42.7ms	21.3ms
1	1	8192/FSO	170.7ms	85.3ms	42.7ms

(default)

Table 86. Soft Mute Cycle Setting

## 2. Semi-Auto Mode

The AK4961 enters Semi-Auto mode by setting SAUTOE bit to “1”. In this mode, the soft mute is cancelled automatically in 4410/fso @ DFTHR1 = SRCO8FS bits = “0” (551.25/fso @ DFTHR1 = SRCO8FS bits = “1”) after setting PMSRCE bit to “1” and the AK4961 will be able to output the data. When power-down state is released (PMSRCE bit = “0” → “1”), the soft mute function is ON if the SMUTEE bit is “1”.

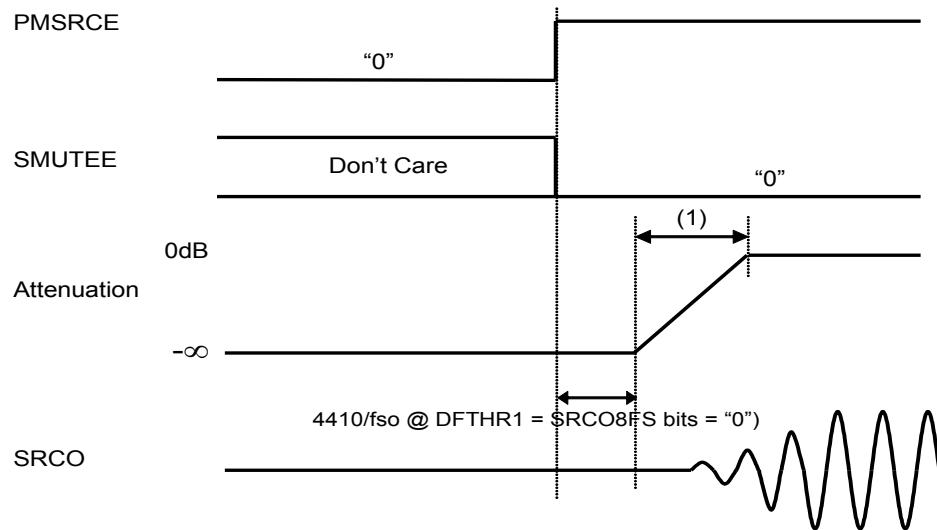


Figure 50. Soft Mute (Semi-Auto Mode)

- (1) The attenuation level returns to 0dB in 1024/fso cycle (@ SMT1-0 bits = “00”).

## ■ SRC System Reset (SRCE)

SRCE is reset by setting PMSRCE bit to “0”, and the digital filter of the SRCE is reset at the same time. The SRCE output is “L” when PMSRCE bit = “0”. A data output becomes available in 20ms (156/fs0 when input/output clocks is stable and PMSRCE bit = “1”) and until then the AK4961 outputs “L”. SRCE settings should be finished before the PMSRCE bit is set to “1”.

### Case 1

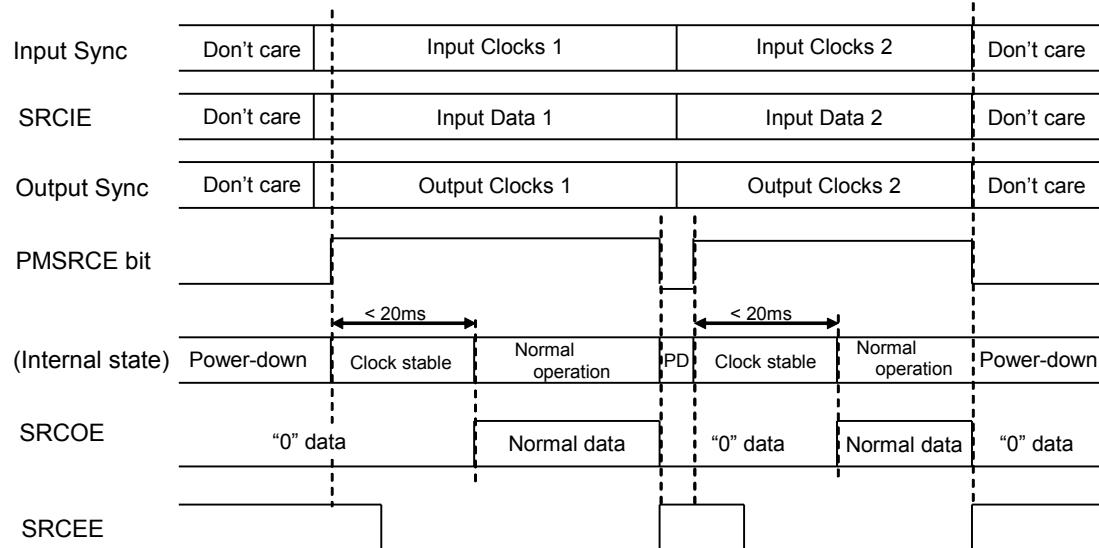


Figure 51. SRCE System Reset 1

### Case 2

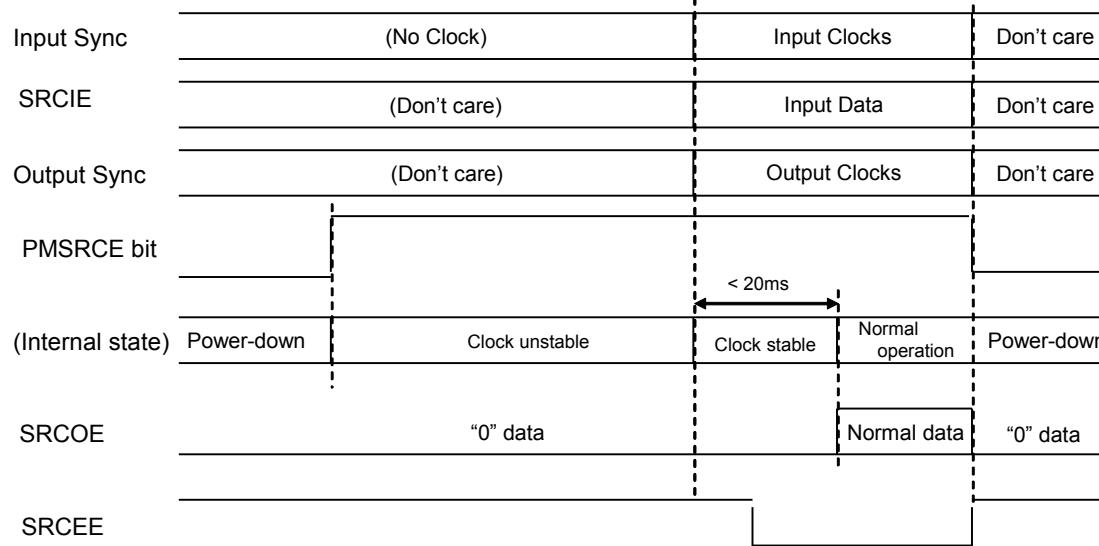


Figure 52. SRCE System Reset 2

## ■ SRC Clock (SRCE)

Figure 53 shows a clock change sequence to SRCE. When PMSRCE bit is set to “1” after the input and output clocks are changed and become stable, SCRE is in normal operation within 20ms (Max. 156/fso).

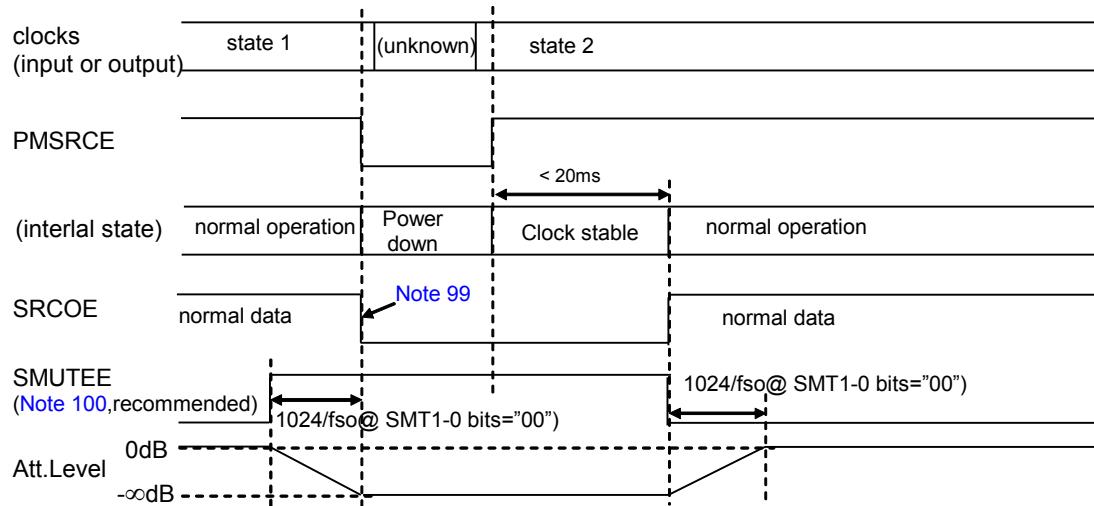


Figure 53. SRCE Clock Change Sequence

Note 99. The data on SRCOE may cause a clicking noise. To prevent the noise, set “0” to the input data of ASRCE before PMSRCE bit is set to “1”. It makes the data on SRCOE remain as “0”.

Note 100. This clicking noise (Note 99) can also be removed by setting SMUTEE bit to “1” even if the input data is not “0”.

**■ DSP Features****[DSP]**

- Data Length: 32 bits
- Machine Cycle: 122.880MHz / 112.896MHz / 110.592MHz / 101.6064MHz
- Step:
  - fs=8kHz : max. 15,360 Steps
  - fs=16kHz : max. 7,680 Steps
  - fs=48kHz: max. 2,560 Steps
- Multiplier: 24 x 24→48-bits (Double precision available)
- Divider: 20 / 20→20-bits (Floating Point Normalizing Function)
- ALU:
  - 52-bit arithmetic operation (with 4-bit overflow margin)
  - 20-bit arithmetic and logic operation
- Shift: Multiple DBUS±15-bits Shift with indirect shifting function
- Program RAM(PRAM): 6144word x 36 bits
- Coefficient RAM(CRAM): 3072word x 20 bits
- Data RAM(DRAM): 2048word x 24 bits (Variable Bank Size)
- Offset Register(OFREG): 32word x 15 bits
- Delay RAM(DLRAM): 20480word x 24 bits (Variable Bank Size)
- Register:
  - 44-bit x 4(ACC) [for ALU]
  - 20.4-bit x 12(TMP) [DBUS connection]
  - 20.4-bit x 6steps Stack (PTMP) [DBUS connection]
- Accelerator

## ■ DSP Block Diagram

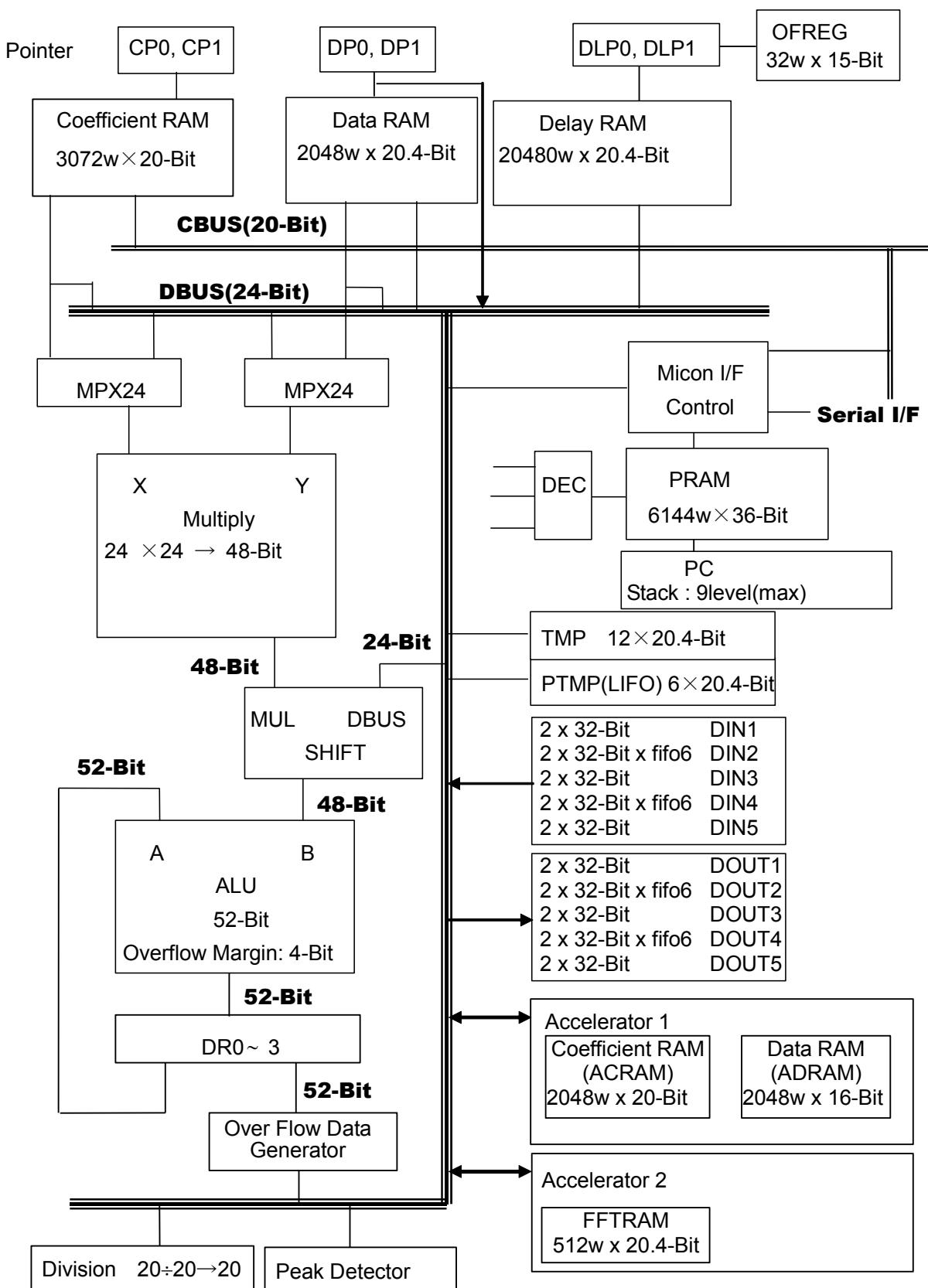


Figure 54. DSP Block Diagram

## ■ System Clock

Name	From	Description
SBCLK	Pin Input	Input clock for SLIMbus interface The dividing ratio of the clock may change during the operation.
SCLK	Pin Input	SPI Interface Input Clock
SCL	Pin Input	I <sup>2</sup> C Interface input Clock
MCKI	Pin Input	Codec Master Clock PLL Reference Clock
XTI	Pin Input	Clock for SRCE and CODEC
MCKO	Internal	Output a synchronized CLK for an external device.
CODECMCLK	Internal	MCLK clock for CODEC
PLLCLK1	Internal	Clock for DSP operation
PLLCLK2	Internal	Clock for DSP operation. Clock frequency different from PLLCLK1 are output.
DSPMCLK	Internal	Main Clock for Digital Block Operation
dport-clock[x]	Internal	256 x “Presence Rate of SLIMbus IP Output Data Port”
SYNCx BCLKx (x=1,2,3,4)	Pin Input/ Output	Input externally in slave mode. It is generated internally in master mode.
MSYNCx MBCLKx (x=1,2,3,4,5)	Internal	A divided clock from PLLCLKx or MCKx for master mode operation.
SDSYNCx SDBCLKx (x=1,2,3,4,5,6,7)	Internal	SYNCs and BCLKs for Sync Domain

Table 87. System Clock

## ■ Clock Source Address

Each clock source has a clock source address as shown below.

Clock Source Address [4:0] bits	Clock Source	
0x00	Tie Low	(default)
0x01	PLLCLK1	
0x02	PLLCLK2	
0x03	N/A(TieLow)	
0x04	MCKI1(pin)	
0x05	XTI(pin)	
0x06	SBCLK(pin)	
0x07	N/A(TieLow)	
0x08	BCLK1(pin)	
0x09	BCLK2(pin)	
0x0A	BCLK3(pin)	
0x0B	BCLK4(pin)	
0x0C	Reserved	
0x0D	Reserved	
0x0E	Reserved	
0x0F	SYNC1(pin)	
0x10	SYNC2(pin)	
0x11	SYNC3(pin)	
0x12	SYNC4(pin)	
0x13	Reserved	
0x14	Reserved	
0x15	Reserved	
0x16	dport-clock0	
0x17	dport-clock1	
0x18	dport-clock2	
0x19	dport-clock3	
0x1A	dport-clock4	
0x1B	dport-clock5	
0x1C	dport-clock6	
0x1D	dport-clock7	
0x1E	dport-clock8	
0x1F	dport-clock9	

Table 88. Clock Source Address

## ■ PLL

The AK4961 has two PLLs (PLL1, PLL2). It generates the following clock by connecting PLL1 and PLL2 in series.

### 1. PLL1

The PLL1 generates PLLCLK1 which is used as a DSP operation clock (DSPMCLK). The output frequency will be the one of those shown in the table below.

	48kHz base rate	44.1kHz base rate
2560/fs	122.88MHz	112.896MHz
2304/fs	110.592MHz	101.6064MHz

Table 89. PLL1 Output

### 2. PLL2

The PLL1 and PLL2 are connected in series so that PLLCLK2 frequency is as shown in [Table 90](#).

PLLCLK1	PLL2 factor	PLLCLK2
122.88MHz	x 147/160	112.896MHz
112.896MHz	x 160/147	122.88MHz
110.592MHz	x 147/160	101.6064MHz
101.6064MHz	x 160/147	110.592MHz

Table 90. PLL2 Output

### 3. Connection of PLL1/2

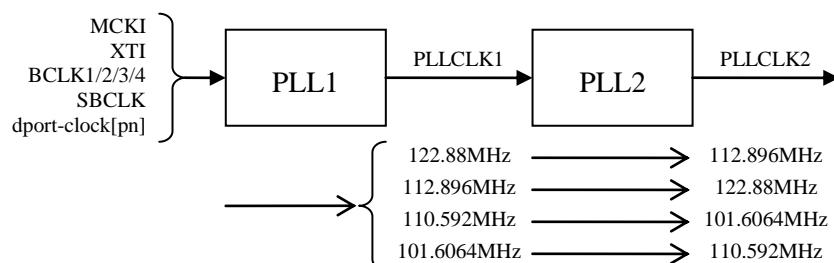


Figure 55. Example of PLL x 2

### 4. Internal Block Diagram of Single PLL

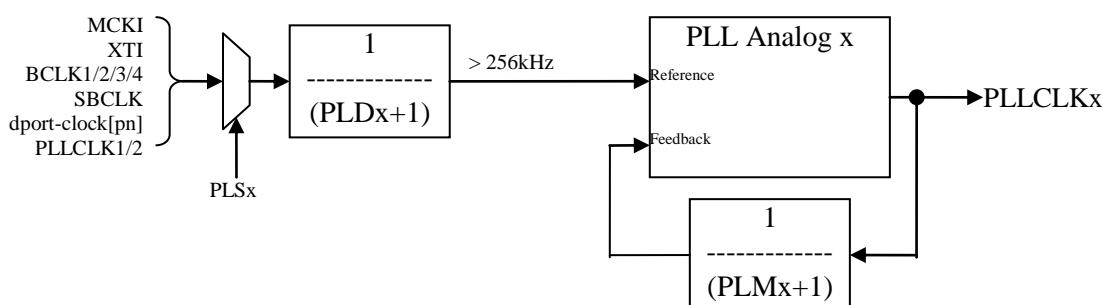


Figure 56. PLL Block Diagram

## ■ Input Clock Select Function (PLS1, PLS2)

Each PLL has a function that selects the input clock. Clock source address is selected by PLS1[4:0] and PLS2[4:0] bits.

PLL1 Clock Source is selected from these sources by PLS1[4:0] bits. Refer to [Table 88](#) for the register value.

- TieLow
- MCKI
- XTI
- SBCLK
- BCLK1/2/3/4
- dport-clock0 to 9

PLL2 Clock Source is selected from these sources by PLS2[4:0] bits. Refer to [Table 88](#) for the register value.

- TieLow
- PLLCLK1

### 1. PLL Reference Clock Divider (PLD1, PLD2)

Each PLL can set the dividing number of the reference clock in 16 bits. The input clock is used as PLL reference clock by dividing by (PLD+1).

PLD1[15:0] bits PLD2[15:0] bits	Dividing Number	
0x0000	1/(PLDx+1)	(default)
0x0001-0xFFFF	1/(PLDx+1)	

Table 91. PLL Reference Clock Divider

Note 101. The reference clock should be set in the range from 256kHz to 3.072MHz after divided by PLDx.

### 2. PLL Feedback Clock Divider (PLM1, PLM2)

The dividing number of feedback clock can be set freely in 16 bits. PLLCLKx is divided by (PLMx + 1) and used as a PLL feedback clock. The feedback clock is fixed to “L” without dividing when PLMx = 0x0000.

PLM1[15:0] bits PLM2[15:0] bits	Dividing Number	
0x0000	Clock Stop	(default)
0x0001-0xFFFF	1/(PLMx+1)	

Table 92. PLL Feedback Clock Divider

### 3. PLL Power Management (PMPLL1,PMPLL2)

PLL1 and PLL2 can be independently controlled by the control register. When PLL2 is powered-up, PMPLL2 bit should be set to “1” after PLL1 is locked (max.2ms) by setting PMPLL1 bit to “1”.

PMPLL1 bit PMPLL2 bit	PLL1 State PLL2 State	
0	Power-down	(default)
1	Power-Up	

Table 93. PLL Power Control

### 4. Example of Frequency Setting

CLKIN		PLL condition			PLL1		
Source	Frequency [Hz]	D+1	REFCLK [Hz]	M+1	Family [Hz]	DSPMCLK	
		[fs]	[Hz]			[fs]	[Hz]
MCLKI	9,600,000	5	1,920,000	64	48,000	2,560	122,880,000
		25	384,000	288		2,304	110,592,000
	19,200,000	10	1,920,000	64		2,560	122,880,000
		25	768,000	144		2,304	110,592,000
	12,288,000	4	3,072,000	40		2,560	122,880,000
		4	3,072,000	36		2,304	110,592,000
	24,576,000	8	3,072,000	40		2,560	122,880,000
		8	3,072,000	36		2,304	110,592,000
	12,000,000	25	480,000	256	44,100	2,560	122,880,000
	24,000,000	25	960,000	128		2,560	122,880,000
	11,289,600	4	2,822,400	40		2,560	112,896,000
		4	2,822,400	36		2,304	101,606,400
	22,579,200	8	2,822,400	40		2,560	112,896,000
		8	2,822,400	36		2,304	101,606,400

Table 94. PLL1 Frequency Setting Example1 (PLL reference source: MCKI)

CLKIN		Expect			PLL1				PLL2			
Source	Frequency [Hz]	Family [Hz]	DSPMCLK		D+1	REFCLK1 [Hz]	M+1	PLL1 out [Hz]	D+1	REFCLK2 [Hz]	M+1	PLL2 out [Hz]
			[fs]	[Hz]								
MCLKI	12,000,000	48,000	2,304	110,592,000	4	3,000,000	36	108,000,000	125	864,000	128	110592000
	24,000,000		2,304	110,592,000	8	3,000,000	36	108,000,000	125	864,000	128	110592000
	13,000,000		2,560	122,880,000	15	866,667	128	110,933,333	65	1,706,667	72	122880000
	13,000,000		2,304	110,592,000	15	866,667	128	110,933,333	325	341,333	324	110592000
	26,000,000		2,560	122,880,000	60	433,333	256	110,933,333	65	1,706,667	72	122880000
	26,000,000		2,304	110,592,000	25	1,040,000	108	112,320,000	65	1,728,000	64	110592000
	13,500,000		2,560	122,880,000	16	843,750	128	108,000,000	225	480,000	256	122880000
	13,500,000		2,304	110,592,000	16	843,750	128	108,000,000	125	864,000	128	110592000
	27,000,000		2,560	122,880,000	16	1,687,500	64	108,000,000	225	480,000	256	122880000
	27,000,000		2,304	110,592,000	16	1,687,500	64	108,000,000	125	864,000	128	110592000
	25,000,000		2,560	122,880,000	15	1,666,667	64	106,666,667	125	853,333	144	122880000
	25,000,000		2,304	110,592,000	25	1,000,000	108	108,000,000	125	864,000	128	110592000
	13,000,000	44,100	2,560	112,896,000	25	520,000	196	101,920,000	65	1,568,000	72	112896000
	13,000,000		2,304	101,606,400	25	520,000	196	101,920,000	325	313,600	324	101606400
	26,000,000		2,560	112,896,000	25	1,040,000	98	101,920,000	65	1,568,000	72	112896000
	26,000,000		2,304	101,606,400	25	1,040,000	98	101,920,000	325	313,600	324	101606400
	13,500,000		2,560	112,896,000	25	540,000	196	105,840,000	15	7,056,000	16	112896000
	13,500,000		2,304	101,606,400	25	540,000	196	105,840,000	25	4,233,600	24	101606400
	27,000,000		2,560	112,896,000	25	1,080,000	98	105,840,000	15	7,056,000	16	112896000
	27,000,000		2,304	101,606,400	25	1,080,000	98	105,840,000	25	4,233,600	24	101606400
	25,000,000		2,560	112,896,000	25	1,000,000	112	112,000,000	125	896,000	126	112896000

Table 95. PLL1 and PLL2 Frequency Setting Example (PLL reference source: MCKI)

CLKIN			PLL condition			PLLCLK		
Source	Frequency [Hz]	D+1	REFCLK [Hz]	M+1	Family [Hz]	DSPMCLK		
						[fs]	[Hz]	
BCLK (32fs)	8,000	256,000	1	256,000	480	48,000	2,560	122,880,000
		256,000	1	256,000	432		2,304	110,592,000
	11,025	352,800	1	352,800	320	44,100	2,560	112,896,000
		352,800	1	352,800	288		2,304	101,606,400
	16,000	512,000	1	512,000	240	48,000	2,560	122,880,000
		512,000	1	512,000	216		2,304	110,592,000
	22,050	705,600	1	705,600	160	44,100	2,560	112,896,000
		705,600	1	705,600	144		2,304	101,606,400
	24,000	768,000	1	768,000	160	48,000	2,560	122,880,000
		768,000	1	768,000	144		2,304	110,592,000
	32,000	1,024,000	1	1,024,000	120	48,000	2,560	122,880,000
		1,024,000	1	1,024,000	108		2,304	110,592,000
44,100	1,411,200	1	1,411,200	80	44,100	2,560	112,896,000	
	1,411,200	1	1,411,200	72		2,304	101,606,400	
48,000	1,536,000	1	1,536,000	80	48,000	2,560	122,880,000	
	1,536,000	1	1,536,000	72		2,304	110,592,000	

Table 96. PLL1 Frequency Setting Example 1 (PLL reference source: BCLK)

CLKIN			PLL condition			PLLCLK		
Source		Frequency [Hz]	D+1	REFCLK [Hz]	M+1	Family [Hz]	DSPMCLK	
						[fs]	[Hz]	
BICK (48fs)	8,000	384,000	1	384,000	320	48,000	2,560	122,880,000
		384,000	1	384,000	288		2,304	110,592,000
	11,025	529,200	1	529,200	192	44,100	2,304	101,606,400
	16,000	768,000	1	768,000	160	48,000	2,560	122,880,000
		768,000	1	768,000	144		2,304	110,592,000
	22,050	1,058,400	3	352,800	320	44,100	2,560	112,896,000
		1,058,400	1	1,058,400	96		2,304	101,606,400
	24,000	1,152,000	3	384,000	320	48,000	2,560	122,880,000
		1,152,000	1	1,152,000	96		2,304	110,592,000
	32,000	1,536,000	1	1,536,000	80	48,000	2,560	122,880,000
		1,536,000	1	1,536,000	72		2,304	110,592,000
BICK (64fs)	44,100	2,116,800	3	705,600	160	44,100	2,560	112,896,000
		2,116,800	1	2,116,800	48		2,304	101,606,400
	48,000	2,304,000	3	768,000	160	48,000	2,560	122,880,000
		2,304,000	1	2,304,000	48		2,304	110,592,000
	8,000	512,000	1	512,000	240	48,000	2,560	122,880,000
		512,000	1	512,000	216		2,304	110,592,000
	11,025	705,600	1	705,600	160	44,100	2,560	112,896,000
		705,600	1	705,600	144		2,304	101,606,400
	16,000	1,024,000	1	1,024,000	120	48,000	2,560	122,880,000
		1,024,000	1	1,024,000	108		2,304	110,592,000
	22,050	1,411,200	1	1,411,200	80	44,100	2,560	112,896,000
		1,411,200	1	1,411,200	72		2,304	101,606,400
	24,000	1,536,000	1	1,536,000	80	48,000	2,560	122,880,000
		1,536,000	1	1,536,000	72		2,304	110,592,000
	32,000	2,048,000	1	2,048,000	60	48,000	2,560	122,880,000
		2,048,000	1	2,048,000	54		2,304	110,592,000
	44,100	2,822,400	1	2,822,400	40	44,100	2,560	112,896,000
		2,822,400	1	2,822,400	36		2,304	101,606,400
	48,000	3,072,000	1	3,072,000	40	48,000	2,560	122,880,000
		3,072,000	1	3,072,000	36		2,304	110,592,000

Table 97. PLL1 Frequency Setting Example 2 (PLL reference source: BCLK)

## ■ Sync Domain

There are seven kinds of Sync Domain (SDSYNC<sub>x</sub>, SDBCLK<sub>x</sub>, x=1, 2, 3, 4, 5, 6, 7). The internal audio data must be synchronized with one of these sync domains.

Master/Slave mode for the SDSYNC1-4 can be selected by a corresponding MSNx bit. SDSYNC5-7 are fixed to Master Mode. In master mode, MSYNC<sub>x</sub>/MBCLK<sub>x</sub> is generated from a clock source which is selected by CKS<sub>x</sub> bit by the divider setting (BDV<sub>x</sub> and SDV<sub>x</sub> bits).

MCKO and CODECMCLK can be generated by dividing the clock source, which is selected by MCKS<sub>x</sub> bit, by (1+MDIV). DSPMCLK uses the clock source which is selected by CKSD. BUSCLK for internal serial data bus can be generated by dividing DSPMCLK, by (1+MDIVD).

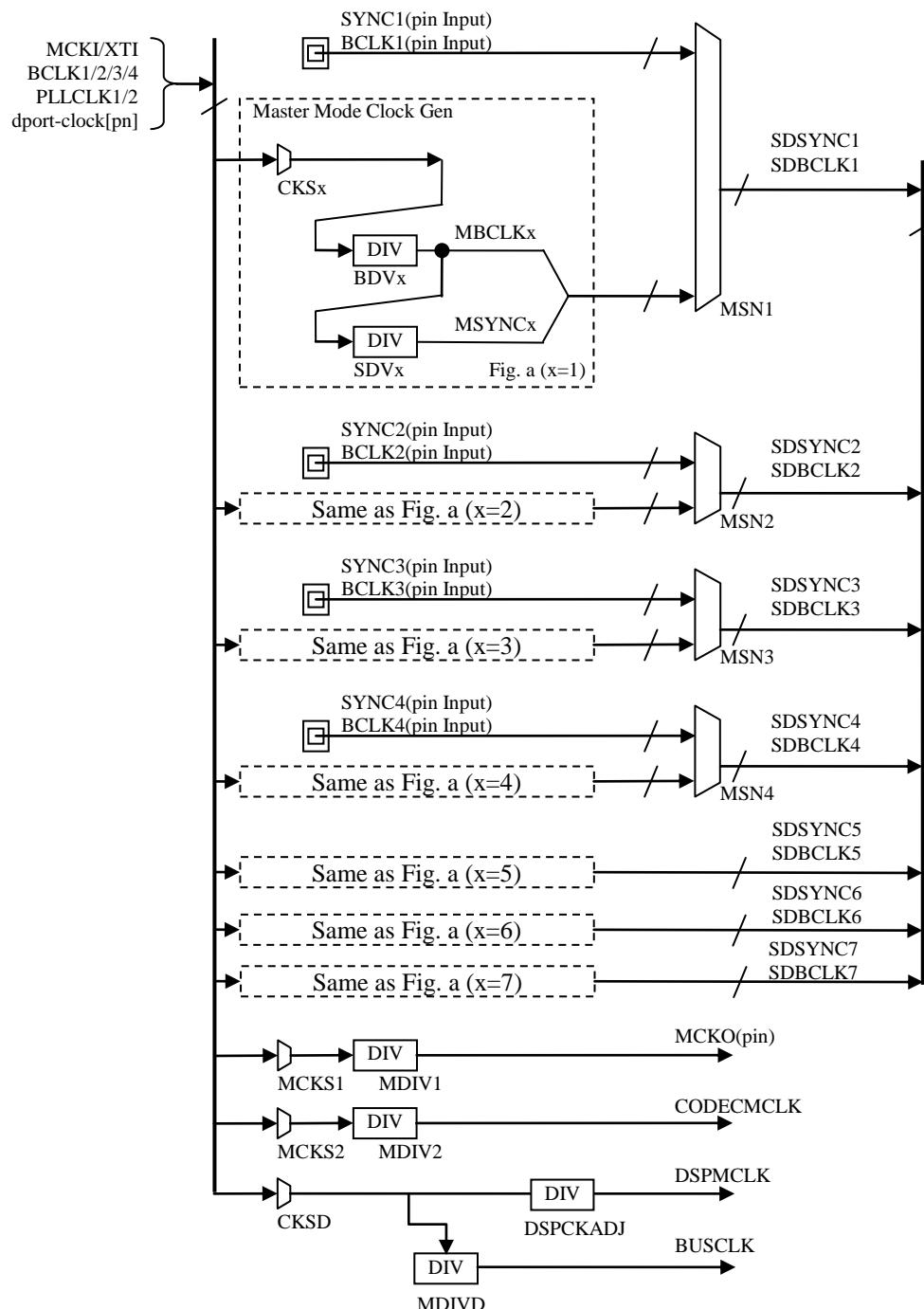


Figure 57. Sync Domain

## 1. Master/Slave Mode Select

Master/Slave mode of the SYNCx pin and BCLKx pin can be selected by MSNx bit.

MSN <sub>x</sub> bit	SYNC <sub>x</sub> (pin), BCLK <sub>x</sub> (pin)
0	Slave Mode
1	PLL Master Mode SYNC timing can adapt another slave port.

Table 98. Maste/Slave Mode Select

## 2. Master Mode Clock Source Select

Clock source address of the MSYNC<sub>x</sub> and MBCLK<sub>x</sub> clocks are selected by MCKS<sub>x</sub>/CKS<sub>x</sub> bits. Available clock sources for CKS<sub>x</sub>[4:0] bits are shown below. The register value refers to [Table 88](#).

- TieLow
- PLLCLK1/2
- MCKI
- XTI
- SBCLK
- BCLK1/2/3/4
- dport-clock0 to 9

## 3. Divider Setting for MBCLK<sub>x</sub> Generation

Divider for MBCLK<sub>x</sub> clock is set by BDV<sub>x</sub> (x=1, 2, 3, 4, 5, 6, 7) bit. MBCLK<sub>x</sub> is generated by dividing the clock, which is selected by CKS<sub>x</sub> bit, by (1+BDV<sub>x</sub>).

BDV <sub>x</sub> [7:0] bits	Dividing Number	
0x00	1	
0x01-0xFF	1/(BDV <sub>x</sub> +1)	(default)

Table 99. BCLK Divider Setting

## 4. Divider Setting for MSYNC<sub>x</sub> Generation

Divider for MSYNC<sub>x</sub> clocks is set by SDV<sub>x</sub> (x=1, 2, 3, 4, 5, 6, 7) bit. MSYNC<sub>x</sub> is generated by dividing MBCLK<sub>x</sub> clock by (1+SDV<sub>x</sub>).

SDV <sub>x</sub> [7:0] bits	Dividing Number	
0x00	Stop	
0x01-0xFF	1/(SDV <sub>x</sub> +1)	(default)

Table 100. Sync Divider Setting

## 5. Divider Setting for MCKO Generation

MCKO divider is set by MDVx bit. MCKO clock is generated by dividing the clock, which is selected by MCKS bit, by  $(1+MDV)$ . The generated MCKO clock can be output as CODECMCLK from the MCKO pin. MCKO output frequency must be set 18.432MHz or lower. The duty of the MCKO output will be 50% (typ.) when dividing the clock with an even number.

MDIVx[7:0] bits	Dividing Number	
0x00	1	
0x01-0xFF	$1/(MDIVx+1)$	(default)

Table 101. MCKO Divider Setting

## 6. Divider Setting for BUSCLK Generation

BUSCLK clock is generated by dividing the clock, which is selected by CKSD bit, by  $(1+MDIVD)$ . BUSCLK is clock for serial audio data bus. BUSCLK frequency must be set “ $\geq 128 \times \text{SYNC}_x$ ” and “ $\leq 24.576\text{MHz}$ ”.

MDIVD[7:0] bits	Dividing Number	
0x00	1	
0x01-0xFF	$1/(MDIVD+1)$	(default=3; 4 dividing)

Table 102. BUSCLK Divider Setting

## 7. Divider Setting for DSPMCLK Generation

DSPMCLK clock is generated by dividing the clock, which is selected by CKSD bit, by “ $\text{DSPMCLK} \times (256 - \text{DSPCKADJ}[7:0] \text{ bits})/256$ ”. DSPMCLK is the digital main clock for DSP, SRC, MIX and etc.

DSPCKADJ[7:0] bits	Dividing Number	
0x00	1	
0x01-0xFF	$\text{DSPMCLK} \times (256 - \text{DSPCKADJ})/256$	(default)

Table 103. DSPMCLK Divider Setting

## 8. Soft SRC

The input data from the DSPI2 and DSPI4 ports can be input to the DSP by down sampling by a synchronous SRC located on the input side of the DSP internally. Also, an internal synchronous SRC located on the output side of the DSP up samples the data when outputting the data from DSPO2 and DSPO4 ports. When using Soft SRC, DSPO2 and DSPO4 need to set Sync Domain independently.

**EDNOPDIS bit must be set to “1” when using Soft SRC.**

Path	DSPI2 → DSP-Input	DSP-Output → DSPO2	DSPI4 → DSP-Input	DSP-Output → DSPO4
Up/Down Sampling	Down Sampling	Up Sampling	Down Sampling	Up Sampling
Sample rate Convert	16kHz→8kHz	8kHz→16kHz	48kHz→8/16kHz	8/16kHz→48kHz

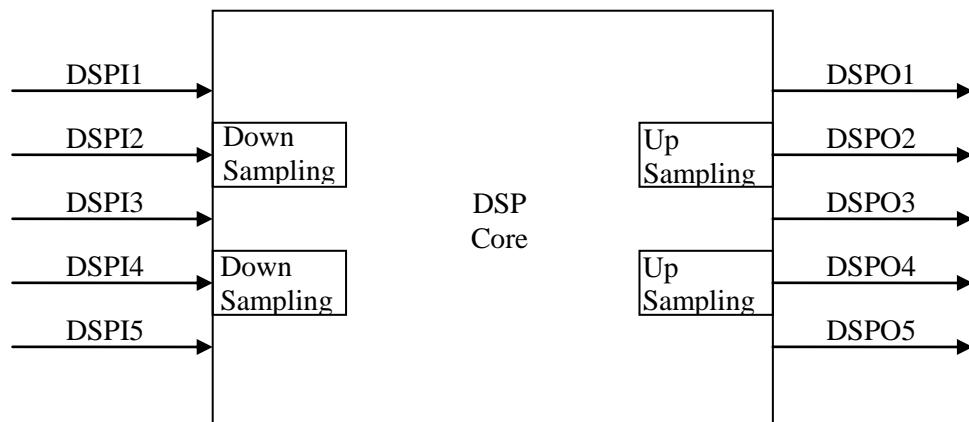


Figure 58. Synchronous SRC

## ■ Audio Data Path Setting

An audio source port is freely connectable to each audio sink port. The audio source port means the data output port to the serial audio data bus in the middle of the figure below. The audio sink port means the input data selecting port from the serial audio data bus. To transmit data on the serial audio data bus, PMAIF bit is set to “1” and DSPMCLK setting is needed.

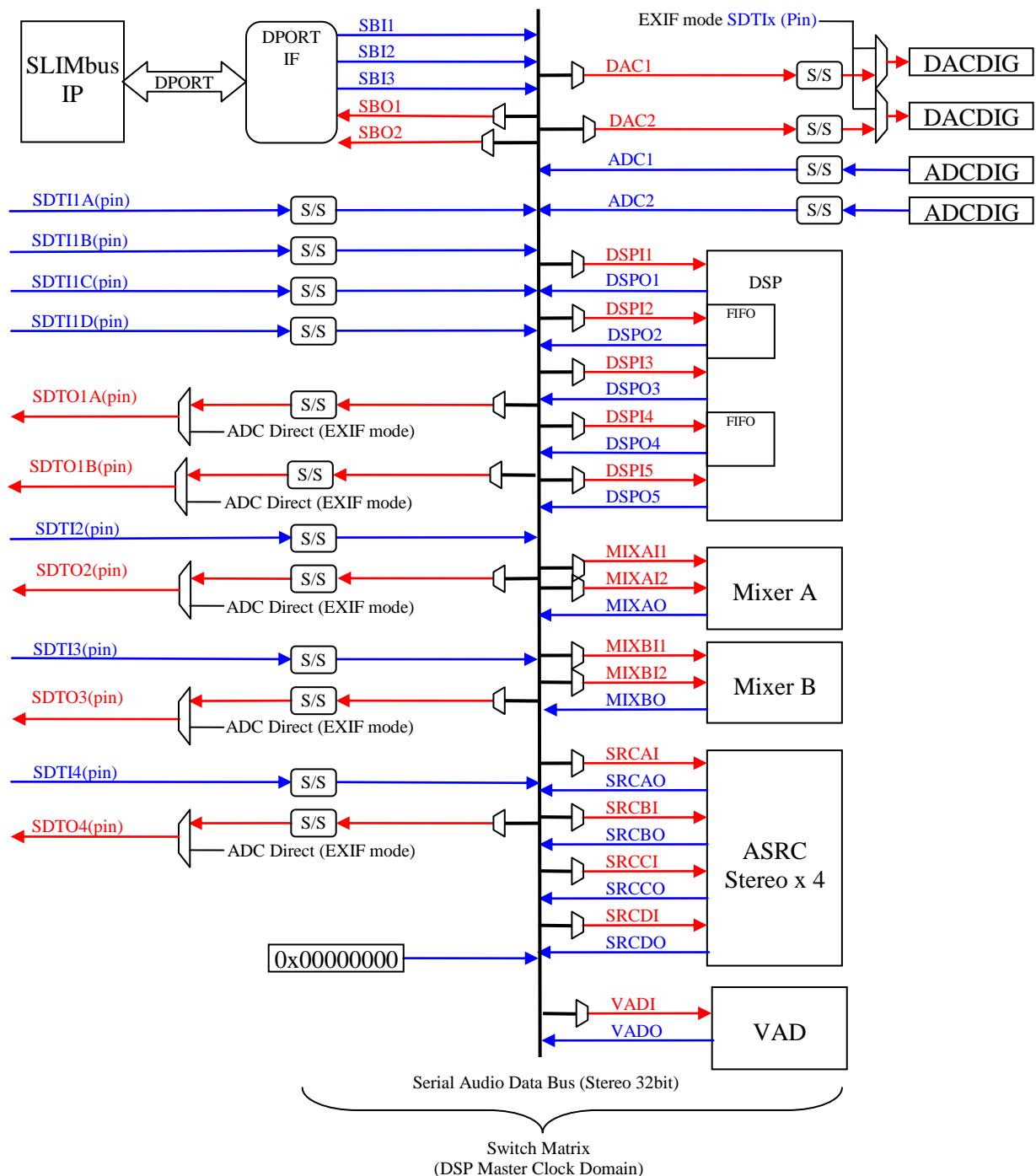


Figure 59. Path Setting

## ■ Audio Source Port Setting

**Table 104** shows a list of Audio Source Ports. A different source address is assigned to each audio source port. The assigned source address is used for connection setting of the audio sink port. The sync domain setting of each audio source port is controlled by a sync domain setting register. If the sync domain setting is in auto mode, a sync domain is automatically set to an audio source port.

Source Address[4:0]	Source	Description	Sync Domain Setting Register
0x00	ALL0	Fixed to “0x0000 0000”	--
0x01	SDTI1A	SDTI1A(pin) Input	SDAIF1[2:0] &MSN1
0x02	SDTI1B	SDTI1B(pin) Input	SDAIF1[2:0] &MSN1
0x03	SDTI1C	SDTI1C(pin) Input	SDAIF1[2:0] &MSN1
0x04	SDTI1D	SDTI1D(pin) Input	SDAIF1[2:0] &MSN1
0x05	SDTI2	SDTI2(pin) Input	SDAIF2[2:0] &MSN2
0x06	SDTI3	SDTI3(pin) Input	SDAIF3[2:0] &MSN3
0x07	SDTI4	SDTI4(pin) Input	SDAIF4[2:0] &MSN4
0x08	Reserved	--	--
0x09	ADC1	ADC1 Output (The analog path like MIC-Amp should be selected separately.)	SDCDC[2:0]
0x0A	ADC2	ADC2 Output (The analog path like MIC-Amp should be selected separately.)	SDCDC[2:0]
0x0B	SBI1	Inputted data to Sink Port on SLIMbus Lch=port-array-0 , Rch=port-array-1	SDSBI1[2:0]
0x0C	SBI2	Inputted data to Sink Port on SLIMbus Lch=port-array-2 , Rch=port-array-3	SDSBI2[2:0]
0x0D	SBI3	Inputted data to Sink Port on SLIMbus Lch=port-array-4 , Rch=port-array-5	SDSBI3[2:0]
0x0E	DSPO1	DSP Output 1	SDDSP[2:0]
0x0F	DSPO2	DSP Output 2 (with DFSC)	SDDSP02[2:0]
0x10	DSPO3	DSP Output 3	SDDSP[2:0]
0x11	DSPO4	DSP Output 4	SDDSP04[2:0]
0x12	DSPO5	DSP Output 5	SDDSP[2:0]
0x13	MIXAO	Mixer A Output	(Auto) =MIXAI1 or MIXAI2
0x14	MIXBO	Mixer B Output	(Auto) =MIXBI1 or MIXBI2
0x15	SRCAO	SRC A Output	SDSRCAO[2:0]
0x16	SRCBO	SRC B Output	SDSRCBO[2:0]
0x17	SRCCO	SRC C Output	SDSRCCO[2:0]
0x18	SRCDO	SRC D Output	SDSRCDO[2:0]
0x19	VADO	VAD Output	(Auto) =VADI
Else	Reserved	-	-

Table 104. Audio Source Port

## ■ Audio Sink Port Setting

**Table 105** shows a list of Audio Sink Port. The source address setting of an audio source port, which is wanted to connect, is controlled by a source address register. The sync domain settings of connected audio source port and audio sink port must be the same. If the sync domain setting is in auto mode, an audio sink port inherits the sync domain of the connected audio source port.

\* Each Source Address setting registers can be written during Run. However it is limited to the same sync domain.

Sink Name	Description	Source Address Setting Register	Sync Domain Setting Register
SDTO1A	SDTO1A(pin) Output	SDTO1ASRC[4:0]	SDAIF1[2:0] &MSN1
SDTO1B	SDTO1B(pin) Output	SDTO1BSRC[4:0]	SDAIF1[2:0] &MSN1
SDTO2	SDTO2(pin) Output	SDTO2SRC[4:0]	SDAIF2[2:0] &MSN2
SDTO3	SDTO3(pin) Output	SDTO3SRC[4:0]	SDAIF3[2:0] &MSN3
SDTO4	SDTO4(pin) Output	SDTO4SRC[4:0]	SDAIF4[2:0] &MSN4
SBO1	Outputted data to Source Port on SLIMbus port-array-6=Lch, port-array-7=Rch	SBO1SRC[4:0]	(Auto)
SBO2	Outputted data to Source Port on SLIMbus port-array-8=Lch, port-array-9=Rch	SBO2SRC[4:0]	(Auto)
DAC1	Inputted to DAC1 (The analog path like HP-Amp should be selected separately)	DAC1SRC[4:0]	(Auto)
DAC2	Inputted to DAC2 (The analog path like Lineout-Amp should be selected separately)	DAC2SRC[4:0]	(Auto)
DSPI1	DSP Input 1	DSPI1SRC[4:0]	(Auto)
DSPI2	DSP Input 2	DSPI2SRC[4:0]	(Auto)
DSPI3	DSP Input 3	DSPI3SRC[4:0]	(Auto)
DSPI4	DSP Input 4	DSPI4SRC[4:0]	(Auto)
DSPI5	DSP Input 5	DSPI5SRC[4:0]	(Auto)
MIXAI1	Mixer A Input 1	MIXAI1SRC[4:0]	(Auto)
MIXAI2	Mixer A Input 2	MIXAI2SRC[4:0]	Same as MIXAI1
MIXBI1	Mixer B Input 1	MIXBI1SRC[4:0]	(Auto)
MIXBI2	Mixer B Input 2	MIXBI2SRC[4:0]	Same as MIXBI1
SRCAI	SRC A Input	SRCAISRC[4:0]	(Auto)
SRCBI	SRC B Input	SRCBISRC[4:0]	(Auto)
SRCCI	SRC C Input	SRCCISRC[4:0]	(Auto)
SRCDI	SRC D Input	SRCDISRC[4:0]	(Auto)
VADI	VAD Input	VADSRC[4:0]	(Auto)

Table 105. Audio Sink Port

Auto: Sync Domain succession source Address selected by xxxSRC[4:0]

## ■ Sync Domain Setting

Set sync domain of Audio Source Port and Audio Sink Port by SDSYNC1-7 and SDBCLK1-7 bits.

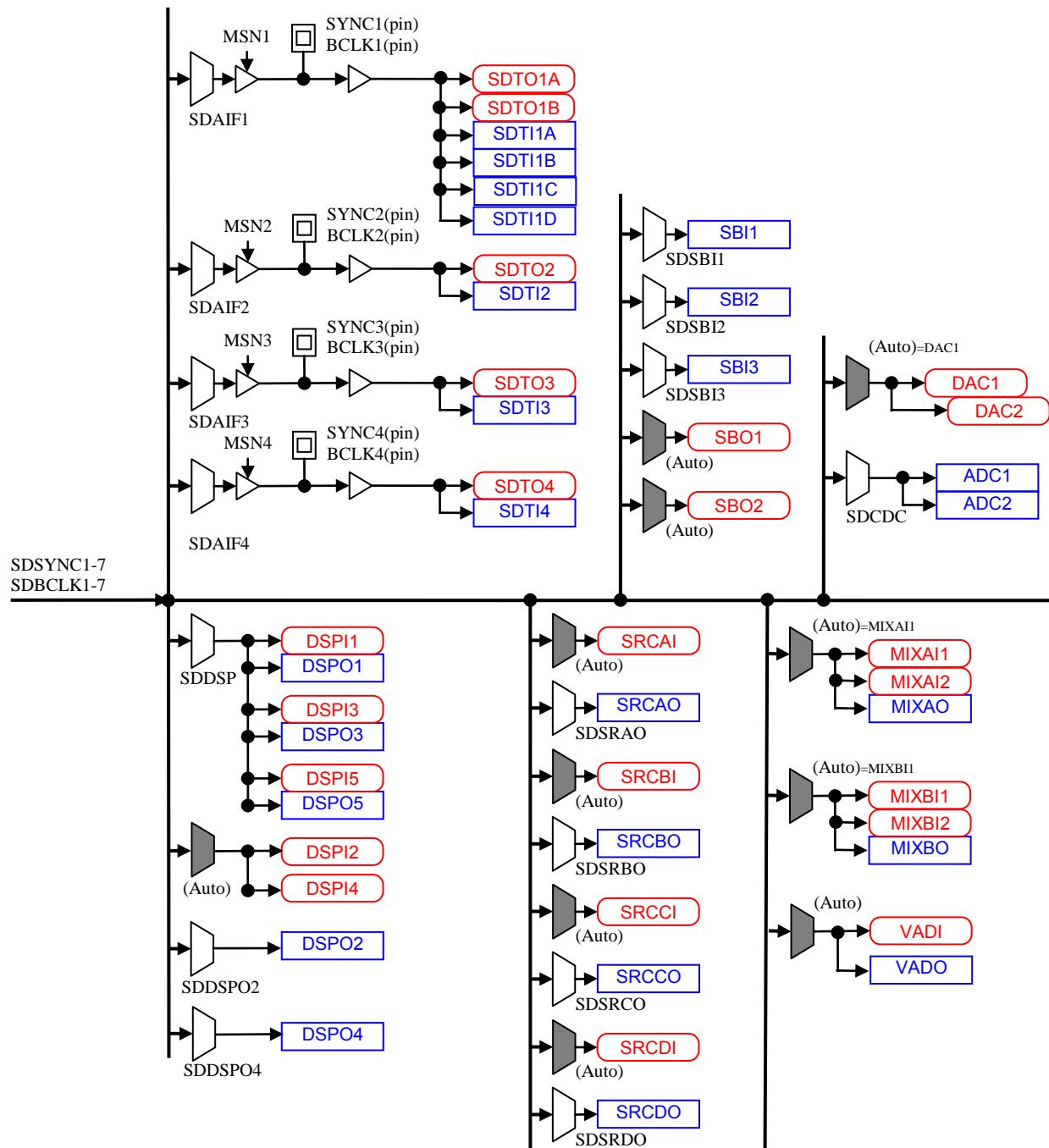


Figure 60. Sync Domain Setting

## ■ Sync Domain Setting Register

Sync Domain Setting Register SDxxx[2:0]		Sync Domain	
0		Not Assigned	(default)
1		SDSYNC1, SDBCLK1	
2		SDSYNC2, SDBCLK2	
3		SDSYNC3, SDBCLK3	
4		SDSYNC4, SDBCLK4	
5		SDSYNC5, SDBCLK5	
6		SDSYNC6, SDBCLK6	
7		SDSYNC7, SDBCLK7	

Table 106. Sync Domain Setting Register

## ■ Serial Audio Interface

Audio interface format can be set for each Sync Domain.

MSNx bit	THR <sub>x</sub> bit	Through	
0	0	Disable	(default)
	1	Enable	

Table 107. SYNC Through

Set THR<sub>x</sub> bit to “1” when selecting another SYNC pin in slave mode to output as master mode. Although the SYNC pin is an output pin, the input clock of the other SYNC pin in slave mode is directly output from the master SYNC pin when it is synchronized to the other slave pin instead of dividing clock of the PLL.

When the SYNC through setting (THR<sub>x</sub> bit) is disabled, DIF signals are reproduced on a rising edge of the other SYNC pin. By this operation, the AK4961 converts the data to the format to which the device is synchronized. However, the duty of SYNC outputs becomes 50% (typ.).

Interface formats of the CODEC and DSP are fixed to I<sup>2</sup>S. Data length (DLC<sub>x</sub> bit) and BICK cycle are set by sync domain.

DIF bit		Digital I/F Format	
[1]	[0]		
0	0	I <sup>2</sup> S compatible	(default)
0	1	MSB justified	
1	0	PCM Short Frame	
1	1	PCM Long Frame	

Table 108. Digital I/F Format Setting

PCM Short/Long Frame requires the BCLK cycle equal to or more than “data length x 2fs”.

BCKPx bit	BCLK edge referenced to SYNC edge	
0	falling (FE)	(default)
1	rising (RE)	

Table 109. BCLK Edge

DLCx			Digital I/O Format
[2]	[1]	[0]	
0	0	0	24bit linear
0	0	1	16bit linear
0	1	0	N/A
0	1	1	N/A
1	x	x	32bit linear

(default)

Table 110. Data Length Setting (x: Do not care, N/A: Not available)

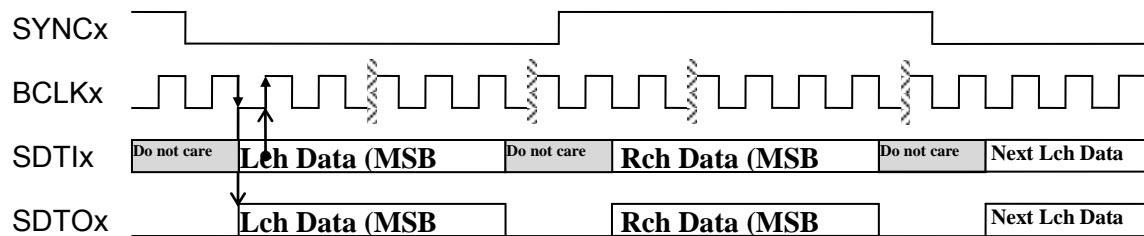
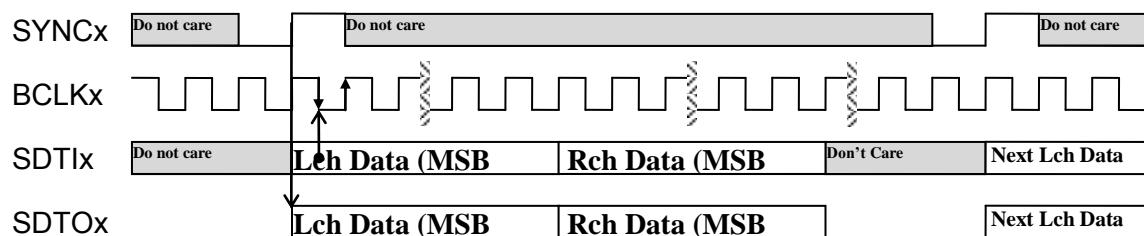
Figure 61. I<sup>2</sup>S Format (DIFx[1:0] bits = "00")

Figure 62. PCM Long Frame Rising-edge (DIFx[1:0] bits = "11", BCKPx bit = "1")

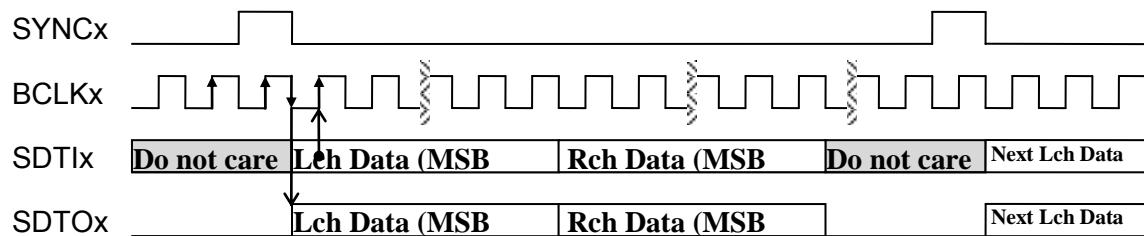


Figure 63. PCM Short Frame Falling-edge (DIFx[1:0] bits = "10", BCKPx bit = "0")

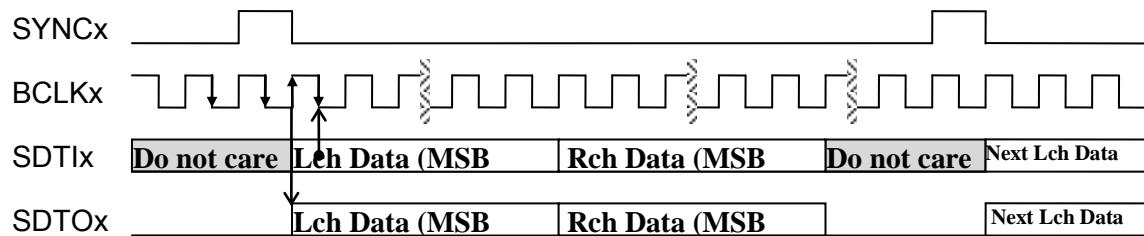


Figure 64. PCM Short Frame Rising-edge (DIFx[1:0] bits = "10", BCKPx bit = "1")

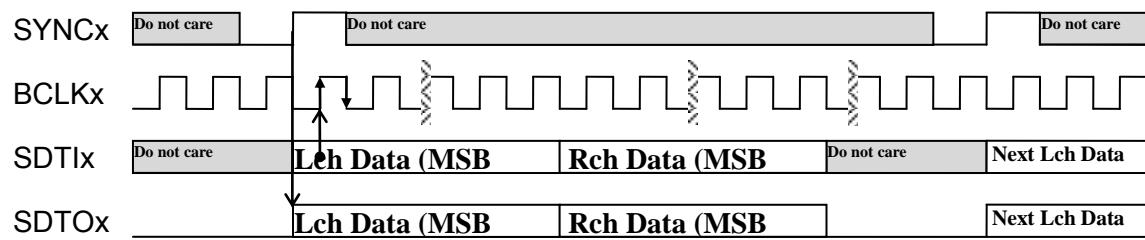


Figure 65. PCM Long Frame Falling-edge (DIFx[1:0] bits = “11”, BCKPx bit = “0”)

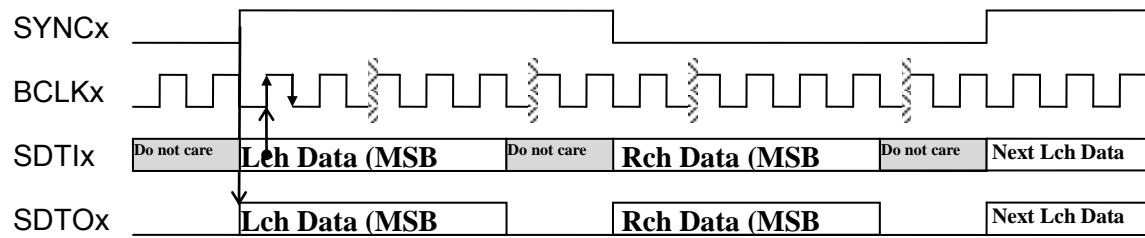


Figure 66. MSB Justified format (DIFx[1:0] bits = “01”)

## ■ Power-up & Operation Mode

### Power Down (PDN pin= “L”)

When the PDN pin is “L”, the AK4961 is in a powered-down state. Power supplies must be applied when the PDN pin = “L”. Set the PDN pin to “H” to release power-down after all the power supplies are on. More than one tPDN cycle of “L” period is needed before releasing power-down. The state of the AK4961 transitions to LDO2 Ctrl state by bringing the PDN pin to “H”.

### LDO2 Ctrl State

This is a state to control the LDO2.

When the LDO2E pin = “L”, the DRSTN signal is immediately changed from “L” to “H” and the AK4961 enters to an SBRSTN Ctrl state. When the LOD2E pin = “H”, LDO2 is powered up and the DRSTN signal is changed from “L” to “H” after 800 $\mu$ s (max.), and the AK4961 enters to a SBRSTN Ctrl state(CIF1 pin = “L”, CIF0 pin = “H”) or Standby state (CIF1 pin = “L/H”, CIF0 pin = “L”).

### SBRSTN Ctrl State (CIF1 pin = “L”, CIF0 pin = “H”)

When the SBRC pin = “L”, the SBRSTN signal is immediately changed from “L” to “H” and the AK4961 enters to Stanby State. When the SBRC pin = “H”, the SBRSTN signalis changed from “L” to “H” after counting 6144x 5 cycles of SBCLK and the AK4961 enters to Standby State.

### Standby State

SPI/I2C/SLIMbus can be operated and control register access is ready. However, accessing to the DSP, RAM and SRC are not possible in standy state. The AK4961 enters DSP/SRC-RDY state by setting PMSW bit = “1” first and SWRSTN bit = “1” next.

### DSP/SRC-RDY Ready

DSP/SRC/SRAM register access is ready. When using the PLL, DSPrSTN and PMSRCx bits should be set to “1” after the clock is stabilized. Registers which are not expressed as accessable registers during Run can only be accessed in this state.

## &lt;Device State Diagram&gt;

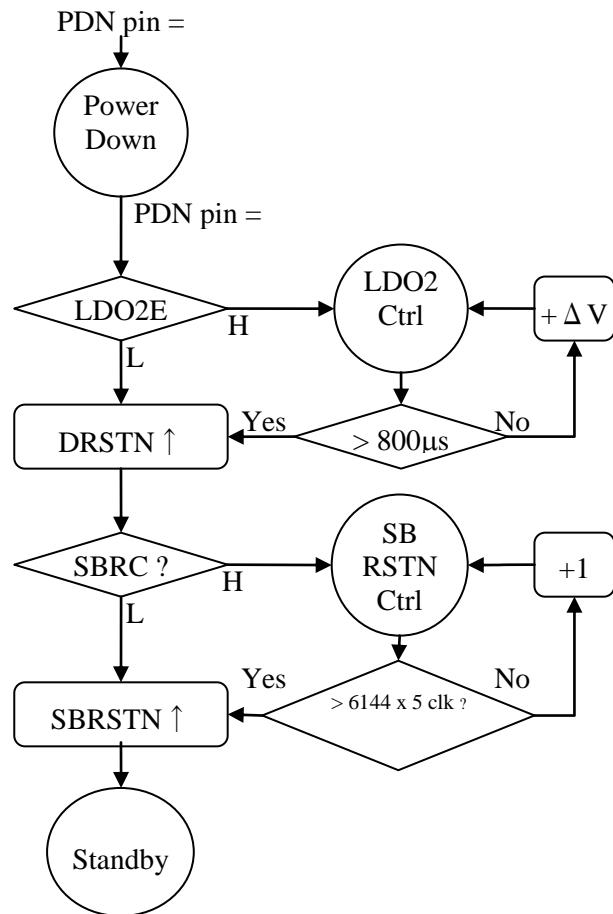


Figure 67. Device State Diagram

## DSP Operation Sequence example (SPI/I2C)

1. PMSW = SWRSTN bits = "0"
2. PMSW bit = "1", SWRSTN bits = "0"
3. PMSW = SWRSTN bits = "1"
4. DLRDY bit = "1"
5. PRIF bit = "1"
6. PRAM Download
7. PRIF bit = "0"
8. CRAM, OFREG Download
9. DLRDY bit = "0"
10. PMPLL1 bit = "1" (When using PLL1)
11. Wait 2ms
12. PMSRCx bit = "1"
13. DSPRSTN bit = "1"
14. DSP Normal Operation Start

## ■ Power Switch

The AK4961 integrates a power switch for DSP, SRCA/B/C/D and SRAM blocks. PMSW bit must be set to “1” when operating DSP, SRCA/B/C/D or SRAM blocks.

PMSW bit	SW Output	
0	Hi-z	
1	1.2V	(default)

Table 111. Power Switch

## ■ Register Access Ready

The DRSTN signal (reset signal for digital block) transitions to “H” from “L” and register access becomes valid in maximum 800μs when using LDO2 circuit by setting the PDN pin to “H” from “L”. (when not using the LDO2 circuit, it becomes valid immediately) When using the SLIMbus circuit, a wait time is necessary depending on the SBRC pin setting.

### <LDO2 is used (LDO2E pin = “H”)>

1. Supply AVDD1, AVDD2 CVDD, LVDD and TVDD1-3
2. PDN pin “L” → “H”
3. Wait 800μs until LDO2 1.2V Output is stable.
4. Internal DRSTN Signal: “L” → “H”
5. Wait (SBRSTN cycle =  $6144 \times 5 \times \text{SBCLK}$  @ SBRC pin = “H”, “0” @ SBRC pin = “L”)
6. Register Access Ready

### <External 1.2V is supplied. (LDO2E pin = “L”)>

1. Supply AVDD1, AVDD2 CVDD, LVDD and TVDD1-3
2. Supply VDD12
3. PDN pin “L” → “H”
4. Internal DRSTN Signal : “L” → “H”
5. Wait (SBRSTN cycle = “ $6144 \times 5 \times \text{SBCLK}$ ” @ SBRC pin = “H”, “0” @ SBRC pin = “L”)
6. Register Access Ready

## ■ Digital Block Power Management

Control of each block is as follows.

	PDN (pin)	DRSTN (Auto)	SBRSTN (Auto)	PMSW SWRSTN (bit)	LDO2	SLIM bus	SPI	PLLx	Codec	AIF MIX	DSP	SRC
Power Down	0	0	X	X	0V /Hi-z	X	X	X	X	X	X	X
LDO2 Startup	1	0	X	X	↓	PD	PD	PD	PD	PD	PD	PD
LDO2 Stable	1	1	0	0	1.2V	PD	PD	PD	PD	PD	PD	PD
SBcnt up	1	1	0	0	1.2V	PD	Act	PD	PD	PD	PD	PD
Standby	1	1	1	0	1.2V	Act	Act		Setup		PD	PD
DSP/SRC -RDY	1	1	1	1	1.2V	Act	Act		Setup			

Table 112. Control of each block

PD: Power Down

Setup: Set path and power Management bits

Act: Release Reset State.

X: Do not care

## ■ RAM Clear

After DSP reset is released (during RUN) and PLL is locked, data RAM, delay RAM, accelerator and coefficient RAM are cleared by “0” (RAM clear). The required time to clear RAM is 400μs. In the RAM clear sequence, it is possible to send commands to the DSP. (DSP is stopped during RAM clear sequence. The send command is accepted automatically after this sequence is completed.)

## ■ DSP Programmable Output

The AK4961 has two General Purpose Output (GP0 and GP1) pins for external device control. The GP1 pin is a versatile pin common to SDTO4. Set GP1E bit to “1” when using the GP1 pin. The output can be controlled by DSP programs. The initial polarity of the GP0 and GP1 pins are “L”.

GP1E bit	Mode
0	SDTO4
1	GP1

Table 113. GP1 Setting

## ■ Port 1 & CPU I/F

Audio I/F and CPU I/F can be changed by CIF0, CIF1, SBE pins and EXIF bit.

Mode	Audio IF	I2S Only	I2S Only	Direct I/F	Direct I/F	SLIMbus +I2S	SLIMbus +I2S	SLIMbus +I2S
CPU IF	SPI	I2C	SPI	I2C	SPI	I2C	SLIMbus	
	CIF0 pin	L	H	L	H	L	H	L
	CIF1 pin	L	L	L	L	L	L	H
	SBE pin	L	L	L	L	H	H	H
	EXIF bit	0	0	1	1	0	0	0
Clock	MCKI	MCKI	←	CODECMCLK	←	MCKI	←	←
	MCKO	MCKO	←	←	←	←	←	←
SLIMbus	SBCLK	N/A	←	←	←	SBCLK	←	←
	SBDATA	N/A	←	←	←	SBDATA	←	←
SPI/I2C	SCLK/SCL	SCLK	SCL	SCLK	SCL	SCLK	SCL	←
	SI/I2CFIL	SI	I2CFIL	SI	I2CFIL	SI	I2CFIL	←
	SO/SDA	SO	SDA	SO	SDA	SO	SDA	←
	CSN/CAD	CSN	CAD	CSN	CAD	CSN	CAD	←
PORT1 (SmartPA)	BCLK1	BCLK1	←	CODECBCLK	←	BCLK1	←	←
	SYNC1	SYNC1	←	CODECSYNC	←	SYNC1	←	←
	SDTI1A	SDTI1A	←	CODECSDTI1	←	PSEL0	←	←
	SDTI1B	SDTI1B	←	CODECSDTI2	←	PSEL1	←	←
	SDTI1C	SDTI1C	←	←	←	PSEL2	←	←
	SDTI1D	SDTI1D	←	←	←	←	←	←
	SDTO1A	SDTO1A	←	CODECSDTO1	←	SBRC	←	←
	SDTO1B	SDTO1B	←	CODECSDTO2	←	SDTO1B	←	←

Table 114. Port 1 &CPU I/F Setting (N/A: Not available)

## ■ SLIMbus Interface

The AK4961 has a SLIMbus interface. A generic device has 10 data ports of 24-bit. A desired port number can be assigned by setting DPxxINDEX[5:0] bits (xx = 00 ~ 09) of the interface device to each data port. Port-array00-05 are for Audio Sink port and Port-array06-09 are for Audio Source port only.

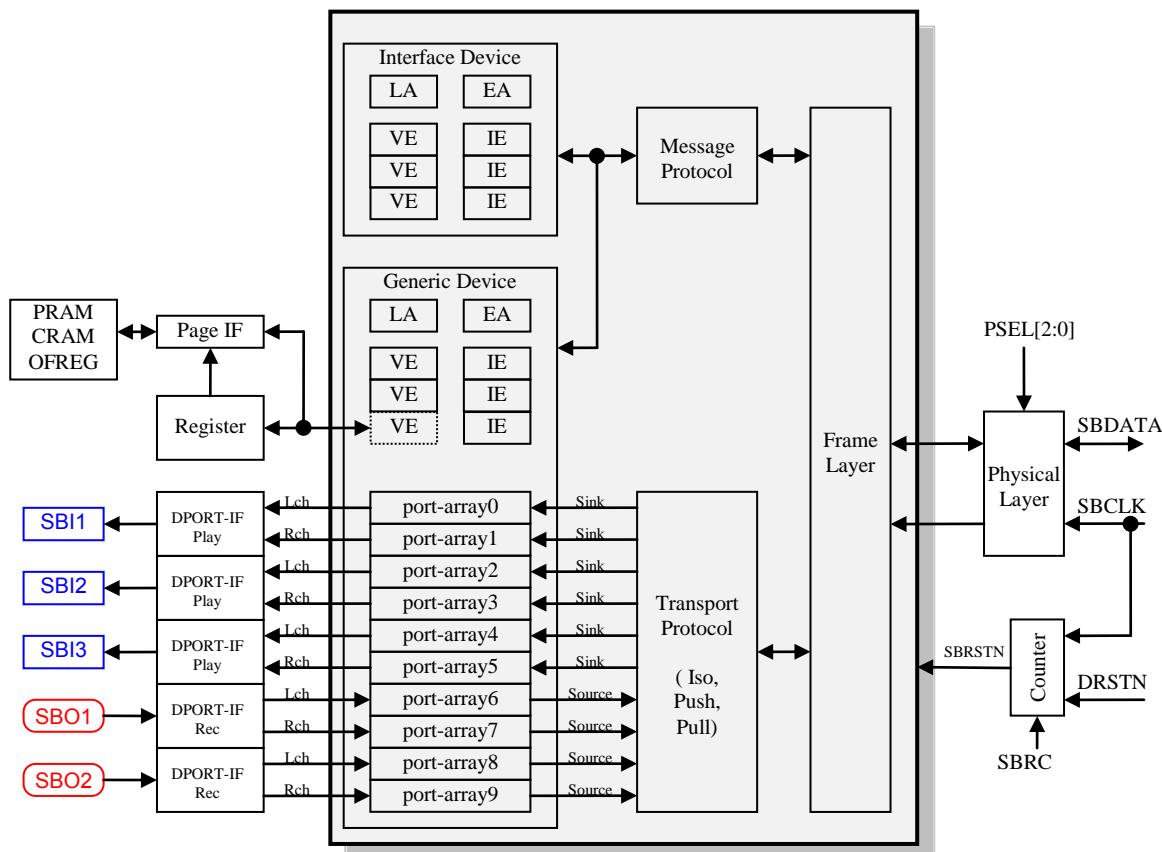


Figure 68. SLIMbus IF

## ■ Enumeration Address

Enumeration Addresses of an Interface Device and a Generic Device are as follows.

	Manufacturer ID	Product Code	Device Index	Instance Value
Interface Device	0x01dd	0x4961	0x00	0x00
Generic Device	0x01dd	0x4961	0x02	0x00

Table 115. Enumeration Address

## ■ SBDATA Drivability Setting

Drivability of the SBDATA pin can be set by the PSEL0 and PSEL1 pins. The PSEL2 pin should be fixed to “L”.

PSEL1 pin	PSEL0 Pin	Load Capacitance
L	L	N/A
L	H	0-90pF
H	L	0-105pF
H	H	0-130pF

Table 116. SBDATA pin Drivability Setting (N/A: Not available)

## ■ SLIMbus Reset Counter

The reset signal (SBRSTN signal) of the SLIMbus can be delayed after a master reset signal (DRSTN = “L” → “H”) of the digital block is released. It is controlled by the SBRC pin. The delay time is 5 super frame =  $6144(192*4*8) \times 5 \times \text{SBCLK}$ .

SBRC pin	SBRSTN “↑” Timing
L	Same as the DRSTN
H	After $6144(192*4*8) \times 5 \times \text{SBCLK}$ from DRSTN “↑”.

Table 117. SBRC(pin)

## ■ μP Interface Setting

When setting CIF0 pin = “L” and CIF1 pin = “H”, a register access by SLIMbus is valid.

### 1. Slice Size

The slice size of VE/IE accessing to each device type is fixed.

Device	SS[2:0]	Slice [byte]
Interface Device	0x0	1
Generic Device	0x4	6

Table 118. Slice Size

The slice size of Generic Device type is fixed to 6-byte, and the data should be transmitted by little endian that is the standard of the SLIMbus specification. However, lower 4bits of CRAM and ACCRAM data should be filled with 24-bit zero data when transmitted.

	PRAM ( <a href="#">Note 102</a> )	ACCRAM CRAM	Register
VU/IS [ 7: 0]	[7:0]	[3:0],0000b	[7:0]
VU/IS [15: 8]	[15:8]	[11:4]	Do not care
VU/IS [23:16]	[23:16]	[19:12]	Do not care
VU/IS [31:24]	[31:24]	Do not care	Do not care
VU/IS [39:32]	[39:32]	Do not care	Do not care
VU/IS [47:40]	Do not Care	Do not care	Do not care

Note 102. PRAM means a 40-bit data after coded.

Table 119. Data Transmitting Order

### 2. Address

Add “0x800” to the address shown in this manual. Accessing SRAM data should be made using a virtual memory address.

### 3. Peripheral Circuit

Enable the data port after the clock is stabilized by setting Sync Domain of SBI1-3/SBO1-2.

## ■ Value Element of Interface Device

SLIMbus interface settings are controlled by Interface Device.

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x800	R/W					PN0[5:0]				0x00
0x801	R/W					PN1[5:0]				0x01
0x802	R/W					PN2[5:0]				0x02
0x803	R/W					PN3[5:0]				0x03
0x804	R/W					PN4[5:0]				0x04
0x805	R/W					PN5[5:0]				0x05
0x806	R/W					PN6[5:0]				0x06
0x807	R/W					PN7[5:0]				0x07
0x808	R/W					PN8[5:0]				0x08
0x809	R/W					PN9[5:0]				0x09
0x900	R					dport-active-n[7:0]				0xff
0x901	R							↑ [9:8]		0x03
0x902	R					dport-dir[7:0]				0x00
0x903	R							↑ [9:8]		0x00
0x904	R					dport-of[7:0]				0x00
0x905	R							↑ [9:8]		0x00
0x906	R					dport-uf[7:0]				0x00
0x907	R							↑ [9:8]		0x00
0x908	R/W	rpt-dis	rpt-atev				Max-retr[3:0]			0x00

Table 120. Value Element of Interface Device

## ■ SPI Interface (CIF1 pin = “L”, CIF0 pin = “L”)

The access format consists of Command code + Address + Data.

	Byte	Comments
Command code	1	R/W Flag, Data Byte Length (BCNT[2:0]), and Access area (TARGET[3:0]) are included.
Address	2	Assign the accessing address.
Data	Data Length x N	Read/Write Data Data length is set by a command code.

Table 121. SPI Interface

Note 103. The address and data that are composed by multi bytes are written in big endian byte order.

Note 104. Every 8bit data of each byte is in MSB first.

Note 105. SOCFG bit controls the SO output(Hi-z or Low) when there is no output data.

Note 106. There is no echo-back function.

### <Write Operation>

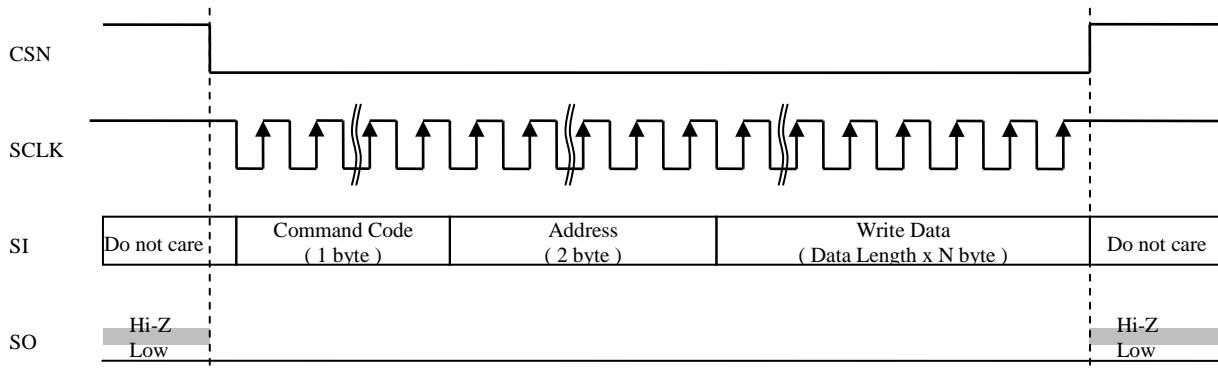


Figure 69. SPI Interface Timing (Write)

### <Read Operation>

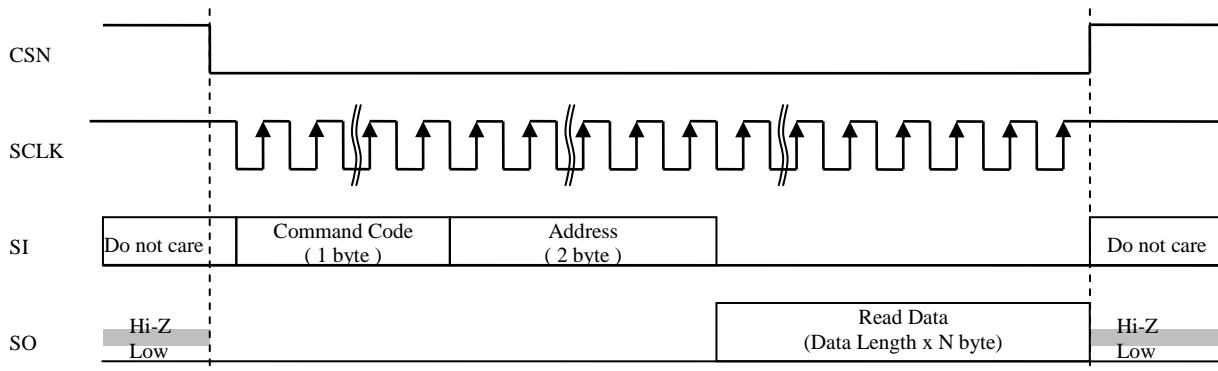


Figure 70. SPI Interface Timing (Read)

## 1. Command Code

Command code is consist of R/W flag, BCNT[2:0] and TARGET[3:0].

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
R/W flag	BCNT[2:0]		TARGET[3:0]				

Table 122. Command Code

## 2. R/W flag

R/W flag	Command
0	READ
1	WRITE

Table 123. R/W flag

## 3. BCNT[2:0] bits

Data length is set by BCNT[2:0] bits. Data length is “BCNT[2:0] bits +1”.

BCNT[2:0] bits	Data Length [byte]
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8

Table 124. Data Length Setting

## 4. TARGET[3:0] bits

Access the accessing register map.

TARGET[3:0] bits	Access Area
0x1	CTREG SRAM page
0x4	PRAM
0x5	CRAM
0x6	ACCRAM
0x7	OFREG
Others	N/A

Table 125. Accessing Register Map Setting (N/A: Not available)

Note 107. The setting of TARGET[3:0] bits = “0x0” and “0xF” are not assigned intentionally in order to prevent the wrong operation.

## 5. Command Code

Command Code	R/W flag	BCNT[2:0]	Target[3:0]	Effective Address Area
0x01	0: Read	0 (1 byte)	0	0x0000~0x01FF (511d) (CTREG)
0x81	1: Write			
0x-1	0: Read	Target Size	0	0x0200~0x03FF (1023d) (SRAM Page)
0x-1	1: Write			
0x44	0: Read	4 (5 byte)	4	0x0000~0x17FF (6143d) (PRAM)
0xC4	1: Write			
0x25	0: Read	2 (3 byte)	5	0x0000~0x0BFF (3071d) (CRAM)
0xA5	1: Write			
0x26	0: Read	2 (3 byte)	6	0x0000~0x07FF (2047d) (ACCRAM)
0xA6	1: Write			
0x17	0: Read	1 (2 byte)	7	0x0000~0x001F (31d) (OFREG)
0x97	1: Write			

Table 126. Command Code List

## 6. Address

The data length is fixed to 2-byte. All address descriptions are in big endian.

## 7. Address Transfer

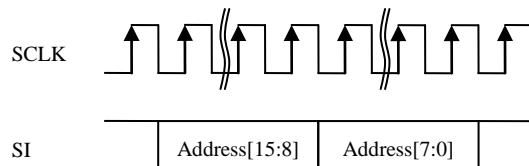


Figure 71. Address Transfer

## 8. Data

### Write/Read Data

The data is in LSB justified in PRAM 5-byte accessing (0000b, PRAM[35:0]).

The data is in MSB justified in CRAM 3-byte accessing (CRAM[19:0], 0000b).

The data is in LSB justified in OFREG 2-byte accessing. (0b, OFREG[14:0])

Data length is assigned by command code. Continuous read/write operation is available by automatic address increment.

## 9. Data Transfer

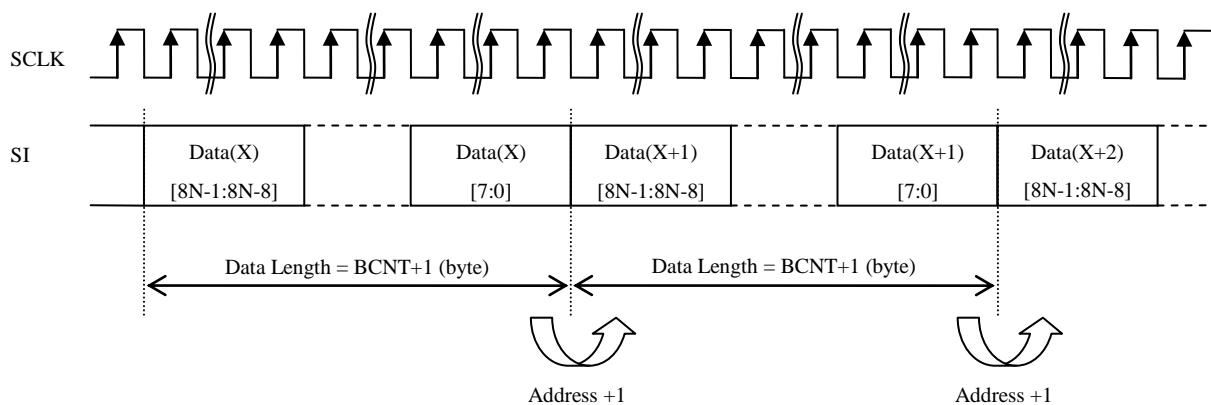


Figure 72. Data Transfer

## ■ SO pin Configuration

SOCFG bit controls the SO output (Hi-z or Low) when there is no output data.

SOCFG bit	SO pin Configuration	
0	L	(default)
1	Hi-z	

Table 127. SO Pin Configuration

## ■ I<sup>2</sup>C bus Interface (CIF1 pin = “L”, CIF0 pin = “H”)

The AK4961 can be controlled by I<sup>2</sup>C bus Interface when the CIF1 pin = “L” and the CIF0 pin = “H”. The format of I<sup>2</sup>C bus supports Fast Mode (max. 400kHz) and Fast Mode Plus (max. 1MHz). It can be set by the I2CFIL pin. The AK4961 does not support HS mode (max. 3.4MHz).

I2CFIL pin	I <sup>2</sup> C bus Mode	
L	Fast Mode	(default)
H	Fast Mode Plus	

Table 128. I<sup>2</sup>C bus Mode Setting

### 1. Data Transfer

In order to access any IC devices on the I<sup>2</sup>C BUS, input a start condition first, followed by a single Slave address which includes the Device Address. IC devices on the BUS compare this Slave address with their own addresses and the IC device which has an identical address with the Slave-address generates an acknowledgement. An IC device with the identical address then executes either a read or write operation. After the command execution, input a Stop condition.

#### 1-1. Data Change

Change the data on the SDA line while SCL line is “L”. SDA line condition must be stable and fixed while the clock is “H”. Change the Data line condition between “H” and “L” only when the clock signal on the SCL line is “L”. Change the SDA line condition while SCL line is “H” only when the start condition or stop condition is input.

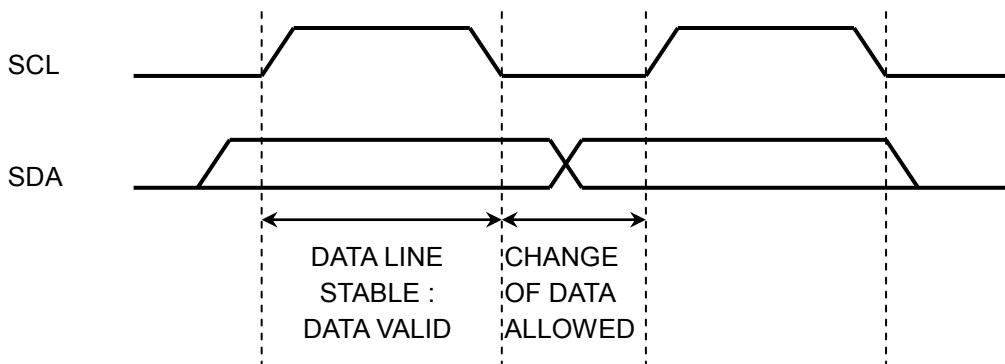


Figure 73. Data Change

## 1-2. Start Condition and Stop Condition

A Start condition is generated by the transition of “H” to “L” on the SDA line while the SCL line is “H”. All instructions are initiated by the Start condition. A Stop condition is generated by the transition of “L” to “H” on SDA line while SCL line is “H”. All instructions end by the Stop condition.

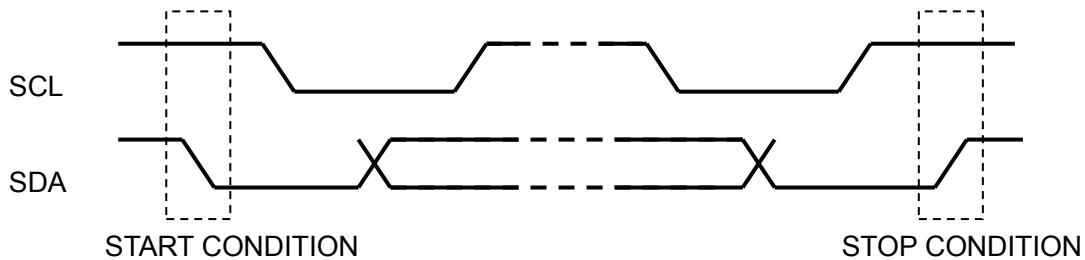


Figure 74. Start Condition and Stop Condition

## 1-3. Repeated Start Condition

When a Start condition is received again instead of a Stop condition, the bus changes to Repeated Start condition. Repeated Start condition is functionally the same as Start condition.

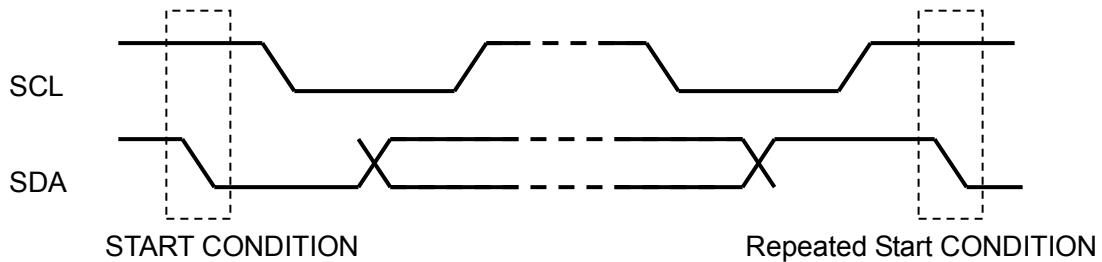


Figure 75. Repeated Start Condition

## 1-4. Acknowledge

An external device that is sending data to the AK4961 releases the SDA line (“H”) after receiving one-byte of data. An external device that receives data from the AK4961 then sets the SDA line to “L” at the next clock. This operation is called “acknowledgement”, and it enables verification that the data transfer has been properly executed. The AK4961 generates an acknowledgement upon receipt of Start condition and Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK4961 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the Master side generates an acknowledgement without sending Stop condition, the AK4961 outputs data at the next address location. When no acknowledgement is generated, the AK4961 ends data output (not acknowledged).

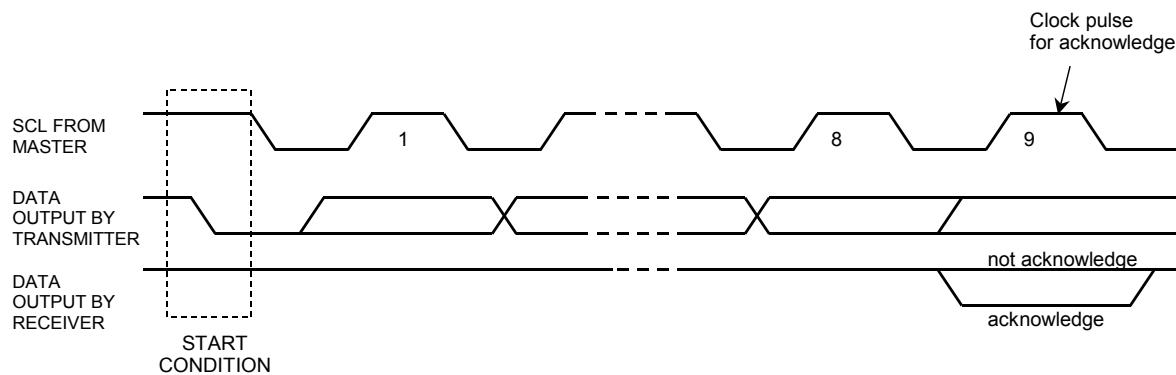


Figure 76. Generation of Acknowledge

### 1-5. The First Byte

The First Byte which includes the Slave-address is input after a Start condition is set, and a target IC device that will be accessed on the bus is selected by the Slave-address. The Slave-address is configured with the upper 7-bits. Data of the upper 6-bits is “001001”. The next 1 bit is address bits that select the desired IC which are set by the CAD pin. When the Slave-address is inputted, an external device that has the identical device address generates an acknowledgement and instructions are then executed. The 8<sup>th</sup> bit of the First Byte (lowest bit) is allocated as the R/W Bit. When the R/W Bit is “1”, the read instruction is executed, and when it is “0”, the write instruction is executed.

0	0	1	0	0	1	CAD	R/W
(CAD is set by pin)							

Figure 77. First Byte Configuration

Note 108. In this document, there is a case that describes a “Write Slave-address assignment” when both address bits match and a Slave-address at R/W Bit = “0” is received. There is a case that describes “Read Slave-address assignment” when both address bits matches and a Slave-address at R/W Bit = “1” is received.

### 1-6. The Second and Succeeding Bytes

The data format of the second and succeeding bytes of the AK4961 Transfer / Receive Serial data (command code, address and data in microcontroller interface format) on the I2C BUS are all configured with a multiple of 8-bits. When transferring or receiving those data on the I2C BUS, they are divided into an 8-bit data stream segment and they are transferred / received with the MSB side data first with an acknowledgement in-between.

Example:

When transferring / receiving A1B2C3 (hex) 24-bit serial data in microprocessor interface format:

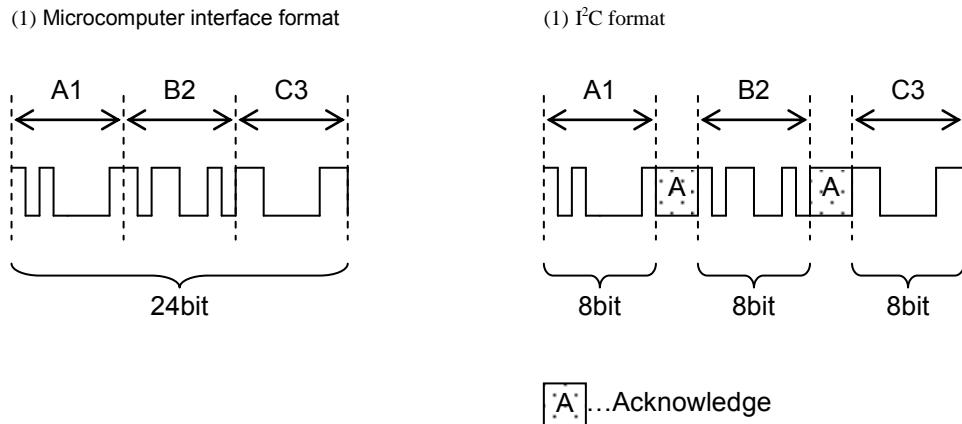


Figure 78. Division of Data

Note 109. In this document, there is a case that describes a write instruction command code which is received at the second byte as “Write Command”. There is a case that describes a read instruction command code which is received at the second byte as “Read Command”.

## 2. Write Sequence

In the AK4961, when a “Write-Slave-address assignment” is received at the first byte, the write command at the second byte and data at the third and succeeding bytes are received. At the data block, address and write data are received in a single-byte unit each in accordance with a command code. The number of write data bytes (Figure 79) is fixed by the received command code. Write command list in Write Sequence is shown in Table 126.

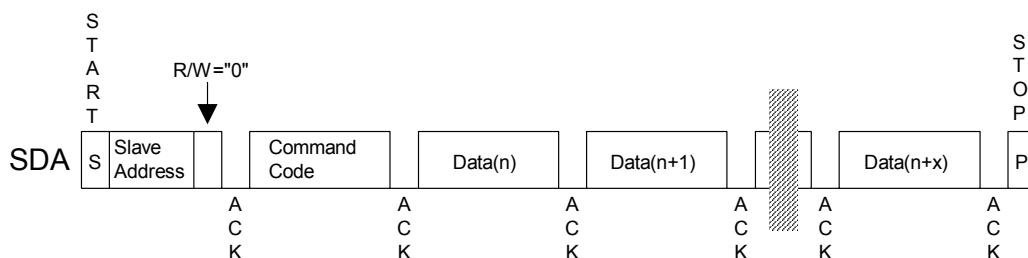


Figure 79. Write Sequence

## 7. Read Sequence

In the AK4961, when a “write- slave-address assignment” is received at the first byte, the read command at the second byte and the data at the third and succeeding bytes are received. At the data block, the address is received in a single byte unit in accordance with a read command code. In a command code without address assignment, the sequence does not have to be repeated ([Figure 80](#)).

When the last address byte (or command code if no address assignment is specified) is received and an acknowledgement is transferred, the read command waits for the next restart condition. When a “read slave-address assignment” is received at the first byte, data is transferred at the second and succeeding bytes. The number of readable data bytes ([Table 126](#)) is fixed by the received read command.

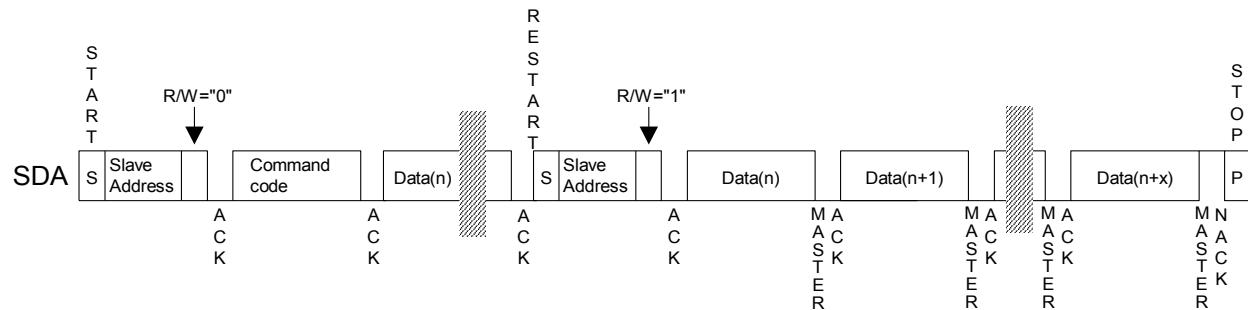


Figure 80. Read Sequence

#### 4. Acknowledgement Polling

The AK4961 cannot receive instructions while internal RDY signal (Data Write Ready) is at a low level. The maximum transition time of internal RDY signal from low level to high level is specified in [Figure 81](#), but it is possible to confirm in a faster cycle that internal RDY signal has become high by checking the AK4961 internal condition, which is made by verifying the acknowledgement.

##### 4-1. Generation of “Not Acknowledged”

The AK4961 does not accept command codes until internal RDY signal is high level, when a command is received to set the RDY pin to a low level. In order to confirm internal RDY signal condition, a “Write Slave-Address assignment” should be sent after the Start condition. If internal RDY signal is then at a low level, “Acknowledgement” is not generated at the succeeding clock (generation of “Not Acknowledged”). After sending “Not Acknowledged”, The BUS is released and all receiving data are ignored until the next start condition (behaves as if it received Slave address of other device).

Refer to item (2) of “[Figure 81](#) Internal RDY Signal Condition and Acknowledgement”.

##### 4-2. Internal RDY Signal condition after receiving Slave-address

Internal RDY signal condition is valid only when a Slave-address is received. If a Slave-address is received, internal circuit operates normally and a proper acknowledgement is generated even if internal RDY signal is forced low by the received command code instruction in the second byte.

For example, when data succeeding the command code is received while internal RDY signal is at low level (caused by external write condition), a proper acknowledgement is generated.

Refer to item (1) in “[Figure 81](#) Internal RDY Signal Condition and Acknowledgement”.

#### 4-3. Confirmation of internal RDY signal to be high level

If internal RDY signal changes to high just before receiving a Slave-address, an acknowledgement is generated after the receipt of the “Write-Slave-Address assignment”.

Note 110. “Not Acknowledged” is generated when internal RDY signal changes to high in the middle of receiving a “Write-Slave-Address assignment”.

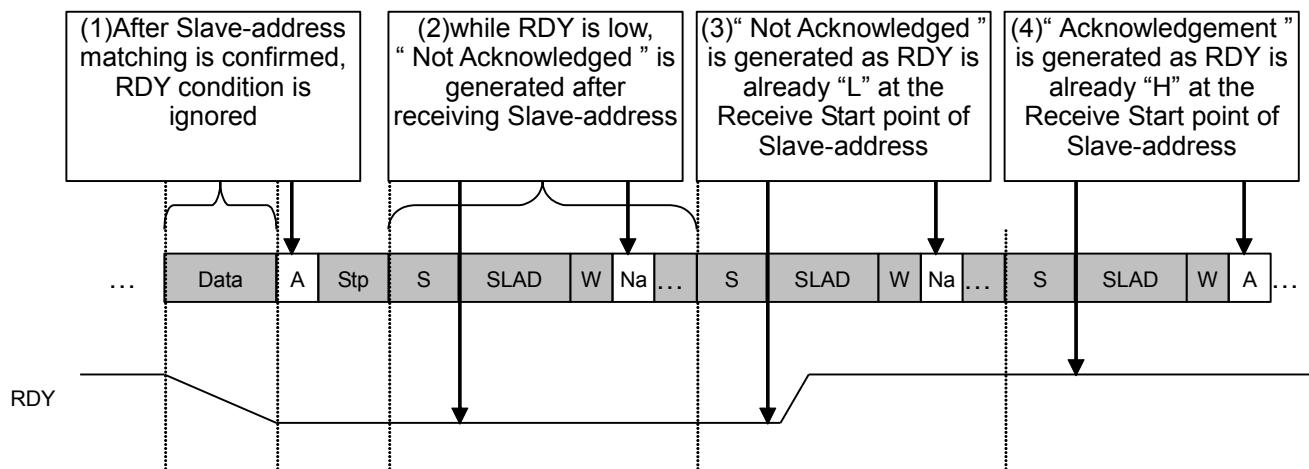


Figure 81. Internal RDY Signal Condition and Acknowledgement

#### 4-4. When Read Slave-address assignment is received without Read command code

Data read in the AK4961 can be made only in the previously documented Read sequence. Data cannot be read out without receiving a read command code. In the AK4961, a “Not Acknowledged” is generated when a “Read Slave-address Assignment” without proper receipt of read command is received. Under this condition, which occurs when internal RDY signal shifts from low level to high level after a “Write Slave-address assignment” in the read sequence and before a “Read Slave-address assignment”, “Not Acknowledged” is generated in return ([Note 111](#)).

Note 111. This condition may be avoided by assigning a read Slave-address only when the acknowledgement is confirmed, by utilizing the acknowledge-polling feature.

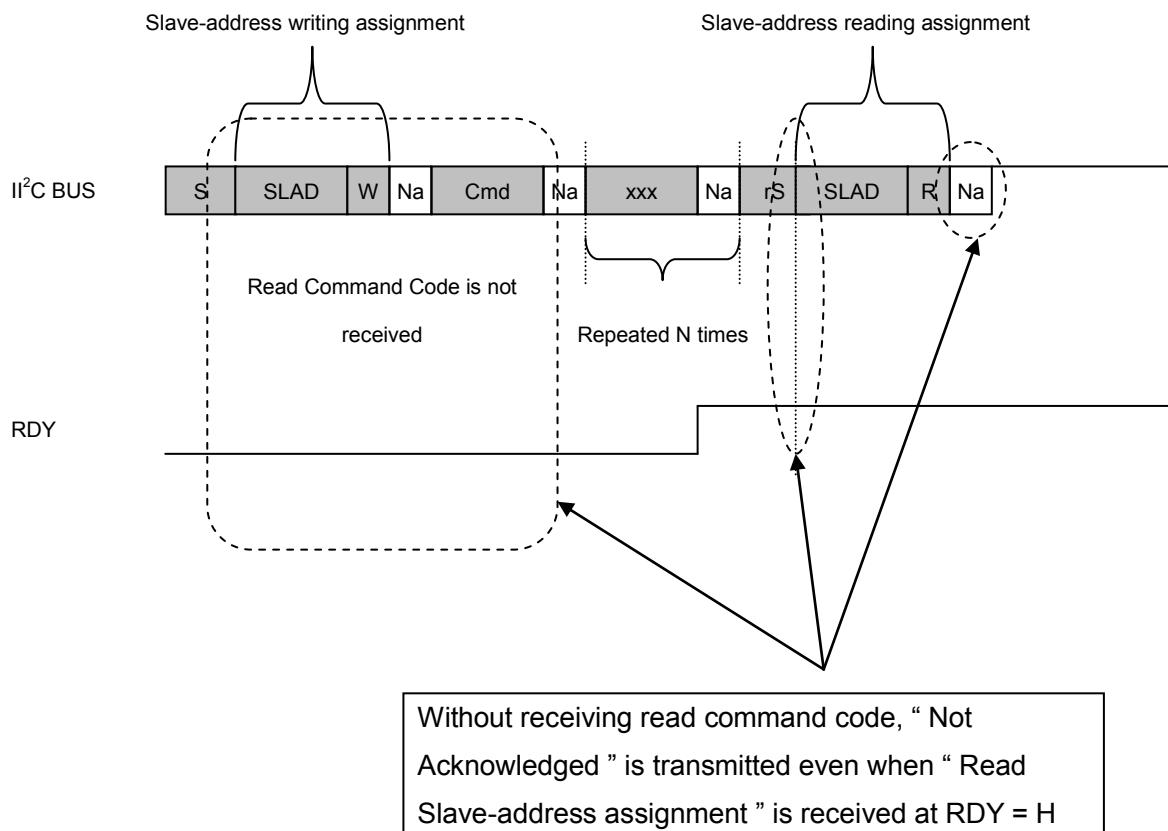


Figure 82. Read Slave-Address Assignment Without Receiving Read Command Code

## Limitation in use of I<sup>2</sup>C Interface

The I<sup>2</sup>C Interface does not support the following features.

- (1) No operation in Hs mode (max = 3.4 MHz)  
(Supports Fast Mode (max = 400 kHz), Fast Mode Plus (max. 1MHz))
- (2) Echo-Back function in Microcontroller Interface format.

Note 112. Do not turn off the power of the AK4961 during the power supplies of surrounding devices are turned on. TVDD1 must not exceed the pull-up of SDA and SCL of I2C BUS. (The diode exists for TVDD1 in the SDA and SCL pins.)

Note: The meaning of symbols in I<sup>2</sup>C format figures.

SLAD	...Slave Address (7 bits)
Cmd	...Command Code (8 bits)
S	...Start Condition
rS	...Repeated Start Condition
Stp	...Stop Condition
W	...R / W bit, the lowest bit of the first byte is at write (= 0) condition, Write ( 1 bit )
R	...R / W bit, the lowest bit of the first byte is at read (= 1) condition, Read ( 1 bit )
A	...Acknowledge (1 bit)
Na	...Not Acknowledge (1 bit)
(Gray)	(Gray) where it is controlled by Master device.
(White)	...(White) where it is controlled by Slave device. It is done by the AK4961.

## ■ Simple Write Error Check

The AK4961 has a cyclic redundancy check (CRC) function for a simple checking of writing data for RAM and registers in SPI interface mode.

### <Simple Write Error Check Sequence>

#### 1. In case of registers

- (1) Write serial data to be checked.
- (2) Readout a CRC result (CRCO[15:0] bits)
- (3) Check the result by a microcontroller.
- (4) Repeat the sequence from (1) to (3) when checking other serial data.

#### 2. In case of RAM

- (1) Set DLRDY bit to “1”
- (2) Write serial data to be checked.
- (3) Readout a CRC result (CRCO[15:0] bits)
- (4) Check the result by a microcontroller.
- (5) Repeat the sequence from (2) to (5) when checking other serial data.
- (6) Set DLRDY bit to “0”

Note 113. The internal CRC result is not updated by a Read command.

## ■ PRAM Access Sequence

Set PRIF bit to “1” before transmitting the data to PRAM. PRIF bit automatically returns to “0” after transmitting the data to PRAM.

## ■ RAM Write Timing during RUN State

These operations below are to rewrite the Coefficient RAM (CRAM) and Offset REG (OFREG) during RUN state. Data writing is executed in two steps; write preparation and write execution. The written data can be confirmed by reading the write preparation data.

### 1. Write Preparation

Input the number of data to RNUM[3:0] bits.

Input the starting address of write to RADR[15:0] bits.

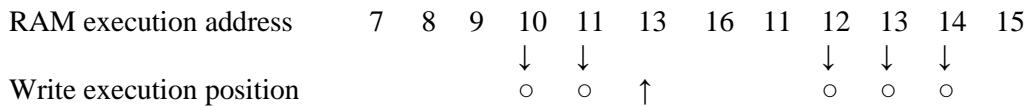
Assign the write data to the register from RBUFO[23:0] to RBUFF[23:0] bits as needed starting with RBUFO bit.

RBN, RADR and RBUFO to RBUFF bits are readable.

### 2. Write Execution

Upon completion of write preparation, execute a RAM write during RUN state by inputting “1” to write execution command RUNC (CRAM) and RUNO (OFREG) bits. RUNC and RUNO bits return to “0” automatically. Access operation by a microcontroller is prohibited until RDY changes to “H”.

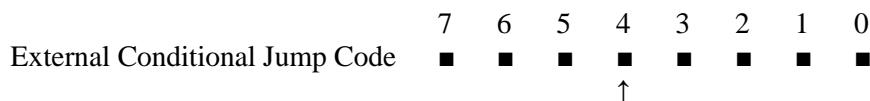
Write modification of the RAM content is executed whenever the RAM address for modification is assigned. For example, when 5 Data are written, from RAM address “10”, it is executed as shown below.



Note 114. Address “13” is not executed until rewriting address “12”.

## ■ External Conditional Jump

An External Conditional Jump code can be input during either DSP Reset or RUN state. Input data is set to the designated register on the rising edge of SYNC. When any single bit of “1” data in the 8-bit External Jump code matches a “1” bit data in the IFCON field, a Jump instruction is executed. IFCON field is the area where the external conditions are written. This Jump code is reset to 00h by setting the PDN pin to “L”, but it is not reset by DSP Reset.



Check if “1” of IFCON field corresponds with External Condition Jump Code including Jump pins by at least one at the same location.

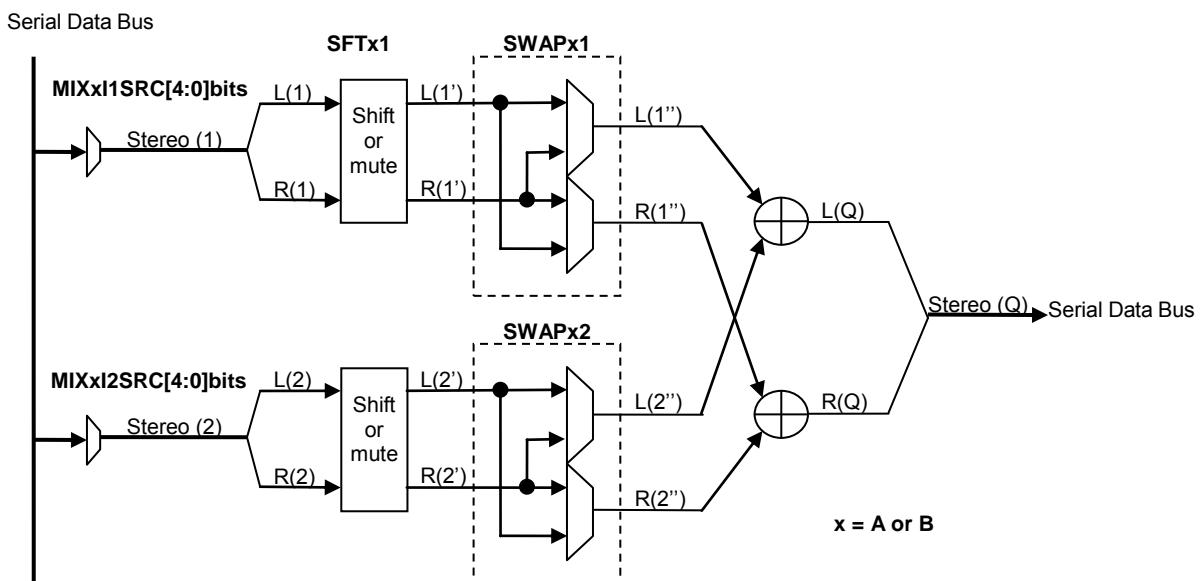


## ■ Mixer

The AK4961 has two stereo input mixers that have level adjustment function for overflow protection after adding and data change function (Mixer A and Mixer B). Level adjustment is processed by shift operation. Since the level adjustment function is only for avoiding overflow by adding, it can only shift 1bit to the right.

SFTA1 bit and SFTA2 bit control the two inputs of the Mixer A.

SFTB1 bit and SFTB2 bit control the two inputs of the Mixer B.



### 1. Level Adjustment Function

SFTxy[1:0] bits (x=A or B, y=1 or 2)	Shift Amount	L(y')	R(y')	Comment
0x0	No Shift	L(y)	R(y)	0dB
0x1	1 bit Right Shift	L(y) >> 1	R(y) >> 1	-6dB (x 1/2)
0x2-3	Mute	0	0	-∞dB

Table 129. SFTxy[1:0] bits

### 2. Data Change Function

SWAPxy[1:0] bits (x=A or B, y=1 or 2)	L(y'')	R(y'')	Comment
0x0	L(y')	R(y')	Through
0x1	L(y')	L(y')	Lin → Lout=Rout
0x2	R(y')	R(y')	Rin → Lout=Rout
0x3	R(y')	L(y')	Swap Signal Lin → Rout Rin → Lout

Table 130. SWAPxy[1:0] bits

## ■ DSP Setting

DSP power control can be set by DSPRSTN bit.

DSPRSTN bit	DSP State	
0	Power-down	(default)
1	Power-up	

Table 131. DSP Power Control

BANK[3:0] bits: Setting of DLRAM Mode

BANK[3:0] bits	Bank0	Bank1	Bank2
	Ring	Linear	$\mu$ -law
0x0	20480	0	0
0x1	18432	2048	0
0x2	16384	4096	0
0x3	14336	6144	0
0x4	12288	8192	0
0x5	10240	10240	0
0x6	8192	12288	0
0x7	6144	14336	0
0x8	4096	16384	0
0x9	2048	18432	0
0xA	0	20480	0
0xB	12288	0	N/A
0xC	8192	4096	N/A
0xD	6144	6144	N/A
0xE	4096	8192	N/A
0xF	0	12288	N/A

(default)

Table 132. Setting of Delay RAM BANK (N/A: Not available)

POMODE bit: DLYRAM Pointer 0 Select

0: OFREG

1: DBUS Immediate Data (default)

DRAM bit: DATA RAM Size Setting

DRAM Mode	DRMS[1:0] bits	DSP Data RAM	
		Bank1	Bank0
0	00b	512	1536
1	01b	1024	1024
2	10b	1536	512
others	others	N/A	

(default)

Table 133. DATA RAM Size Setting (N/A: Not available)

## DRAD bit: Addressing Mode Setting

Addressing mode	DRAD bits	DSP Data RAM	
		Bank1 DP1	Bnak0 DP0
0	00	Ring	Ring
1	01	Ring	Liner
2	10	Linear	Ring
3	11	Linear	Linear

(default)

Table 134. Addressing Mode Setting

## WAVP[1:0] bits: CRAM Memory Assignment of DSP

WAVP Mode	WAVP1 bit	WAVP0 bit	CRAM Memory Assignment	FFT Point
0	0	0	33word	128
1	0	1	65word	256
2	1	0	129word	512
3	1	1	257word	1024

(default)

Table 135. CRAM Memory Assignment of DSP

## ■ Bit Assignment for MIR register

Serial data (MIR register) of DSP programm output can be readout from the control interface. Bit assignment of the serial data is shown below.

MIRx[31:0] bits	Assignment
D[31:12]	20-bit Real Part Data
D[11:8]	N/A
D[7:4]	4-bit Exponent Part Data
D[3:0]	Available Flag

Table 136. Bit Assignment of MIR Register (N/A: Not Available)

## ■ Control Register Setting

All registers are initialized after releasing power down mode (PDN pin = “L”). To ensure control register settings, this system reset must always be executed when powering up the AK4961. Control register settings should be made during DSP reset (DSPRSTN bit = “0”).

## ■ Virtual Address Space of SRAM

On SLIMbus connection, USER defined address space of value element of a Generic Devices has only 1024 addresses. Accessing to RAM (such as SRAM) is made by expanding the address space virtually with VAT and Page control registers.

## ■ Virtual Access Target

VAT[3:0] bits	Access Area	
0x0	N/A	(default)
0x4	PRAM	
0x5	CRAM	
0x6	ACCRAM	
0x7	OFREG	
Others	N/A	

Table 137. Virtual Access Target Setting (N/A: Not available)

## ■ Page Setting

RAM control register area can be set in SLIMbus mode as shown below. RAMPAGE bit must be set to “0” in SPI or I<sup>2</sup>C mode.

RAMPAGE bit	RAM Register Area	
0	0xA00 ~ 0xAF	(default)
1	0xB00 ~ 0xBFF	

Table 138. RAM Control Register Area Setting

The address assigned by SPI is defined as A<sub>spi</sub>; the target address in SRAM that is defined as A<sub>sram</sub> can be described as below.

A <sub>sram</sub> [15:13]	A <sub>sram</sub> [12:8]	A <sub>sram</sub> [7:0]
000b	Page[4:0]	A <sub>spi</sub> [7:0]

Table 139. SRAM Address Space Expanding Setting

When accessing to control register area A<sub>spi</sub>=Address=0x0200 to 0x02FF (“0xA00 ~ 0xAF”/ “0xB00 ~ 0xBFF” on SLIMbus), SRAM address A<sub>sram</sub> assigned by VAT[3:0] bits is also accessed.

## ■ Register Map

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	SW REG		
0000	Flow Control 1	PSW4N	PSW3N	PSW2N	PSW1N	0	SOCFG	SWRSTN	PMSW	-		
0001	Flow Control 2	0	0	0	0	0	0	0	DLRDY	Y		
0002	Flow Control 3	0	0	0	0	0	0	0	DSPRSTN	Y		
0003	Power Management 1	0	0	0	PMOSC	0	0	PMPLL2	PMPLL1	-		
0004	Power Management 2	0	0	0	PMAIF (Note 115)	PMSRCD	PMSRCC	PMSRCB	PMSRCA	Y		
0005	Power Management 3	PMLDO3N	PMLDO3P	0	PMLDO1	0	PMCP3	PMCP2	PMCP1	-		
0006	Power Management 4	0	0	0	0	PMMP2	PMMP1C	PMMP1B	PMMP1A	-		
0007	Power Management 5	0	0	PMAIN6	PMAIN5	PMAIN4	PMAIN3	PMAIN2	PMAIN1	-		
0008	Power Management 6	0	0	0	0	PMAD2V	PMAD2M	PMAD1R	PMAD1L	-		
0009	Power Management 7	0	0	0	0	0	0	0	0	-		
000A	Power Management 8	PMSRCE	0	0	0	0	PMDA2	0	PMDA1	-		
000B	Power Management 9	0	0	PMLO1R	PMLO1L	0	0	PMHPR	PMHPL	-		
000C	Power Management 10	PMRCV	0	PMLO2RN	PMLO2RP	0	0	PMLO2LN	PMLO2LP	-		
000D	Lineout2 Setting	0	0	0	0	0	0	0	LO2DIF	-		
000E	Output Setting Mode	0	0	0	0	0	0	HPRHZ	HPLHZ	-		
000F	MIC Power Level	0	0	0	0	MICL2[1:0]		MICL1[1:0]		-		
0010	MIC-Amp 1 Lch Gain	0	0	0	0	MG1L[3:0]						
0011	MIC-Amp 1 Rch Gain	0	0	0	0	MG1R[3:0]						
0012	MIC-Amp 2 Gain	0	0	0	0	MG2M[3:0]						
0013	MIC-Amp 3 Gain	0	0	0	0	MG2V[3:0]						
0014	Reserved	0	0	0	0	0	0	0	0	-		
0015	Reserved	0	0	0	0	0	0	0	0	-		
0016	Charge Pump 1 Setting 1	0	0	0	0	0	0	CKSELCP1[1:0]		-		
0017	Reserved	0	0	0	0	0	0	0	0	-		
0018	Reserved	0	0	0	0	0	0	0	0	-		
0019	Reserved	0	0	0	0	0	0	0	0	-		
001A	Clock Mode Select	IBIAS	CM[1:0]		FS[4:0]					-		
001B	Digital Filter Select 1	DA1SD	DA1SL	AD1SD[1:0]		DFTHR1	HPFC1[1:0]		HPFAD1N	-		
001C	Digital Filter Select 2	0	0	AD2SD[1:0]		DFTHR2	HPFC2[1:0]		HPFAD2N	-		
001D	Test Register 1	TEST	0	0	0	0	0	0	0	-		
001E	Digital MIC 1	0	0	PMMDM1R	PMMDM1L	DCLKE1	0	DCLKP1	DMIC1	-		
001F	Digital MIC 2	0	0	PMMDM2R	PMMDM2L	DCLKE2	0	DCLKP2	DMIC2	-		
0020	DAC1 Mono Mixing	INV1R	MDAC1R	RDAC1R	LDAC1R	INV1L	MDAC1L	RDAC1L	LDAC1L	-		
0021	DAC2 Mono Mixing	INV2R	MDAC2R	RDAC2R	LDAC2R	INV2L	MDAC2L	RDAC2L	LDAC2L	-		
0022	Output Volume Setting	0	0	0	0	0	0	OVOLC2N	OVOLC1N	-		
0023	Charge Pump 2 Setting 1	0	LVDTM[2:0]				CPMODE[1:0]					
0024	Charge Pump 2 Setting 2	0	0	VDDTM[3:0]				0	0	-		
0025	Reserved	0	0	0	0	0	0	0	0	-		
0026	Mode Control	DSMLP2	DSMLP1	0	0	0	0	ADRST[1:0]		-		
0027	Reserved	0	0	0	0	0	0	0	0	-		
0028	Reserved	0	0	0	0	0	0	0	0	-		
0029	Reserved	0	0	0	0	0	0	0	0	-		
002A	Reserved	0	0	1	1	0	0	0	0	-		
002B	Reserved	0	0	0	0	0	0	0	0	-		
002C	Jitter Cleaner Setting 1	0	CM2[1:0]		FS2[4:0]							
002D	Jitter Cleaner Setting 2	DIV	0	SRCESD	SRCESL	SMT[1:0]		SAUTOE	SMUTEE	-		
002E	Jitter Cleaner Setting 3	XCKCPSEL	XCKSEL	SRCO8FS	DITHERE	0	SELDAA2IN	SELDAA1IN	SELSRCIN	-		

Note 115. PMAIF bit is available even if PMSW bit is "0".

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	SW REG
002F	Detection Event Reset	0	0	0	0	0	0	0	CLR	-
0030	Event Mask Setting	0	0	0	0	0	0	MJDE	MRCE	-
0031	Detection Power Management	PMDTE	PMRCB	0	0	MDMODE	MDDIF	DTINTN	CMPL	-
0032	Detection Setting 1	0	0	CMPWT[1:0]		MPWT[2:0]		JDT		-
0033	Detection Setting 2	0	0	0	0	0	CMPRST	AVG[1:0]		-
0034	MIC Input Selector 1	0		INS1R[2:0]		0		INS1L[2:0]		-
0035	MIC Input Selector 2	0		INS2V[2:0]		0		INS2M[2:0]		-
0036	Lch Output Volume 1	0	0	0		OVL1[4:0]				-
0037	Rch Output Volume 1	0	0	0		OVR1[4:0]				-
0038	Lch Output Volume 2	0	0	0		OVL2[4:0]				-
0039	Rch Output Volume 2	0	0	0		OVR2[4:0]				-
003A	HP Volume Control		HPTM[2:0]			HP1G[4:0]				-
003B	Lineout1 Volume Control	0	0	0	0	0		LO1G[2:0]		-
003C	Lineout2 Volume Control	0		LO2G[2:0]		0		RCVG[2:0]		-
003D	Reserved	0	0	0	0	0	0	0	0	-
003E	PLL1 CLK Source Select	0	0	0		PLS1[4:0]				-
003F	PLL1 Ref CLK Divider 1			PLD1[15:8]						-
0040	PLL1 Ref CLK Divider 2			PLD1[7:0]						-
0041	PLL1 FB CLK Divider 1			PLM1[15:8]						-
0042	PLL1 FB CLK Divider 2			PLM1[7:0]						-
0043	PLL2 CLK Source Select	0	0	0		PLS2[4:0]				-
0044	PLL2 Ref CLK Divider 1			PLD2[15:8]						-
0045	PLL2 Ref CLK Divider 2			PLD2[7:0]						-
0046	PLL2 FB CLK Divider 1			PLM2[15:8]						-
0047	PLL2 FB CLK Divider 2			PLM2[7:0]						-
0048	MCLK1 Source Select	0	0	MSN1		CKS1[4:0]				-
0049	MBCLK1 Divider				BDV1[7:0]					-
004A	MSYNC1 Divider				SDV1[7:0]					-
004B	MCLK2 Source Select	0	0	MSN2		CKS2[4:0]				-
004C	MBCLK2 Divider				BDV2[7:0]					-
004D	MSYNC2 Divider				SDV2[7:0]					-
004E	MCLK3 Source Select	0	0	MSN3		CKS3[4:0]				-
004F	MBCLK3 Divider				BDV3[7:0]					-
0050	MSYNC3 Divider				SDV3[7:0]					-
0051	MCLK4 Source Select	0	0	MSN4		CKS4[4:0]				-
0052	MBCLK4 Divider				BDV4[7:0]					-
0053	MSYNC4 Divider				SDV4[7:0]					-
0054	MCLK5 Source Select	0	0	1		CKS5[4:0]				-
0055	MBCLK5 Divider				BDV5[7:0]					-
0056	MSYNC5 Divider				SDV5[7:0]					-
0057	MCLK6 Source Select	0	0	1		CKS6[4:0]				-
0058	MBCLK6 Divider				BDV6[7:0]					-
0059	MSYNC6 Divider				SDV6[7:0]					-
005A	MCLK7 Source Select	0	0	1		CKS7[4:0]				-
005B	MBCLK7 Divider				BDV7[7:0]					-
005C	MSYNC7 Divider				SDV7[7:0]					-
005D ~ 0061	Reserved	0	0	0	0	0	0	0	0	-
0062	MCKO Source Select	0	0	0		MCKS1[4:0]				-
0063	MCKO Divider				MDIV1[7:0]					-
0064	CODEC CLK Source Select	0	0	0		MCKS2[4:0]				-
0065	CODEC CLK Divider				MDIV2[7:0]					-
0066	DSP MCLK Source Select	0	0	0		CKSD[4:0]				-
0067	BUS CLK Divider				MDIVD[7:0]					-

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	SW REG
0068	AIN1/2 Sync Domain Setting	0		SDAIF1[2:0]		0		SDAIF2[2:0]		-
0069	AIN3/4 Sync Domain Setting	0		SDAIF3[2:0]		0		SDAIF4[2:0]		-
006A	ADC Sync Domain Setting	0	0	0	0	0		SDCDC[2:0]		-
006B	SB1/2 Sync Domain Setting	0		SDSB1[2:0]		0		SDSB2[2:0]		-
006C	SB3/DSPO Sync Domain Setting	0		SDSB3[2:0]		0		SDDSP[2:0]		-
006D	DSPO2/4 Sync Domain Setting	0		SDDSP02[2:0]		0		SDDSP04[2:0]		-
006E	SRCA/B Sync Domain Setting	0		SDSRCAO[2:0]		0		SDSRCBO[2:0]		Y
006F	SRCC/D Sync Domain Setting	0		SDSRC CO[2:0]		0		SDSRCDO[2:0]		Y
0070	Reserved	0	0	0	0	0	0	0	0	-
0071	Reserved	0	0	0	0	0	0	0	0	-
0072	SDTO1A Source Select	0	0	0			SDTO1ASRC[4:0]			-
0073	SDTO1B Source Select	0	0	0			SDTO1BSRC[4:0]			-
0074	SDTO2 Source Select	0	0	0			SDTO2SRC[4:0]			-
0075	SDTO3 Source Select	0	0	0			SDTO3SRC[4:0]			-
0076	SDTO4 Source Select	0	0	0			SDTO4SRC[4:0]			-
0077	SBO1 Source Select	0	0	0			SBO1SRC[4:0]			-
0078	SBO2 Source Select	0	0	0			SBO2SRC[4:0]			-
0079	DAC1 Source Select	0	0	0			DAC1SRC[4:0]			-
007A	DAC2 Source Select	0	0	0			DAC2SRC[4:0]			-
007B	DSPI1 Source Select	0	0	0			DSPI1SRC[4:0]			-
007C	DSPI2 Source Select	0	0	0			DSPI2SRC[4:0]			-
007D	DSPI3 Source Select	0	0	0			DSPI3SRC[4:0]			-
007E	DSPI4 Source Select	0	0	0			DSPI4SRC[4:0]			-
007F	DSPI5 Source Select	0	0	0			DSPI5SRC[4:0]			-
0080	MIXAI1 Source Select	0	0	0			MIXAI1SRC[4:0]			-
0081	MIXAI2 Source Select	0	0	0			MIXAI2SRC[4:0]			-
0082	MIXBI1 Source Select	0	0	0			MIXBI1SRC[4:0]			-
0083	MIXBI2 Source Select	0	0	0			MIXBI2SRC[4:0]			-
0084	SRCA1 Source Select	0	0	0			SRCAISRC[4:0]			-
0085	SRCB1 Source Select	0	0	0			SRCBISRC[4:0]			-
0086	SRCC1 Source Select	0	0	0			SRCCISRC[4:0]			-
0087	SRCD1 Source Select	0	0	0			SRCDISRC[4:0]			-
0088	VAD Source Select	0	0	0			VADSRC[4:0]			-
0089	Reserved	0	0	0	0	0	0	0	0	-
008A	Reserved	0	0	0	0	0	0	0	0	-
008B	SDTIOA/B/C I/F Format	0	THR1	DIF1[1:0]	BCKP1		DLC1[2:0]			-
008C	SDTIO2 I/F Format	0	THR2	DIF2[1:0]	BCKP2		DLC2[2:0]			-
008D	SDTIO3 I/F Format	0	THR3	DIF3[1:0]	BCKP3		DLC3[2:0]			-
008E	SDTIO4 I/F Format	GPE1	THR4	DIF4[1:0]	BCKP4		DLC4[2:0]			-
008F	CODEC I/F Format	EXIF	THRC	0	0	BCKPC		DLCC[2:0]		-
0090	SRC Clock Setting	0	0	0	0	0	0	SRCLK[1:0]		Y
0091	SRC Mute Setting	SAUTOD	SAUTOC	SAUTOB	SAUTOA	SMUTED	SMUTEC	SMUTEB	SMUTEA	Y
0092	MIXA Setting		SFTA2[1:0]	SFTA1[1:0]		SWPA2[1:0]		SWPA1[1:0]		-
0093	MIXB Setting		SFTB2[1:0]	SFTB1[1:0]		SWPB2[1:0]		SWPB1[1:0]		-
0094	DSP Setting 1		DRMS[1:0]	DRAD[1:0]			BANK[3:0]			Y
0095	Reserved	0	0	0	0	0	0	0	0	Y
0096	DSP Setting 2	0	0	0	0	POMODE	0		WAVP[1:0]	Y
0097	DSP Setting 3	0	0	0	EDNOPDIS	0	0	0	0	Y
0098	DSP Setting 4				DSPCKADJ[7:0]					Y
0099	Virtual Address Control	0	0	0	RAMPAGE		VAT[3:0]			-
009A	Page Setting	0	0	0			PAGE[4:0]			-
009B	External Jump Condition				JX[7:0]					Y
009C	Run State Data Length	0	0	0	0		RNUM[3:0]			Y
009D	Run State Start Address 1				RADR[15:8]					Y
009E	Run State Start Address 2				RADR[7:0]					Y

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	SW REG
009F	Run State Data Setting 1				RBUFO[23:16]					Y
00A0	Run State Data Setting 2				RBUFO[15:8]					Y
00A1	Run State Data Setting 3				RBUFO[7:0]					Y
00A2	Run State Data Setting 4				RBUF1[23:16]					Y
00A3	Run State Data Setting 5				RBUF1[15:8]					Y
00A4	Run State Data Setting 6				RBUF1[7:0]					Y
00A5	Run State Data Setting 7				RBUF2[23:16]					Y
00A6	Run State Data Setting 8				RBUF2[15:8]					Y
00A7	Run State Data Setting 9				RBUF2[7:0]					Y
00A8	Run State Data Setting 10				RBUF3[23:16]					Y
00A9	Run State Data Setting 11				RBUF3[15:8]					Y
00AA	Run State Data Setting 12				RBUF3[7:0]					Y
00AB	Run State Data Setting 13				RBUF4[23:16]					Y
00AC	Run State Data Setting 14				RBUF4[15:8]					Y
00AD	Run State Data Setting 15				RBUF4[7:0]					Y
00AE	Run State Data Setting 16				RBUF5[23:16]					Y
00AF	Run State Data Setting 17				RBUF5[15:8]					Y
00B0	Run State Data Setting 18				RBUF5[7:0]					Y
00B1	Run State Data Setting 19				RBUF6[23:16]					Y
00B2	Run State Data Setting 20				RBUF6[15:8]					Y
00B3	Run State Data Setting 21				RBUF6[7:0]					Y
00B4	Run State Data Setting 22				RBUF7[23:16]					Y
00B5	Run State Data Setting 23				RBUF7[15:8]					Y
00B6	Run State Data Setting 24				RBUF7[7:0]					Y
00B7	Run State Data Setting 25				RBUF8[23:16]					Y
00B8	Run State Data Setting 26				RBUF8[15:8]					Y
00B9	Run State Data Setting 27				RBUF8[7:0]					Y
00BA	Run State Data Setting 28				RBUF9[23:16]					Y
00BB	Run State Data Setting 29				RBUF9[15:8]					Y
00BC	Run State Data Setting 30				RBUF9[7:0]					Y
00BD	Run State Data Setting 31				RBUFA[23:16]					Y
00BE	Run State Data Setting 32				RBUFA[15:8]					Y
00BF	Run State Data Setting 33				RBUFA[7:0]					Y
00C0	Run State Data Setting 34				RBUFB[23:16]					Y
00C1	Run State Data Setting 35				RBUFB[15:8]					Y
00C2	Run State Data Setting 36				RBUFB[7:0]					Y
00C3	Run State Data Setting 37				RBUFC[23:16]					Y
00C4	Run State Data Setting 38				RBUFC[15:8]					Y
00C5	Run State Data Setting 39				RBUFC[7:0]					Y
00C6	Run State Data Setting 40				RBUFD[23:16]					Y
00C7	Run State Data Setting 41				RBUFD[15:8]					Y
00C8	Run State Data Setting 42				RBUFD[7:0]					Y
00C9	Run State Data Setting 43				RBUFE[23:16]					Y
00CA	Run State Data Setting 44				RBUFE[15:8]					Y
00CB	Run State Data Setting 45				RBUFE[7:0]					Y
00CC	Run State Data Setting 46				RBUFF[23:16]					Y
00CD	Run State Data Setting 47				RBUFF[15:8]					Y
00CE	Run State Data Setting 48				RBUFF[7:0]					Y
00CF	CRAM Operation during Run State	0	0	0	0	0	0	0	RUNC	Y
00D0	OFFREG Operation during Run State	0	0	0	0	0	0	0	RUNO	Y
00D1	PRAM Ready	0	0	0	0	0	0	0	PRIF	Y
00D2	MIR Hold	0	0	0	0	0	0	0	MIRH	Y
00D3	CRC Result 1				CRCO[15:8]					-
00D4	CRC Result 2				CRCO[7:0]					-
00D5	Device Code				DEVICECODE[7:0]					-
00D6	Reserved	0	0	0	0	0	0	0	0	Y

Addr [Hex]	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	SW REG
00D7	Jack Detection Event	0	0	0	0	0	VWE	JDE	RCE	-
00D8	Jack Detection Status	MDTE	0	0	0	0	VDF	JDS	RCS	-
00D9	MIC Level Detection	0	0	0	0		CPL[3:0]			-
00DA	Test Register 2					TO[7:0]				-
00DB	SRC Status	0	0	0	0	SRCSTD	SRCSTC	SRCSTB	SRCSTA	Y
00DB	Reserved	0	0	0	0	0	0	0	0	Y
00DC	MIR1 Register 1					MIR1[31:24]				Y
00DD	MIR1 Register 2					MIR1[23:16]				Y
00DE	MIR1 Register 3					MIR1[15:8]				Y
00DF	MIR1 Register 4					MIR1[7:0]				Y
00E0	MIR2 Register 1					MIR2[31:24]				Y
00E1	MIR2 Register 2					MIR2[23:16]				Y
00E2	MIR2 Register 3					MIR2[15:8]				Y
00E3	MIR2 Register 4					MIR2[7:0]				Y
00E4	MIR3 Register 1					MIR3[31:24]				Y
00E5	MIR3 Register 2					MIR3[23:16]				Y
00E6	MIR3 Register 3					MIR3[15:8]				Y
00E7	MIR3 Register 4					MIR3[7:0]				Y
00E8	MIR4 Register 1					MIR4[31:24]				Y
00E9	MIR4 Register 2					MIR4[23:16]				Y
00EA	MIR4 Register 3					MIR4[15:8]				Y
00EB	MIR4 Register 4					MIR4[7:0]				Y
00EC	~ Reserved	0	0	0	0	0	0	0	0	-
00EF										
00F0	VAD Setting 1	0	0	0	FBYP	VADE	DLYE	AWE	DLE	-
00F1	VAD Setting 2					PT[7:0]				-
00F2	VAD Setting 3			TSW[3:0]		0		AT[2:0]		-
00F3	VAD Setting 4					ONGT[7:0]				-
00F4	VAD Setting 5					OFFGT[7:0]				-
00F5	VAD Setting 6	0	0	0			MINTH[12:8]			-
00F6	VAD Setting 7					MINTH[7:0]				-
00F7	VAD Setting 8		VDFS[1:0]		NVFS[1:0]			NLDTH[11:8]		-
00F8	VAD Setting 9					NLDTH[7:0]				-
00F9	VAD Setting 10	0		VLS[2:0]		0		VRS[2:0]		-
00FA	VAD HPF Setting 1					B0[15:8]				-
00FB	VAD HPF Setting 2					B0[7:0]				-
00FC	VAD HPF Setting 3					B1[15:8]				-
00FD	VAD HPF Setting 4					B1[7:0]				-
00FE	VAD HPF Setting 5					A1[15:8]				-
00FF	VAD HPF Setting 6					A1[7:0]				-
0100	CREG0 Setting 1					CREG0[7:0]				-
0101	CREG0 Setting 2					CREG0[15:8]				-
0102	CREG1 Setting 1					CREG1[7:0]				-
0103	CREG1 Setting 2					CREG1[15:8]				-
0104	CREG2 Setting					CREG2[7:0]				-
0105	CREG3 Setting					CREG3[7:0]				-
0106	CREG4 Setting					CREG4[7:0]				-
0107	CREG5 Setting					CREG5[7:0]				-
0108	CREG6 Setting					CREG6[7:0]				-
0109	CREG7 Setting					CREG7[7:0]				-

Note 116. PDN pin = "L" resets the registers to their default value.

Note 117. Shaded addresses are writable registers during RUN. "Y" described in SWREG column become valid by setting PMSW = PWRSTN bits to "1".

Note 118. The bits defined as "0" must contain a "0" value.

Note 119. The bits defined as "1" must contain a "1" value.

Note 120. Do not write to registers in the address after 010AH.

## ■ Register Definition

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0000	Flow Control 1	PSW4N	PSW3N	PSW2N	PSW1N	0	SOCFG	SWRSTN	PMSW
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMSW: Power Switch of DSP, SRCA/B/C/D and SRAM blocks

- 0: OFF (Hi-z) (default)
- 1: ON (1.2V Power Supply)

SWRSTN: Logic reset of DSP, SRCA/B/C/D and SRAM blocks

- 0: Reset (default)
- 1: Normal Operation

SOCFG: SO pin Configuration

- 0: "L" Output (default)
- 1: Hi-z

PSW4N/3N/2N/1N: Pull-down resistor Enable bit

- 0: Pull –down (typ. 50kΩ) ON (default)
- 1: Pull-down OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0001	Flow Control 2	0	0	0	0	0	0	0	DLRDY
	R/W	R	R	R	R	R	R	R	R/W
	Default	0	0	0	0	0	0	0	0

DLRDY: Down Load Ready

- 0: Download Inhibit (default)
- 1: Download Ready

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0002	Flow Control 3	0	0	0	0	0	0	0	DSPRSTN
	R/W	R	R	R	R	R	R	R	R/W
	Default	0	0	0	0	0	0	0	0

DSPRSTN: DSP Reset

- 0: DSP Reset (default)
- 1: DSP Normal Operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0003	Power Management 1	0	0	0	PMOSC	0	0	PMPLL2	PMPLL1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

**PMPLL1: PLL1 Power Management**

- 0: Power down (default)  
1: Power up

**PMPLL2: PLL2 Power Management**

- 0: Power down (default)  
1: Power up

**PMOSC: X'tal oscillator circuit Power Management**

- 0: Power down (default)  
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0004	Power Management 2	0	0	0	PMAIF	PMSRCD	PMSRCC	PMSRCB	PMSRCA
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

**PMSRCA/B/C/D: SRCA/B/C/D Power Management**

- 0: Power down (default)  
1: Power up

**PMAIF: Audio Interface Power Management**

- 0: Power down (default)  
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0005	Power Management 3	PMLDO3N	PMLDO3P	0	PMLDO1	0	PMCP3	PMCP2	PMCP1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMCP1: Charge Pump 1 Power Management

- 0: Power down (default)
- 1: Power up

PMCP2: Charge Pump 2 Power Management

- 0: Power down (default)
- 1: Power up

PMCP3: Charge Pump 3 Power Management

- 0: Power down (default)
- 1: Power up

PMLDO1: LDO1 Power Management

- 0: Power down (default)
  - 1: Power up
- \* LDO1 outputs VSS1 at Power-down state.

PMLDO3P: LDO3P Power Management

- 0: Power down (default)
- 1: Power up

PMLDO3N: LDO3N Power Management

- 0: Power down (default)
- 1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0006	Power Management 4	0	0	0	0	PMMP2	PMMP1C	PMMP1B	PMMP1A
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMMP2/1C/1B/1A: MPWR2/1C/1B/1A Power Management

- 0: Power down: Hi-Z (default)
- 1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0007	Power Management 5	0	0	PMAIN6	PMAIN5	PMAIN4	PMAIN3	PMAIN2	PMAIN1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMAIN1-6: AIN1-6 pins Input Circuit Power Management

- 0: Power down (default)
- 1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0008	Power Management 6	0	0	0	0	PMAD2V	PMAD2M	PMAD1R	PMAD1L
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMAD1L: MIC-Amp 1 Lch & ADC1 Lch Power Management

- 0: Power down (default)
- 1: Power up

PMAD1R: MIC-Amp 1 Rch & ADC1 Rch Power Management

- 0: Power down (default)
- 1: Power up

PMAD2M: MIC-Amp 2 & ADC2 Lch Power Management

- 0: Power down (default)
- 1: Power up

PMAD2V: MIC-Amp 3 & ADC2 Rch Power Management

- 0: Power down (default)
- 1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0009	Power Management 7	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000A	Power Management 8	PMSRCE	0	0	0	0	PMDA2	0	PMDA1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMDA1: DAC1 Power Management

- 0: Power down (default)
- 1: Power up

PMDA2: DAC2 Power Management

- 0: Power down (default)
- 1: Power up

PMSRCE: SRCE Power Management

- 0: Power down (default)
- 1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000B	Power Management 9	0	0	PMLO1R	PMLO1L	0	0	PMHPR	PMHPL
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMHPL/R: HP-Amp L/Rch Power Management

- 0: Power down (default)
- 1: Power up

PMLO1L/R: Line Out-Amp 1 L/Rch Power Management

- 0: Power down (default)
- 1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000C	Power Management 10	PMRCV	0	PMLO2RN	PMLO2RP	0	0	PMLO2LN	PMLO2LP
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

PMLO2LP/N: Line Out-Amp 2 Lch Power Management

- 0: Power down (default)
- 1: Power up

Singled-ended mode or full differential mode can be changed by LO2DIF bit.

PMLO2RP/N: Line Out-Amp 2 Rch Power Management

- 0: Power down (default)
- 1: Power up

Singled-ended mode or full differential mode can be changed by LO2DIF bit.

PMRCV: Receiver-Amp Power Management

- 0: Power down (default)
- 1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000D	Lineout2 Setting	0	0	0	0	0	0	0	LO2DIF
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

LO2DIF: Lineout-Amp 2 Output Mode Select

- 0: Single-ended Mode (default)
- 1: Full differential Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000E	Output Setting Mode	0	0	0	0	0	0	HPRHZ	HPLHZ
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

HPRHZ, HPLHZ: Each output amplifiers GND switch setting

- 0: Pull-down by 9 Ω(typ.) (default)
- 1: Pull-down by 200kΩ(typ.)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
000F	MIC Power Level	0	0	0	0	MICL2[1:0]	MICL1[1:0]		
	R/W	R/W	R/W	R/W	R/W	R/W		R/W	
	Default	0	0	0	0	00		00	

MICL1[1:0]: MIC Power (MPWR1A/1B/1C pins) Output Voltage Setting

Default “00”, typ. 2.8V ([Table 20](#))

MICL2[1:0]: MIC Power (MPWR2 pin) Output Voltage Setting

Default “00”, typ. 2.8V ([Table 21](#))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0010	MIC-Amp 1 Lch Gain	0	0	0	0		MG1L[3:0]		
	R/W	R/W	R/W	R/W	R/W		R/W		
	Default	0	0	0	0		0000		

MG1L[3:0]: MIC-Amp 1 Lch Analog Volume ([Table 18](#))

Default: “0000” (0dB) (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0011	MIC-Amp 1 Rch Gain	0	0	0	0		MG1R[3:0]		
	R/W	R/W	R/W	R/W	R/W		R/W		
	Default	0	0	0	0		0000		

MG1R[3:0]: MIC-Amp 1 Rch Analog Volume ([Table 18](#))

Default: “0000” (0dB) (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0012	MIC-Amp 2 Gain	0	0	0	0		MG2M[3:0]		
	R/W	R/W	R/W	R/W	R/W		R/W		
	Default	0	0	0	0		0000		

MG2M[3:0]: MIC-Amp 2 Analog Volume ([Table 18](#))

Default: “0000” (0dB) (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0013	MIC-Amp 3 Gain	0	0	0	0		MG2V[3:0]		
	R/W	R/W	R/W	R/W	R/W		R/W		
	Default	0	0	0	0		0000		

MG2V[3:0]: MIC-Amp 3 Analog Volume ([Table 18](#))

Default: “0000” (0dB) (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0014	Reserved	0	0	0	0	0	0	0	0
0015		R/W							
	Default	0	0	0	0	0	0	0	0

Do not write anything to the addresses from 0014H to 0015H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0016	Charge Pump 1 Setting 1	0	0	0	0	0	0	CKSELCP1[1:0]	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
	Default	0	0	0	0	0	0		00

## CKSELCP1[1:0]: CP1 Operation Clock Setting

00: 500kHz (default)

01: 250kHz

10: 125kHz

11: 62.5kHz

The power consumption can be suppressed by setting CKSELCP1[1:0] bits = “11” in Voice Wakeup mode (MIC Power = Direct Mode, MIC-Amp 3 + ADC2,  $f_s \leq 48\text{kHz}$ ).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0017 ~ 0019	Reserved	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Do not write anything to the addresses from 0017H to 0019H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001A	Clock Mode Select	IBIAS	CM[1:0]				FS[4:0]		
	R/W	R/W	R/W				R/W		
	Default	0	0				00000		

FS[4-0]: Sampling Frequency Select ([Table 5](#))Default: “00000” ( $f_s=8\text{kHz}$ )CM[1:0]: CODEC Master Clock Select ([Table 4](#))

Default: 256fs

## IBIAS:LINEOUT1/2 Operation Mode Select

0: Normal Speed, Double Speed (default)

1: Quad Speed

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001B	Digital Filter Select 1	DA1SD	DA1SL	AD1SD[1:0]	DFTHR1	HPFC1[1:0]	HPFAD1N		
	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Default	0	0	00	0	00	0		

HPFAD1N: ADC1 HPF Control

0: ON (default)

1: OFF

When HPFAD1N bit = “0”, the setting of HPFC1[1-0] bits becomes valid. The audio data passes through the HPFAD1 block by 0dB gain when HPFAD1N bit = “1”.

Set HPFAD1N bit to “0” when PMAD1L or PMAD1R bit = “1” (when PMDM1R bit = “1” or PMDR1L bit = “1” if DMIC1 bit = “1”).

HPFC1[1-0]: Cut-off frequency of HPF1(ADC) ([Table 24](#))

Default: “00” (3.4Hz @ fs = 44.1kHz)

DASD1, DASL1, DFTHR1: DAC1 Digital Filter Mode Setting ([Table 26](#))

Default: “0, 0, 0” (Sharp Roll-Off Filter)

AD1SD[1:0]: ADC1 Digital Filter Mode Setting ([Table 25](#))

Default: “00” (Sharp Roll-Off Filter 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001C	Digital Filter Select 2	0	0	AD2SD[1:0]	DFTHR2	HPFC2[1:0]	HPFAD2N		
	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
	Default	0	0	00	0	00	0		

HPFAD2N: ADC2 HPF Control

0: ON (default)

1: OFF

When HPFAD2N bit = “0”, the setting of HPFC2[1-0] bits becomes valid. The audio data passes through the HPFADC2 block by 0dB gain when HPFAD2N bit = “1”.

Set HPFAD2N bit to “0” when PMAD2L or PMAD2R bit = “1” (when PMDM2R bit = “1” or PMDR2L bit = “1” if DMIC2 bit = “1”).

HPFC2[1-0]: HPF(ADC2) Cut-off Frequency of HPF(ADC2) ([Table 24](#))

Default: “00” (3.4Hz @ fs = 44.1kHz)

DFTHR2: DAC2 Digital Filter Mode Setting ([Table 27](#))

Default: “0” (Sharp Roll-Off Filter)

AD2SD[1:0]: ADC2 Digital Filter Mode Setting ([Table 25](#))

Default: “00” (Sharp Roll-Off Filter 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001D	Test Register 1	TEST	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

TEST: Test Mode Enable

**TEST bit must always be “0”.**

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001E	Digital MIC 1	0	0	PMMDM1R	PMMDM1L	DCLKE1	0	DCLKP1	DMIC1
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DMIC1: ADC1 Digital Microphone Connection Select

0: Analog Microphone (default)

1: Digital Microphone

DCLKP1: Data Latching Edge Select

0: Lch data is latched on the DMCLK1 rising edge (“↑”). (default)

1: Lch data is latched on the DMCLK1 falling edge (“↓”).

DCLKE1: DMCLK1 pin Output Clock Control

0: “L” Output (default)

1: 64fs Output

PMMDM1L/R: Input Signal Select with Digital Microphone

0: Power Down (default)

1: Power Up

When DMIC1 bit is “1”, the registers are enabled. ADC1 digital block is powered-down by PMMDM1L = PMMDM1R bits = “0” when selecting a digital microphone input (DMIC1 bit = “1”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
001F	Digital MIC 2	0	0	PMDM2R	PMDM2L	DCLKE2	0	DCLKP2	DMIC2
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

DMIC2: ADC2 Digital Microphone Connection Select

- 0: Analog Microphone (default)
- 1: Digital Microphone

DCLKP2: Data Latching Edge Select

- 0: Lch data is latched on DMCLK2 rising edge (“↑”). (default)
- 1: Lch data is latched on DMCLK2 falling edge (“↓”).

DCLKE2: DMCLK2 pin Output Clock Control

- 0: “L” Output (default)
- 1: 64fs Output

PMDM2L/R: Input Signal Select with Digital Microphone

- 0: Power Down (default)
- 1: Power Up

When DMIC2 bit is “1”, the registers are enabled. ADC2 digital block is powered-down by PMDM2L = PMDM2R bits = “0” when selecting a digital microphone input (DMIC2 bit = “1”)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0020	DAC1 Mono Mixing	INV1R	MDAC1R	RDAC1R	LDAC1R	INV1L	MDAC1L	RDAC1L	LDAC1L
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

MDAC1L, RDAC1L, LDAC1L bits: DAC1 Lch Input Signal Select ([Table 29](#))

Default: “000” (MUTE)

MDAC1R, RDAC1R, LDAC1R bits: DAC1 Rch Input Signal Select ([Table 29](#))

Default: “000” (MUTE)

INV1L/R: DAC1 Input Signal Polarity Select

- 0: Normal (default)
- 1: Inverting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0021	DAC2 Mono Mixing	INV2R	RDAC2R	RDAC2R	LDAC2R	INV2L	MDAC2L	RDAC2L	LDAC2L
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

MDAC2L, RDAC2L, LDAC2L bits: DAC2 Lch Input Signal Select ([Table 30](#))

Default: “000” (MUTE)

MDAC2R, RDAC2R, LDAC2R bits: DAC2 Rch Input Signal Select ([Table 30](#))

Default: “000” (MUTE)

INV2L/R: DAC2 Input Signal Polarity Select

- 0: Normal (default)
- 1: Inverting

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0022	Output Volume Setting	0	0	0	0	0	0	OVOLC2N	OVOLC1N
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

## OVOLC1N: Digital Volume 1 Control

0: Dependent (default)

1: Independent

When OVOLC1N bit = “0”, OVL1[4:0] bits control both Lch and Rch volume levels while register values of OVL1[4:0] bits are not written to OVR1[4:0] bits. When OVOLC1N bit = “1”, OVL1[4:0] bits control Lch level and OVR1[4:0] bits control Rch level, respectively.

## OVOLC2N: Digital Volume 2 Control

0: Dependent (default)

1: Independent

When OVOLC2N bit = “0”, OVL2[4:0] bits control both Lch and Rch volume levels while register values of OVL2[4:0] bits are not written to OVR2[4:0] bits. When OVOLC2N bit = “1”, OVL2[4:0] bits control Lch level and OVR2[4:0] bits control Rch level, respectively.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0023	Charge Pump2 Setting 1	0	0	0	LVDTM[2:0]			CPMODE[1:0]	
	R/W	R/W	R/W	R/W	R/W			R/W	
	Default	0	0	0	000			00	

CPMODE[1-0]: Charge-pump Mode Setting ([Table 33](#))

Default: “00” (Automatic Switching Mode)

LVDTM[2-0]: Undetected Minimum Frequency Period in 1/2VDD Mode Detection ([Table 35](#))

Default: “000” (64/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0024	Charge Pump 2 Setting 2	0	0	VDDTM[3:0]				0	0
	R/W	R/W	R/W	R/W				R/W	R/W
	Default	0	0	0000				0	0

VDDTM[3-0]: VDD Mode Waiting Period ([Table 34](#))

Default: “0000” (1024/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0025	Reserved	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Do not write anything to the address 0025H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0026	Mode Control	DSMLP2	DSMLP1	0	0	0	0	ADRST[1:0]	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

ADRST[1:0]: ADC Initialization Cycle Select ([Table 8](#))

Default: “00” (2115/fs) (default)

ADC1 and ADC2 are common setting.

DSMLP1: DAC1 Low Speed Operation Setting

Default 0 ([Table 4](#), [Table 6](#))

DSMLP2: DAC2 Low Speed Operation Setting

Default 0 ([Table 4](#), [Table 6](#))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0027 ~ 0029	Reserved	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Do not write anything to the address from 0027H to 0029H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
002A	Reserved	0	0	1	1	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	1	1	0	0	0	0

Do not write anything to the address 002AH.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
002B	Reserved	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Do not write anything to the address 002BH.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
002C	Jitter Cleaner 1	0		CM2[1:0]				FS2[4:0]	
	R/W	R/W		R/W			R/W		
	Default	0		00			0 0000		

FS2[4-0]: Sampling Frequency Select ([Table 7](#))

Default: “00000” (fs=8kHz)

CM2[1:0]: CODEC Master Clock Select ([Table 6](#))

Default: 256fs

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
002D	Jitter Cleaner 2	DIV	0	SRCESD	SRCESL	SMT[1:0]		SAUTOE	SMUTEE
	R/W	R/W	R/W	R/W	R/W	R/W		R/W	R/W
	Default	0	0	0	0	00		0	0

SMUTEE: SRCE Soft Mute Enable

0: Disable (Default)

1: Enable

SAUTOE: SRCE Semi-Auto Mode Enable

0: Disable (Default)

1: Enable

SMT[1:0]: SRCE Soft Mute Cycle Setting

Default: “00”, 1024/FSO ([Table 86](#))

SRCESL, SRCESD: SRCE Digital Filter Setting

Default: “00”, Sharp Roll-Off

DIV:CODECMCK Divider

Default: “0” (divided by 1, [Table 82](#))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
002E	Jitter Cleaner 3	XCKSPSEL	XCKSEL	SRCO8FS	DITHERE	0	SELD A2IN	SELD A1IN	SELSRCIN
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

SELSRCIN, SELDA1IN, SELDA2IN: SRCE Input Data Select

Default: "000", Through

DITHERE: SRCE Dither Setting

0: Dither OFF (Default)

1: Dither ON

SRCO8FS: SRCE 8fs Data Output Mode

0: Disable (Default)

1: Enable

DAC digital filter must be in bypass mode (DFTHR bit = "1") when the SRC is 8fs output mode (SRCO8FS bit = "1") and the SRCE output is selected as DAC input data.

XCKSEL: DAC1 Operation Clock Setting

0: CODECMCLK (default)

1: X'tal

XCKPSEL: Charge-pump Operation Clock Setting

0: CODECMCLK (default)

1: X'tal

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
002F	Detection Event Reset	0	0	0	0	0	0	0	CLR
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

CLR: Event Clear bit

0: Not clear (default)

1: Clear

When CLR bit = "1", event bits (JDE and RCE bits) are set to "0" and the INTN pin goes "H" from "L". CLR bit becomes "0" when all the event are cleared completely.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0030	Event Mask Setting	0	0	0	0	0	0	MJDE	MRCE
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

MRCE: Mask Enable for RCE bit (Remote Control Event bit)

0: Mask Disable (default)

1: Mask Enable

MJDE: Mask Enable for JDE bit (JACK Detection Event bit)

0: Mask Disable (Default)

1: Mask Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0031	Detection Power Management	PMDTE	PMRCB	0	0	MDMODE	MDDIF	DTINTN	CMPL
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

CMPL: Comparator Level Select of Remote Control Button Detection Function

0: 1/3 x MPWR2 (default)

1: 4/9 x MPWR2

DTINTN: Polarity Setting of Plug Detection Switch

0: Normally Shorted (default)

1: Normally Open

MDDIF: Microphone Detection Operation Mode Select

0:  $\mu$ P Control (default)

1: Automatic

MDMODE: Microphone Detection Operation Mode Select

0: Single Detection Mode (default)

1: Continuous Detection Mode

PMDTE: Jack Detection Circuit Power Management

0: Power down (default)

1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0032	Detection Setting 1	0	0	CMPWT[1:0]		MPWT[2:0]		JDT	
	R/W	R/W	R/W	R/W		R/W		R/W	
	Default	0	0	00		000		0	

JDT: De-bounce Time 1 Setting

0: typ. 2ms (default)

1: typ. 4ms

MPWT[2:0]: MIC Power Wait Timer Setting ([Table 60](#))

Default: “000”, 50ms

CMPWT[1:0]: De-bounce Time 2 Setting ([Table 71](#))

00: typ. 3ms (default)

01: typ. 8ms

10: typ. 20ms

11: typ. 50ms

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0033	Detection Setting 1	0	0	0	0	0	CMPRST	AVG[1:0]	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Default	0	0	0	0	0	0	00	

AVG[1:0]: Output Data Averaging Setting of the Comparator for Remote Controlling

00: 10 times (default)

01: 6 times

10: 1 time

11: N/A (Not available)

CMPRST: Read Clear Setting of the Output Data (CMP[3:0] bits) for the Comparator for Remote Controlling

0: Reset (default)

1: Hold

When CMRST bit = “0”, the values of CMP[3:0] bits are reset by reading CMP[3:0] bits.

When CMRST bit = “1”, the values of CMP[3:0] bits are held even if CMP[3:0] bits are read.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0034	MIC Input Selector 1	0		INS1R[2:0]		0		INS1L[2:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	0		001		0		000	

INS1L[2:0]: MIC-Amp 1 Lch Input Source Select ([Table 14](#))

Default: “000” (AIN1)

INS1R[2:0]: MIC-Amp 1 Rch Input Source Select ([Table 15](#))

Default: “001” (AIN2)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0035	MIC Input Selector 2	0		INS2V[2:0]		0		INS2M[2:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	0		000		0		010	

INS2M[2:0]: MIC-Amp 2 Input Source Select ([Table 16](#))

Default: “010” (AIN3)

INS2V[2:0]: MIC-Amp 3 Input Source Select ([Table 17](#))

Default: “000” (AIN1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0036	Lch Output Volume 1	0	0	0			OVL1[4:0]		
0037	Rch Output Volume 1	0	0	0			OVR1[4:0]		
0038	Lch Output Volume 2	0	0	0			OVL2[4:0]		
0039	Rch Output Volume 2	0	0	0			OVR2[4:0]		
	R/W	R/W	R/W	R/W			R/W		
	Default	0	0	0			19H		

OVL1[4:0]: DAC1 Lch Digital Volume; +3dB ~ -12dB & Mute, 0.5dB step ([Table 32](#))

OVR1[4:0]: DAC1 Rch Digital Volume; +3dB ~ -12dB & Mute, 0.5dB step ([Table 32](#))

OVL2[4:0]: DAC2 Lch Digital Volume; +3dB ~ -12dB & Mute, 0.5dB step ([Table 32](#))

OVR2[4:0]: DAC2 Rch Digital Volume; +3dB ~ -12dB & Mute, 0.5dB step ([Table 32](#))

Default: “19H” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
003A	HP Volume Control		HPTM[2:0]				HPG[4:0]		
	R/W		R/W				R/W		
	Default		011				15H		

HPG[4:0]: HP-Amp Analog Volume Setting; +6dB ~ -40dB, 2dB step ([Table 36](#))

Default: 15H (0dB)

HPTM[2:0]: HP-Amp Analog Volume Zero Crossing Timeout Setting ([Table 37](#))

Default: “011” (1024/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
003B	Lineout1 Volume Ctrl	0	0	0	0	0		LO1G[2:0]	
	R/W	R/W	R/W	R/W	R/W	R/W		R/W	
	Default	0	0	0	0	0		101	

LO1G[2:0]: Lineout-Amp 1 Analog Volume Setting; +3dB ~ -7.5dB, 1.5dB step ([Table 40](#))

Default: “101” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
003C	Lineout2 Volume Ctrl	0		LO2G[2:0]		0		RCVG[2:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	0		101		0		101	

RCVG[2:0]: Receiver-Amp Analog Volume Setting; +3dB ~ -7.5dB, 1.5dB step ([Table 47](#))

Default: “101” (0dB)

LO2G[2:0]: Lineout-Amp 2 Analog Volume Setting; +3dB ~ -7.5dB, 1.5dB step ([Table 44](#))

Default: “101” (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
003D	Reserved	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Do not write anything to the addresses 003DH.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
003E	PLL1 CLK Source Select	0	0	0		PLS1[4:0]			
	R/W	R	R	R/W		R/W			
	Default	0	0	0		00H			

PLS1[4:0]: PLL1 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
003F	PLL1 Ref CLK Divider 1			PLD1[15:8]					
0040	PLL1 Ref CLK Divider 2			PLD1[7:0]					
	R/W			R/W					
	Default			0000H					

PLD1[15:0]: PLL1 Reference Clock Divider Setting ([Table 91](#))

Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0041	PLL1 FB CLK Divider 1			PLM1[15:8]					
0042	PLL1 FB CLK Divider 2			PLM1[7:0]					
	R/W			R/W					
	Default			0000H					

PLM1[15:0]: PLL1 Feedback Clock Divider Setting ([Table 92](#))

Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0043	PLL2 CLK Source Select	0	0	0					PLS2[4:0]
	R/W	R	R	R					R/W
	Default	0	0	0					00H

PLS2[4:0]: PLL2 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0044	PLL2 Ref CLK Divider 1								PLD2[15:8]
0045	PLL2 Ref CLK Divider 2								PLD2[7:0]
	R/W								R/W
	Default								0000H

PLD2[15:0]: PLL1 Reference Clock Divider Setting ([Table 91](#))

Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0046	PLL2 FB CLK Divider 1								PLM2[15:8]
0047	PLL2 FB CLK Divider 2								PLM2[7:0]
	R/W								R/W
	Default								0000H

PLM2[15:0]: PLL1 Feedback Clock Divider Setting ([Table 92](#))

Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0048	MCLK1 Source Select	0	0	MSN1					CKS1[4:0]
	R/W	R	R	R/W					R/W
	Default	0	0	0					00H

CKS1[4:0]: MCLK1 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

MSN1: SDBCLK1/SDSYNC1 Master/Slave Setting ([Table 98](#))

Default: “0”, Slave Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0049	MBCLK1 Divider								BDV1[7:0]
	R/W								R/W
	Default								00H

BDV1[7:0]: MBCLK1 Divider Setting ([Table 99](#))

Default: 00H, Divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004A	MSYNC1 Divider				SDV1[7:0]				
	R/W				R/W				
	Default				00H				

SDV1[7:0]: MSYNC1 Divider Setting ([Table 100](#))

Default: 00H, Stop

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004B	MCLK2 Source Select	0	0	MSN2		CKS2[4:0]			
	R/W	R	R	R/W		R/W			
	Default	0	0	0		00H			

CKS2[4:0]: MCLK2 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

MSN2: SDBCLK2/SDSYNC2 Master/Slave Setting ([Table 98](#))

Default: “0”, Slave Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004C	MBCLK2 Divider				BDV2[7:0]				
	R/W				R/W				
	Default				00H				

BDV2[7:0]: MBCLK2 Divider Setting ([Table 99](#))

Default: 00H, Divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004D	MSYNC2 Divider				SDV2[7:0]				
	R/W				R/W				
	Default				00H				

SDV2[7:0]: MSYNC2 Divider Setting ([Table 100](#))

Default: 00H, Stop

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004E	MCLK3 Source Select	0	0	MSN3		CKS3[4:0]			
	R/W	R	R	R/W		R/W			
	Default	0	0	0		00H			

CKS3[4:0]: MCLK3 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

MSN3: SDBCLK3/SDSYNC3 Master/Slave Setting ([Table 98](#))

Default: “0”, Slave Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
004F	MBCLK3 Divider				BDV3[7:0]				
	R/W				R/W				
	Default				00H				

BDV3[7:0]: MBCLK3 Divider Setting ([Table 99](#))

Default: 00H, Divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0050	MSYNC3 Divider				SDV3[7:0]				
	R/W				R/W				
	Default				00H				

SDV3[7:0]: MSYNC3 Divider Setting ([Table 100](#))

Default: 00H, Stop

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0051	MCLK4 Source Select	0	0	MSN4			CKS4[4:0]		
	R/W	R	R	R/W			R/W		
	Default	0	0	0			00H		

CKS4[4:0]: MCLK4 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

MSN4: SDBCLK4/SDSYNC4 Master/Slave Setting ([Table 98](#))

Default: “0”, Slave Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0052	MBCLK4 Divider				BDV4[7:0]				
	R/W				R/W				
	Default				00H				

BDV4[7:0]: MBCLK4 Divider Setting ([Table 99](#))

Default: 00H, divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0053	MSYNC4 Divider				SDV4[7:0]				
	R/W				R/W				
	Default				00H				

SDV4[7:0]: MSYNC4 Divider Setting ([Table 100](#))

Default: 00H, Stop

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0054	MCLK5 Source Select	0	0	1					CKS5[4:0]
	R/W	R	R	R					R/W
	Default	0	0	1					00H

CKS5[4:0]: MCLK5 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0055	MBCLK5 Divider								BDV5[7:0]
	R/W								R/W
	Default								00H

BDV5[7:0]: MBCLK5 Divider Setting ([Table 99](#))

Default: 00H, Divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0056	MSYNC5 Divider								SDV5[7:0]
	R/W								R/W
	Default								00H

SDV5[7:0]: MSYNC5 Divider Setting ([Table 100](#))

Default: 00H, Stop

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0057	MCLK6 Source Select	0	0	1					CKS6[4:0]
	R/W	R	R	R					R/W
	Default	0	0	1					00H

CKS6[4:0]: MCLK6 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0058	MBCLK6 Divider								BDV6[7:0]
	R/W								R/W
	Default								00H

BDV6[7:0]: MBCLK6 Divider Setting ([Table 99](#))

Default: 00H, Divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0059	MSYNC6 Divider								SDV6[7:0]
	R/W								R/W
	Default								00H

SDV6[7:0]: MSYNC6 Divider Setting ([Table 100](#))

Default: 00H, Stop

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005A	MCLK7 Source Select	0	0	1					CKS7[4:0]
	R/W	R	R	R					R/W
	Default	0	0	1					00H

CKS7[4:0]: MCLK7 Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005B	MBCLK7 Divider								BDV7[7:0]
	R/W								R/W
	Default								00H

BDV7[7:0]: MBCLK7 Divider Setting ([Table 99](#))

Default: 00H, Divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005C	MSYNC7 Divider								SDV7[7:0]
	R/W								R/W
	Default								00H

SDV7[7:0]: MSYNC7 Divider Setting ([Table 100](#))

Default: 00H, Stop

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
005D ~ 0061	Reserved	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0062	MCKO Source Select	0	0	0					MCKS1[4:0]
	R/W	R	R	R					R/W
	Default	0	0	0					00H

MCKS1[4:0]: MCKO Clock Source Select ([Table 88](#))

Default: 00H, Tie Low

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0063	MCKO Divider								MDIV1[7:0]
	R/W								R/W
	Default								00H

MDIV1[7:0]: MCKO Divider Setting ([Table 101](#))

Default: 00H, Divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0064	CODEC CLK Source Select	0	0	0					MCKS2[4:0]
	R/W	R	R	R					R/W
	Default	0	0	0					00H

MCKS2[4:0]: CODEC Clock Source Select ([Table 88](#))

Default: 00H, Tie Low (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0065	CODEC CLK Divider								MDIV2[7:0]
	R/W								R/W
	Default								00H

MDIV2[7:0]: CODECMCLK Divider Setting ([Table 101](#))

Default: 00H, divided by 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0066	DSP MCLK Source Select	0	0	0					CKSD[4:0]
	R/W	R	R	R					R/W
	Default	0	0	0					00H

CKSD[4:0]: DSP MCLK Source Select ([Table 88](#))

Default: 00H, Tie Low

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0067	BUS CLK Divider								MDIVD[7:0]
	R/W								R/W
	Default								03H

MDIVD[7:0]: BUS CLK Divider Setting ([Table 102](#))

Default: 03H, Divided by 4

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0068	AIN1/2 Sync Domain Setting	0		SDAIF1[2:0]		0		SDAIF2[2:0]	
0069	AIN3/4 Sync Domain Setting	0		SDAIF3[2:0]		0		SDAIF4[2:0]	
006A	ADC Sync Domain Setting	0	0	0	0	0		SDCDC[2:0]	
006B	SB1/2 Sync Domain Setting	0		SDSB1[2:0]		0		SDSB1[2:0]	
006C	SB3/DSPO Sync Domain Setting	0		SDSB3[2:0]		0		SDDSP[2:0]	
006D	DSPO2/4 Sync Domain Setting	0		SDDSP02[2:0]		0		SDDSP04[2:0]	
006E	SRCA/B Sync Domain Setting	0		SDSRCAO[2:0]		0		SDSRCBO[2:0]	
006F	SRCC/D Sync Domain Setting	0		SDSRCCO[2:0]		0		SDSRCDO[2:0]	
	R/W					R/W			
	Default					Except for SDSRCAO[2:0]: “000”, SDSRCAO[2:0]: “001”			

SDxxx[2:0]: Sync Domain Setting ([Table 106](#))

Default: “000”, Not Assigned (Except for SDSRCAO[2:0] bits)  
“001”: SDSYNC1, SDBCLK1 (SDSRCA[2:0] bits)

\* Refer to [Figure 60](#) for Sync Domain of each data.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0070 0071	Reserved	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0072	SDTO1A Source Select	0	0	0		SDTO1ASRC[4:0]			
0073	SDTO1B Source Select	0	0	0		SDTO1BSRC[4:0]			
0074	SDTO2 Source Select	0	0	0		SDTO2SRC[4:0]			
0075	SDTO3 Source Select	0	0	0		SDTO3SRC[4:0]			
0076	SDTO4 Source Select	0	0	0		SDTO4SRC[4:0]			
0077	SBO1 Source Select	0	0	0		SBO1SRC[4:0]			
0078	SBO2 Source Select	0	0	0		SBO2SRC[4:0]			
0079	DAC1 Source Select	0	0	0		DAC1SRC[4:0]			
007A	DAC2 Source Select	0	0	0		DAC2SRC[4:0]			
007B	DSPI1 Source Select	0	0	0		DSPI1SRC[4:0]			
007C	DSPI2 Source Select	0	0	0		DSPI2SRC[4:0]			
007D	DSPI3 Source Select	0	0	0		DSPI3SRC[4:0]			
007E	DSPI4 Source Select	0	0	0		DSPI4SRC[4:0]			
007F	DSPI5 Source Select	0	0	0		DSPI5SRC[4:0]			
0080	MIXAI1 Source Select	0	0	0		MIXAI1SRC[4:0]			
0081	MIXAI2 Source Select	0	0	0		MIXAI2SRC[4:0]			
0082	MIXBI1 Source Select	0	0	0		MIXBI1SRC[4:0]			
0083	MIXBI2 Source Select	0	0	0		MIXBI2SRC[4:0]			
0084	SRCAI Source Select	0	0	0		SRCAISRC[4:0]			
0085	SRCB1 Source Select	0	0	0		SRCBISRC[4:0]			
0086	SRCC1 Source Select	0	0	0		SRCCISRC[4:0]			
0087	SRCD1 Source Select	0	0	0		SRCDISRC[4:0]			
0088	VAD Source Select	0	0	0		VADSRC[4:0]			
	R/W		R				R/W		
	Default					00H			

SDTO1ASRC[4:0]: SDTO1A (pin) Output  
 SDTO1BSRC[4:0]: SDTO1B (pin) Output  
 SDTO2SRC[4:0]: SDTO2 (pin) Output  
 SDTO3SRC[4:0]: SDTO3 (pin) Output  
 SDTO4SRC[4:0]: SDTO4 (pin) Output  
 SBO1SRC[4:0]: Output to Source Port of SLIMbus (port-array6 = Lch, port-array7 = Rch)  
 SBO2SRC[4:0]: Output to Source Port of SLIMbus (port-array8 = Lch, port-array9 = Rch)  
 DAC1SRC[4:0]: Input to DAC1 (Analog path is selected independently.)  
 DAC2SRC[4:0]: Input to DAC2 (Analog path is selected independently.)  
 DSPI1SRC[4:0]: DSP Input 1  
 DSPI2SRC[4:0]: DSP Input 2  
 DSPI3SRC[4:0]: DSP Input 3  
 DSPI4SRC[4:0]: DSP Input 4  
 DSPI5SRC[4:0]: DSP Input 5  
 MIXAI1SRC[4:0]: Mixer A Input 1  
 MIXAI2SRC[4:0]: Mixer A Input 2  
 MIXBI1SRC[4:0]: Mixer B Input 1  
 MIXBI2SRC[4:0]: Mixer B Input 2  
 SRCAISRC[4:0]: SRCA Input  
 SRCBISRC[4:0]: SRCB Input  
 SRCCISRC[4:0]: SRCC Input  
 SRCDISRC[4:0]: SRCD Input  
 VADSRC[4:0]: VAD Input

Default: 00H, Source = ALL0 (0x0000 0000)

- \* Set a desired source address of an Audio Source Port to each Audio Sink Port ([Table 105](#)) by Source address setting register ([Table 104](#)). Refer to “Audio Source Port Setting” and “Audio Sink Port Setting” for details.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0089 008A	Reserved	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
008B	SDTIOA/B/C/D I/F Format	0	THR1	DIF1[1:0]	BCKP1	DLC1[2:0]			
008C	SDTIO2 I/F Format	0	THR2	DIF2[1:0]	BCKP2	DLC2[2:0]			
008D	SDTIO3 I/F Format	0	THR3	DIF3[1:0]	BCKP3	DLC3[2:0]			
008E	SDTIO4 I/F Format	GPE1	THR4	DIF4[1:0]	BCKP4	DLC4[2:0]			
008F	CODEC I/F Format	EXIF	THRC	0	0	BCKPC	DLCC[2:0]		
	R/W				R/W				
	Default					00H			

DLCx[2:0]: Data Length Setting ([Table 110](#)), (x=1~4, C)

Default: “000”, 24bit Linear

BCKPx: BCLK Edge ([Table 109](#)), (x=1~4, C)

Default: “0”, Falling Edge

DIFx[1:0]: Digital I/F Format Setting ([Table 108](#)), (x=1~4)

Default: “00”, I<sup>2</sup>S compatible

THR<sub>x</sub>: Sync Through Mode ([Table 107](#)), (x=1~4, C)

Default: “0”, Disable

GPE1: SDTO4 Function Setting

0: SDTO4 (default)

1: GPO1

EXIF: Direct I/F Mode ([Table 28](#))

Default: “0”, Normal Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0090	SRC Clock Setting	0	0	0	0	0	0		SRCCCLK[1:0]
	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W
	Default	0	0	0	0	0	0		00

SRCCCLK[1:0]: SRCMCLK Setting ([Table 72](#))

Default: “00”, N/A (Not available)

When operating SRCA, SRCB, SRCC or/and SRCD, SRCCCLK[1:0] bits are set to “01”, “10” or “11”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0091	SRC Mute Setting	SAUTOD	SAUTOA	SAUTOB	SAUTOA	SMUTED	SMUTEC	SMUTEB	SMUTEA
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

SMUTEA/B/C/D: SRCA/B/C/D Soft Mute Enable

0: Disable (Default)

1: Enable

SAUTOA/B/C/D: SRCA/B/C/D Semi-Auto Mode Enable

0: Disable (Default)

1: Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0092	MIXA Setting	SFTA2[1:0]		SFTA1[1:0]		SWPA2[1:0]		SWPA1[1:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	00		00		00		00	

SWPA1[1:0]: Mixer A1 Input Data Swap Function

SWPA2[1:0]: Mixer A2 Input Data Swap Function

Default: “00”, Through ([Table 130](#))

SFTA1[1:0]: Mixer A1 Input Level Adjustment Function

SFTA2[1:0]: Mixer A2 Input Level Adjustment Function

Default: “00”, 0dB ([Table 129](#))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0093	MIXB Setting	SFTB2[1:0]		SFTB1[1:0]		SWPB2[1:0]		SWPB1[1:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	00		00		00		00	

SWPB1[1:0]: Mixer B1 Input Data Swap Function

SWPB2[1:0]: Mixer B2 Input Data Swap Function

Default: “00”, Through ([Table 130](#))

SFTB1[1:0]: Mixer B1 Input Level Adjustment Function

SFTB2[1:0]: Mixer B2 Input Level Adjustment Function

Default: “00”, 0dB ([Table 129](#))

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0094	DSP Setting 1		DRMS[1:0]		DRAD[1:0]		BANK[3:0]		
	R/W		R/W		R/W		R/W		
	Default		00		10		1001		

BANK[3:0]: DLRAM Mode Setting of DSP ([Table 132](#))

Default: “1001”, Bank0 (Ring, 2048), Bank1(Linear, 18432), Bank2=0

DRAD[1:0]: Addressing Mode Setting ([Table 134](#))

Default: “10”, Addressing Mode 2 (DRAD Pointer = “10”, Bank1 DP1 = Linear, Bank0 DP0 = Ring)

DRMS[1:0]: Data RAM Size Setting ([Table 133](#))

Default: “00”, DRAM Mode 0 (Bank1 = 512 words, Back2 = 1536 words)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0095	Reserved	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Do not write anything to the address 0095H.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0096	DSP Setting 2	0	0	0	0	POMODE	0	WAVP[1:0]	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	Default	0	0	0	0	1	0	10	

WAVP[1:0]: CRAM Memory Assignment of DSP ([Table 135](#))

Default: “10”, WAVP Mode 2 (129words, FFT points = 512)

POMODE: DLYRAM Pointer0 Select

0: OFFREG

1: DBUS Immediate Data (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0097	DSP Setting 3	0	0	0	EDNOPDIS	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

EDNOPDIS: DSP Clock Mode Setting

0: Low Power Mode (default)

1: Normal Mode

When using Soft SRC, EDNOPDIS bit must be set to “1”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0098	DSP Setting 4					DSPCKADJ[7:0]			
	R/W					R/W			
	Default					00H			

DSPCKADJ[7:0]: DSP Operation Clock Adjustment

Default: 00H, Not divided

$$\text{DSP Operation Clock} = \text{DSPMCLK} * (256 - \text{DSPCKADJ}) / 256$$

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0099	Virtual Address Control	0	0	0	RAMPAGE			VAT[3:0]	
	R/W	R	R	R	R/W			R/W	
	Default	0	0	0	0			0000	

RAMPAGE: RAM Access Area Setting ([Table 138](#))

0: 0xA00 ~ 0xAF (Default)

1: 0xB00 ~ 0xBFF

VAT[3:0]: Virtual Access Target Setting ([Table 137](#))

Default: “0000”, Not available

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
009A	Virtual Address Control	0	0	0			PAGE[4:0]		
	R/W	R	R	R			R/W		
	Default	0	0	0			00000		

PAGE[4:0]: SRAM Address Space Extension ([Table 139](#))

Default: “00000”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
009B	External Jump Condition				JX[7:0]				
	R/W				R/W				
	Default				00H				

JX[7:0]: DSP Program Conditional Jump Register

Default: 00H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
009C	Run State Data Length	0	0	0	0		RNUM[3:0]		
	R/W	R	R	R	R		R/W		
	Default	0	0	0	0		0000		

RNUM[3:0]: RAM Write Data Number Setting during RUN state

Default: “0000”

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
009D	Run State Start Address 1				RADR[15:8]				
009E	Run State Start Address 1				RADR[7:0]				
	R/W				R/W				
	Default				0000H				

RADR[15:0]: Start Address Setting of RAM Write during RUN state

Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
009F	Run State Data Setting 1				RBUF0[23:16]				
00A0	Run State Data Setting 2				RBUF0[15:8]				
00A1	Run State Data Setting 3				RBUF0[7:0]				
00A2	Run State Data Setting 4				RBUF1[23:16]				
00A3	Run State Data Setting 5				RBUF1[15:8]				
00A4	Run State Data Setting 6				RBUF1[7:0]				
00A5	Run State Data Setting 7				RBUF2[23:16]				
00A6	Run State Data Setting 8				RBUF2[15:8]				
00A7	Run State Data Setting 9				RBUF2[7:0]				
00A8	Run State Data Setting 10				RBUF3[23:16]				
00A9	Run State Data Setting 11				RBUF3[15:8]				
00AA	Run State Data Setting 12				RBUF3[7:0]				
00AB	Run State Data Setting 13				RBUF4[23:16]				
00AC	Run State Data Setting 14				RBUF4[15:8]				
00AD	Run State Data Setting 15				RBUF4[7:0]				
00AE	Run State Data Setting 16				RBUF5[23:16]				
00AF	Run State Data Setting 17				RBUF5[15:8]				
00B0	Run State Data Setting 18				RBUF5[7:0]				
00B1	Run State Data Setting 19				RBUF6[23:16]				
00B2	Run State Data Setting 20				RBUF6[15:8]				
00B3	Run State Data Setting 21				RBUF6[7:0]				
00B4	Run State Data Setting 22				RBUF7[23:16]				
00B5	Run State Data Setting 23				RBUF7[15:8]				
00B6	Run State Data Setting 24				RBUF7[7:0]				
00B7	Run State Data Setting 25				RBUF8[23:16]				
00B8	Run State Data Setting 26				RBUF8[15:8]				
00B9	Run State Data Setting 27				RBUF8[7:0]				
00BA	Run State Data Setting 28				RBUF9[23:16]				
00BB	Run State Data Setting 29				RBUF9[15:8]				
00BC	Run State Data Setting 30				RBUF9[7:0]				
00BD	Run State Data Setting 31				RBUFA[23:16]				
00BE	Run State Data Setting 32				RBUFA[15:8]				
00BF	Run State Data Setting 33				RBUFA[7:0]				
00C0	Run State Data Setting 34				RBUFB[23:16]				
00C1	Run State Data Setting 35				RBUFB[15:8]				
00C2	Run State Data Setting 36				RBUFB[7:0]				
00C3	Run State Data Setting 37				RBUFC[23:16]				
00C4	Run State Data Setting 38				RBUFC[15:8]				
00C5	Run State Data Setting 39				RBUFC[7:0]				
00C6	Run State Data Setting 40				RBUFD[23:16]				
00C7	Run State Data Setting 41				RBUFD[15:8]				
00C8	Run State Data Setting 42				RBUFD[7:0]				
00C9	Run State Data Setting 43				RBUFE[23:16]				
00CA	Run State Data Setting 44				RBUFE[15:8]				
00CB	Run State Data Setting 45				RBUFE[7:0]				
00CC	Run State Data Setting 46				RBUFF[23:16]				
00CD	Run State Data Setting 47				RBUFF[15:8]				
00CE	Run State Data Setting 48				RBUFF[7:0]				
R/W		R/W							
Default		RBUFx[23:0] = 000000H							

RBUFx[23:0]: RAM Write Data value during RUN state

Default: 000000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00CF	CRAM Operation during Run State	0	0	0	0	0	0	0	RUNC
	R/W	R	R	R	R	R	R	R	R/W
	Default	0	0	0	0	0	0	0	0

RUNC: CRAM Write Execution during RUN state

0: Write wait (default)

1: Write execute

RUNC bit returns to “0” automatically after finishing CRAM write.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D0	OFFREG Operation during Run State	0	0	0	0	0	0	0	RUNO
	R/W	R	R	R	R	R	R	R	R/W
	Default	0	0	0	0	0	0	0	0

RUNO: OFREG Write Execution during RUN state

0: Write wait (default)

1: Write execute

RUNO bit returns to “0” automatically after finishing OFREG write.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D1	PRAM Ready	0	0	0	0	0	0	0	PRIF
	R/W	R	R	R	R	R	R	R	R/W
	Default	0	0	0	0	0	0	0	0

PRIF: PRAM Write Command

0: PRAM Data Transmit Preparation Complete (default)

1: PRAM Data Transmit Preparation

PRIF bit is automatically updated to “0” after transmitting PRAM data.

The read result of PRIF bit is always “0”.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D2	MIR Hold	0	0	0	0	0	0	0	MIRH
	R/W	R	R	R	R	R	R	R	R/W
	Default	0	0	0	0	0	0	0	0

MIRH: MIR Read Register Hold

0: Always Updated (default)

1: Stop Updating

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D3	CRC Result 1					CRCO[15:8]			
00D4	CRC Result 2					CRCO[7:0]			
	R/W					R			
	Default					0000H			

CRCO[15:0]: CRC Result

Default: 0000H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D5	Device Code					DEVICECODE[7:0]			
	R/W					R			
	Default					61H			

DEVICECODE[7:0]: Device Code

Default: 61H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D6	Reserved	0	0	0	0	0	0	0	0
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D7	Jack Detection Event	0	0	0	0	0	VWE	JDE	RCE
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

RCE: Remote Control Event

0: Not detection (default)

1: Detection

JDE: Jack Detection Event

0: Not detection (default)

1: Detection

VWE: Voice Wakeup Event

0: Not detection (default)

1: Detection

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D8	Jack Detection Status	MDTE	0	0	0	0	VDF	JDS	RCS
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

RCS: Remote Control Status Bit

0: Button Release (default)

1: Button Push

JDS: Jack Detection Status Bit

0: Removal (default)

1: Insertion

VDF: Voice Detect Flag

0: No Voice Detection (default)

1: Voice Detection

VDF bit condition is set by VDFS[1:0] bits.

MDTE: Microphone Detection Status

0: No Microphone (Headphone) (default)

1: Microphone (Headset)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00D9	MIC Level Detection	0	0	0	0			CPL[3:0]	
	R/W	R	R	R	R			R	
	Default	0	0	0	0			0H	

CPL[3:0]: Output Data of Comparator for Remote Control ([Table 68](#))

Default: 0H

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00DA	Test Register 2				TO[7:0]				
	R/W				R				
	Default				FCH				

TO[7:0]: Test Register

Default: FCH

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00DB	SRC Status	0	0	0	0	SRCSTD	SRCSTC	SRCSTB	SRCSTA
	R/W	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0

SRCSTD/C/B/A: SRCD/C/B/A Status

0: Normal Operation or SRC power-down (Default)

1: Error

SRC operation status can be checked by reading these registers after power-up the SRC.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00DC	MIR1 Register 1					MIR1[31:24]			
00DD	MIR1 Register 2					MIR1[23:16]			
00DE	MIR1 Register 3					MIR1[15:8]			
00DF	MIR1 Register 4					MIR1[7:0]			
00E0	MIR2 Register 1					MIR2[31:24]			
00E1	MIR2 Register 2					MIR2[23:16]			
00E2	MIR2 Register 3					MIR2[15:8]			
00E3	MIR2 Register 4					MIR2[7:0]			
00E4	MIR3 Register 1					MIR3[31:24]			
00E5	MIR3 Register 2					MIR3[23:16]			
00E6	MIR3 Register 3					MIR3[15:8]			
00E7	MIR3 Register 4					MIR3[7:0]			
00E8	MIR4 Register 1					MIR4[31:24]			
00E9	MIR4 Register 2					MIR4[23:16]			
00EA	MIR4 Register 3					MIR4[15:8]			
00EB	MIR4 Register 4					MIR4[7:0]			
R/W						R			
Default						MIRx[31:0] = 00000008H			

MIRx[31:0]: MIR Register (Monitor of internal signal of DSP)

Default: 00000008H

x: 1~4

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00EC ~ 00EF	Reserved	0	0	0	0	0	0	0	0
R/W		R	R	R	R	R	R	R	R
Default		0	0	0	0	0	0	0	0

\* Refer to the VAD application note for details.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F0	VAD Setting 1	0	0	AWSRCA	FBYP	VADE	DLYE	AWE	DLE
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F1	VAD Setting 2				PT[7:0]				
	R/W				R/W				
	Default				00H				

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F2	VAD Setting 3			TSW[3:0]		0		AT[2:0]	
	R/W			R/W		R/W		R/W	
	Default			0000		0		000	

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F3	VAD Setting 4				ONGT[7:0]				
	R/W				R/W				
	Default				00H				

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F4	VAD Setting 5				OFFGT[7:0]				
	R/W				R/W				
	Default				00H				

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F5	VAD Setting 6	0	0	0			MINTH[12:8]		
00F6	VAD Setting 7				MINHT[7:0]				
	R/W				R/W				
	Default				0000H				

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F7	VAD Setting 8		VDFS[1:0]		NVFS[1:0]		NLDTH[11:8]		
00F8	VAD Setting 9				NLDTH[7:0]				
	R/W				R/W				
	Default				00H				

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00F9	VAD Setting 10	0		VLS[2:0]		0		VRS[2:0]	
	R/W	R/W		R/W		R/W		R/W	
	Default	0		000		0		000	

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00FA	VAD HPF Setting 1				B0[15:8]				
00FB	VAD HPF Setting 2				B0[7:0]				
00FC	VAD HPF Setting 3				B1[15:8]				
00FD	VAD HPF Setting 4				B0[7:0]				
00FE	VAD HPF Setting 5				A1[15:8]				
00FF	VAD HPF Setting 6				A1[7:0]				
	R/W				R/W				
	Default				0000H				

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0100	CREG0 Setting 1				CREG0[7:0]				
0101	CREG0 Setting 2				CREG0[15:8]				
0102	CREG1 Setting 1				CREG1[7:0]				
0103	CREG1 Setting 2				CREG1[15:8]				
0104	CREG2 Setting				CREG2[7:0]				
0105	CREG3 Setting				CREG3[7:0]				
0106	CREG4 Setting				CREG4[7:0]				
0107	CREG5 Setting				CREG5[7:0]				
0108	CREG6 Setting				CREG6[7:0]				
0109	CREG7 Setting				CREG7[7:0]				
	R/W				R/W				
	Default				0000H				

## 10. Recommended External Circuits

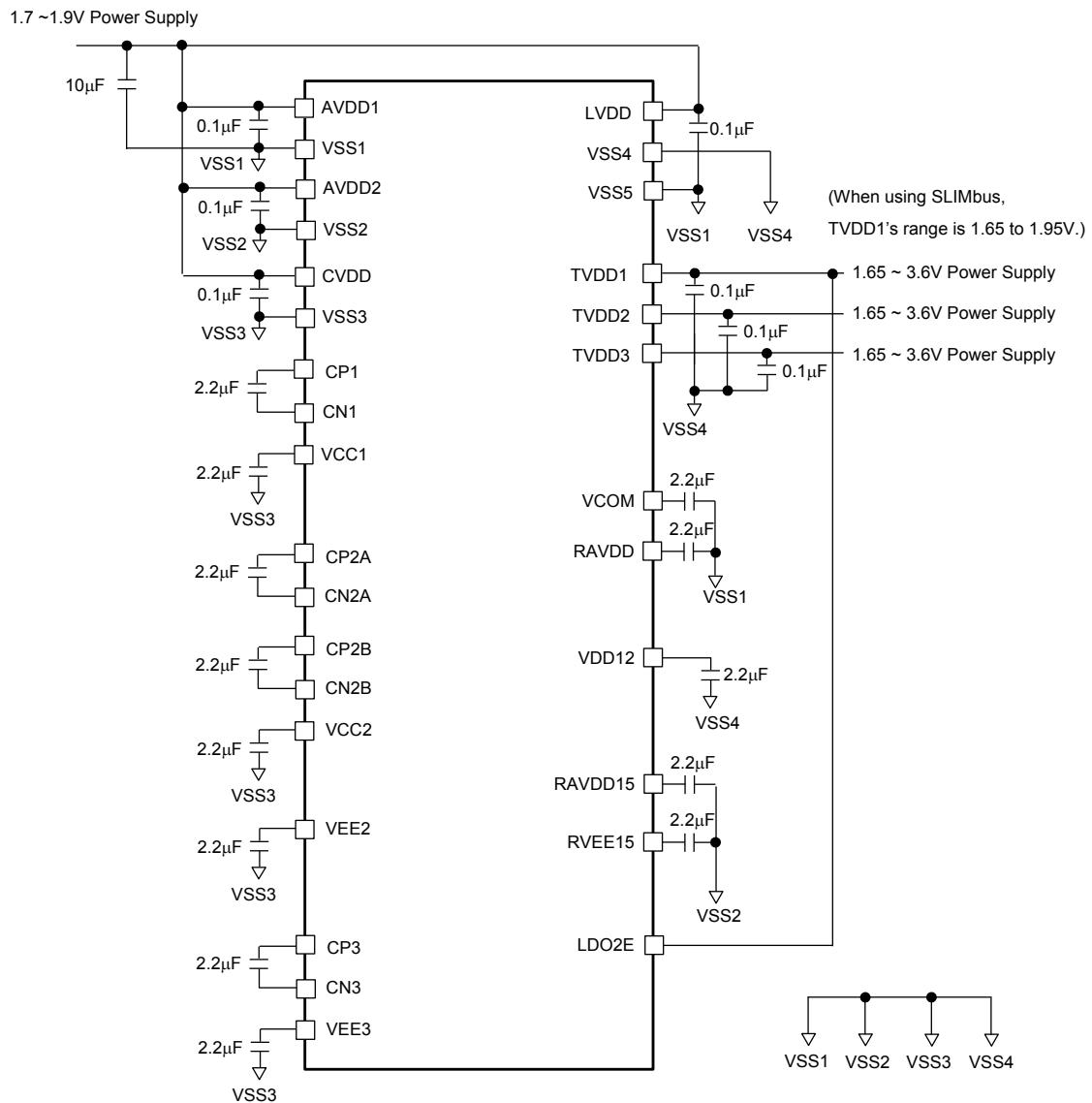


Figure 83. Connection example of Power Supply, Charge Pump, LDO (LDO2E pin = "H"; LDO2 Enable)

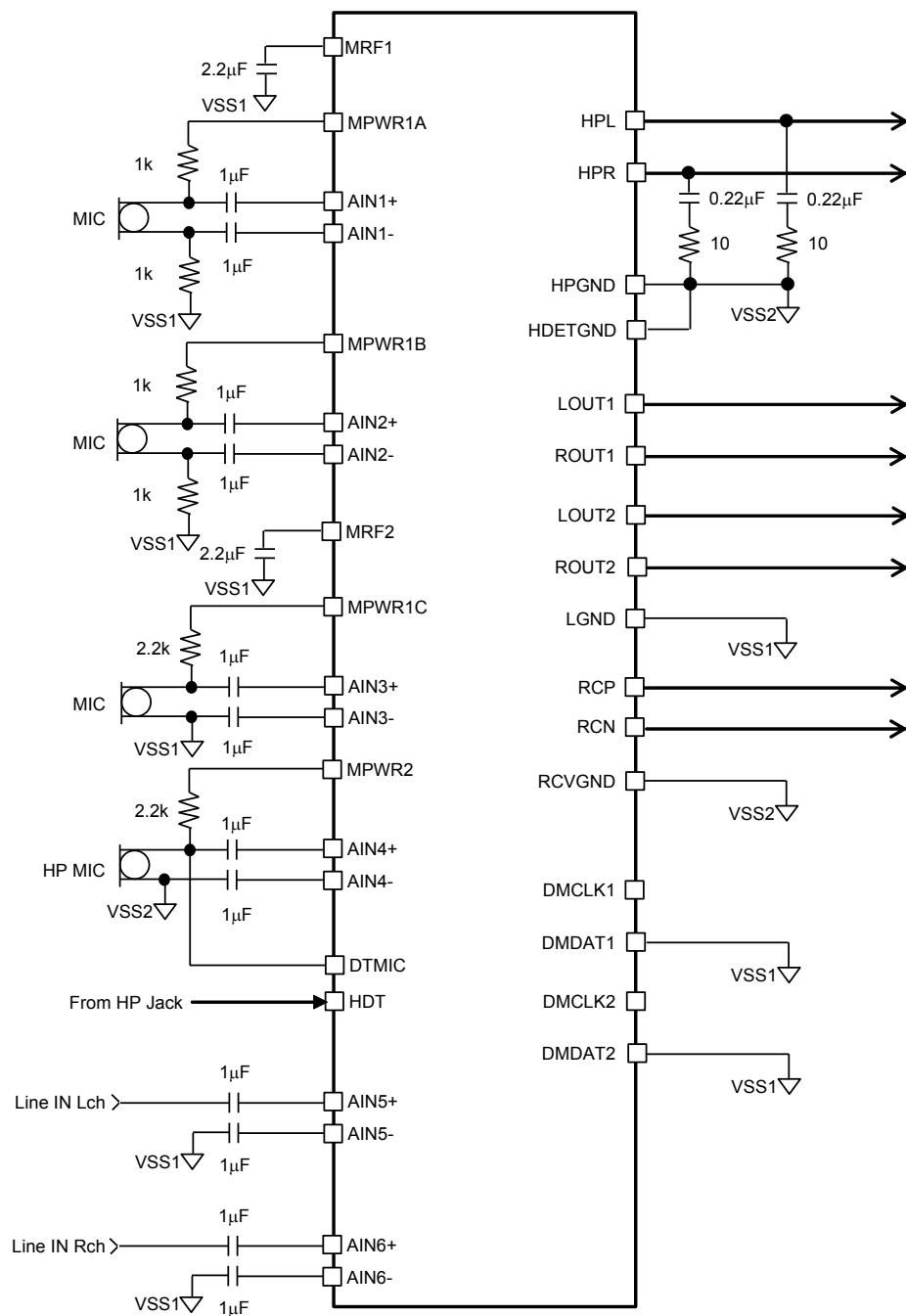


Figure 84. Connection example of analog input/output circuit  
 (AIN1/2: Differential Microphone, AIN3/4: Single-ended Microphone, AIN5/6: Line Input.  
 Digital MIC: Not use)

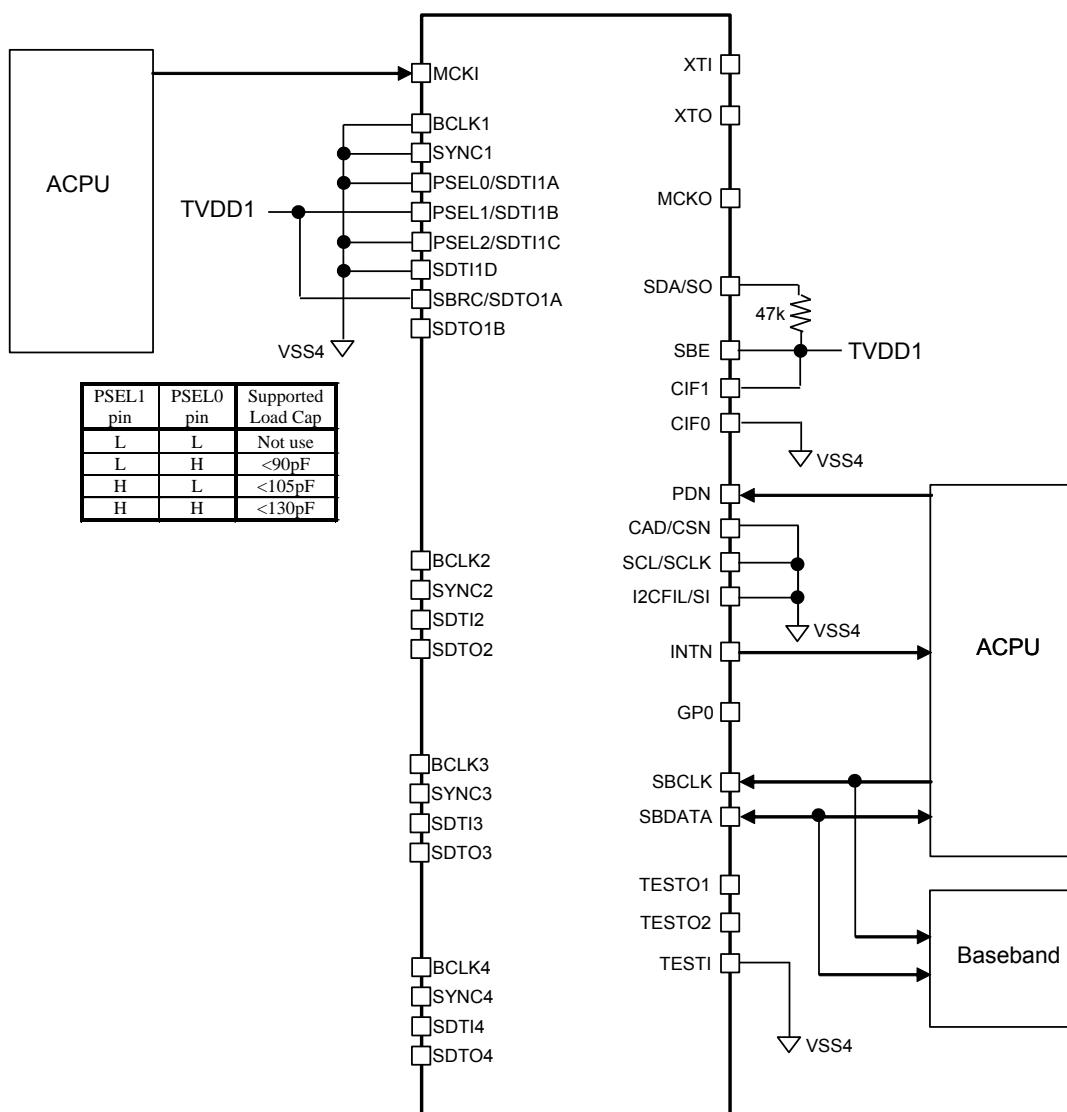


Figure 85. Connection Example of Digital Block (Using SLIMbus interface)

## Connection Conditions

- ACPU(Master) - CODEC (Slave), MCKI Input
- SLIMbus Enable
- X'tal Disable
- Not using the SPI I/F

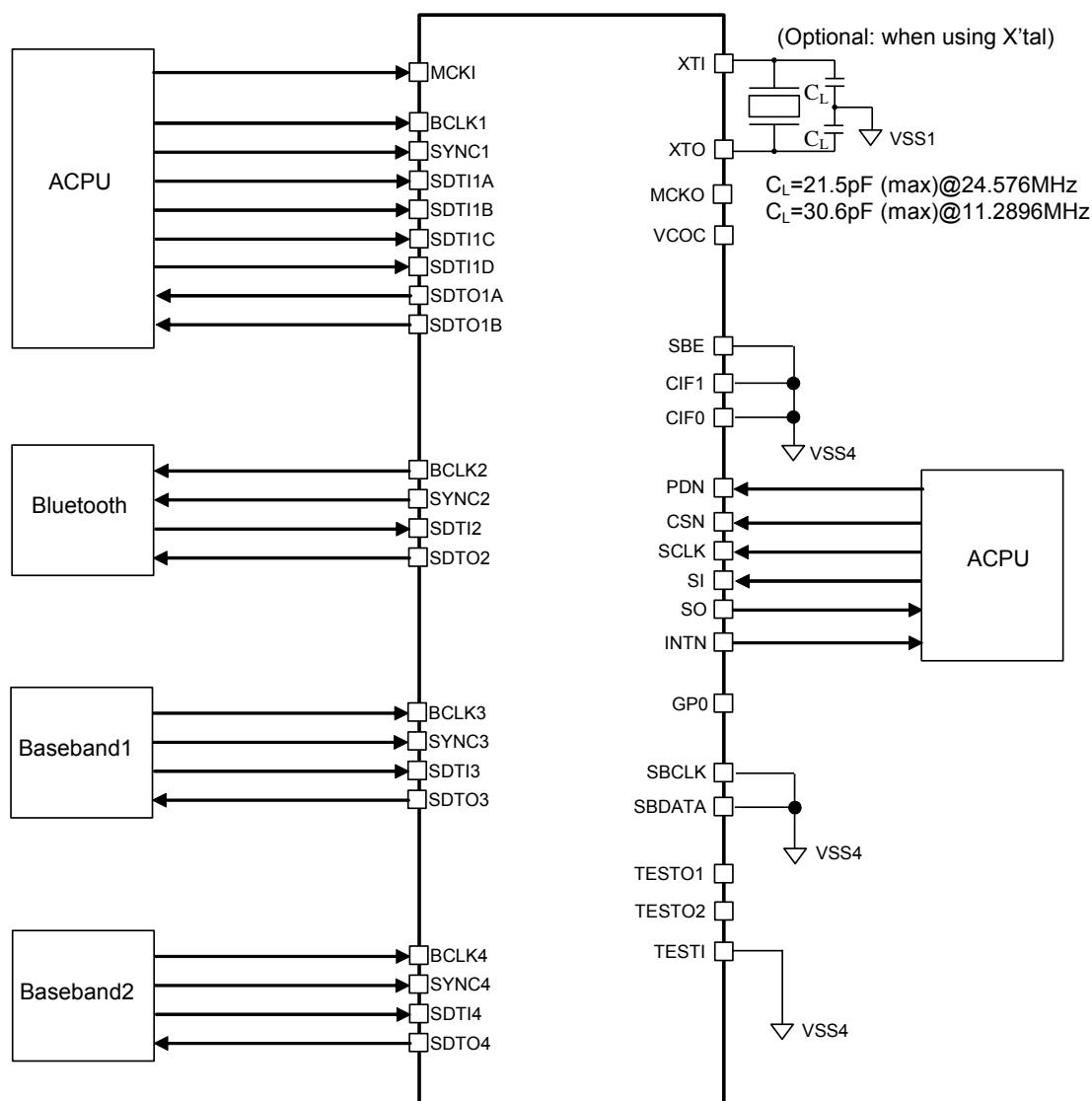


Figure 86. Connection Example of Digital Block (Using I2S/SPI interface)

## Connection Conditions

- ACPU(Master) - CODEC (Slave), MCKI Input
- Bluetooth (Slave) - CODEC (Master)
- Baseband1(Master) - CODEEC (Slave)
- Baseband2(Master) - CODEEC (Slave)
- SPI I/F Enable
- X'tal Enable
- Not using the SLIMbus.

## 1. Grounding and Power Supply Decoupling

The AK4961 requires careful attention to power supply and grounding arrangements. When LDO2 is disable (LDO2E pin = "L"), AVDD1/2, CVDD, LVDD and TVDD1/2/3 must be powered up before VDD12 (The power-up sequence among AVDD1/2, CVDD, LVDD and TVDD1/2/3 is not critical.). The PDN pin should be held "L" when power supplies are turning on. The PDN pin is allowed to be "H" after all power supplies are applied and settled.

To power down the AK4961, set the PDN pin to "L" first and power down VDD12 before AVDD, CVDD, LVDD and TVDD1/2/3 if a 1.2V external power supply is applied (LDO2E pin = "L"). (Power-up sequence of AVDD, CVDD, LVDD and TVDD1/2/3 is not critical.)

To avoid pop noise of analog outputs, the AK4961 should be operated along the following recommended power-up/down sequence.

### 1) Power-up

- The PDN pin should be held "L" when power supplies are turning on. The AK4961 can be reset by keeping the PDN pin "L" for 1ms (@ LDO2E pin = "H") or longer after all power supplies are applied and settled. Then release the reset by setting the PDN pin to "H".

### 2) Power-down

- Each of power supplies can be powered OFF after the PDN pin is set to "L".

VSS1, VSS2, VSS3, VSS4 and VSS5 of the AK4961 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near the AK4961 as possible. Especially, decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

## 2. Voltage Reference

VCOM is a signal ground of this chip. A  $2.2\mu\text{F}$  ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current is allowed to be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4961.

## 3. Charge Pump

Flying capacitor (e.g. between CP2A and CN2A) and decoupling capacitor between the Negative Power Output (e.g. VEE2 pin) and ground pin (e.g. VSS2) should be  $2.2\mu\text{F}\pm50\%$  low ESR ceramic capacitor. These capacitors must be connected as close to the pins as possible. No load current may be drawn from the Negative Power Output pin (e.g. VEE2 pin).

## 4. Analog Inputs

The input signal range scales with  $2.02 \times \text{AVDD Vpp (typ.)} @ \text{MIC-Amp} = 0\text{dB}$ , centered around the internal common voltage (typ. 2.2V). The input signal must be AC coupled using a capacitor. The cut-off frequency ( $f_c$ ) is  $1/(2\pi RC)$ . An AIN<sub>x</sub>- pin must be connected to VSS1 via a capacitor with the same capacitance as the AIN+ pin.

## 5. Analog Outputs

Headphone outputs (HPL/HPR pins) are single-ended and centered at 0V. They should be directly connected to a headphone without AC coupling.

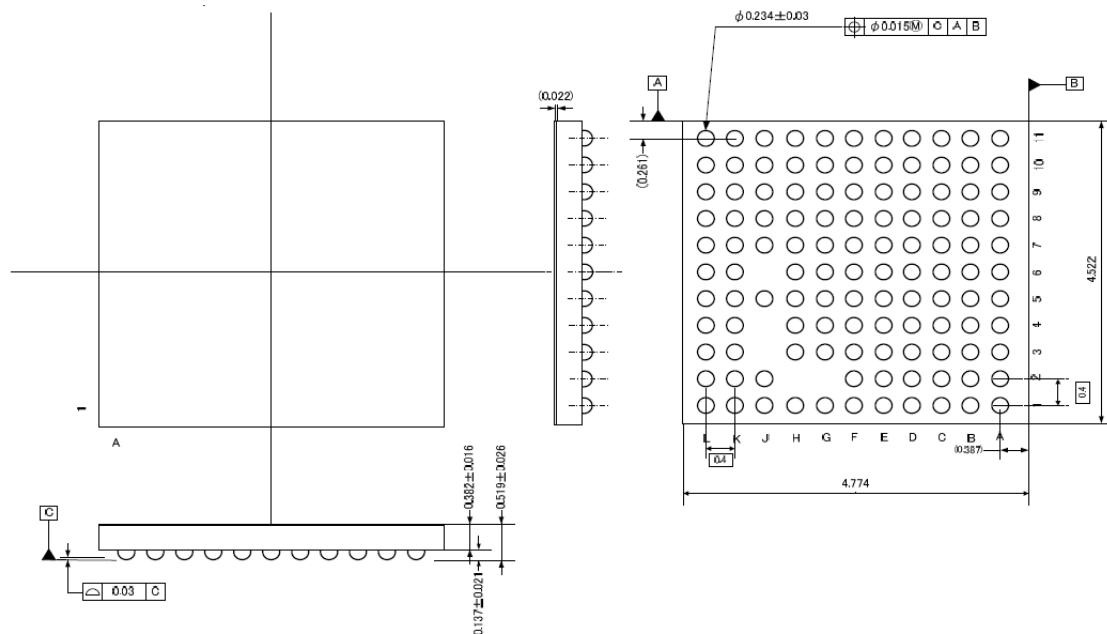
Lineout1/2 outputs are single-ended and centered at 0V or differential (Differential mode is only supported by Lineout2). When Lineout1/2 outputs are connected to a Speaker-Amp, be aware of the common voltage of the Speaker-Amp, and connect an AC coupling capacitor if necessary.

Receiver outputs (RCP/RCN pins) are differential and centered at 0V. They should be directly connected to a receiver without AC coupling.

## 11. Package

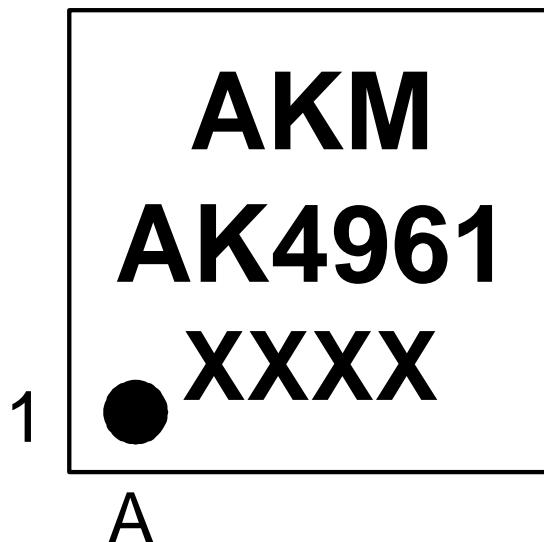
### ■ Outline Dimensions

#### 116 pin CSP Package



### ■ Material & Lead finish

Package molding compound: Epoxy, Halogen (bromine and chlorine) free  
Solder ball material: SnAgCuNi

**■ Marking**

XXXX: Date code (4 digit)  
Pin #A1 indication

**Revision History**

Date (Y/M/D)	Revision	Reason	Page	Contents
14/06/10	00	First Edition		

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### Restriction of Hazardous Substances (RoHS): Directive 2002/95/EC

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December 2009