**CPU V8 datasheet**

1 Memory Map

|  |  |  |  |
| --- | --- | --- | --- |
| Bus Slave | Address Range | [31] [30][29] | Allocation |
| 0 | 0x00000000-0x1FFFFFFF | 3`b000 | Internal ROM |
| 1 | 0x20000000-0x3FFFFFFF | 3`b001 | Internal SPM |
| 2 | 0x40000000-0x5FFFFFFF | 3`b010 | Timer |
| 3 | 0x60000000-0x7FFFFFFF | 3`b011 | UART |
| 4 | 0x80000000-0x9FFFFFFF | 3`b100 | GPIO |
| 5 | 0xA0000000-0xBFFFFFFF | 3`b101 | N/A |
| 6 | 0xC0000000-0xDFFFFFFF | 3`b110 | N/A |
| 7 | 0xE0000000-0xFFFFFFFF | 3`b111 | N/A |

2 Bus

|  |  |
| --- | --- |
| Master | |
| Number | Module |
| 0 | CPU IF Stage |
| 1 | CPU MEM Stage |
| 2 | N/A |
| 3 | N/A |

|  |  |
| --- | --- |
| Slave | |
| Number | Module |
| 0 | Internal ROM |
| 1 | Internal RAM |
| 2 | Timer |
| 3 | UART |
| 4 | GPIO |
| 5 | N/A |
| 6 | N/A |
| 7 | N/A |

3IRQ

|  |  |
| --- | --- |
| CPU irq number | Description |
| IRQ0 | Timer |
| IRQ1 | UART Send Complete |
| IRQ2 | UART Receive Complete |
| IRQ3 | N/A |
| IRQ4 | N/A |
| IRQ5 | N/A |
| IRQ6 | N/A |
| IRQ7 | N/A |

4 Exception & Interruption

|  |  |  |  |
| --- | --- | --- | --- |
| Exception or Interruption name | Description | Root Cause | Exception Code |
| Normal | no exception | - | 0x0 |
| Interruption | External Interruption | - | 0x1 |
| Undefined Instruction | Undefined Instruction In Decode Stage | - | 0x2 |
| Arithmetic Overflow | Arithmetic Overflow | ADDSR,ADDSI,SUBSR | 0x3 |
| Address not Aligned | Address not Aligned | LDW,STW | 0x4 |
| Trap | Run Trap Instruction | TRAP | 0x5 |
| CPU Mode Violation | User Mode Access C registers | RDCR,WRCR,EXRT | 0x6 |

5 CPU control registers

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register number | Description | Access | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | Status | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | IE | EM |
| 1 | Previoous Status | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | IE | EM |
| 2 | PC | R | PC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 |
| 3 | EPC | R/W | EPC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 |
| 4 | EVector | R/W | EXCEPTION\_VECTOR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | 0 | 0 |
| 5 | E | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | D | CODE | | |
| 6 | IRQ Mask | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | MASK | | | | | | | |
| 7 | IRQ Request | R | N/A | | | | | | | | | | | | | | | | | | | | | | | | IRQ | | | | | | | |
| 8-28 | N/A | - |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 29 | ROM | R | ROM SIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 30 | RAM | R | RAM SIZE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 31 | CPU | R | YEAR | | | | | | | | MONTH | | | | | | | | VER | | | | | | | | REV | | | | | | | |

6 Io Peripherals

Timer

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register number | Description | Offset address | Acess | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | 0 | |
| 0 | Control | 0x0 | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | M | | S | |
| 1 | IRQ | 0x4 | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | I | |
| 2 | Expire Number | 0x8 | R/W | EXPIRE VALUE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | Counter | 0xC | R/W | COUNTER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

UART

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register number | Description | Offset address | Acess | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | Control | 0x0 | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | | | | | TB | RB | TI | RI |
| 1 | Transceiver | 0x4 | R/W | N/A | | | | | | | | | | | | | | | | | | | | | | | | DATA | | | | | | | |

GPIO

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Register number | Description | Offset address | Acess | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | Input | 0x0 | R | INPUT\_DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Output | 0x4 | R/W | OUTPUT\_DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | InOut | 0x8 | R/W | INOUT\_DATA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3 | InOut Direction | 0xC | R/W | INOUT\_DIR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |