EE227 Digital Logic Design

Friday, June 05, 2020

Course Instructor

Engr. Muhammad Abdullah
Mr. Waheed Ahmad
Engr. Amir Zahoor

Serial No:

2nd Mid Term Exam
Spring Semester 2020
Max Time:
1 Hr 15 Mins
Max Marks: 40
Exam Weight (Out of 100). 10

_____	_____
Roll No	Section

Guidelines for Submission:

1. You should submit only one PDF document and **all text should be handwritten**. Equations, figures should be hand draw.
2. You must submit your solution before due time via **Google Classroom/Slate**. Submissions submitted after the due time shall not be considered.
3. If you don't finish every part of a question, don't worry! You can still submit what you've done to get marks based on your efforts.
4. In case of copied or plagiarized solutions in exam Or If a student provided help to another student during exam both will be awarded "F" grade and it will affect the student CGPA.
5. Viva of any student can be conducted by the instructor after conducting an online exam in case of any doubt.
6. This document should be submitted through LMS (**Google Classroom)**. But in worst case, you can email it within the deadline.

Question	1	2	3	4	Total
Points	10	10	10	10	40
Score					

Question No. 1 **(10)**

Using a Karnaugh map, convert the following standard POS expression into
(a) A minimum SOP expression**.**
(b) A minimum POS expression,

$$\mathbf{F} = (\overline{\mathbf{A}} + \overline{\mathbf{B}} + \mathbf{C} + \mathbf{D})(\mathbf{A} + \overline{\mathbf{B}} + \mathbf{C} + \mathbf{D})(\mathbf{A} + \mathbf{B} + \mathbf{C} + \overline{\mathbf{D}})(\mathbf{A} + \mathbf{B} + \overline{\mathbf{C}} + \overline{\mathbf{D}})(\overline{\mathbf{A}} + \mathbf{B} + \mathbf{C} + \overline{\mathbf{D}})(\mathbf{A} + \mathbf{B} + \overline{\mathbf{C}} + \mathbf{D})$$

Question No. 2 **(10)**

Design a combinational circuit that can detect whether the 3-bit input binary number is even, odd or prime number.
(a) Draw the truth table for the design problem
(b) Implement the circuit using 3 × 8 Decoder

Question No. 3 **(10)**

Design and Implement Odd Parity Generator Circuit, combinational circuit that checks the 4-bit data and generates a parity bit along with data bits.

Question No. 4 **(10)**

Design and implement a combinational circuit that can detect BCD code which is either ‘divisible by 3 or 4’.
(a) Draw the truth table and circuit for the design problem
(b) Implement the circuit using 8 × 1 Multiplexer