EE227 – DLD Assignment 4

EE227 – Digital Logic Design

Assignment 4

Spring 2020

Instructor Name: Engr. Amir Zahoor

Instructions for Submission:

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- Partially or fully **copied assignments** will be marked as **zero**.
- You should submit only one PDF document and all text should be hand written. Equations,
- figures can only be hand written (all figures/equations can be pasted as images inside
- that document).
- Only **handwritten** solution.
- Late submissions are not allowed.
- Viva of any student can be conducted by the instructor after conducting an online
- exam in case of any doubt.
- You can submit your assignment during Google Classroom only.

Question Number 1

Design and implement Even parity generator for three bit number. Implement using S.O.P and P.O.S.

Question Number 2

Design and implement Odd parity generator circuit. Implement using S.O.P and P.O.S.

Question Number 3

Design and Implement BCD to 7- segment display circuit

Good Luck