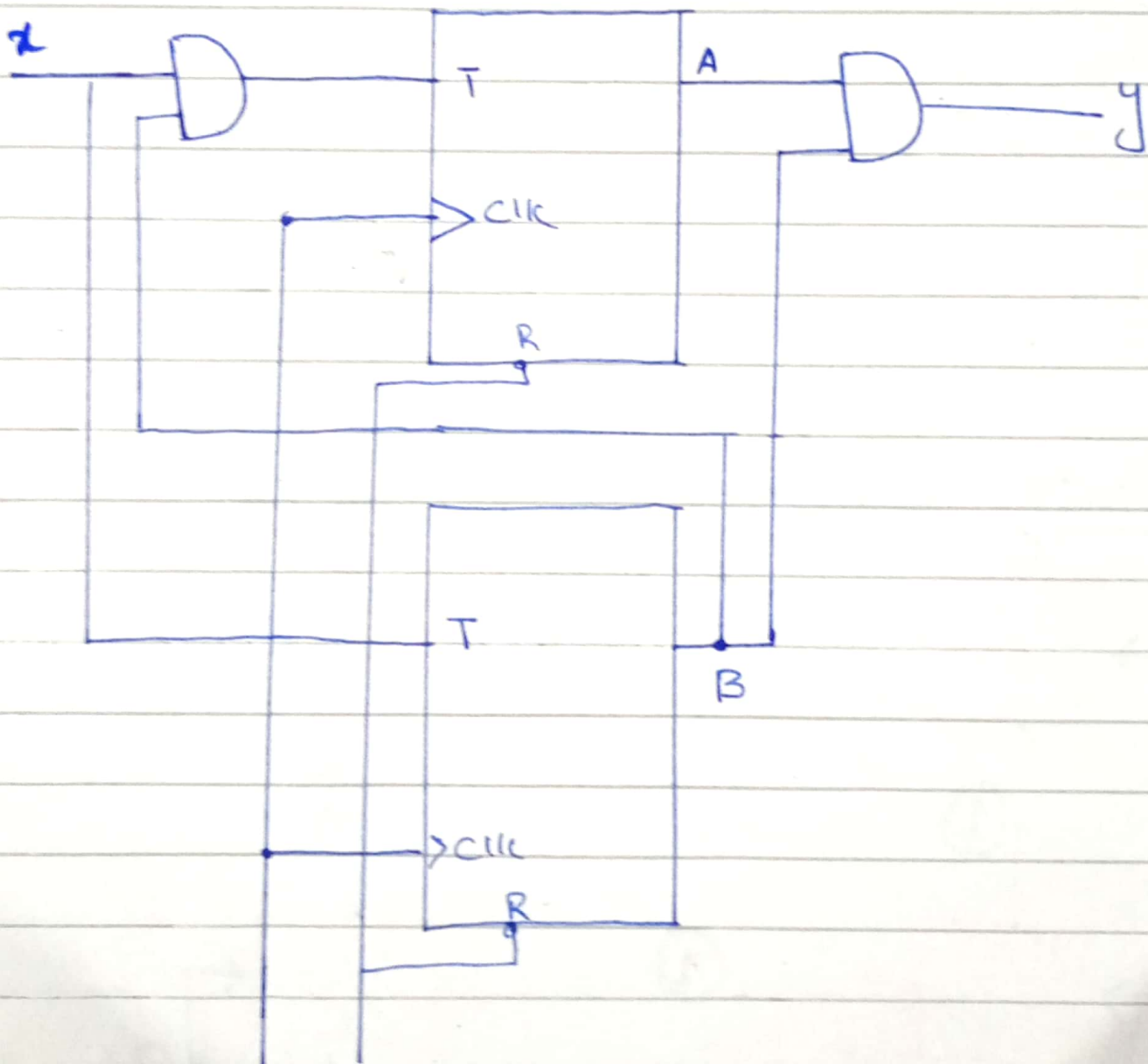


Qb12 05

19F-0228

Analysis of ~~clocked~~ sequential circuit
to write state table form, second
form also draw state diagram.



clock reset

Present State		Input x	Next State		Output y
A	B		A	B	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1 1	1	1
1	1	1	0	0	1

State Diagram

