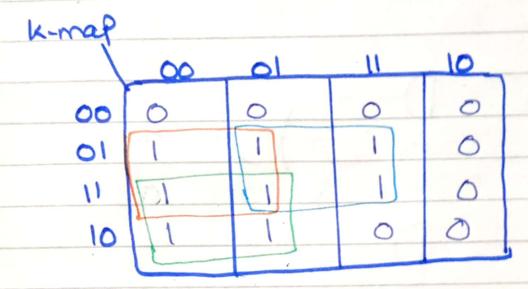




Draw NAND gate logic diagram.

F(A,B,C,D)= \(\Sigma\) (0,1,2,3,6,10,11,14)



Equation

