EE227 – Digital Logic Design

Assignment 3

Spring 2020

Instructor Name: Engr. Amir Zahoor

Instructions for Submission:

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- Partially or fully **copied assignments** will be marked as **zero**.
- You should submit only one PDF document and all text should be hand written. Equations,
- figures can only be hand written (all figures/equations can be pasted as images inside
- that document).
- Only **handwritten** solution.
- Late submissions are not allowed.
- Viva of any student can be conducted by the instructor after conducting an online
- exam in case of any doubt.
- You can submit your assignment **during Google Classroom only.**

Question Number 1

Design and implement a comparator circuit that compares two numbers A and B and each number have two bits. Please check for following condition :

a) A>B b) A<B c) A=B

Question Number 2

Design and implement a circuit that detect two consecutive 1's and implement through following way :

a) S.O.P and P.O.S b) NAND and NOR gate

Question Number 3

Design and implement a four bit Even Parity bit generator. Also, implement by S.O.P And P.O.S .

Good Luck