EE227 Digital Logic Design

Monday, July 20, 2020

Course Instructor

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Serial No:

Final Term Exam
Spring Semester 2020
Max Time:
3 Hours
Max Marks: 85
Exam Weight (Out of 100). 50

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Roll No	Section

Guidelines for Submission:

1. You should submit only one PDF document and **all text should be handwritten**. Equ ations, figures should be hand draw.
2. You must submit your solution before due time via **Google Classroom/Slate**. Submis sions submitted after the due time shall not be considered.
3. If you don't finish every part of a question, don't worry! You can still submit what you've done to get marks based on your efforts.
4. In case of copied or plagiarized solutions in exam Or If a student provided help to ano ther student during exam both will be awarded "F" grade and it will affect the student CGPA.
5. Viva of any student can be conducted by the instructor after conducting an online exa m in case of any doubt.
6. This document should be submitted through LMS (**Google Classroom)**. But in worst case, you can email it within the deadline.

Question	1	2	3	4	5	6	Total
Points	10	15	15	15	15	15	85
Score							

Question No. 1 **(10)**

Convert each of the following expressions into sum of products and product of sums:

a) $(u + xw)(x + u'v)$

b) $x' + x(x + y')(y + z')$

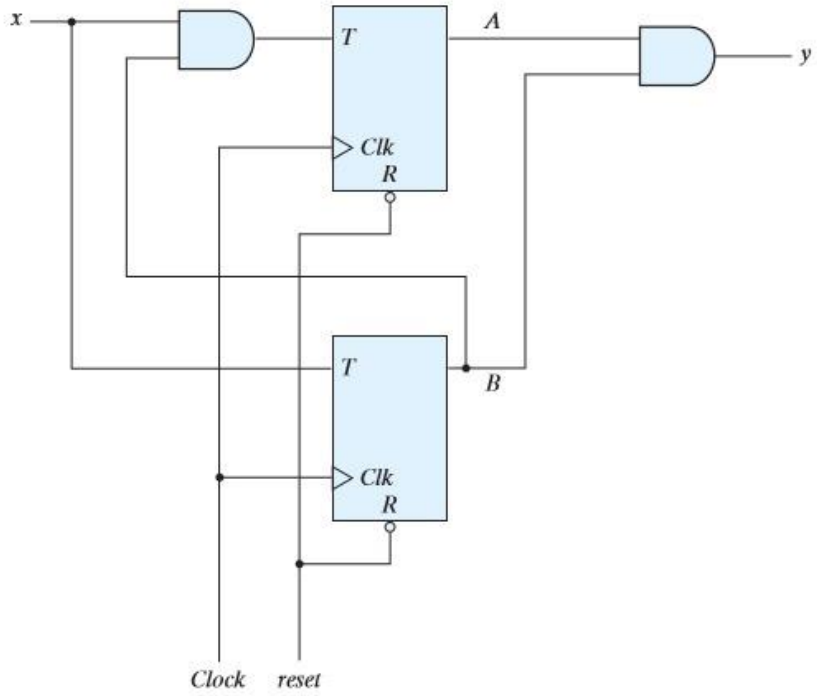
Question No. 2 **(15)**

Using Truth table and Karnaugh Maps, design a 7-segment Display combinational circuit. The circuit receives a BCD number input ABCD and displays decimal number 0 to 9 on a single digit 7-segment display. The six invalid combinations in BCD should be treated as don't care conditions.

Question No. 3 **(15)**

Analyze the given sequential circuit and answers following;

a) Write down the state equations?
b) Write down the first form of state table?
c) Write second form of State Table?
d) Draw the state diagram?



Question No. 4 **(15)**

Design a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. (You can consider 010 and 101 as don't care conditions)
Draw the logic diagram.

Question No. 5 **(15)**

Consider the following state table obtained from state transition diagram of a circuit with 2 inputs (x and y) and 1 output (F).

State	**Next State**				**Output (F)**			
	$xy = 00$	$xy = 01$	$xy = 10$	$xy = 11$	$xy = 00$	$xy = 01$	$xy = 10$	$xy = 11$
a	b	d	c	b	0	1	1	0
b	a	c	f	d	1	0	1	1
c	b	d	c	b	0	1	1	0
d	b	d	a	b	0	1	1	0
e	b	c	a	b	0	1	1	0
f	c	d	g	f	0	1	1	0
g	a	b	d	g	1	1	0	1

(a) Reduce the number of states in the state transition diagram **Marks: 10**
(b) Draw the reduced state transition diagram **Marks: 5**

Question No. 6 **(15)**

Design Moore type FSM having one input X and one output Y to detect the single pulse.
Desired functionality of the FSM is described as;

1. Whenever there is pulse on the input X, the output Y should go HIGH, and it should remain HIGH until new pulse appears on input X. (The duration of the pulse on input X can be of one or more clock cycles)
2. If output Y is at logic HIGH and new pulse appears on input X, then output Y first must go to logic LOW, and then it should again go to logic HIGH and should remain at logic HIGH until next pulse appears on input X.

For your convenience, the block diagram of FSM and sample input 'X' and sample output 'Y' is shown below;