

第二章 组合逻辑.

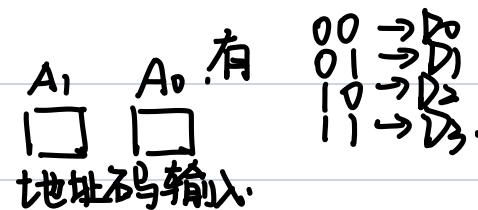
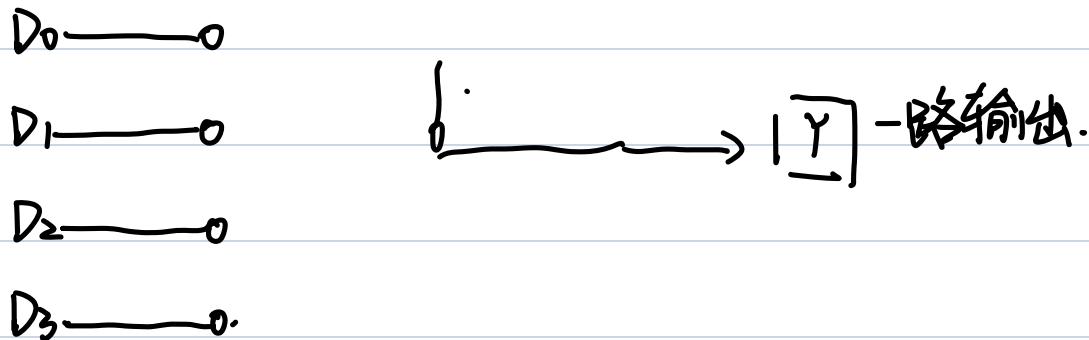
1、

数据选择器与分配器.

多输入

单输出.

4选1 数据选择器工作示意图.



输入信号 n 个与地址码 n 个函数关系 $N = 2^n$.

例 使用与或门设计一个4选1数据选择器.

具有使能控制端. 控制信号为1, 不工作,

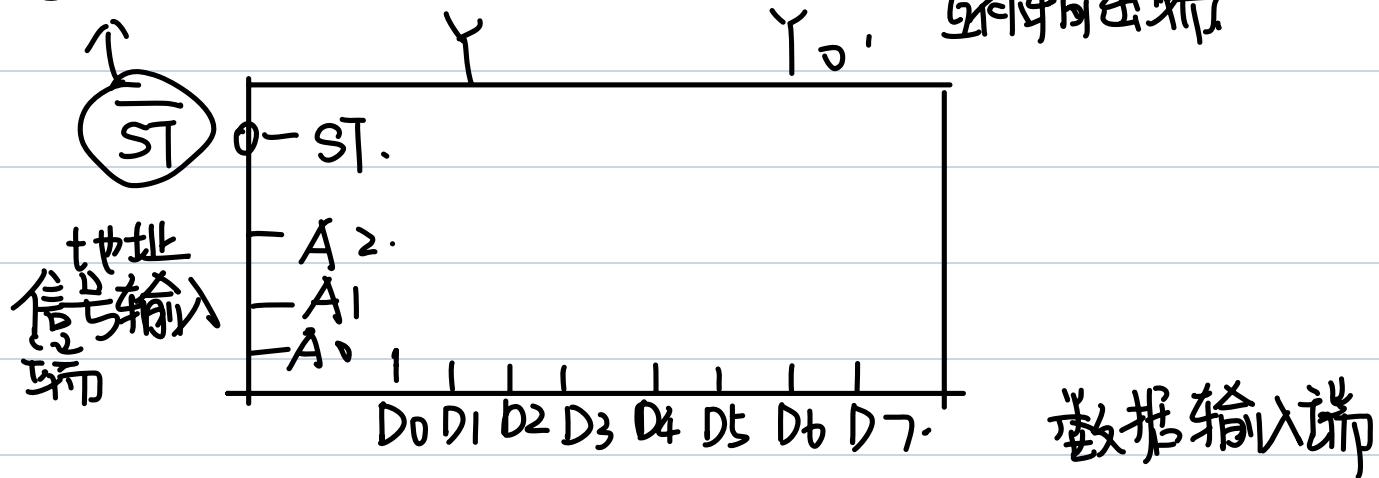
控制信号为0 处于工作.

输入				输出				
S/T	A ₁	A ₀		D ₀	D ₁	D ₂	D ₃	Y
1	X	X		X	X	XX		0
0	0	0		1	X	XX		1
0	0	1		X	1	XX		1
0	1	0		X	X	1X		1
0	1	1		X	X	X1		1

→ 为0为1不影响输出

$$Y = (D_0 \bar{A}_1 \bar{A}_0 + D_1 \bar{A}_1 A_0 + D_2 A_1 \bar{A}_0 + D_3 A_1 A_0) \overline{ST}$$

8选1数据选择器
选通使能端



功能表

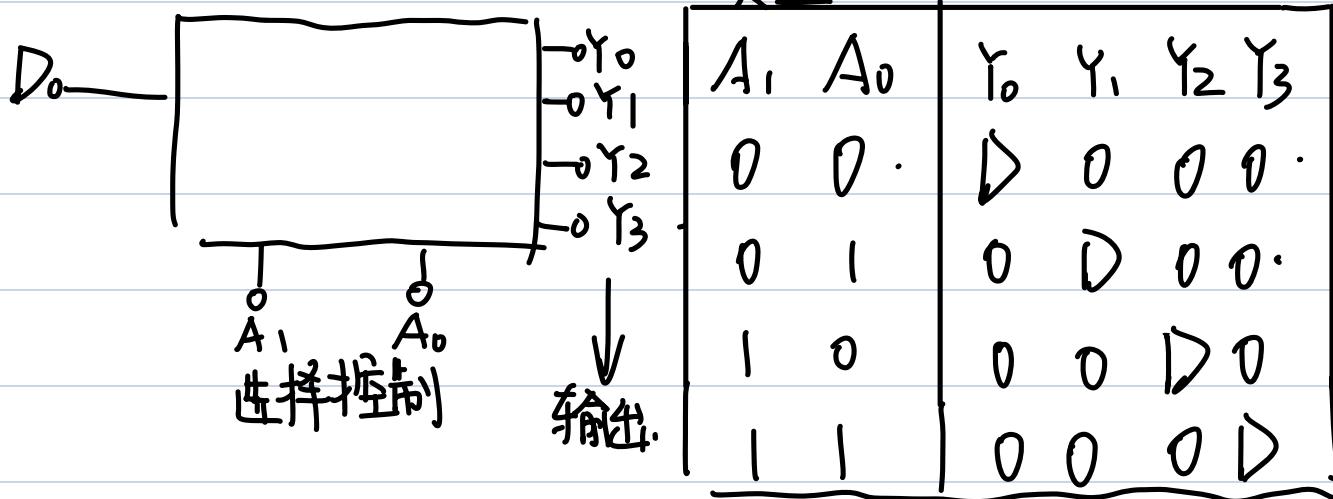
输入			输出	
\overline{ST}	A_2	A_1	Y	\overline{Y}
1	x	x	x	0 1
0	0	0	0	$D_0 \overline{D_0}$
0	0	0	1	$D_1 \overline{D_1}$
0	0	1	0	$D_2 \overline{D_2}$
0	0	1	1	$D_3 \overline{D_3}$
0	1	0	0	$D_4 \overline{D_4}$
0	1	0	1	$D_5 \overline{D_5}$
0	1	1	0	$D_6 \overline{D_6}$

0 | 1 | 1. | D₇ | D₇' |

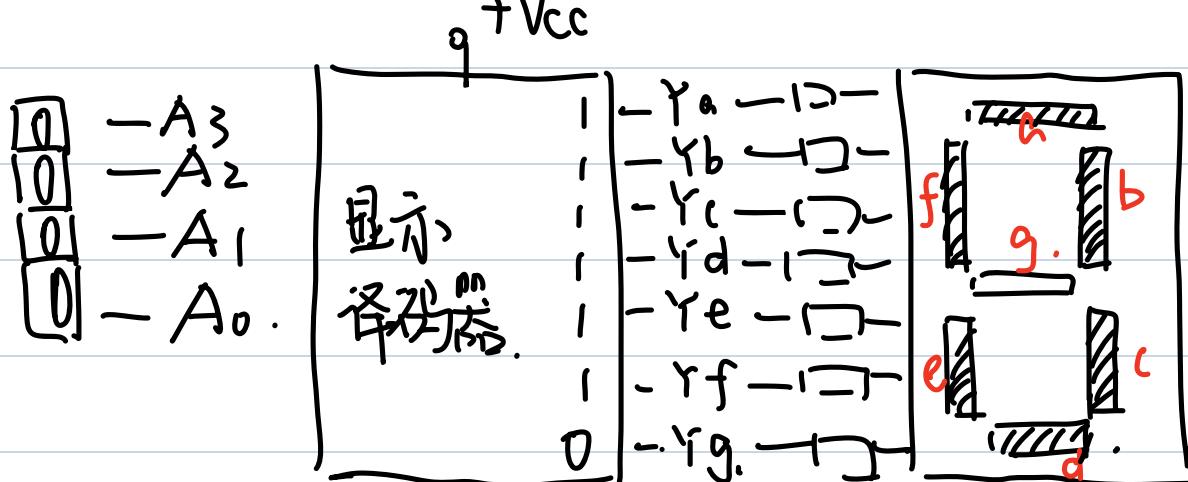
$$Y = D_0 A_2 \bar{A}_1 \bar{A}_0 + D_1 \cdot \bar{A}_2 \bar{A}_1 A_0 + D_2 \bar{A}_2 A_1 \bar{A}_0 \\ + D_3 \bar{A}_2 A_1 A_0 + D_4 A_2 \bar{A}_1 \bar{A}_0 + D_5 A_2 \bar{A}_1 A_0 \\ + D_6 A_2 A_1 \bar{A}_0 + D_7 A_2 A_1 A_0.$$

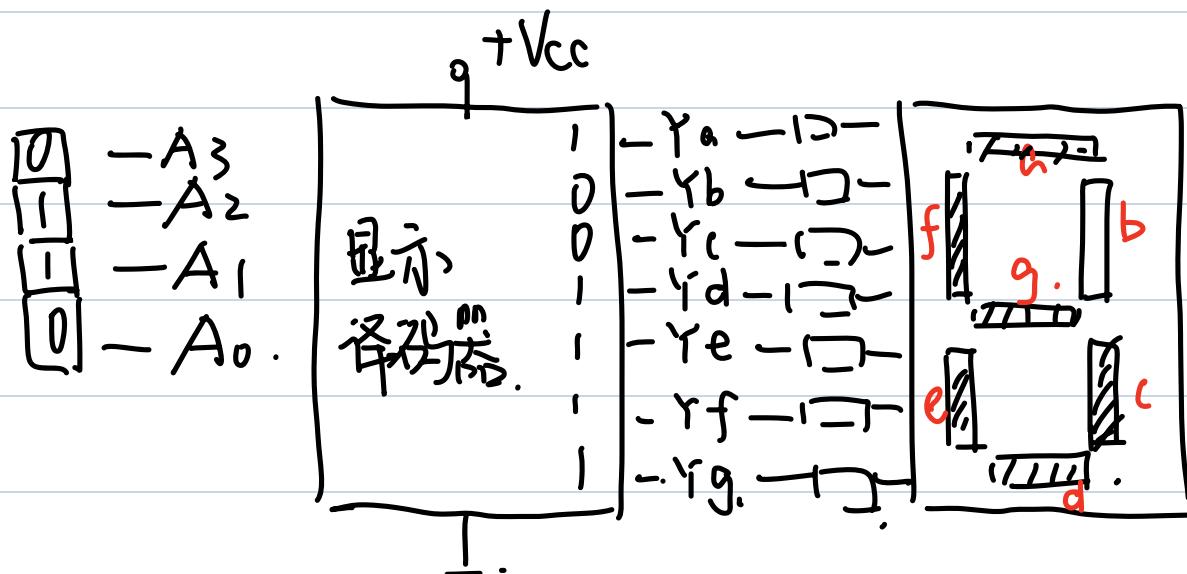
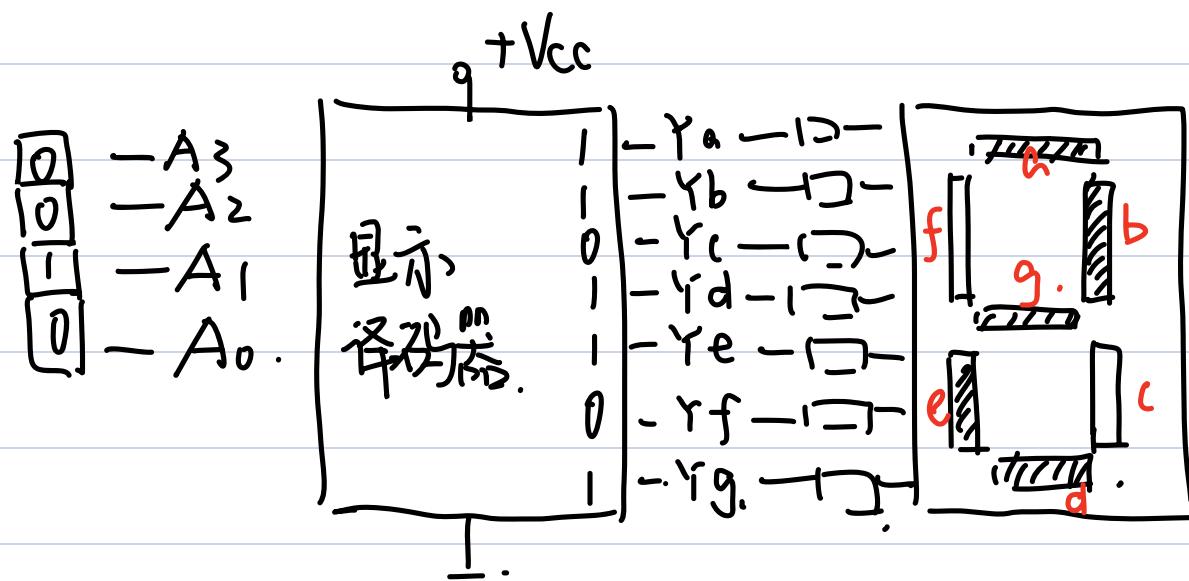
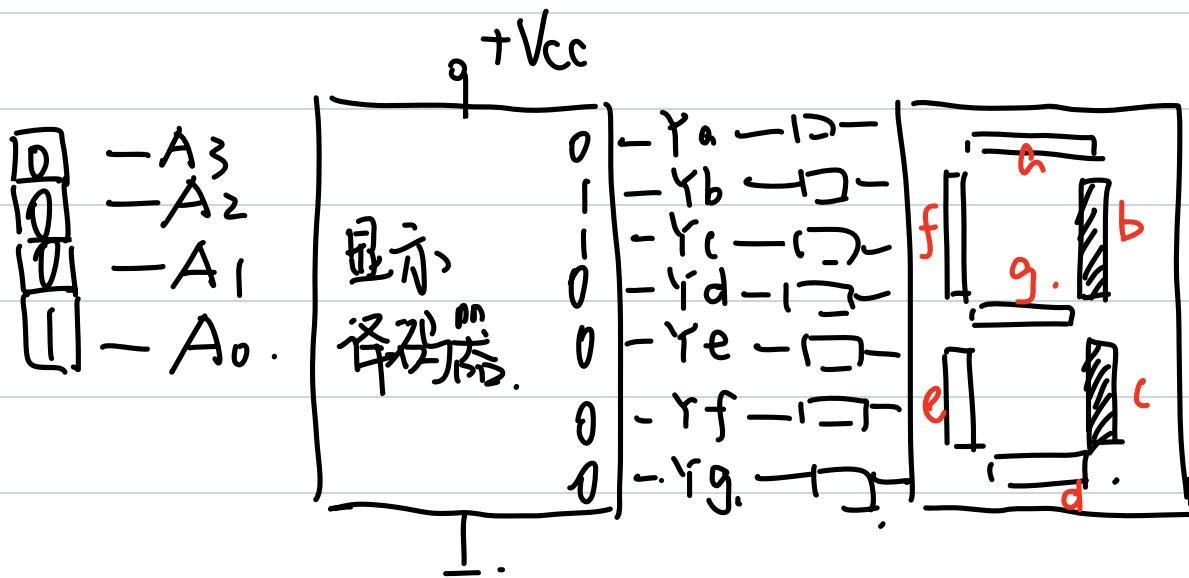
2. 数据分配器。一路输入数据分配到多路输出。

真值表。



3. 译码器。显示 (LED) 74LS48 共阴极
高电平





4. 编码器

二进制编码器

将 $N=2^n$ 个输入信号换成 m 位 = 二进制代码逻辑电路.

例 设计一个能将 I_0, I_1, \dots, I_7 8 个输入信号 编成 = 二进制代码输出的
编码器 用与非门 实现.

输入	输出
$I_7\ I_6\ I_5\ I_4\ I_3\ I_2\ I_1\ I_0$	$Y_2\ Y_1\ Y_0$
0 0 0 0 0 0 0 1	0 0 0
0 0 0 0 0 0 1 0	0 0 1
0 0 0 0 0 1 0 0	0 1 0
0 0 0 0 1 0 0 0	0 1 1
0 0 0 1 0 0 0 0	1 0 0
0 0 1 0 0 0 0 0	1 0 1
0 1 0 0 0 0 0 0	1 1 0
1 0 0 0 0 0 0 0	1 1 1

$$Y_2 = I_4 + I_5 + I_6 + I_7$$

$$Y_1 = I_2 + I_3 + I_6 + I_7$$

$$Y_0 = I_1 + I_3 + I_5 + I_7$$

优先编码器

允许同

是或0皆可

输入							输出			
I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Y_2	Y_1	Y_0
1	X	X	X	X	X	X	X	1	1	1
0	1	X	X	X	X	X	X	1	1	0
0	0	1	X	X	X	X	X	1	0	1
0	0	0	1	X	X	X	X	1	0	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	0	0	1	0	0	0

5. 数值比较器.

1. n位二进制数值比较器.

输入		输出		
A	B	$Y_{(A>B)}$	$Y_{(A<B)}$	$Y_{(A=B)}$
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

$$Y(A > B) = \bar{A}\bar{B}$$

$$Y(A < B) = \bar{A}B$$

$$Y(A = B) = \bar{A}\bar{B} + AB = \overline{A \oplus B}$$

2 多位数值比较器.

从最高位开始逐位向低位比较.

例 $A = A_3 A_2 A_1 A_0$ $B = B_3 B_2 B_1 B_0$ · 大小

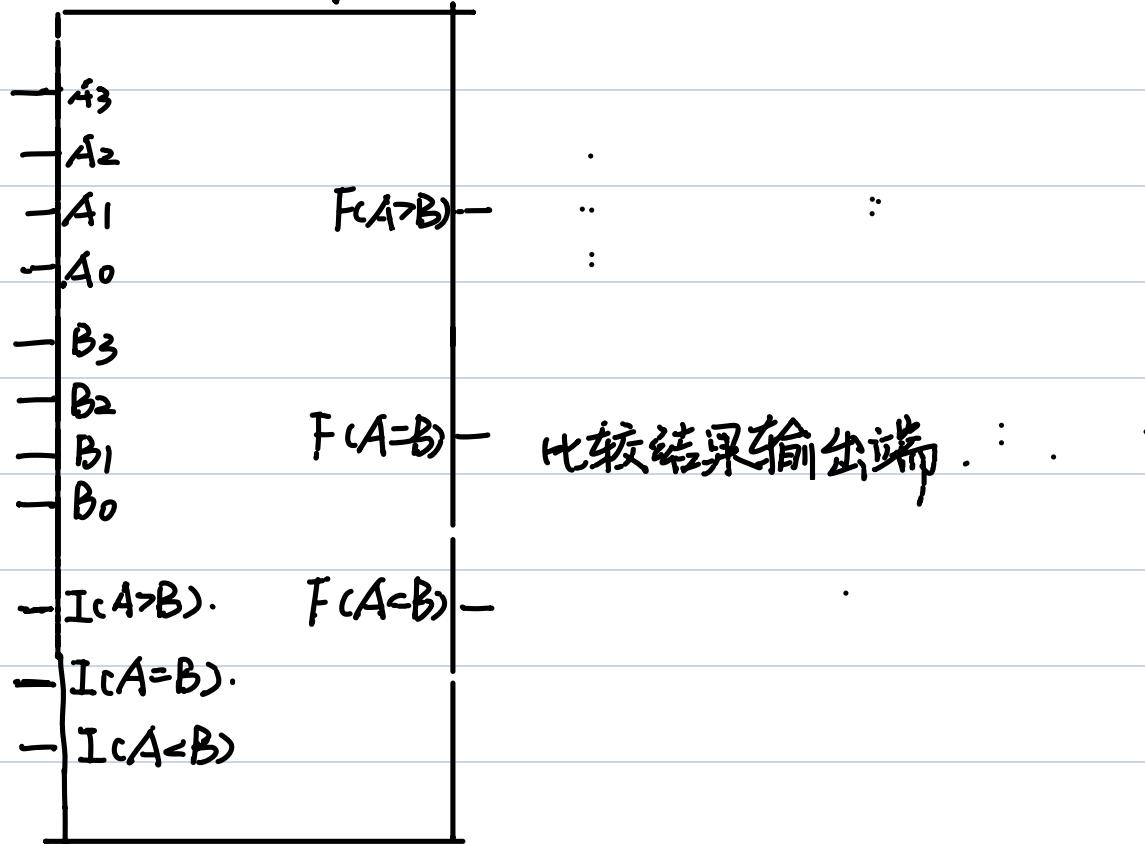
若 $A_3 > B_3$ 则 $A > B$

$A_3 = B_3$ 则 $A_2 \text{ 与 } B_2$ $A_2 > B_2$ 则 $A > B$

3. 4位数值比较器 T4LS85

两组相
比的
4位二进制
的输入端

级联
输入端



输入

$A_3 B_3 A_2 B_2 A_1 B_1 A_0 B_0$	$I_{(A=B)}$ $I_{(A=B)}$ $I_{(A>B)}$ $I_{(A<B)}$	$F_{(A<B)}$ $F_{(A=B)}$ $F_{(A>B)}$
-----------------------------------	---	-------------------------------------

输出

$A_3 < B_3$	X	X	X	X	X	X	1	0	0
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	1	0	0	1	0	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	1	0	0	1	0
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	0	0	1	0	0	1
$A_3 > B_3$	X	X	X	X	X	X	0	0	1
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	0	0	1
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	0	0	1

6 加法器.

1. 全加概念

设2个四位二进数 $A = A_3A_2A_1A_0 = 1011$.

$B = B_3B_2B_1B_0 = 1110$ 相加, 得 1111 .

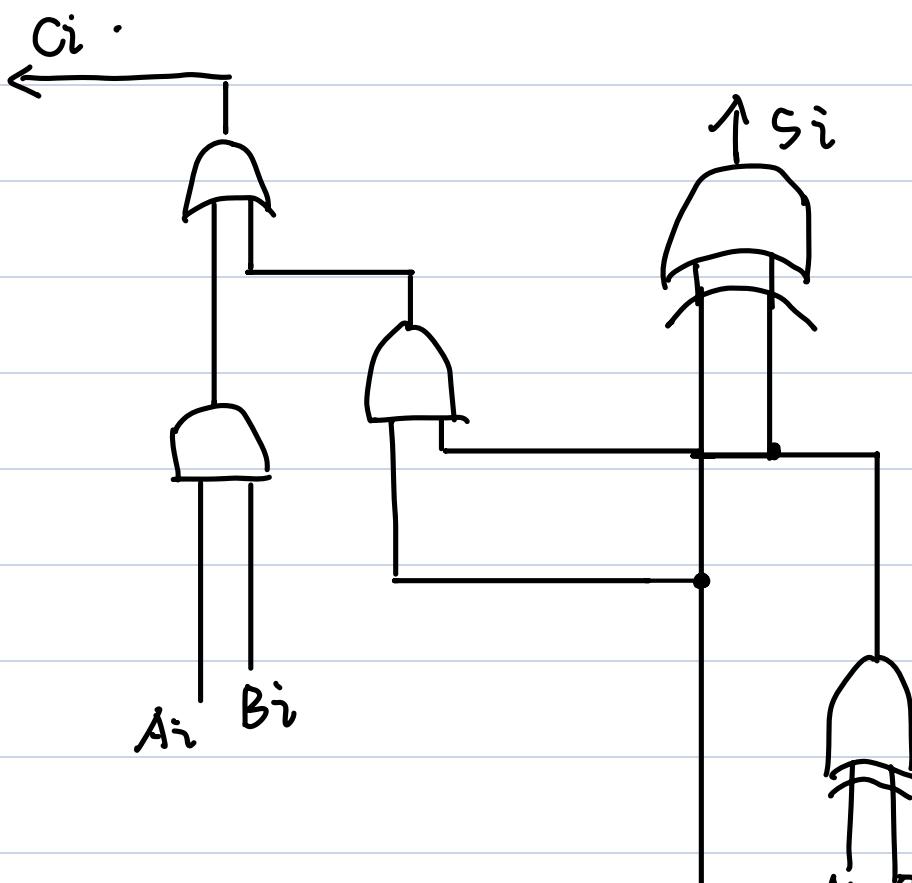
$$\begin{array}{r}
 & | & 0 & | & 1 & | & - - A \\
 & | & | & | & 0 & & - - B \\
 + & 1 & 1 & | & 0 & 0 & - - \text{低位进位} \\
 \hline
 & 1 & 1 & 0 & 0 & 1 & .
 \end{array}$$

2 全加真值表

输入			输出		A_i 与 B_i 表示A、B两数中的第i位， C_{i-1} 表示来自低位(筹计)的进位， S_i 表示全加和， C_i 表示送给高位(筹计+1)的进位	
A_i	B_i	C_{i-1}	S_i	C_i		
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

$$S_i = A_i \oplus B_i \oplus C_{i-1}.$$

$$C_i = (A_i \oplus B_i) C_{i-1} + A_i B_i.$$



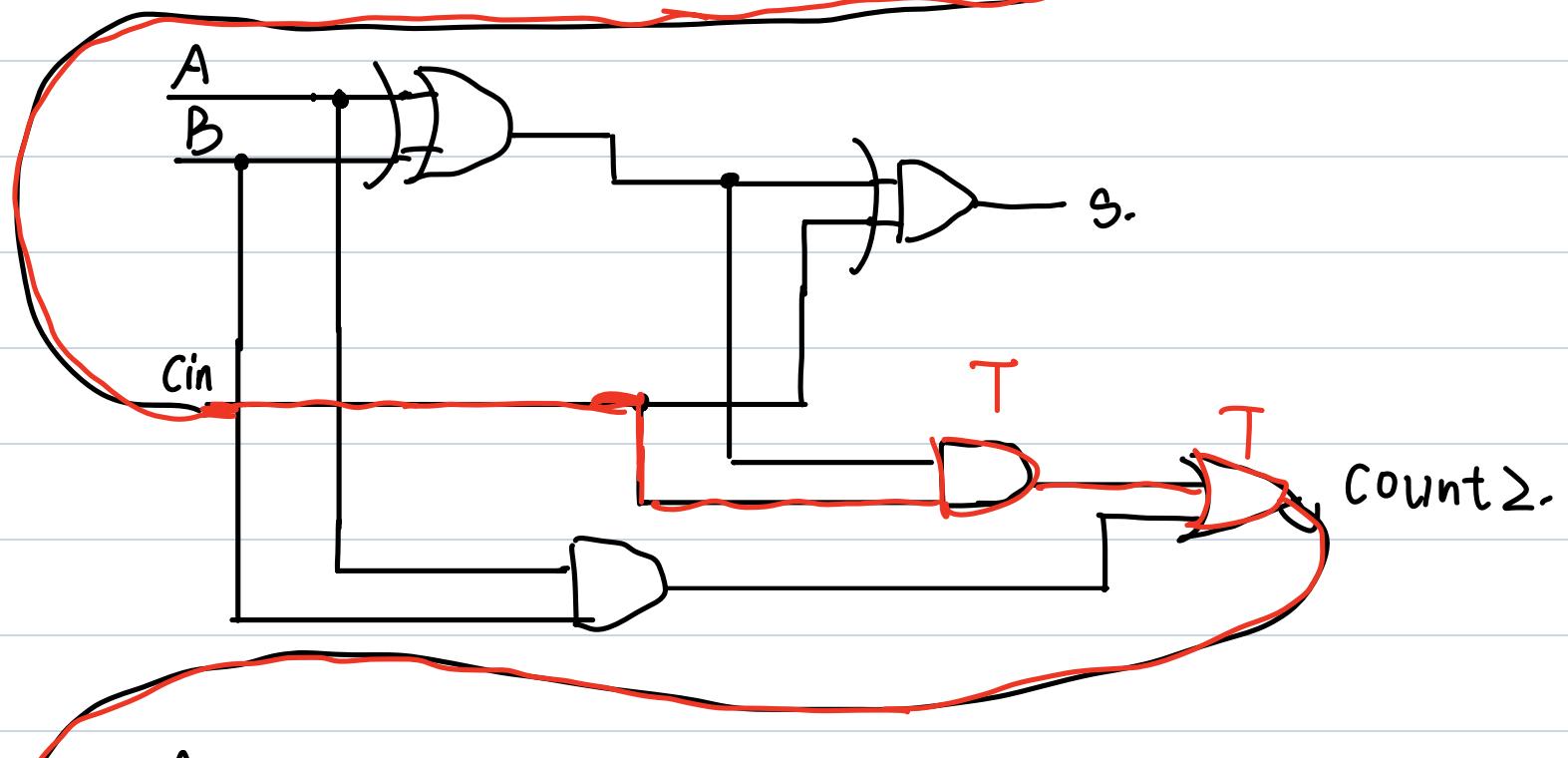
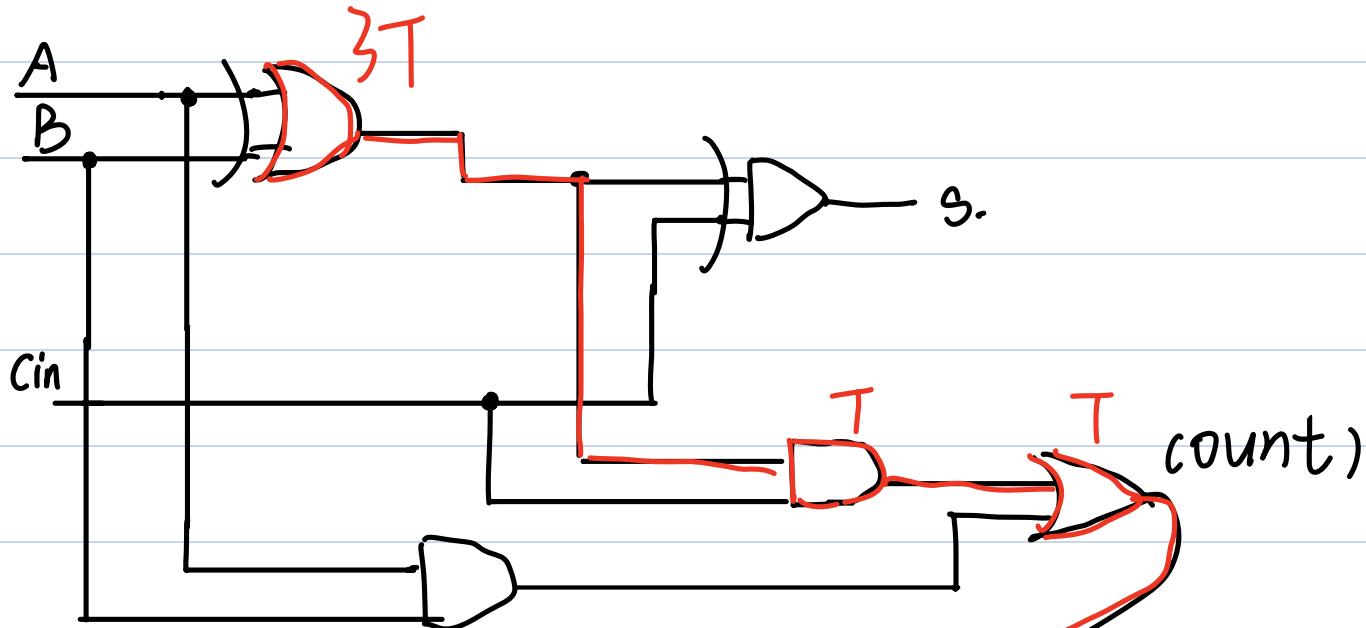
c_{i-1}, A_i B_i

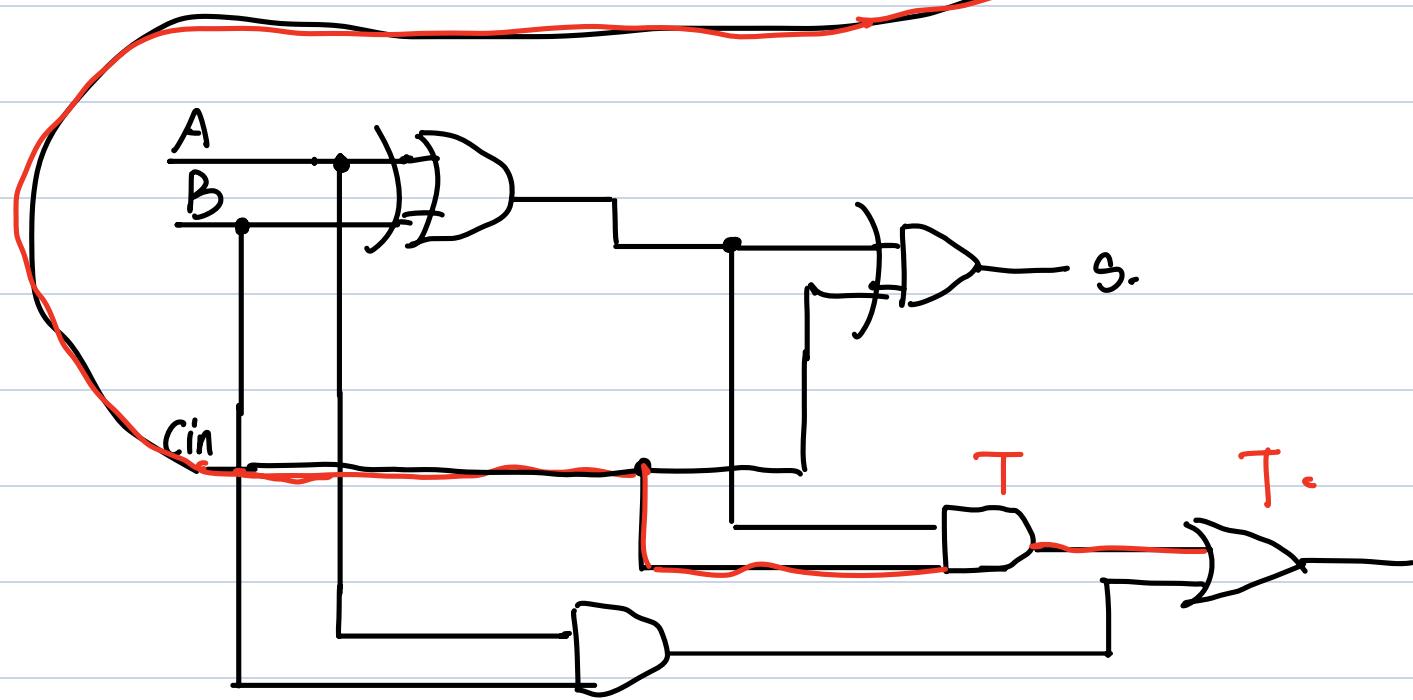
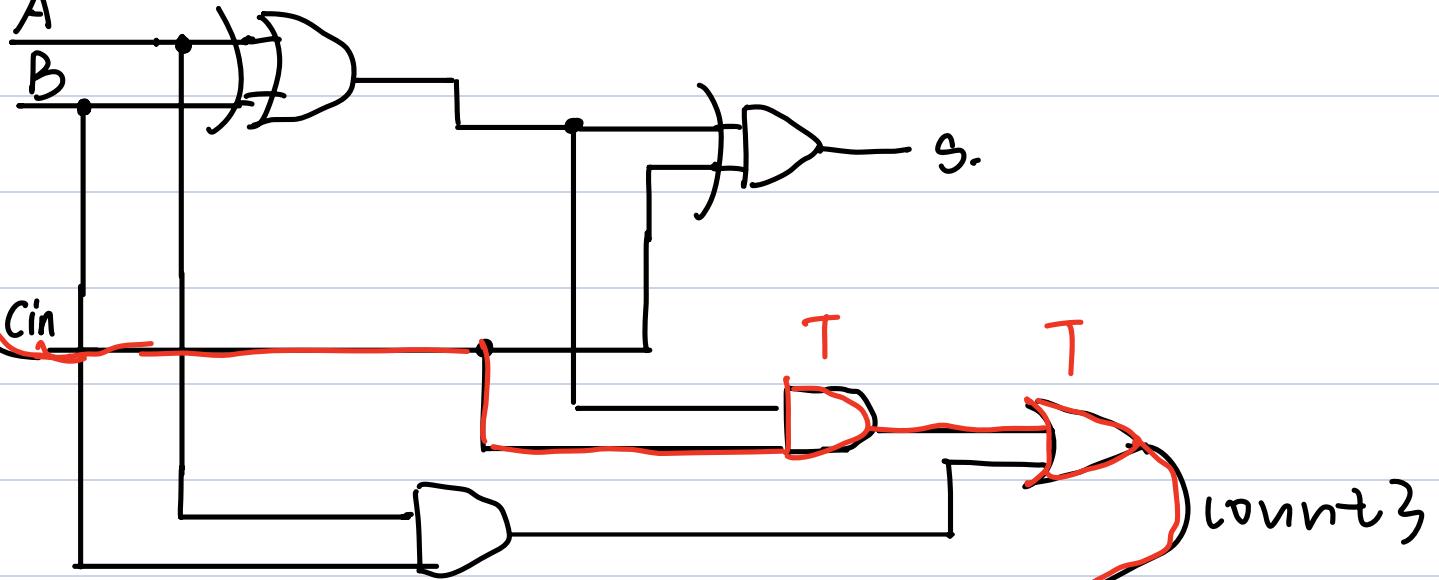
假设 T 表示一级门延迟. 一个异或门以延迟为 3T.

→ 或非 T.

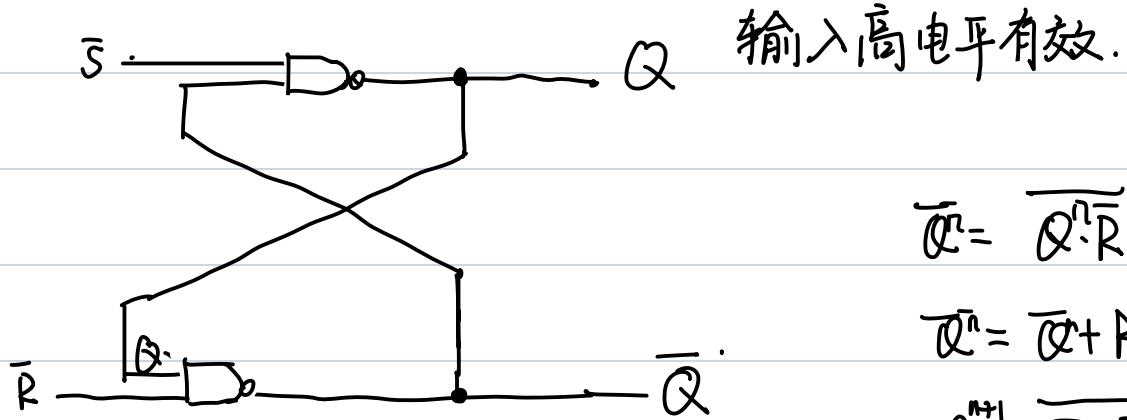
$$3T + 8T = 11T.$$

与非 或非





3.12 基本SR锁存器



$$\bar{Q}^n = \overline{\bar{Q}^n \cdot R}$$

$$\bar{Q}^n = \bar{Q}^n + R.$$

$$Q^{n+1} = \frac{S \cdot (\bar{Q}^n + R)}{\bar{S} \cdot (\bar{Q}^n + R)}$$

$$= S + \bar{R}Q^n.$$

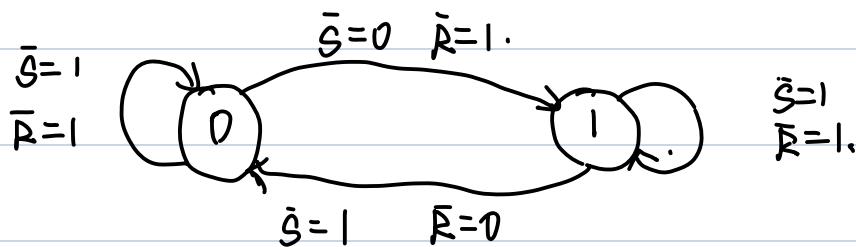
$$\left\{ \begin{array}{l} Q^{n+1} = \bar{S} + \bar{R}Q^n \\ \bar{S} + \bar{R} = 1. \end{array} \right.$$

$\bar{S}\bar{R} = 00$ 组合

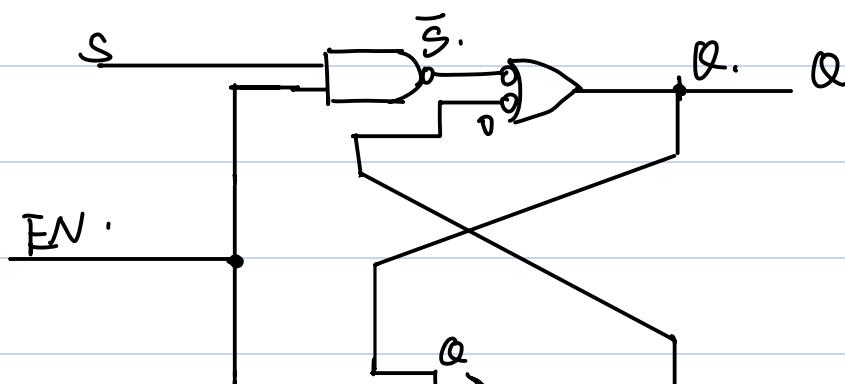
锁存器不稳 $Q^{n+1} = \bar{Q}^{n+1} = 1.$

$\bar{S}\bar{R} = 11$ 组合为保持状态.

输入	输出	(Q^{n+1})	
\bar{S}	\bar{R}	Q \bar{Q}	
0	0	1 1	不稳
0	1	1 0	置 1
1	0	0 1	置 0
1	1	Q^n \bar{Q}^n	保持



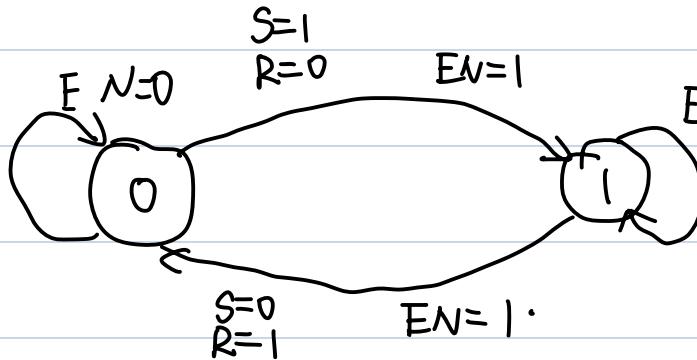
3.13 i门控SR锁存器





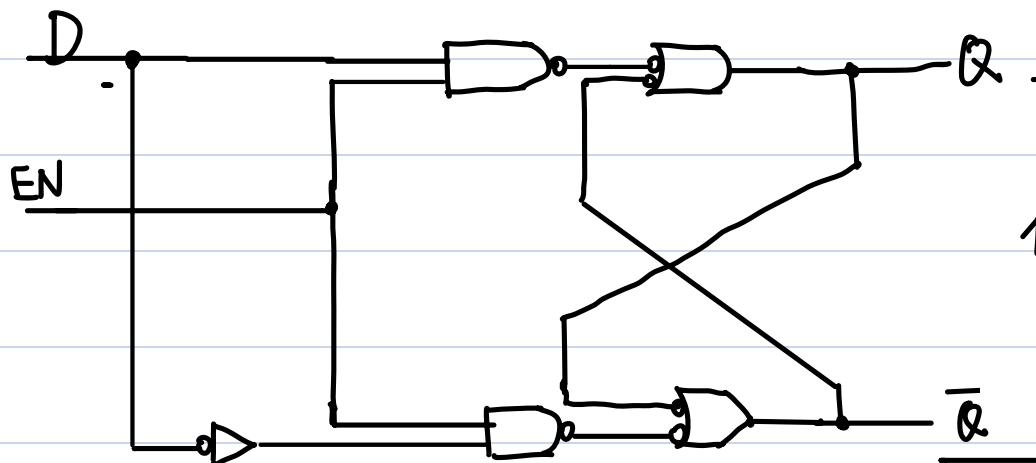
EN有效时，锁存器接收信号

EN无效时，锁存器拒绝接收信号。

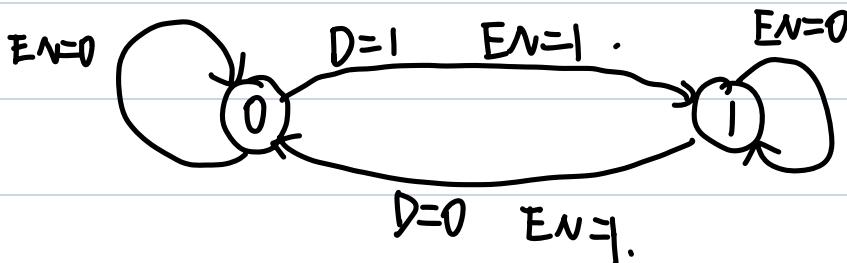


输入		输出		
EN	S	R	Q^{n+1}	\bar{Q}^{n+1}
0	x	x	保持 Q^n 不变	
1	1	0	1	0
1	0	1	0	1

3.14. 门控 D 锁存器

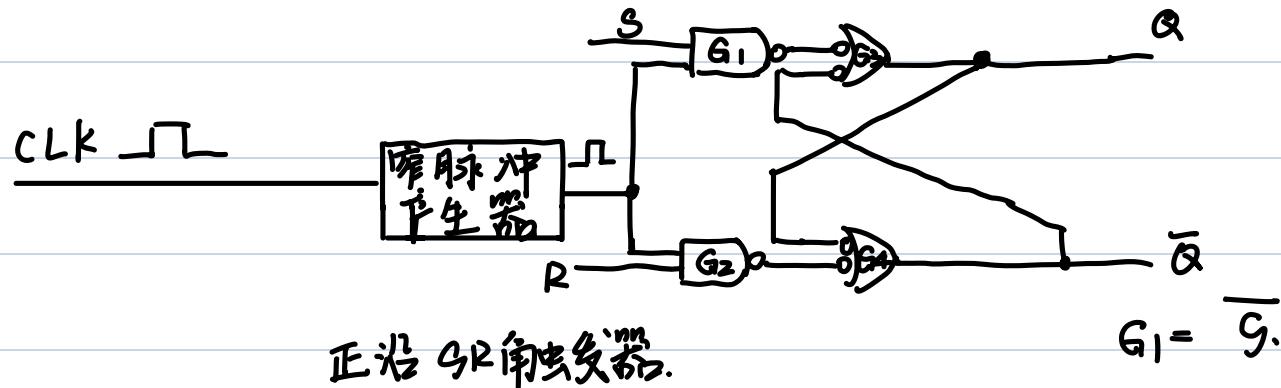


先决条件 数据信号D先到
使能控制信号EN后到.

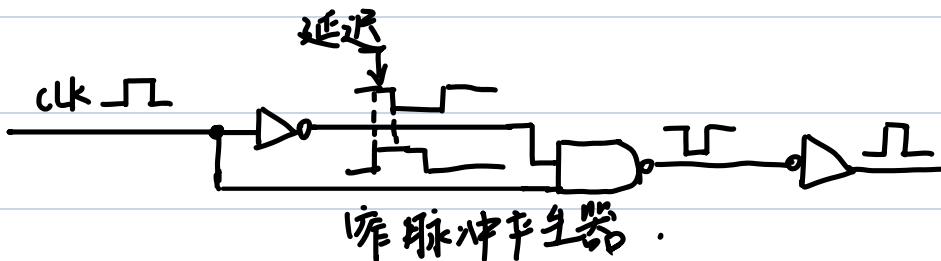


输入		输出		说明
D	EN	Q	\bar{Q}	
0	1	0	1	置0.
1	1	1	0	置1.
x	0	Q^n	\bar{Q}^n	保持

3.21 触发器.



正沿 SR 触发器.



当 S 高 R 低 Q 在时钟脉冲上升沿变高, 触发器置 1.

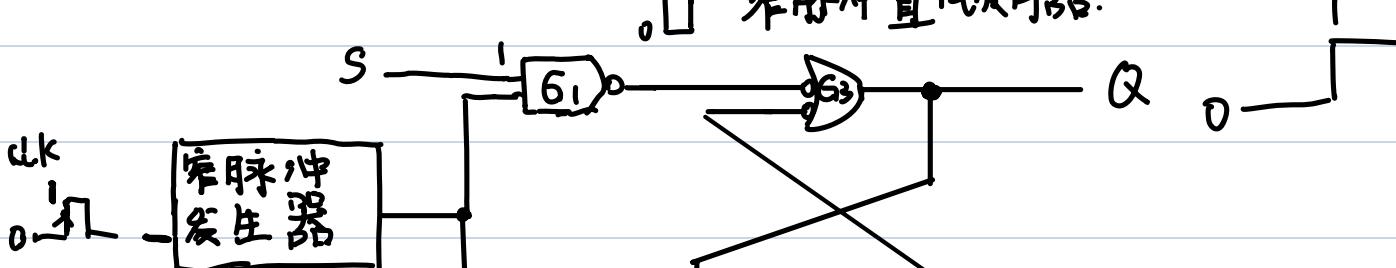
当 S 低 R 高 Q 在时钟脉冲上升沿变低 触发器置 0.

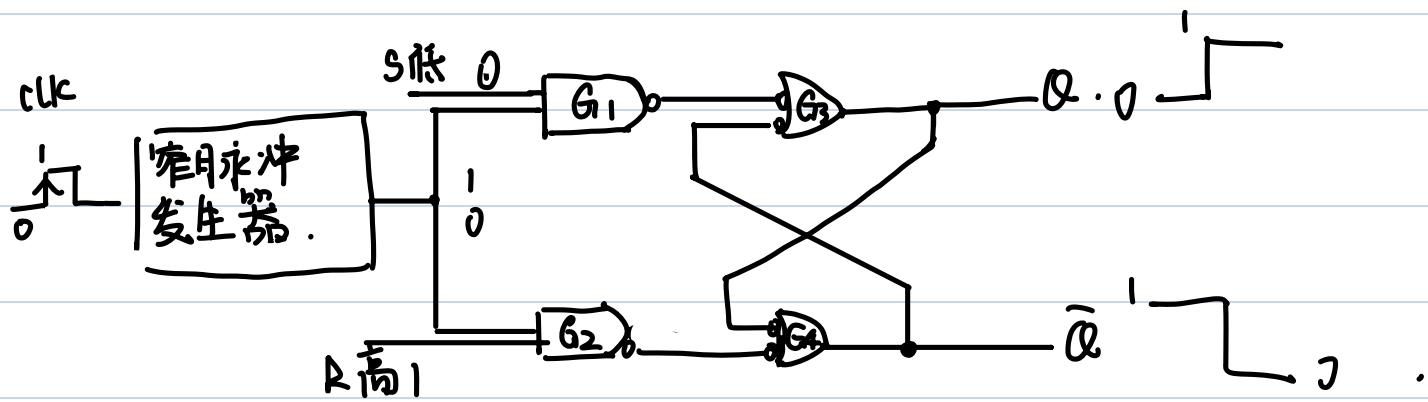
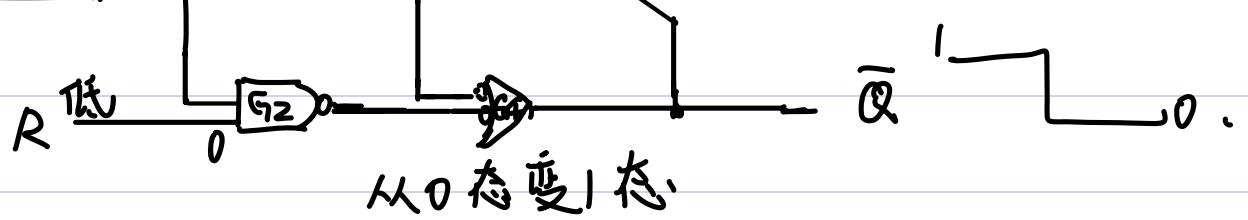
当 S 低 R 低 Q 保持

当 S 高 R 高 Q 输出不稳定.

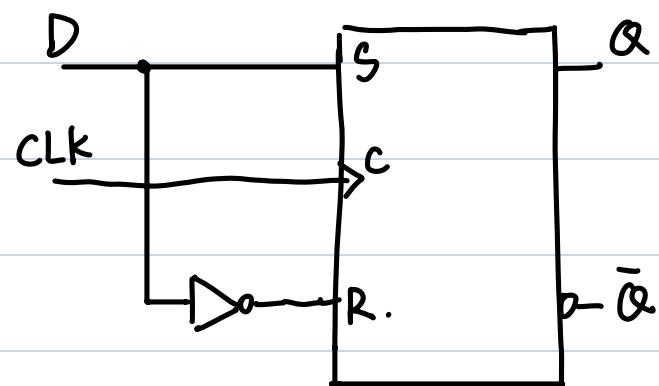
输入			输出		说明
S	R	CLK	Q	\bar{Q}	
0	0	X	Q^n	\bar{Q}^n	保持
0	1	↑	0	1	置 0.
1	0	↑	1	0	置 1.
1	1	↑	?	?	不稳

'↑' 窄脉冲置 1 锁存器.

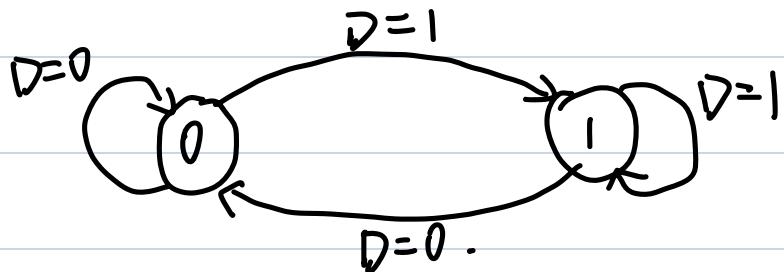




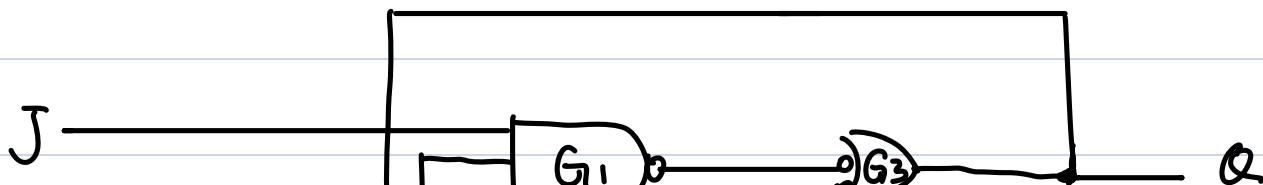
3.2.2 D 触发器

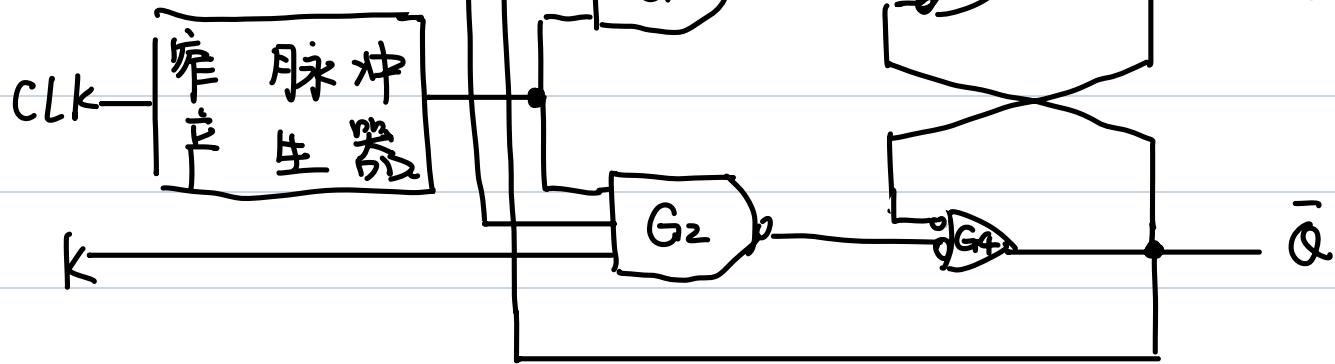


输入	输出	说明
D	Q	
CLK	\bar{Q}	
1	↑	1 0. 置位(有1)
0	↑	0 1 复位(有0)



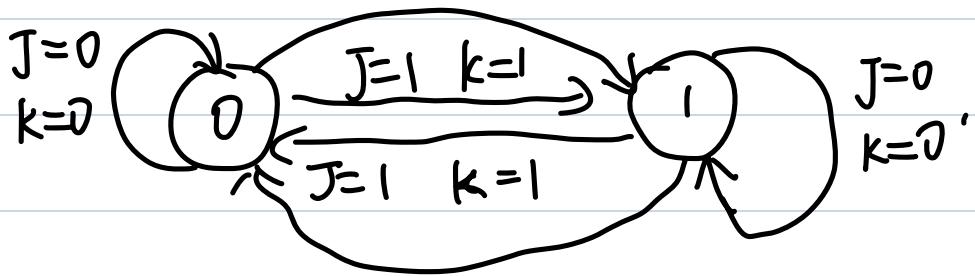
3.2.3 JK 触发器.





输入			输出		说明
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q^n	\bar{Q}^n	保持
0	1	↑	0	1	置0
1	0	↑	1	0	置1
1	1	↑	\bar{Q}^n	Q^n	交替

$J=1 \quad K=0$



$J=0 \quad K=1$

$$Q^{n+1} = J\bar{Q}^n + \bar{K}Q^n$$

\overline{PRE} 和 \overline{CLR} 前者使触发器强置1

后者使触发器强置0

优先级大于 J、K。

