digital



PROGRAMMING CARI

FOR FAMILY OF PDP-11 COMPUTERS





MODE

Mode Name

0	register
1	register deferred
2	auto-increment
3	auto-incr deferred
4	auto-decrement

auto-decr deferred 6 index index deferred

Symbolic Description

R
(R)
(R)+
@(R)+ -(R)
@-(R)
Y/P)

@X(R)

(R) is operand [ex. R2=%2] (R) is address (R) is adrs; (R) + (1 or 2) (R) is adrs of adrs; (R) +2

(R) - (1 or 2); (R) is adrs (R) - 2; (R) is adrs of adrs (R) - 2; (R) is adrs of adrs (R) + X is adrs (R) + X is adrs of adrs

PROGRAM COUNTER ADDRESSING:

44-	
#11	

Reg = 7

MODE

2 immediate 3 absolute 6 relative relative deferred

@#A A @A

operand n follows instr address A follows instr instr adrs + 4 + X is adrs instr adrs + 4 + X is adrs of adrs

LEGEND:

Op Codes

= 0 for word/1 for byte = source field (6 bits) DD = destination field (6 bits) R = gen register (3 bits), 0 to 7 XXX = offset (8 bits), +127 to -128 = number (3 bits)

NN = number (6 bits)

Operations

) = contents of = contents of source d = contents of destination = contents of register = becomes = relative address

= register definition

Boolean

A = AND V = inclusive OR **★** = exclusive OR ~= NOT

Condition Codes

* = conditionally set/cleared

- = not affected 0 = cleared

1 = set

NOTE:

lacktriangle = Applies to the 11/35, 11/40, 11/45 & 11/70 computers = Applies to the 11/45 & 11/70 computers

digital equipment corporation



NUMERICAL OP CODE LIST:

OP Code	Mnemonic	OP Code	Mnemonic	OP Code	Mnemonic
00 00 00 00 00 01 00 00 02 00 00 03 00 00 04 00 00 05 00 00 06 00 00 07 00 00 77	HALT WAIT RTI BPT IOT RESET RIT (unused)	00 60 DD 00 61 DD 00 62 DD 00 63 DD 00 64 NN 00 65 SS 00 66 DD 00 67 DD	ROR ROL ASR ASL MARK MFPI MTPI SXT	10 43 77	EMT
00 01 DD 00 02 OR 00 02 10	JMP RTS	00 70 00 7 00 77 77 7 01 SS DD 02 SS DD	(unused) MOV	10 51 DD 10 52 DD 10 53 DD 10 54 DD	CLRB COMB INCB DECB NEGB
00 02 27 00 02 3N 00 02 40	SPL NOP	03 SS DD 04 SS DD 05 SS DD 06 SS DD	BIT BIC BIS ADD	10 56 DD 10 57 DD 10 60 DD 10 61 DD	ADCB SBCB TSTB RORB ROLB
00 02 41 00 02 77 00 03 DD	cond codes	07 OR SS 07 1R SS 07 2R SS 07 3R SS 07 4R DD	MUL DIV ASH ASHC XOR	10 62 DD 10 63 DD	ASRB ASLB (unused)
00 04 XXX 00 10 XXX 00 14 XXX 00 20 XXX	BR BNE BEQ BGE	07 50 OR 07 50 1R 07 50 2R 07 50 3R	FADD FSUB FMUL FDIV	10 64 77 10 65 SS 10 66 DD	MFPD MTPD
00 24 XXX 00 30 XXX 00 34 XXX	BLT BGT BLE JSR	07 50 40 7 07 67 77	(unused)	10 77 77	(unused)
00 50 DD 00 51 DD 00 52 DD .00 53 DD 00 54 DD 00 55 DD	CLR COM INC DEC NEG ADC	07 7R NN 10 00 XXX 10 04 XXX 10 10 XXX 10 14 XXX 10 20 XXX	BPL BMI BHI BLOS BVC	12 SS DD 13 SS DD 14 SS DD 15 SS DD	MOVB CMPB BITB BICB BISB SUB
00 56 DD 00 57 DD	SBC TST	10 24 XXX 10 30 XXX 10 34 XXX	BVS BCC, BHIS BCS, BLO		floating point

TRAP VECTORS:

030

034

EMT instruction

TRAP instruction

000 004 010 014	(reserved) Time Out & other errors illegal & reserved instr BPT instruction	114 240 244 250	Memory Parity PIRQ, prog int req Floating Point Memory Management
020	10T instruction		,
024	Power Fail		

SINGLE OPERAND: OPR dst OP CODE Mnemonic Op Code Instruction dst Result N Z V C General 0 1 0 0 * * 0 1 * * * -* * * * ■ 050DD CLR(B) clear 0 COM(B) ■ 051DD complement (1's) ~ d INC(B) ■ 052DD increment d+1■ 053DD DEC(B) decrement d-1NEG(B) ■ 054DD negate (2's compl) -d * * 0 0 ■ 057DD TST(B) test d Rotate & Shift ROR(B) ■ 060DD \rightarrow C, d * * * * rotate right ROL(B) * * * * ■ 061DD rotate left C, d ← ■ 062DD d/2 * * * * ASR(B) arith shift right * * * * ASL(B) ■ 063DD arith shift left 2d * * * 0 SWAB 0003DD swap bytes Multiple Precision ADC(B) ■ 055DD d + C* * * * add carry * * * * SBC(B) ■ 056DD d - Csubtract carry A SXT 0067DD sign extend - * 0 -0 or -1 OPR src, dst OPR src, R or OPR R, dst DOUBLE OPERAND: OP CODE SS DD OP CODE SS OR DD Mnemonic Op Code Instruction Operation NZVC General MOV(B) ■ 1SSDD move * * 0 $d \leftarrow s$ CMP(B) compare ■ 2SSDD s - dADD 06SSDD * * * * add $d \leftarrow s + d$ SUB 16SSDD subtract $d \leftarrow d - s$ Logical * * 0 -BIT(B) ■ 3SSDD bit test (AND) s A d BIC(B) ■ 4SSDD $d \leftarrow (\sim s) \wedge d * * 0$ bit clear BIS(B) * * 0 -■ 5SSDD bit set (OR) d ← s v d **▲**Register MUL 070RSS multiply r ← rxs * * 0 * DIV 071RSS * * * * divide $r \leftarrow r/s$

shift arithmetically

arith shift combined

exclusive OR

ASH

ASHC

XOR

072RSS

073RSS

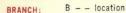
074RDD

* * * *

* * * *

* * 0 -

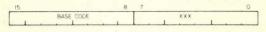
 $d \leftarrow r + d$



If condition is satisfied:

Branch to location. New PC ← Updated PC + (2 x offset)

adrs of br instr + 2



Op Code = Base Code + XXX

Mnemonic	Base	Code	

Branch Condition

Branches

BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	# 0	Z = 0
BEQ	001400	br if equal (to 0)	= 0	Z = 1
BPL	100000	branch if plus	+	N = 0
BMI	100400	branch if minus	_	N=1
BVC	102000	br if overflow is clear		V = 0
BVS	102400	br if overflow is set		V = 1
BCC	103000	br if carry is clear		C = 0
BCS	103400	br if carry is set		C = 1

Instruction

Signed Conditional Branches

BGE	002000	br if greater or eq (to 0)	≥0	N + V = 0
BLT	002400	br if less than (0)	<0	N + V = 1
BGT	003000	br if greater than (0)	>0	$Z \vee (N + V) = 0$
BLE	003400	br if less or equal (to 0)	€0	$Z \vee (N + V) = 1$

Unsigned Conditional Branches

BHI BLOS BHIS	101000 101400 103000	branch if higher branch if lower or same branch if higher or same	NW/	$\begin{array}{c} C \ v \ Z = 0 \\ C \ v \ Z = 1 \\ C = 0 \end{array}$
BLO	103400	branch if lower	2	C = 0 C = 1

JUMP & SUBROUTINE:

Mnemonic	Op Code	Instruction	Notes
JMP JSR RTS AMARK ASOB	0001DD 004RDD 00020R 0064NN 077RNN	jump jump to subroutine } return from subroutine } mark subtract 1 & br (if \neq 0)	PC \leftarrow dst use same R aid in subr return (R) $-$ 1, then if (R) \neq 0: PC \leftarrow Updated PC $-$ (2 x NN)

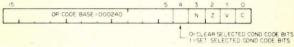
TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
▲RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT WAIT RESET NOP	000000 000001 000005 000240	halt wait for interrupt reset external bus (no operation)
● SPL ▲ MFPI ▲ MTPI ● MFPD ● MTPD	00023N 0065SS 0066DD 1065SS 1066DD	set priority level (to N) move from previous instr space move to previous instr space move from previous data space move to previous data space

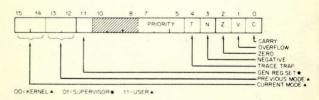
CONDITION CODE OPERATORS:



Mnemonic	Op Code	Instruction	NZVC
CLC CLV CLZ CLN	000241 000242 000244 000250	clear C clear V clear Z clear N	0 0 - - 0
SEC SEV SEZ SEN SCC	000257 000261 000262 000264 000270 000277	set C set V set Z set N set all cc bits	0 0 0 0 1 1- 1 1 1 1 1

PROCESSOR REGISTER ADDRESSES:

Processor Status Word PS - 777 776



R4 — 777 704 R5 — 777 705 R6 — 777 706 R7 — 777 707

▲Stack Limit Register — 777 774

(not for 11/45)

Program Interrunt Remuest __777 772

Togram Interrupt Request -/// //2						
General Registers	RO 777 700					
(console use only)	R1 — 777 701					
	R2 — 777 702					
(not for 11/45)	R3 — 777 703					

Console Switches & Display Register - 777 570

DEVICE REGISTER ADDRESSES:

Dev	vice Regis	sters	Address	Int Vec- tor	Prior- ity	NPR	Device	Registe	ers	Address	Int Vec- tor	Prior- ity	NPR
CD11	Card Reader, high speed status & control column count current address data	(CDST) (CDCC) (CDBA) (CDDB)	777 160 777 162 777 164 777 166	230	BR4	Х	RP04 wo UN de	ord count (R NIBUS address (R esired sector/track (R	RPCS1) RPWC) RPBA) RPDA)	776 700 776 702 776 704 776 706	254*	BR5**	X
CR11	Card Reader status buffer, 12-bit char buffer, 8-bit char	(CRS) (CRB1) (CRB2)	777 160 777 162 777 164	230	BR6		RH	status ive status (R	RPCS2) RPDS) RPER1)	776 710 776 712 776 714			
KW11-L	Line Clock	(LKS)	777 546	100	BR6		att	tention summary (F	RPAS)	776 716 776 720			
KW11-F	Programmable Clock control & status count set buffer counter		772 540 772 542 772 544	104	BR6		ma dri se off	aintenance register (R ive type (R rial number (R fset (R	RPDB) RPMR) RPDT) RPSN) RPOF)	776 722 776 724 776 726 776 730 776 732			
LA30, LA36, LT33, VT05, VT50	Console Terminal keyboard/reader status keyboard/reader buffer printer/punch status printer/punch buffer		777 560 777 562 777 564 777 566	60 64	BR4 BR4		cu eri eri EC EC	rrent cylinder (R ror #2 (R ror #3 (R CC position (R CC pattern (R	RPDC) RPCC) RPER2) RPER3) RPEC1)	776 734 776 736 776 740 776 740 776 744 776 746			
LP11, LS11, LV11	Line Printer printer status printer data		777 514 777 516	200	BR4				RPBAE) RPCS3)	776 750† 776 752†	204*	BR5**	Y
PC11	Paper Tape reader status reader buffer punch status punch buffer	(PRS) (PRB) (PPS) (PPB)	777 550 777 552 777 554 777 556	70 74	BR4 BR4		RWS04/ co RS04, wo RJS03/ UN RWS03 de RS03 RH	ord count (F NIBUS address (F esired disk adrs (F H11 control & status (F ive status (F	RSCS2) RSDS)	772 040 772 042 772 044 772 046 772 050 772 052	204	DIKO .	
RK11/ RK05	Disk Cartridge drive status error control & status word count current bus adrs disk address data buffer	(RKDS) (RKER) (RKCS) (RKWC) (RKBA) (RKDA) (RKDB)	777 400 777 402 777 404 777 406 777 410 777 412 777 416	220	BR5	X	ati loc da ma dri bu	tention summary (Fock ahead (F	RSER) RSAS) RSLA) RSDB) RSMR) RSDT) RSBAE) RSCS3)	772 054 772 056 772 060 772 062 772 064 772 066 772 070† 772 072†			
RF11/ RS11	Disk disk control status word count current mem adrs disk address disk address disk error disk data buffer maintenance adrs of disk segment	(DCS) (WC) (CMA) (DAR) (DAE) (DBR) (MA) (ADS)	777 460 777 462 777 464 777 466 777 470 777 472 777 474 777 476	204	BR5	X	TU16 WC UN fra RH dr er at ch	ontrol & status #1 (1) ord count (1) NIBUS address (1) ame count (1) H11 control & status (1) rive status (1) rror (1) ttention summary (1) neck character (1)	MTWC) MTBA) MTFC) MTCS2) MTDS) MTER) MTAS) MTCK)	772 440 772 442 772 444 772 446 772 450 772 452 772 454 772 456 772 460	224*	BR5**	X
RP11-C RP03, RPR11 RPR02	device status / error	(RPDS) (RPER) (RPCS) (RPWC) (RPBA) (RPCA) (RPDA) (RPM1) (RPM2) (RPM3) (SUCA)	776 710 776 712 776 714 776 720 776 720 776 722 776 724 776 730 776 732 776 732	254	BR5	X	m dr se ta bi TMA11/Mag TU10, st TS03 co	laintenance (I rive type (I erial number (I ape control (I us address ext ontrol & status #3 (I netic Tape latus ontrol (I us address ext ontrol (MTMR) MTDT) MTSN) MTTC) MTBAE) MTCS3) MTC) MTS) MTC) MTBRC)	772 462 772 464 772 466 772 470 772 472 772 476† 772 520 772 522 772 524 772 526	224	BR5	X
RX11/	cyl adrs silo memory Floppy Disk	(SILO)	776 736	264	BR5		da re *Jumper Se	ata buffer (l ead lines (l electable	MTD) MTRD)	772 530 772 532			
RX01	command & status data buffer	(RXCS) (RXDB)	777 170 777 172				**Plug Selec		1				

	ec- Prior- tor ity NPR 260 BR6 214 BR6 X	Starting Ad Memory Siz	dress: — e: —————————————————————————————————	7 7 7 7 7 7 7	— 744 — 746 — 750 — 752 — 754 — 756 — 760	isk/DECta ard Reade assette Bo	r Boots r Bootstr potstrap	000 005 177 000 177 or 177	002 400 267 756
BM873-YA BOOTSTRAP LOADER:	MI	R11-DB B0			R:	9)	ia .		
Starting Address Device 773 000 RF11 773 010 RK11 773 020 Transfer to address collowitch Register 5 Switch Register TC11 773 050 TM11 773 100 RP11 773 144 RC11 773 210 ASR paper tape reader 773 230 TA11	_	Sta	rting Add 773 100 773 120 773 120 773 136 773 154 773 220	- 30	Devi RFJ RK TC: TM RP RC	11 11 11 11			
773 312 PC11		Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
2 TC11 7 RV 3 RK11 10 RV	e switch register e switch register ter e switch register	000 001 002 003 004 005 006 007 010 011 012 013 014 015 016 017 020 021 022 023 024 025 026 027 030 031 032 033 034 035 036 037	NUL SOH STX ETX EOT ENQ ACK BEL BS HT LF VT FF CR SO SI DLE DC2 DC3 DC4 NAK SYN ETB CAN EM SUB ESC FS GS RS US	040 041 042 043 044 045 046 047 050 051 052 053 054 055 066 067 060 061 062 063 064 065 067 070 071 072 073 074 075 076 077	SP!"#\$%&,()*+/0123456789:;\\=\?	100 101 102 103 104 105 106 107 110 111 112 113 114 115 116 117 120 121 122 123 124 125 126 127 130 131 132 133 134 135 136 137	@ABCDEFGHIJKLMNOPQRSTUVWXYZ[/]^	140 141 142 143 144 145 146 147 150 151 152 153 154 155 160 161 162 163 164 165 166 167 170 171 172 173 174 175 176 177	abcdefghijklmnopqrstuvwxyz{ }

BOOTSTRAP LOADER

ABSOLUTE LOADER

PDP-11/45, 11/70 FLOATING POINT PROCESSOR:

15	8	7 6	5)_
OP CODE BASE = 170000		AC		SS OR DD	
	1				

Mnemonic	Op Code	Instruction	Operation
	170000 170001 170002 170011 170012	copy fl cond codes set floating mode set integer mode set fl dbl mode set long integer mode	FD ← 0 FL ← 0 FD ← 1 FL ← 1
LDFPS STFPS STST	1701 src 1702 dst 1703 dst	load FPP prog status store FPP prog status store (exc codes & adrs)
CLRF, CLRD TSTF, TSTD ABSF, ABSD NEGF, NEGD	1704 fdst 1705 fdst 1706 fdst 1707 fdst	clear floating/double test fl/dbl make absolute fl/dbl negate fl/dbl	fdst ← 0 fdst ← fdst fdst ← -fdst
MULF, MULD MODF, MODD ADDF, ADDD LDF, LDD SUBF, SUBD	172 (AC) fsrc	add fl/dbl	$AC \leftarrow AC \times fsrc$ $AC \leftarrow AC + fsrc$ $AC \leftarrow fsrc$ $AC \leftarrow fsrc$ $AC \leftarrow AC - fsrc$
CMPF, CMPD STF, STD DIVF, DIVD	174 (AC) fdst	store fl/dbl	fdst ← AC AC ← AC/fsrc
STEXP STCFI, STCFL) STCDI, STCDL) STCFD, STCDF			
LDEXP LDCIF, LDCID) LDCLF, LDCLE) LDCDF, LDCFD	177 (AC) STC	long int to fl or dbl	
	CFCC SETF SETI SETI SETI SETI SETI SETI LDFPS STFPS STFPS STFPS STFPS STFPS CLRF, CLRD TSTF, TSTD ABSF, ABSD NEGF, NEGD MULF, MULD MODDF, MODD ADDF, ADDD LDF, LDD SUBF, SUBD CMPF, CMPD STF, STD DIVF, DIVD STEXP STCFI, STCFL STCDI, STCDI STCFD, STCDF LDEXP LDCIF, LDCID LDCLF, LDCID LDCLF, LDCLI	CFCC 170000 SETF 170001 SETI 170001 SETI 170001 SETI 170001 SETI 170001 SETI 170011 SETL 170012 LDFPS 1701 src STFPS 1702 dst STSTS 1703 dst CLRF, CLRD 1704 fdst TSTF, TSTD 1705 fdst ABSF, ABSD 1706 fdst NEGF, NEGD 1707 fdst MULF, MULD 1707 fdst MULF, MULD 1707 fdst MULF, MULD 1707 fdst MULF, MULD 1707 fdst CMPF, CMPD 1707 fdst CMPF, CMPD 1707 fdst CMPF, CMPD 173 (AC + 4) fsrc STF, STD 174 (AC) fsrc STF, STD 174 (AC) fdst DIVF, DIVD 174 (AC + 4) fsrc STF, STD 174 (AC) fdst DIVF, DIVD 174 (AC + 4) fsrc STEXP 175 (AC) dst STCDI, STCDL 175 (AC) dst STCDI, STCDL 175 (AC) fdst LDEXP 176 (AC + 4) src LDCLF, LDCLD 177 (AC) src 176 (AC + 4) src LDCLF, LDCLD 177 (AC) src	CFCC 170000 copy fl cond codes SETF 170001 set floating mode SETI 1700012 set integer mode SETD 170011 set floating mode SETD set integer mode SETL 170012 set long integer mode LDFPS 1701 src load FPP prog status STSTS 1702 dst store FPP prog status STST 1703 dst store FPP prog status STST 1705 fdst clear floating/double TSTF, TSTD 1705 fdst make absolute fl/dbl MBSF, ABSD 1706 fdst make absolute fl/dbl MULF, MULD 171 (AC) fsrc multiply fl/dbl MODF, ADDD 172 (AC) fsrc add fl/dbl LDF, LDD 172 (AC) fsrc multiply fl/dbl SUBF, SUBD 173 (AC) fsrc add fl/dbl SUBF, SUBD 173 (AC) fsrc store fl/dbl CMPF, CMPD 174 (AC) fdst store fl/dbl STEXP 175 (AC) dst store fl/dbl STEXP 175 (AC) dst

PDP-11/35, 11/40 FLOATING POINT UNIT:

			N	Z	٧	C
FADD	07500R	floating add	*	*	0	0
FSUB	07501R	floating subtract	*	*	0	0
FMUL	07502R	floating multiply	*	*	0	0
FDIV	07503R	floating divide	*	*	0	0

POWERS OF 2:

n	2 ⁿ	1 <u>n</u>	<u>2</u> n
0	- 1	10	1,024 2,048 4,096 8,192 16,384 32,768
ì	2	10 11 12 13 14 15 16 17 18	2,048
2	4	12	4,096
3 4 5	8	13	8,192
4	16	14	16,384
	32	15	32,768
6	64	16	65,536
7	8 16 32 64 128 256	17	131,072
8	256	18	262,144
9	512	19	524,288

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