

浙江大学

本科实验报告

课程名称：计算机组成

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浙江大学实验报告

课程名称：计算机组成 实验类型：综合

实验项目名称：Lab3 Setup environment for CPU design and test

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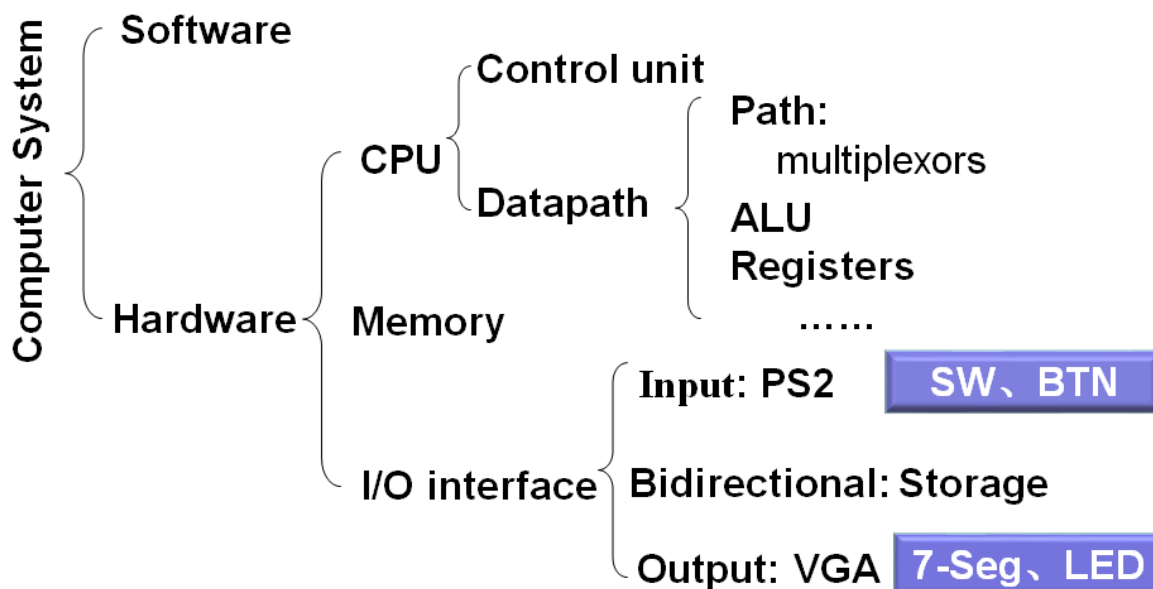
实验地点：无 实验日期：2020 年 3 月 29 日

一、实验目的和要求

1. 初步了解GPIO接口与设备
2. 了解计算机系统的基本结构
3. 了解计算机各组成部分的关系
4. 了解并掌握IP核的使用方法
5. 了解SOC系统并用IP核实现简单的SOC系统

二、实验内容和原理

Decomposability of computer systems



SOC

U1: CPU -SCPU

U2: ROM -ROM_D

U3: RAM -RAM_B

U4: 总线(含外设3~4) -MIO_BUS

U5: 七段显示接口 -Multi_8CH32

U6: 外设1- 七段显示设备 -Seg7_Dev

U7: 外设2-GPIO接口及LED -PIO

U8: 辅助模块一, 通用分频模块 -clk_div

U9: 辅助模块二, 机械去抖模块 -Anti_jitter

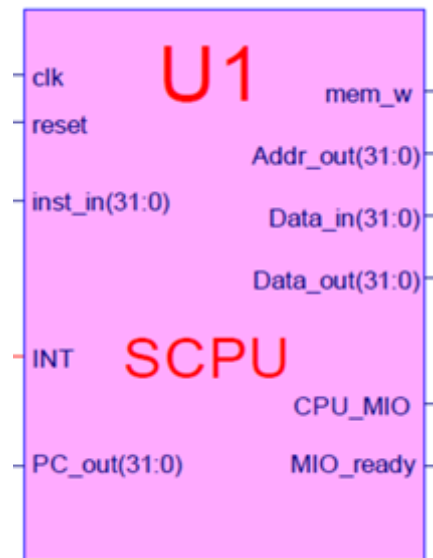
U10: 通用计数器 -Counter_x

U1-SCPU

R-Type: add, sub, and, or, xor, nor, slt, srl, jr, jalr, eret

I-Type: addi, andi, ori, xori, lui, lw, sw, beq, bne, slti

J-Type: J, Jal



U2-ROM_B

•1024×32bit



U3-RAM_B

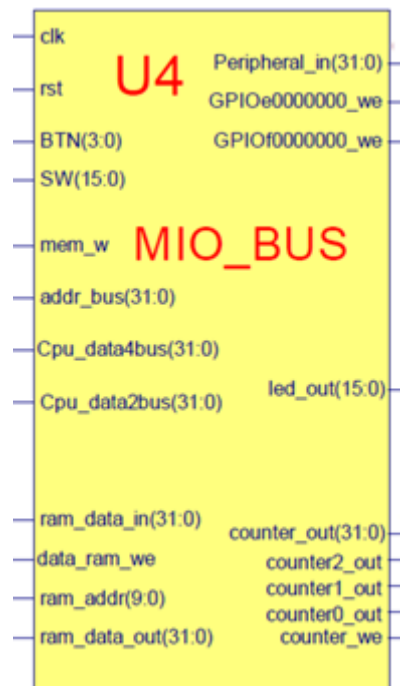
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U4-MIO_BUS

the data exchange module between CPU and the outside devices

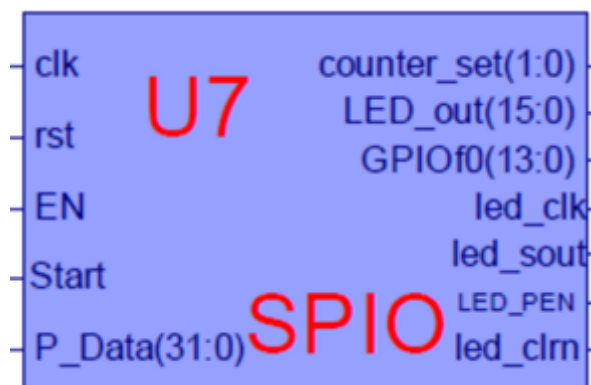
store data and buses of 7-Seg, SW, BTN and LED



U7-SPIO

LEDs devices and counter controller read and write

can be recalled to check condition



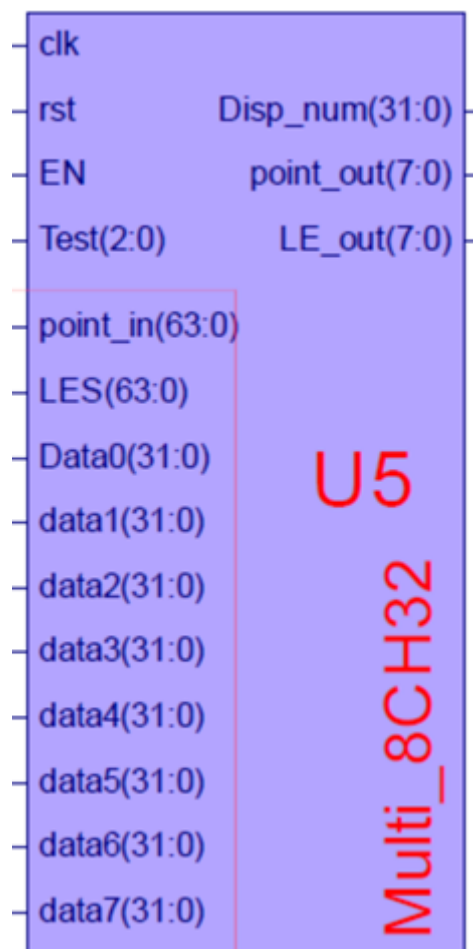
U6-Seg7_Dev

7 segments display devices



U5-Multi_8CH32

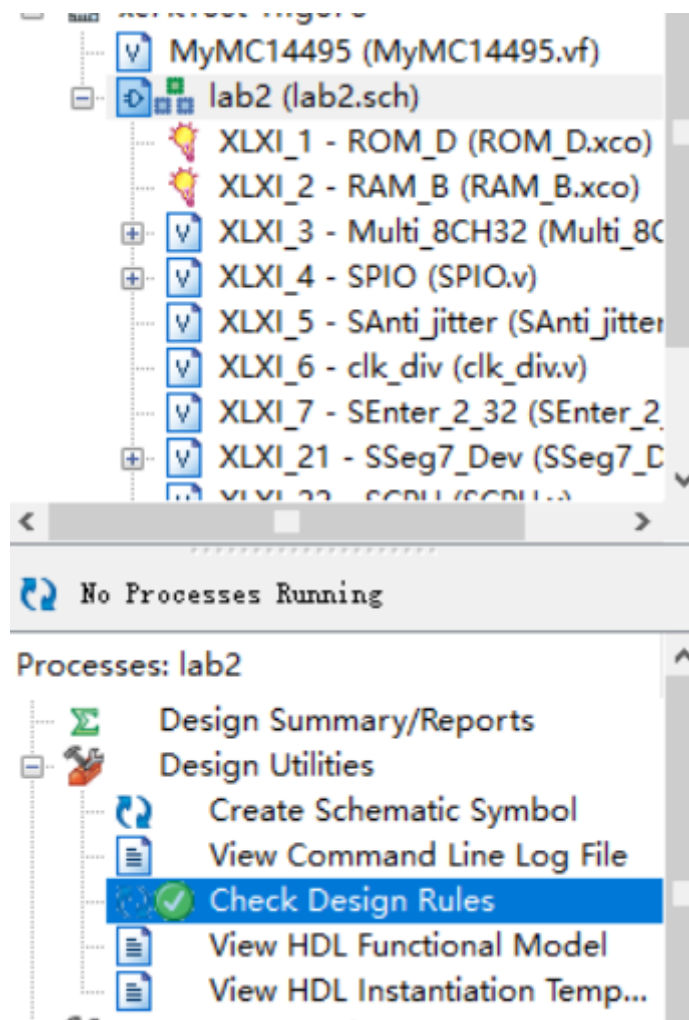
bus module for Seg7_Dev



U10-Counter_x

3 channel counter, using for timing problem

- counter_set=00、01、10 -> channel 0、1、2
- counter_set=11 -> set up counting channel



四、讨论与心得

The relation of all the wires and buses really need me to pay attention and be careful. In fact the time I spend on correcting the mistaken is much longer than that on drawing for the first time. Why do I made so much mistake? I think one of the reason is I didn't strictly follow the procidure suggested in the power points. In addition, maybe in the next experiment I should display the names of the wires in the scheme to make the graph more readable.

To make a conclusion, I think this time I've successfully done all the job required and learned a lot.