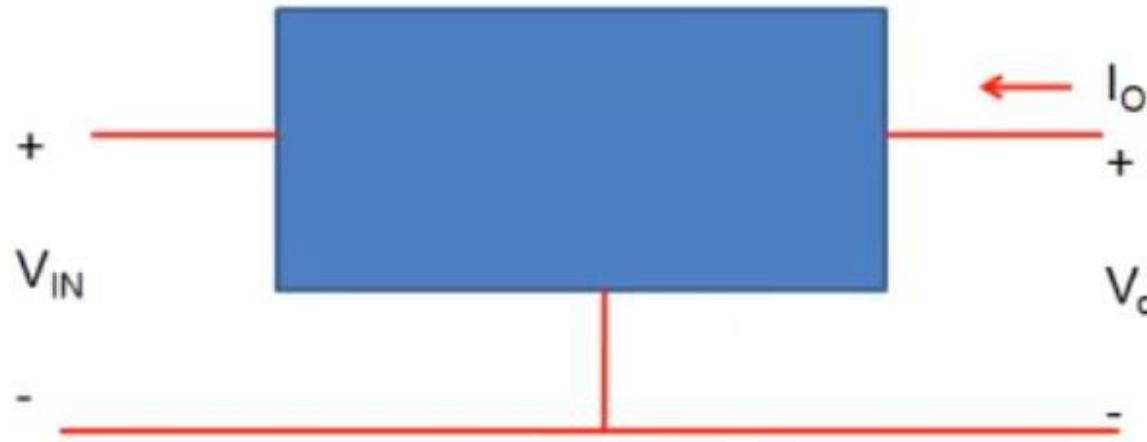


MOSFET

Transistor



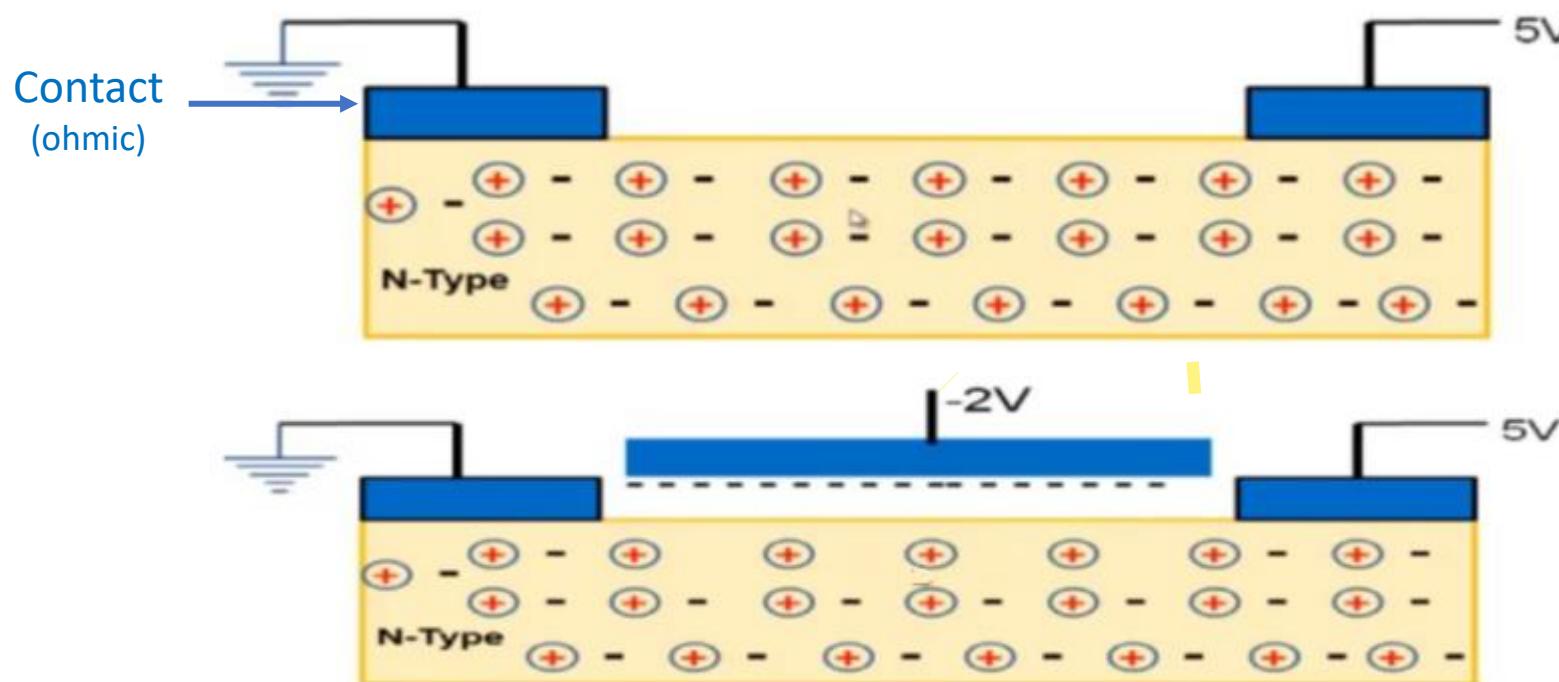
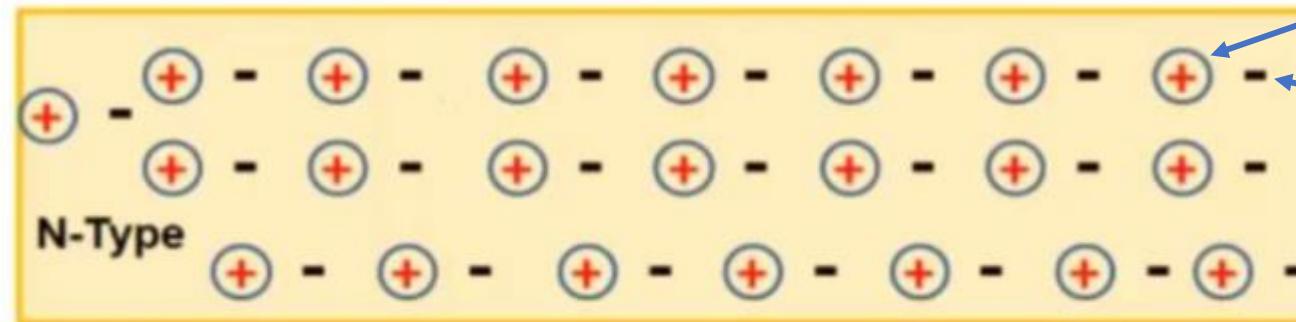
Current I_O is much more sensitive to V_{IN} than V_o

transconductance

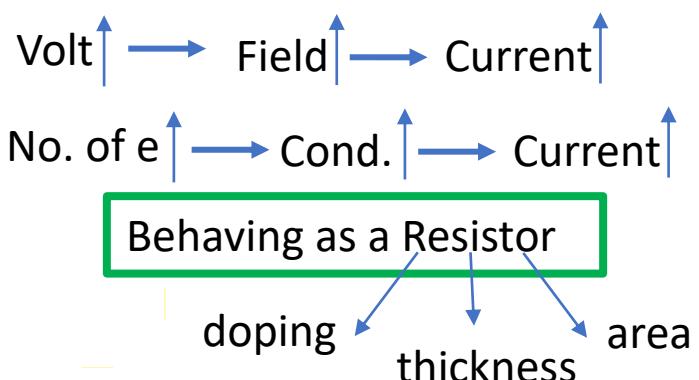
$$\frac{\partial I_O}{\partial V_{in}} \gg \frac{\partial I_O}{\partial V_o}$$

Field Effect Principle

$$\frac{\partial I_o}{\partial V_{in}} \gg \frac{\partial I_o}{\partial V_o}$$



- Amount of current flow depend on applied voltage



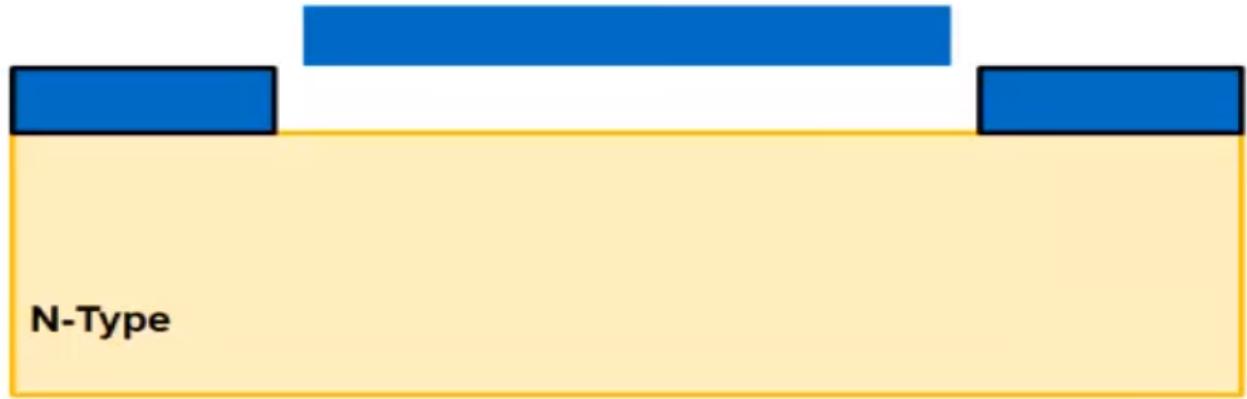
- Take another plate, place very close (by some means) to n-type semiconductor.
- Appy a negative voltage.
- Push the e away from the surface.

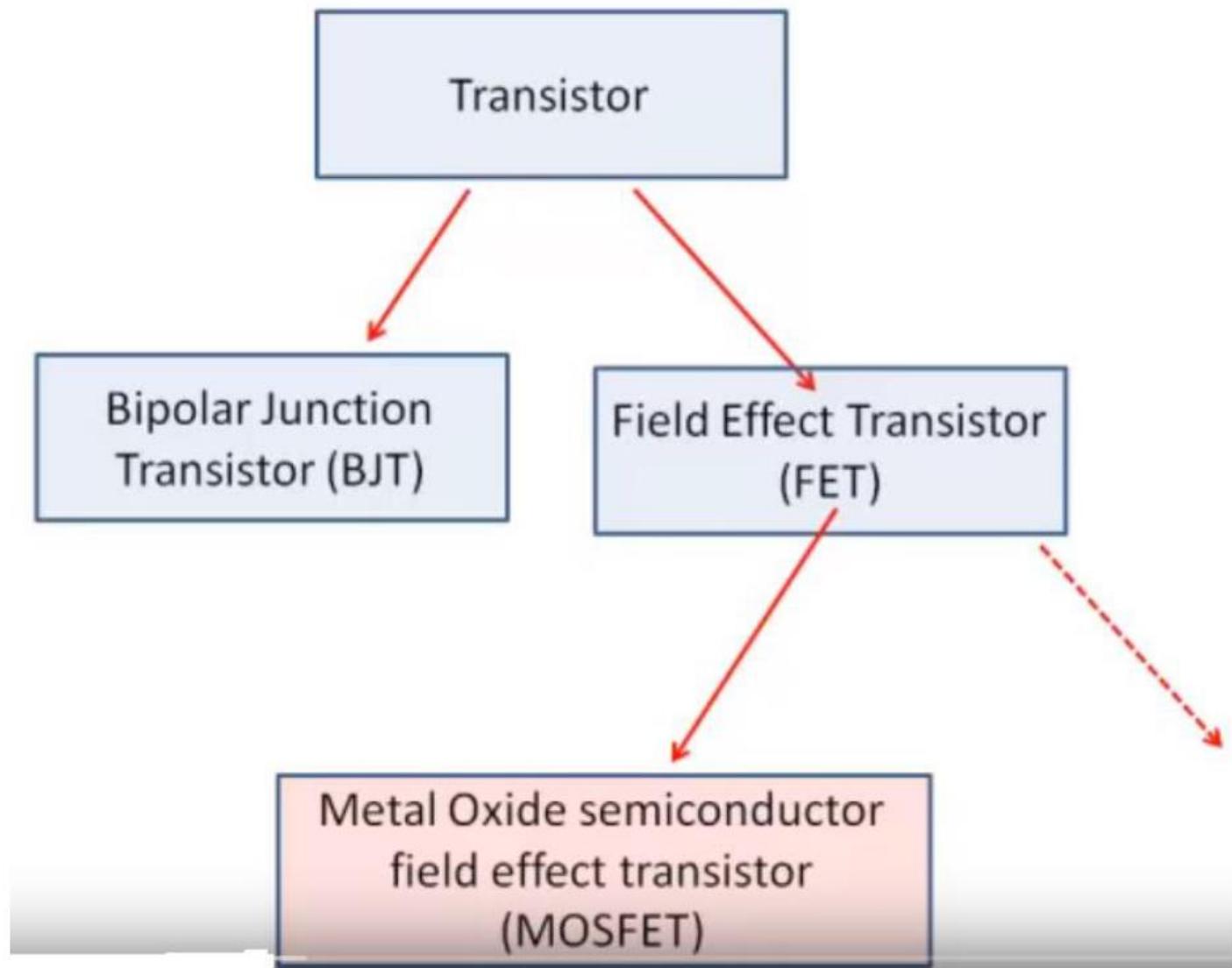
Capacitor

Modulation of conductivity using electric field

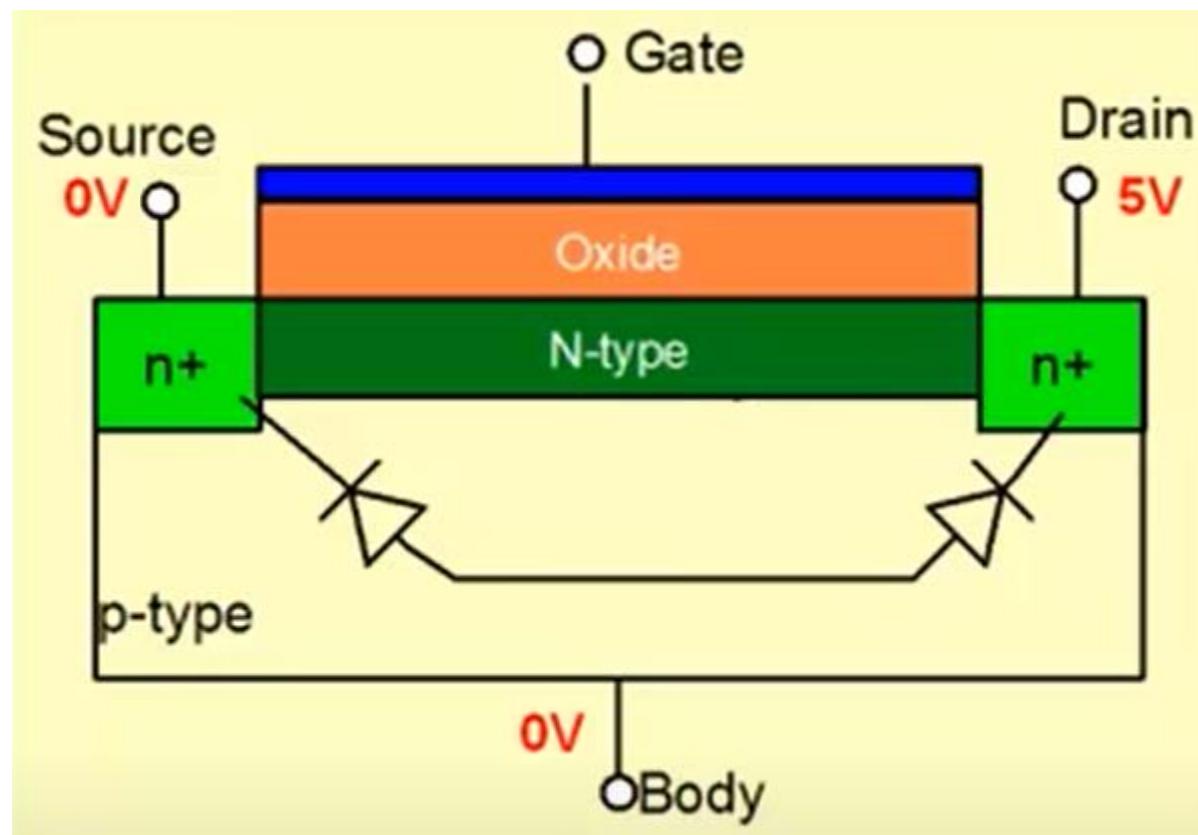
Transconductance

Field Effect Principle



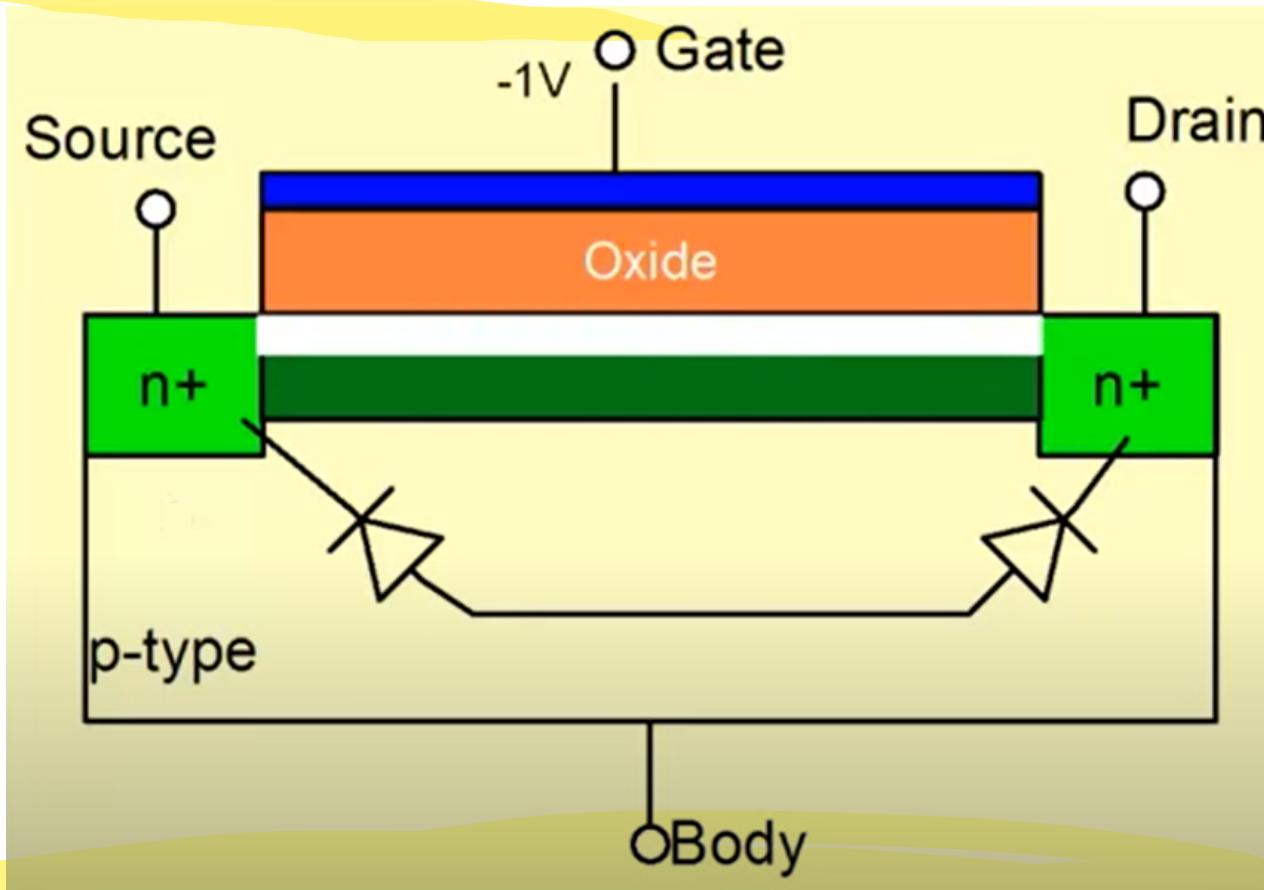


Depletion-Mode Transistor



Depletion-Mode Transistor

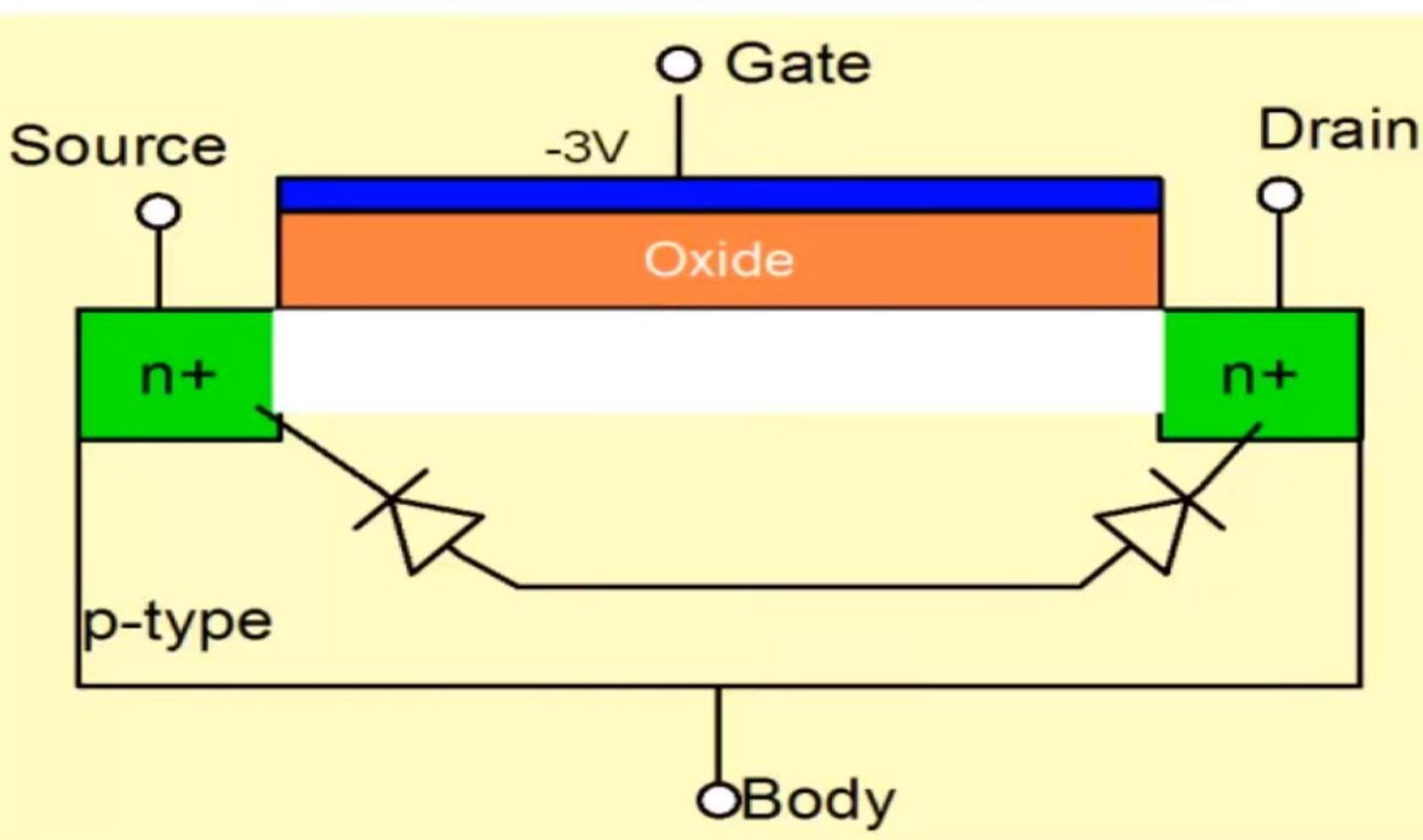
Channel exists at zero gate voltage and is depleted by gate voltage



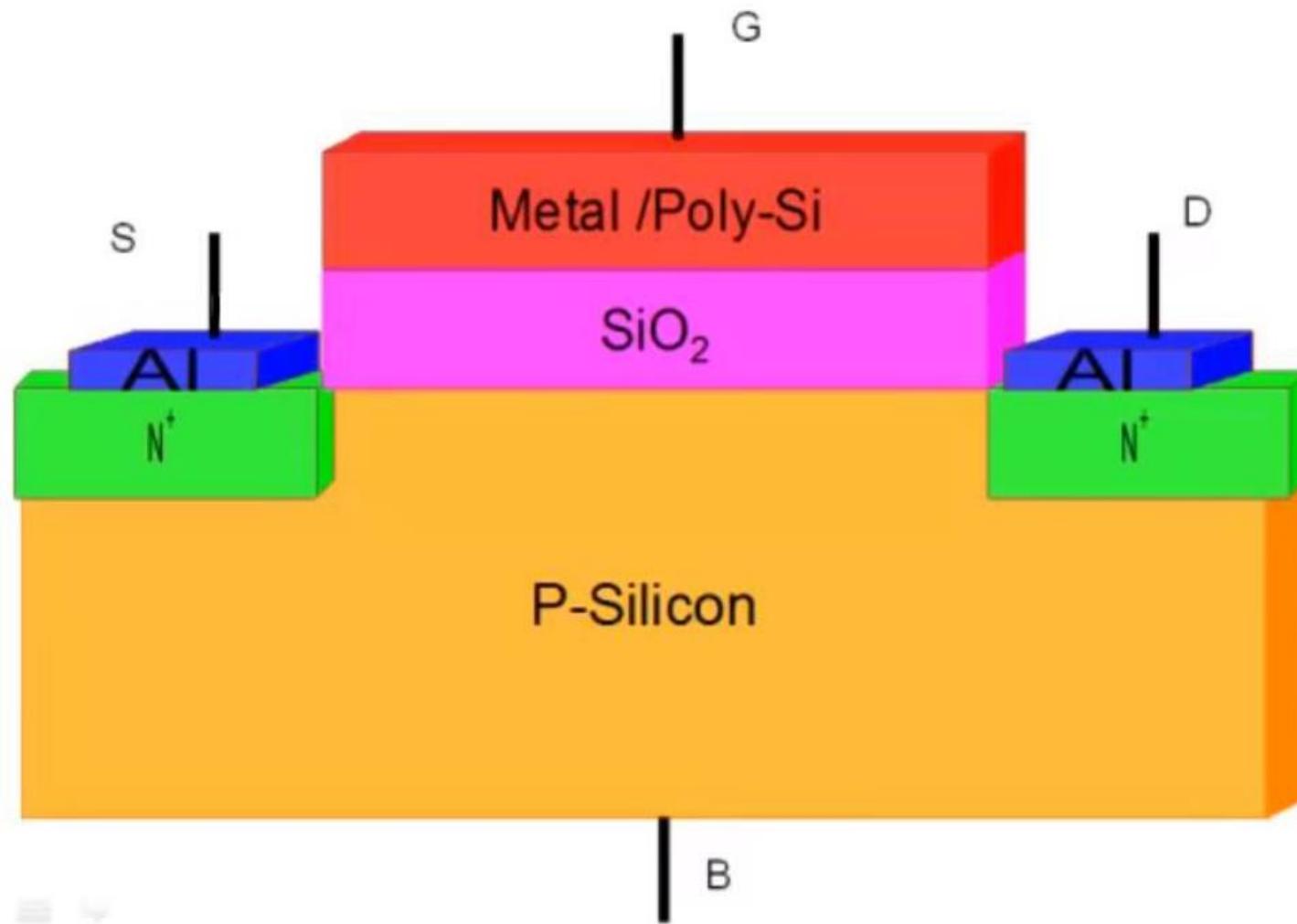
In a depletion-mode transistor, a channel exists without any gate voltage being applied and current flows when drain voltage is applied.

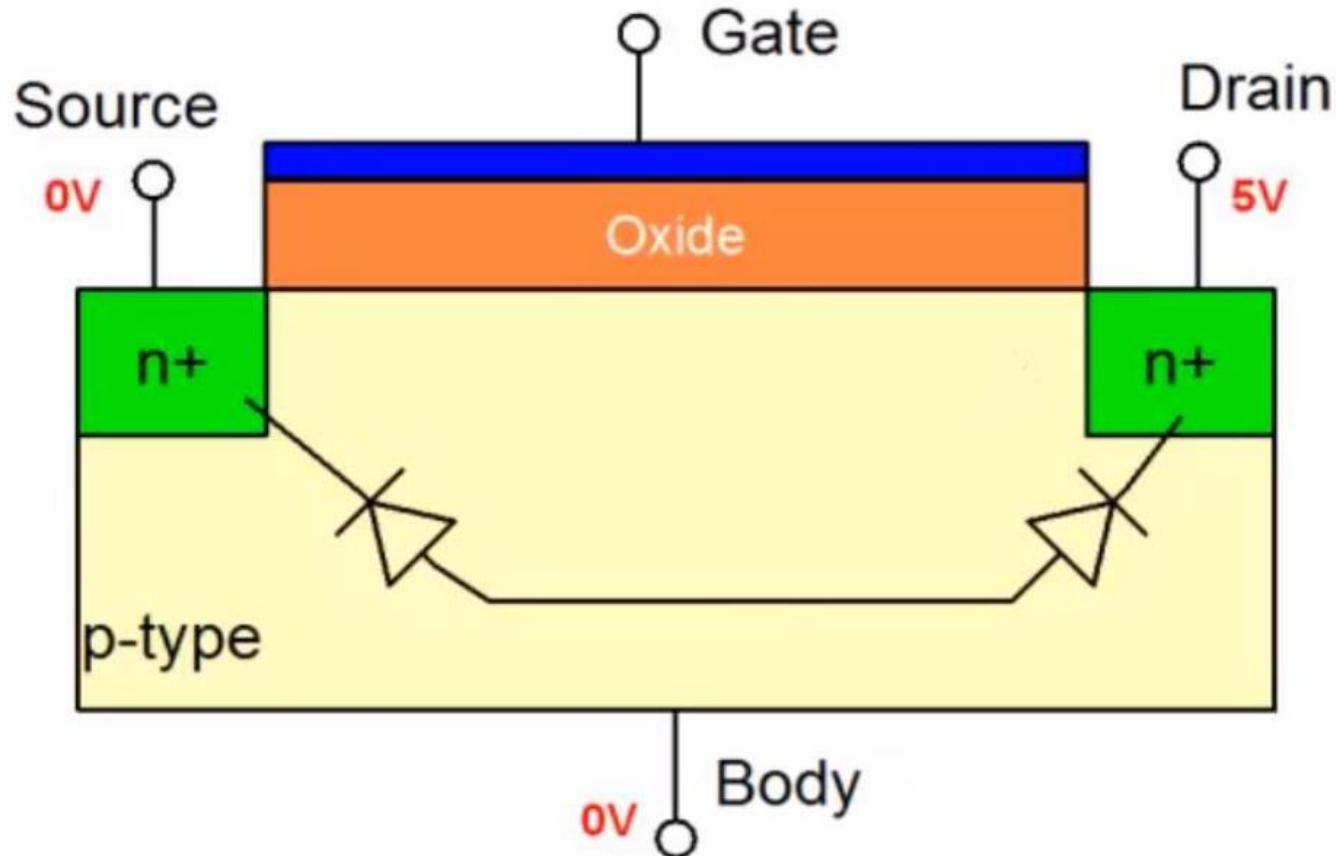
Negative gate voltage is applied to deplete the channel of carriers and cause current to reduce.

Channel exists at zero gate voltage and is depleted by gate voltage

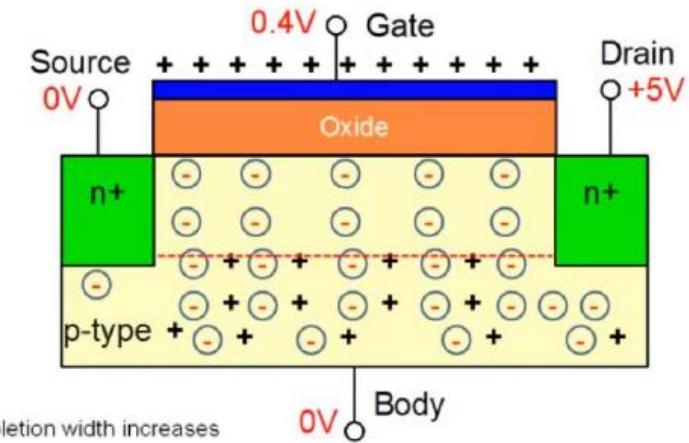
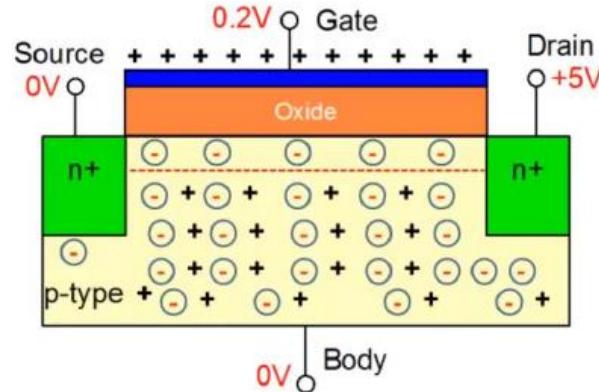
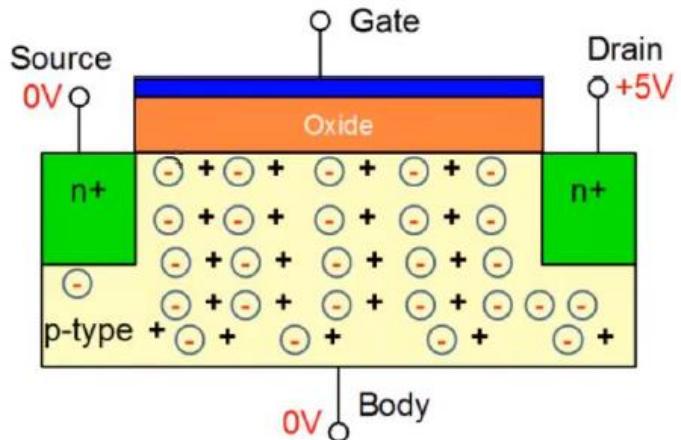


Channel is completely pinched off and current ~zero



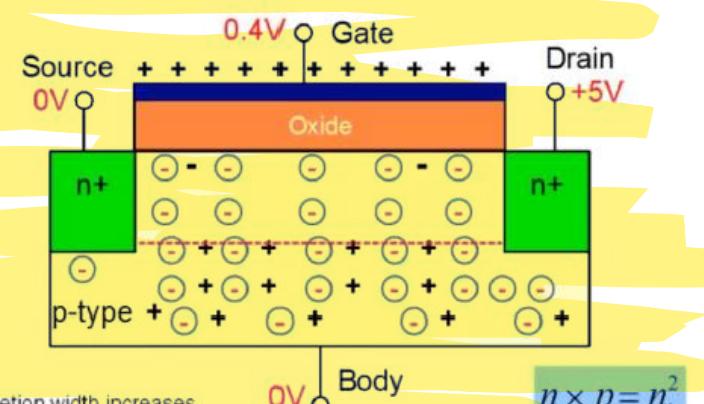


No channel exists when gate voltage is zero and current is zero as well.



Depletion Region is formed near the Si/SiO₂ interface

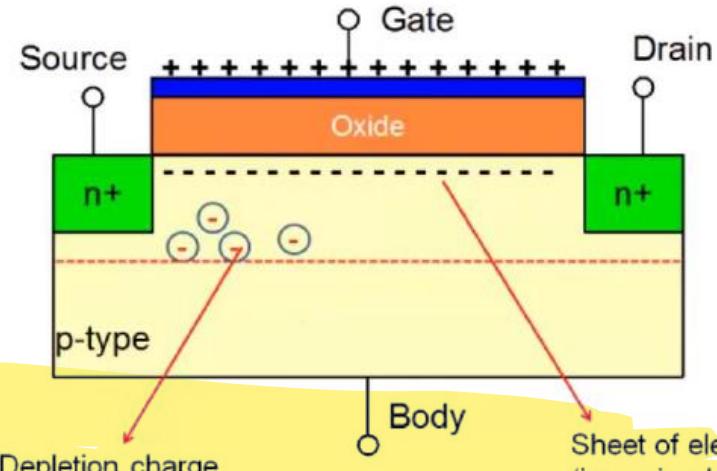
Depletion width increases



Depletion width increases

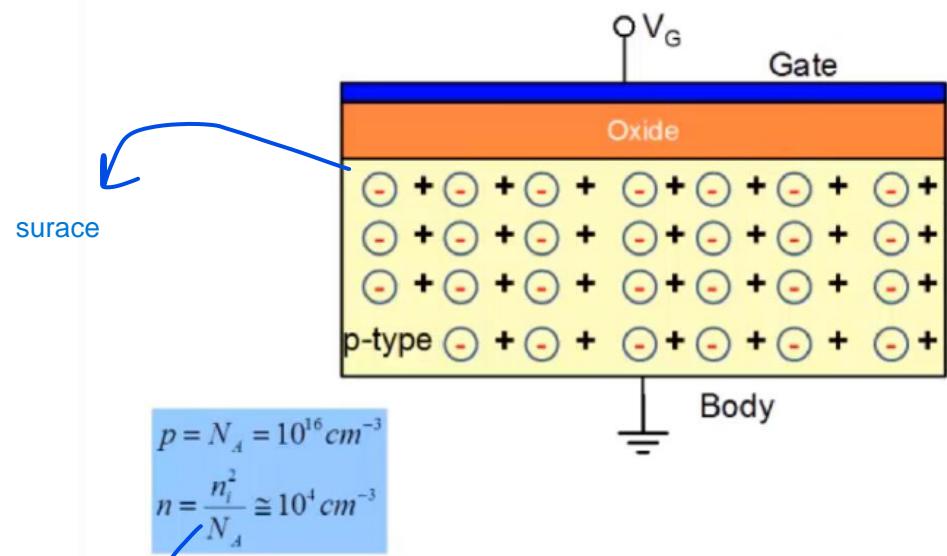
But something interesting happens: electron density at the surface also increases

At a sufficiently large voltage ($>V_{THN}$) a channel of electrons forms at the Si/SiO₂ interface.



Conductivity modulation at the surface?

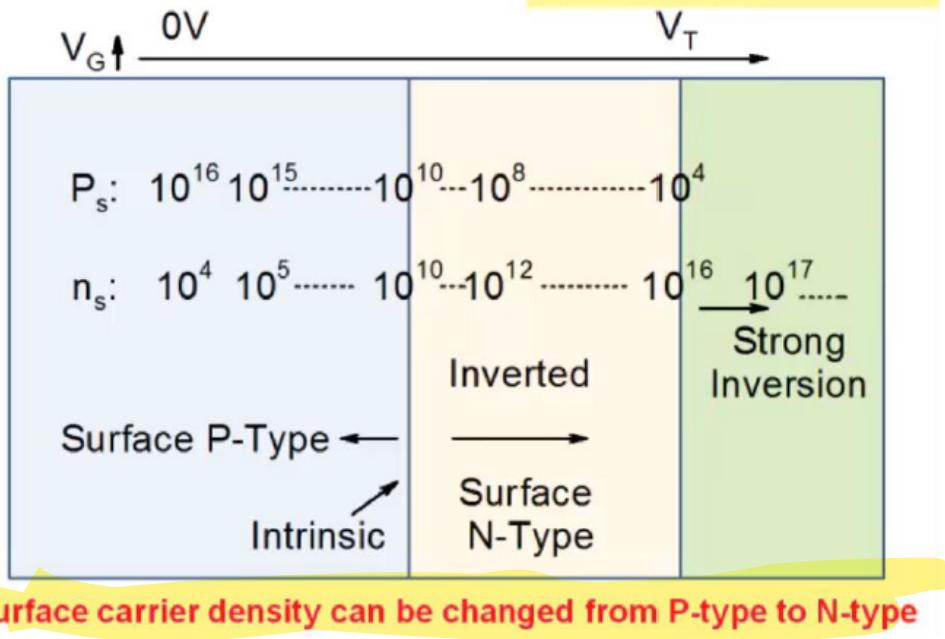
MOS capacitor constitutes the heart of a MOSFET



this is for intrinsic

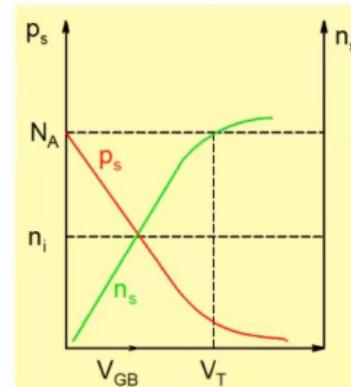
Field Effect...

$$n_s \times p_s = n_i^2 \cong 10^{20} \text{ cm}^{-3}$$



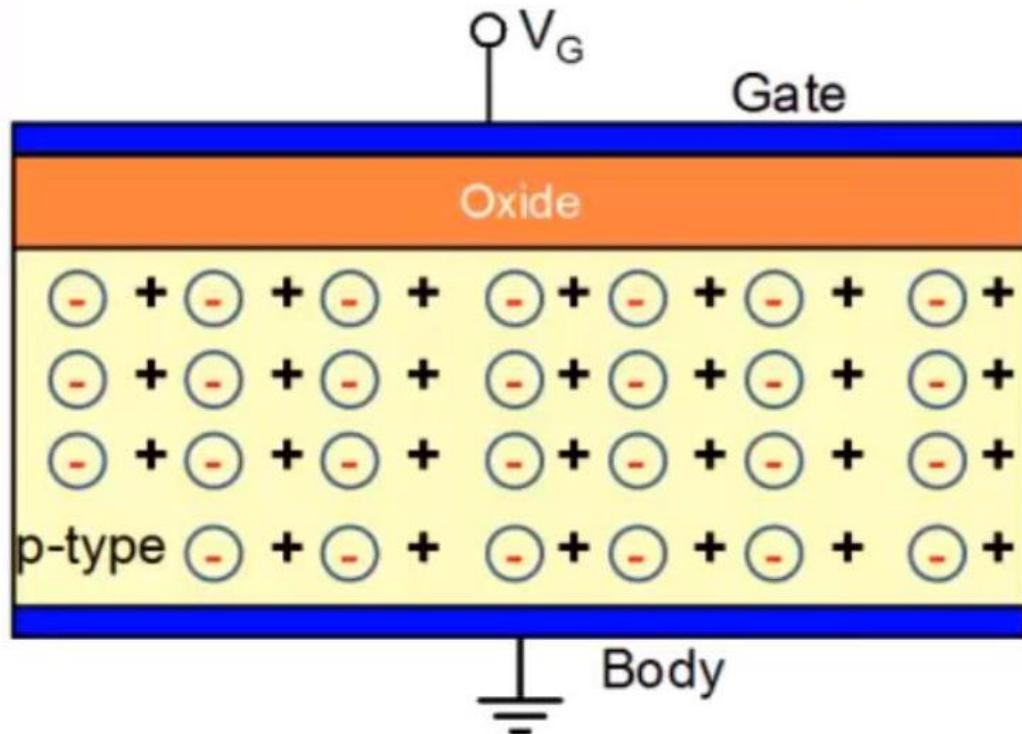
Surface carrier density can be changed from P-type to N-type

Surface Carrier Density



Flat band condition

$$V_G = V_{FB}$$

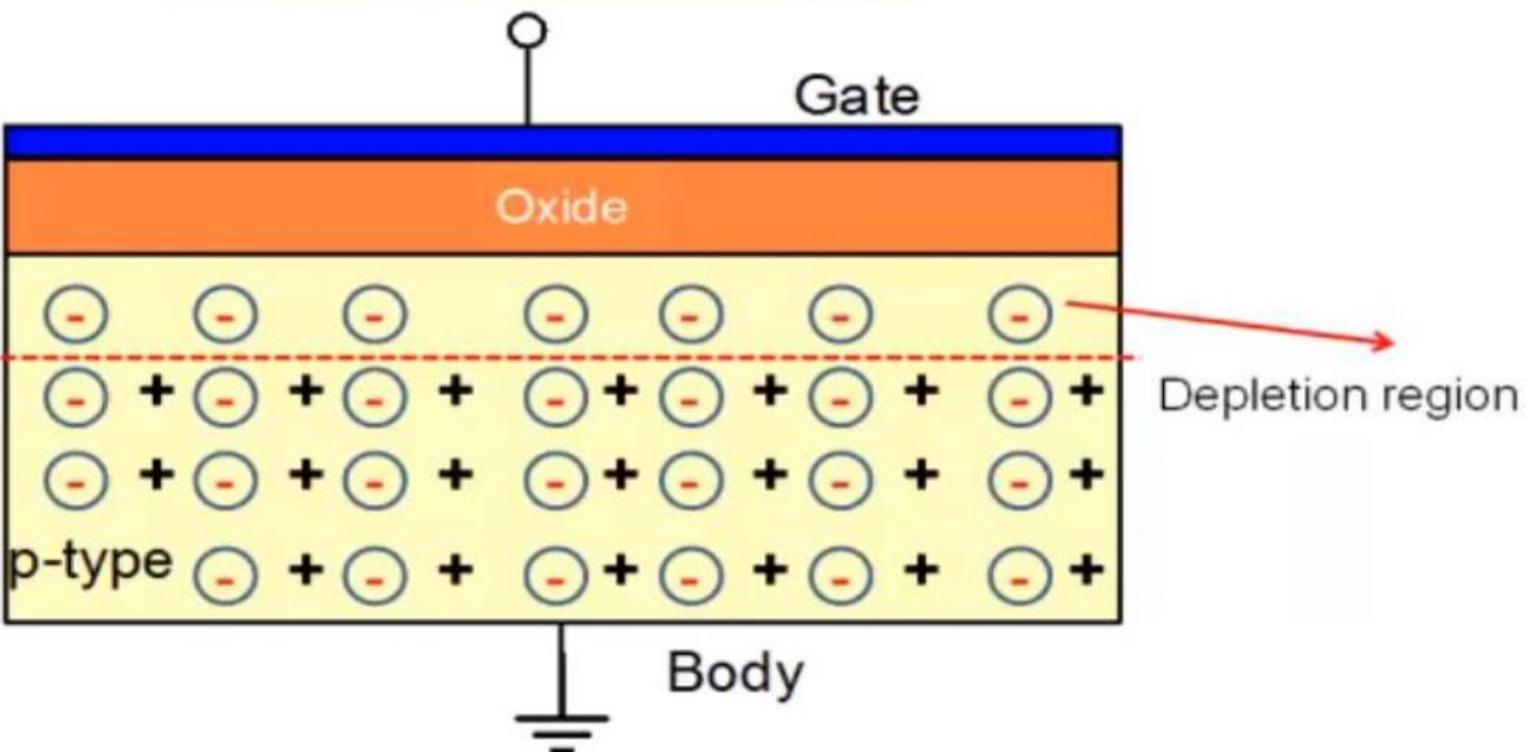


Whenever two different material are brought into contact, an internal potential difference develops like in a pn junction. Thus even when no gate voltage is applied, there is a voltage across the mos capacitor.

$V_G = V_{FB}$; Flat-band condition meaning no NET voltage across the capacitor.
Uniform hole density everywhere

Depletion

$$V_G > V_{FB} \text{ but } V_G < V_{THN}$$

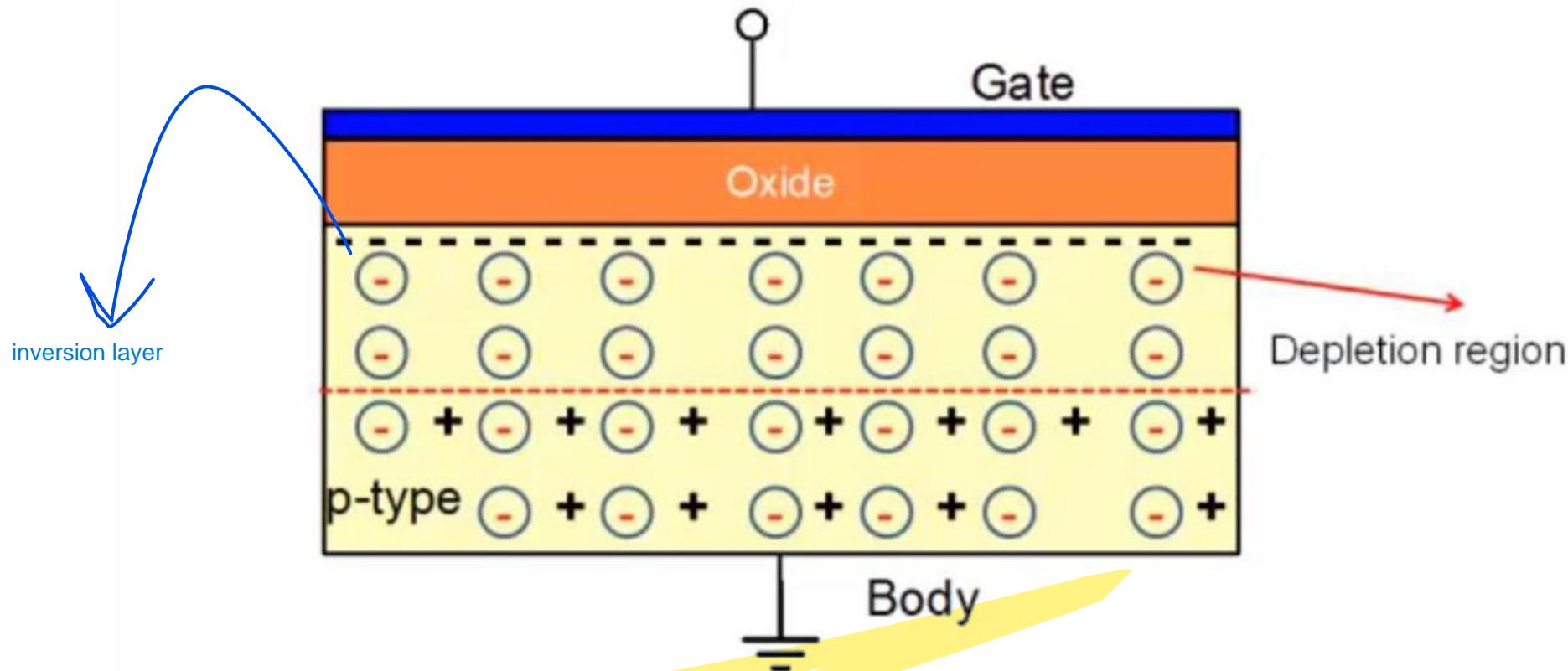


Holes are depleted from the surface $p_s < p_b$

Although $n_s > n_b$ electron density is also very small

Strong Inversion

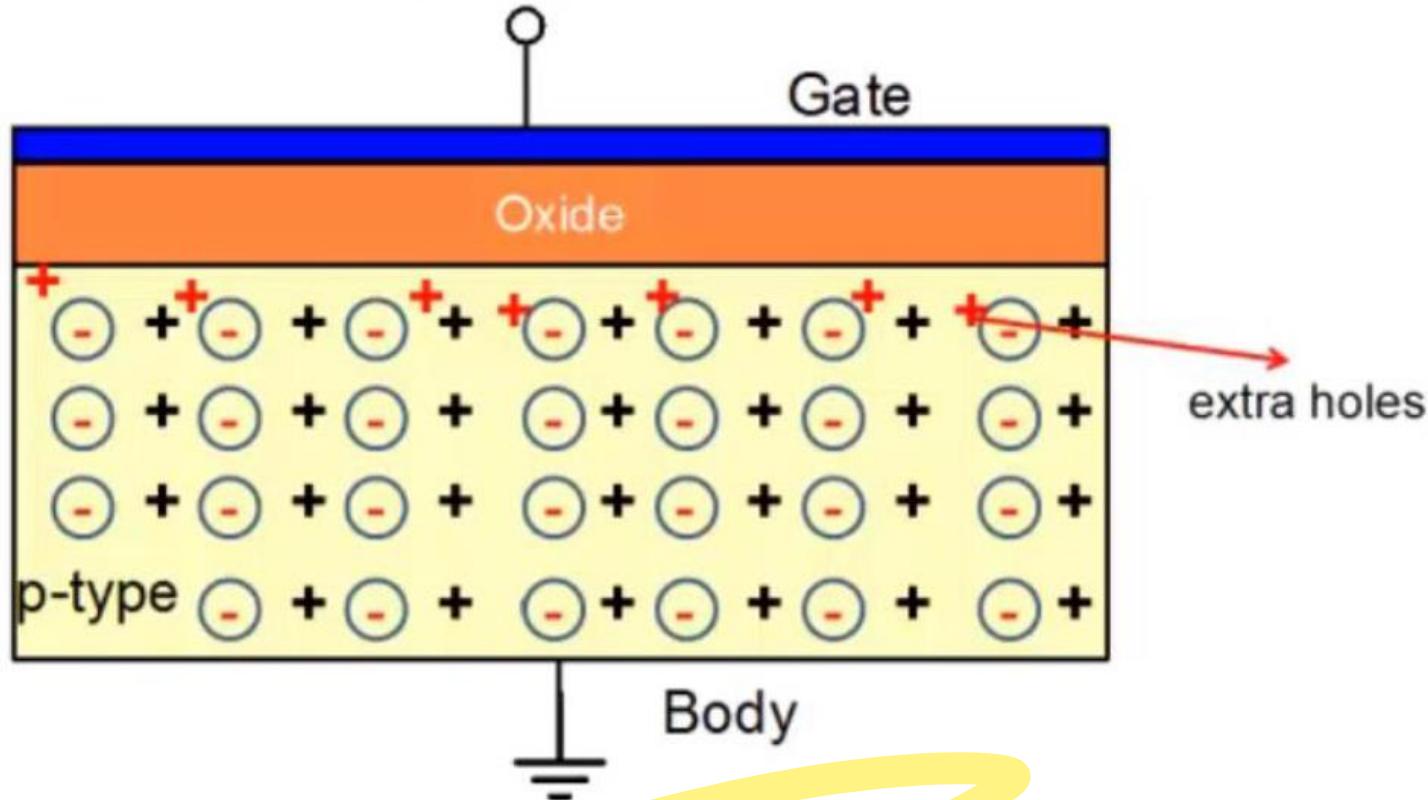
$$V_G > V_{THN}$$



Electrons are accumulated at the surface $n_s \gg N_A$

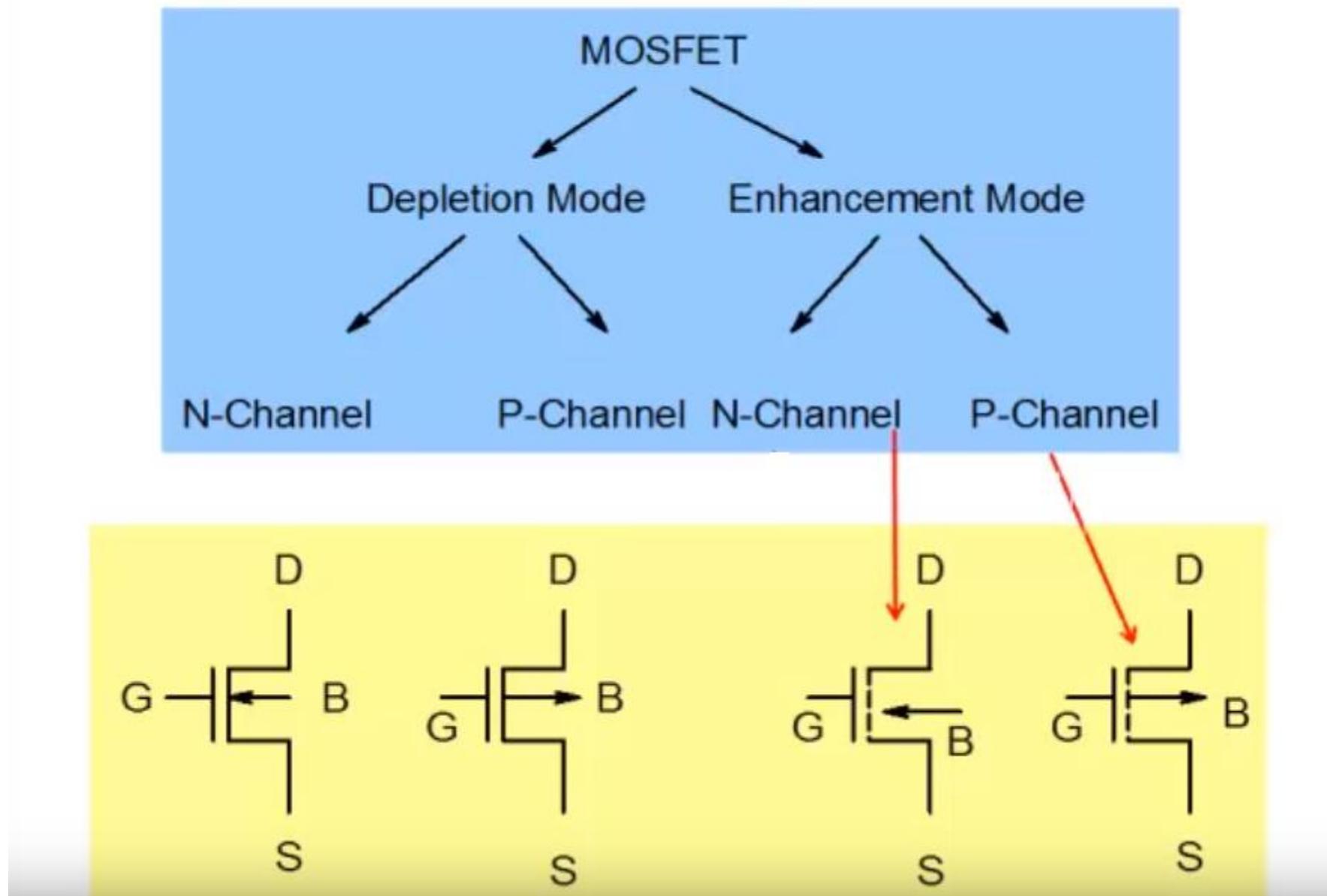
Accumulation

$$V_G < V_{FB}$$

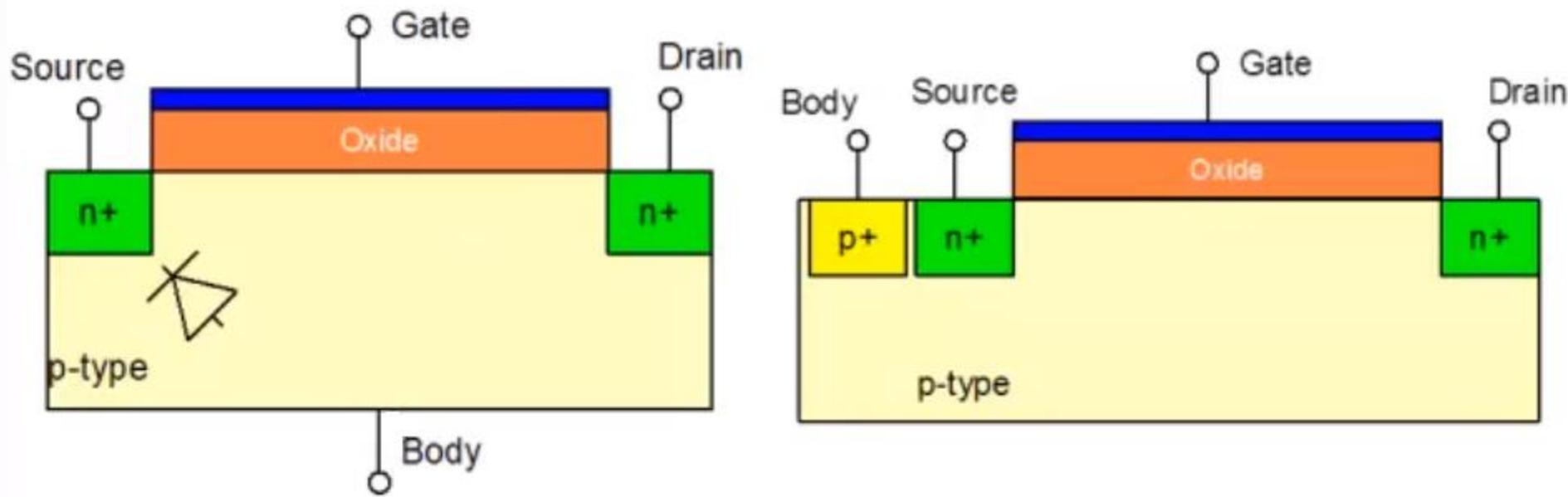
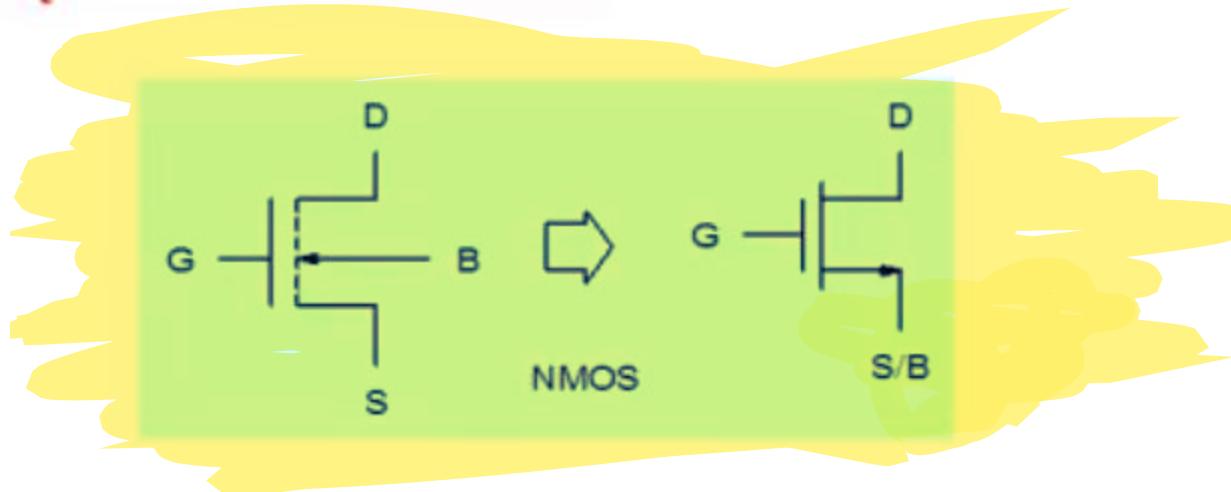


Holes are accumulated at the surface $p_s > p_b$

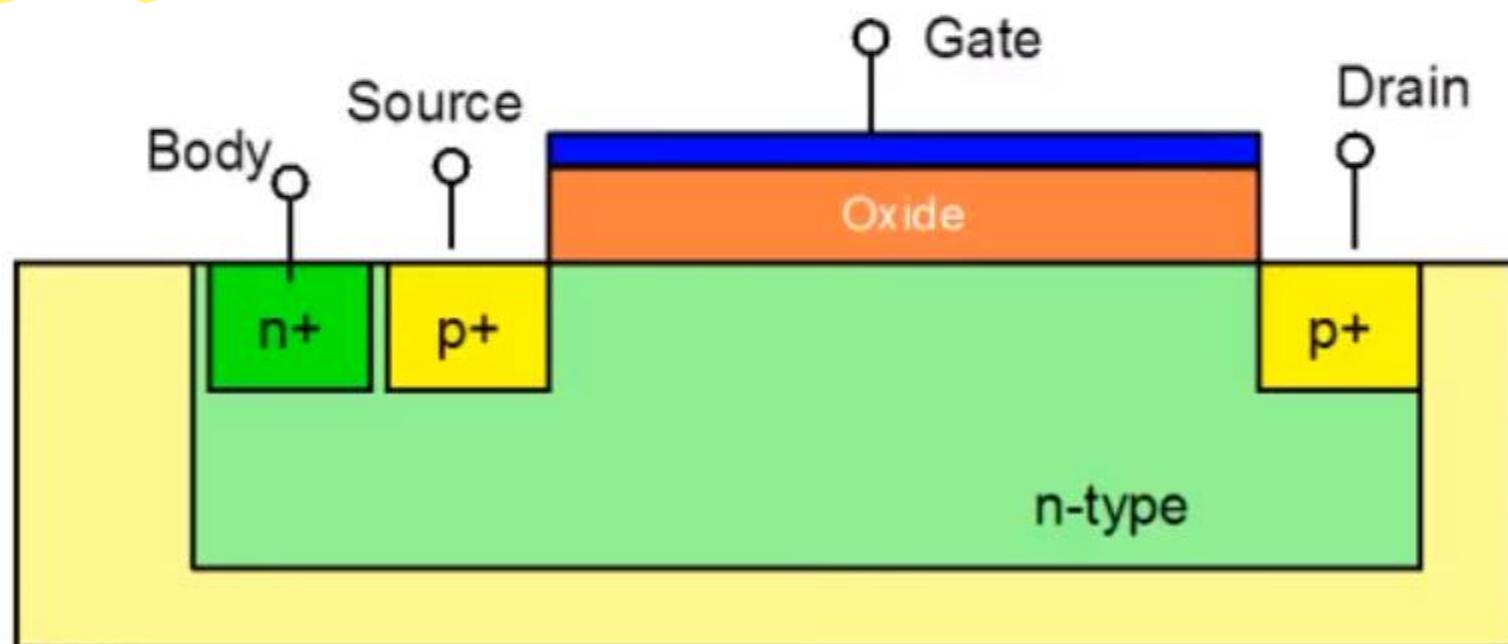
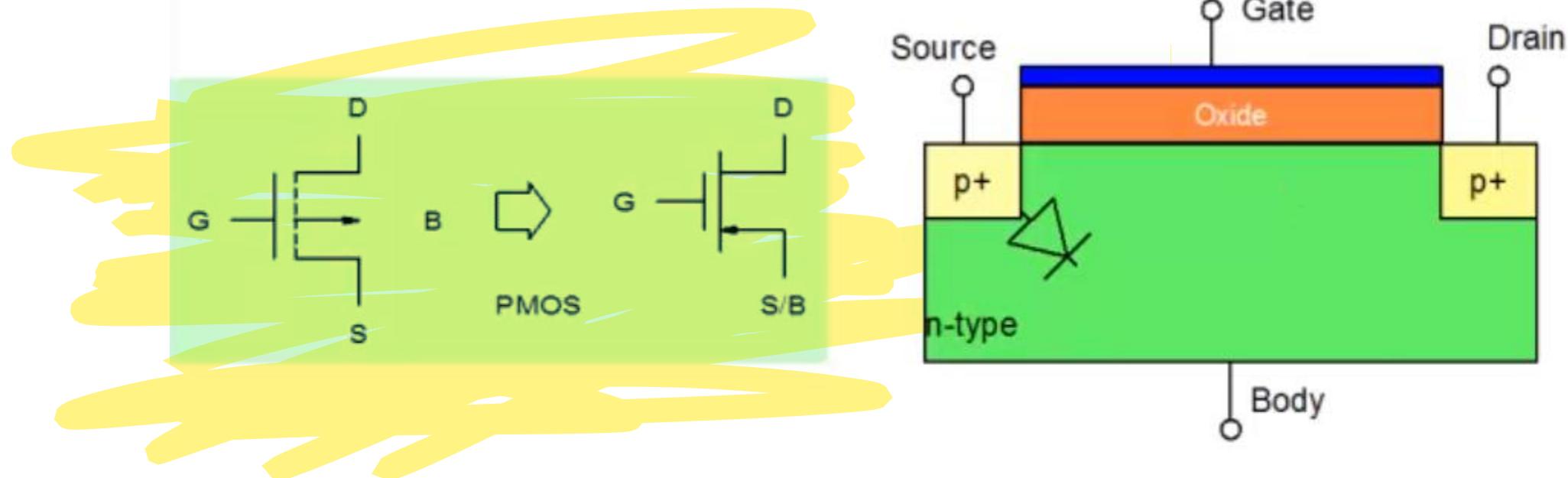
Metal Oxide Semiconductor Field Effect Transistor:

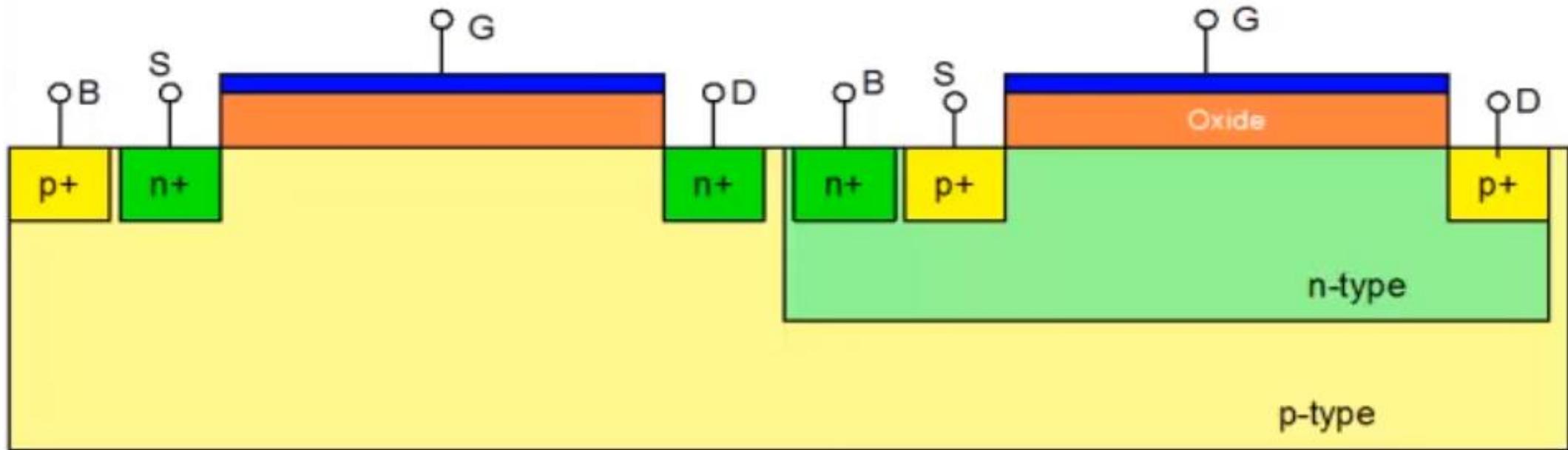


Simplified Symbols and structure

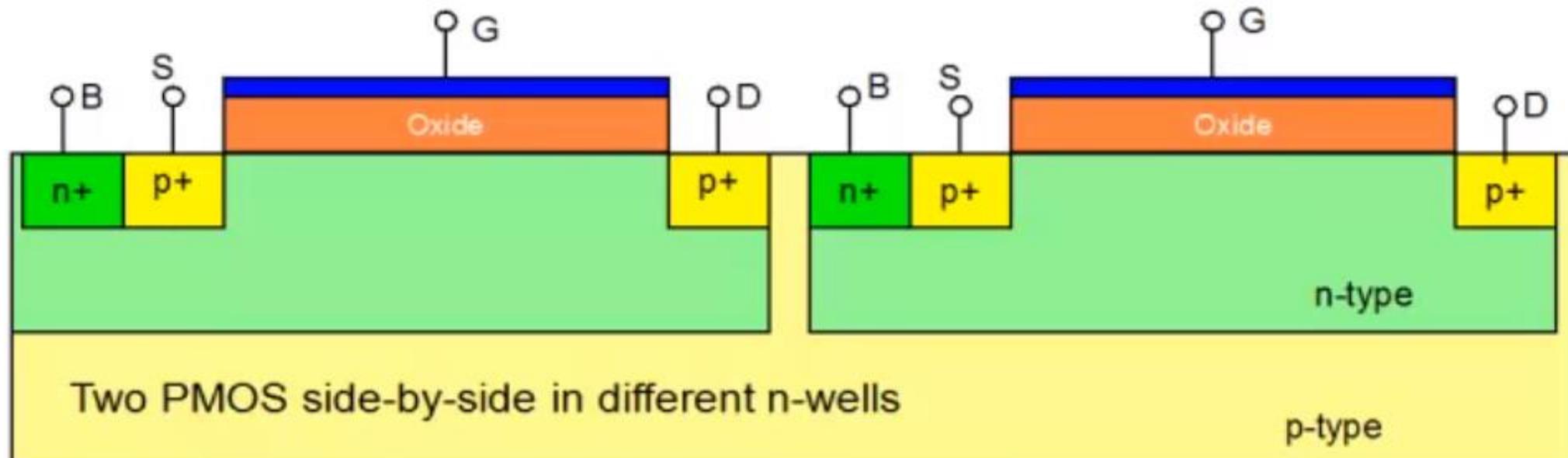
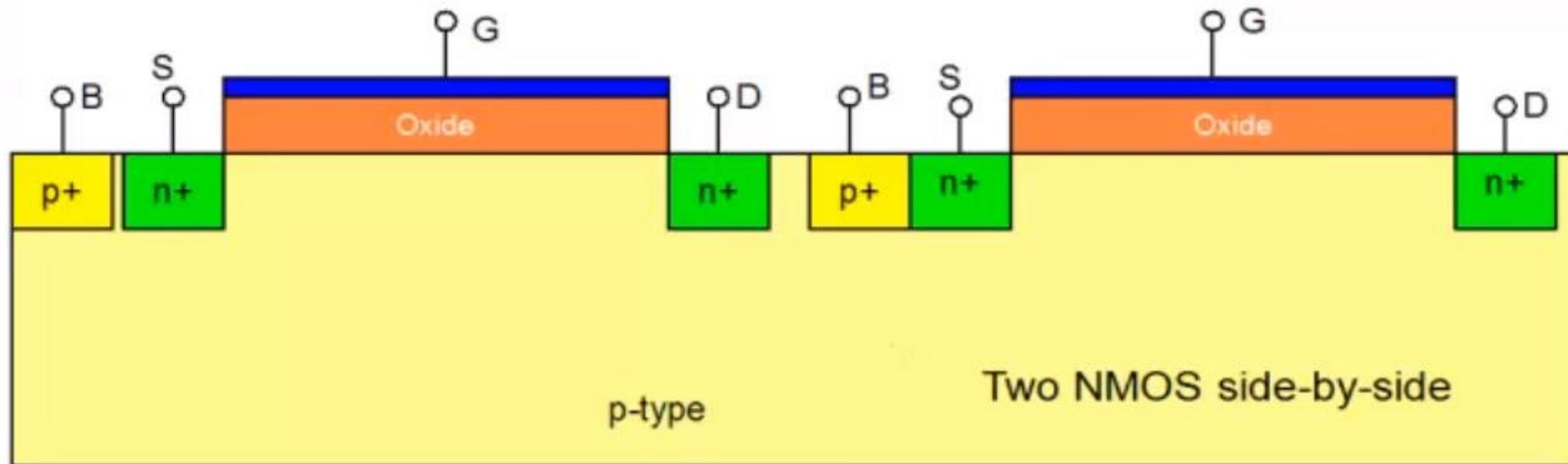


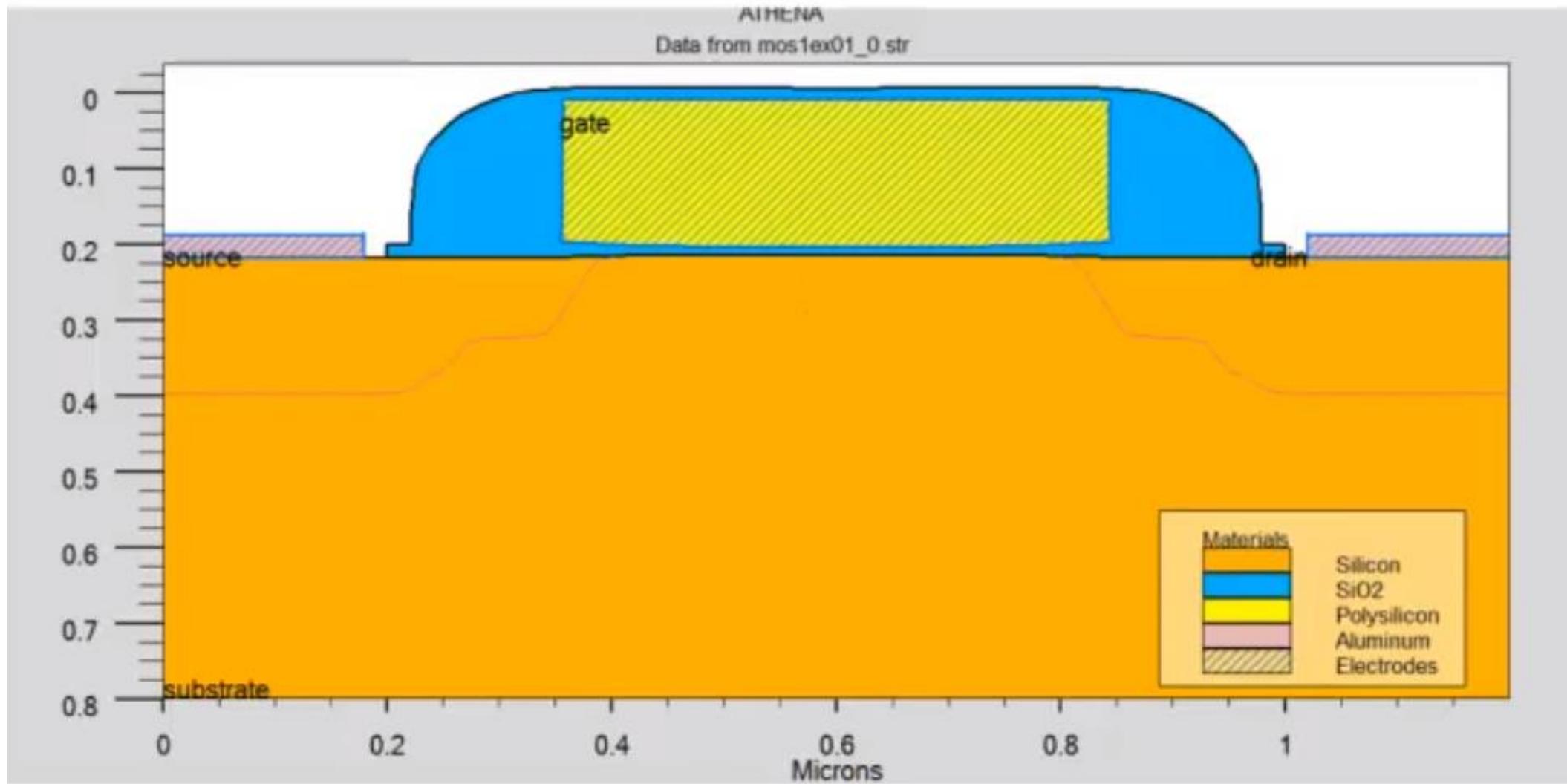
Simplified Symbols and structure

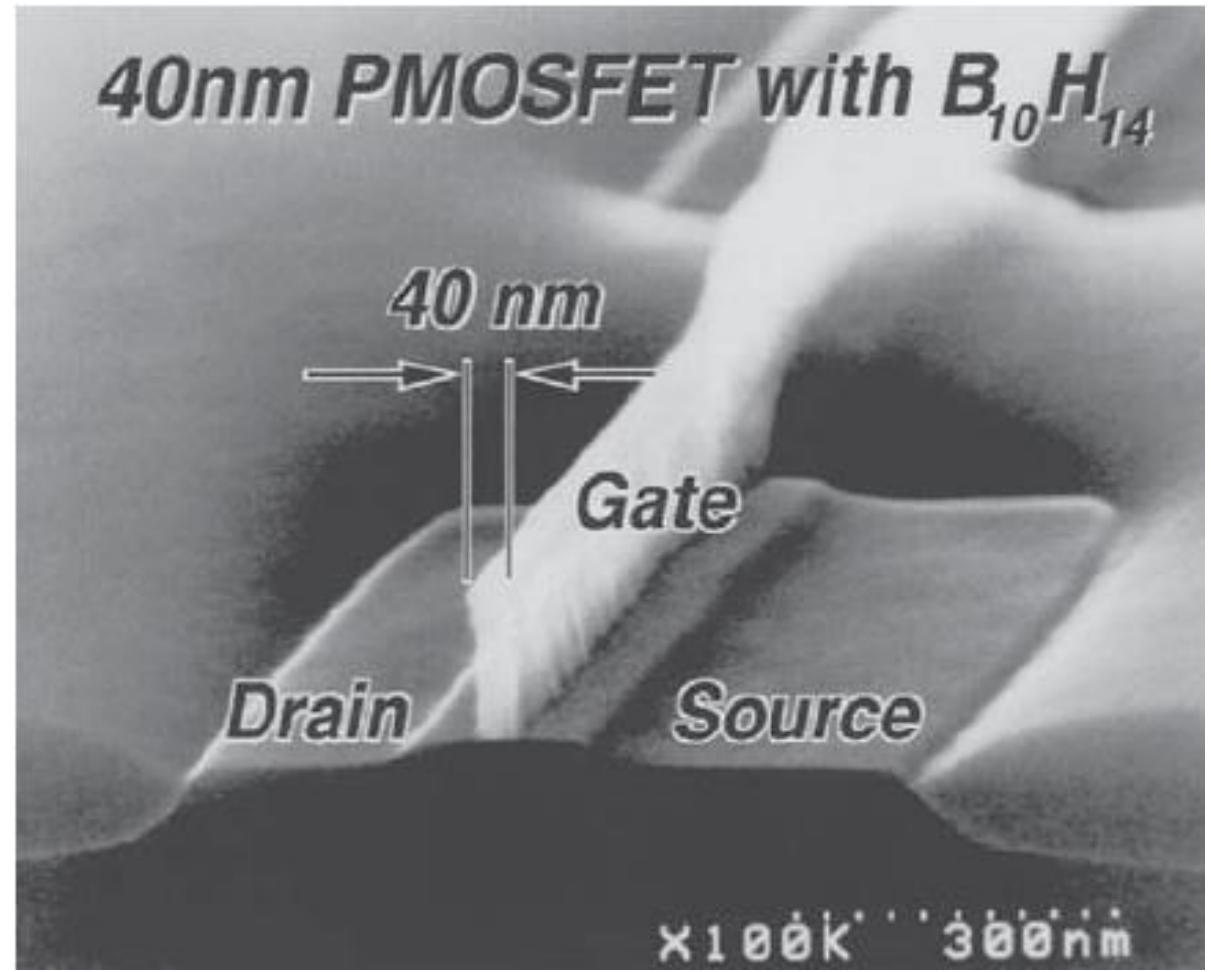
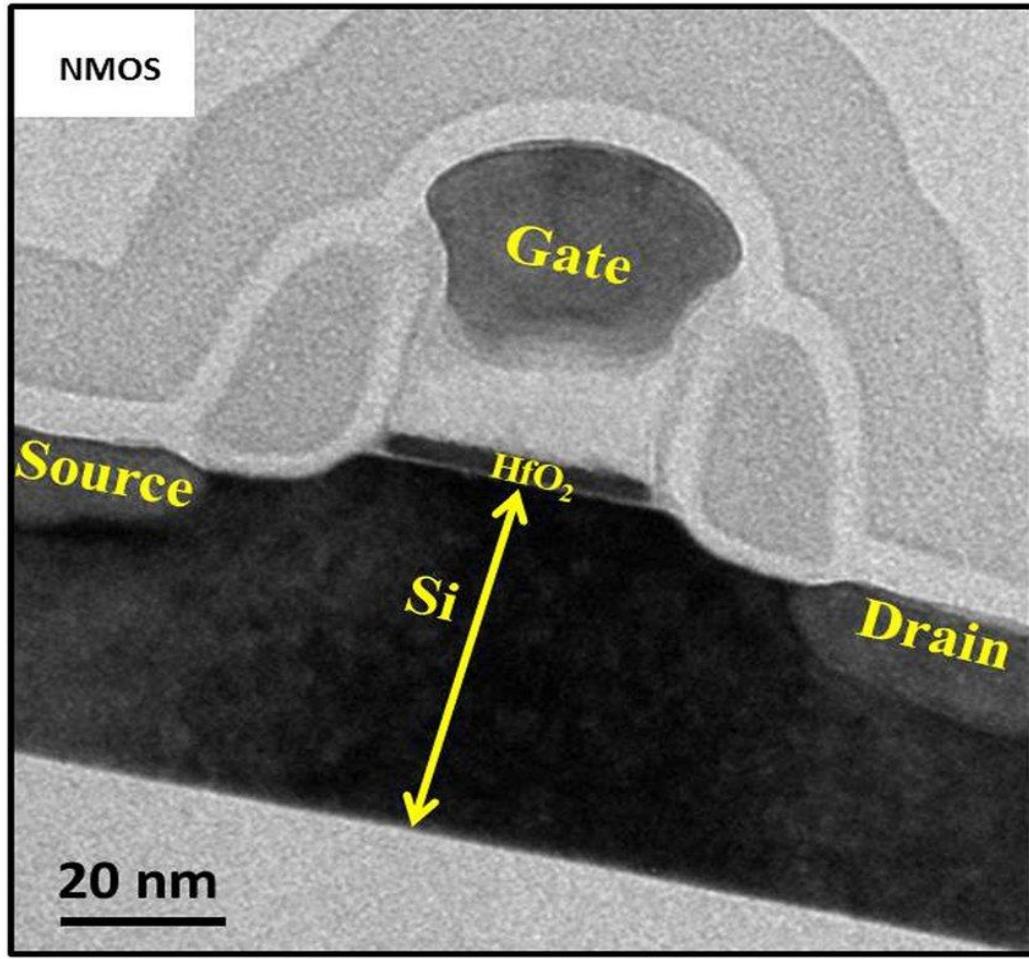




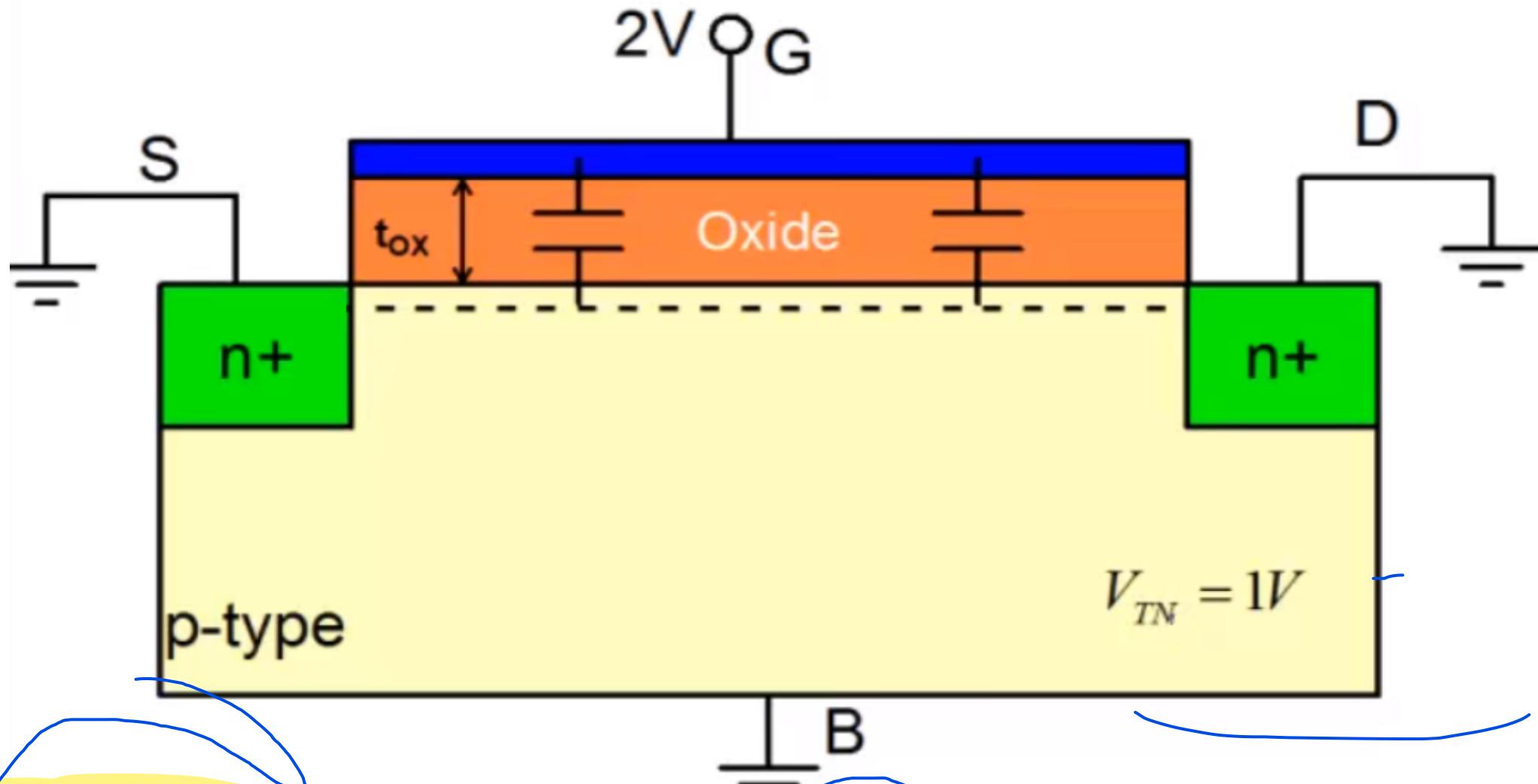
- Body potential of NMOS transistors is same and is normally connected to the most negative voltage in the circuit to ensure that $V_{BS} < 0$ and thus body-source PN junction is reverse biased.
- Each PMOS can be fabricated in a separate individual N-well and thus each pmos body terminal can have a distinct voltage. Normally body and source terminals of PMOS are shorted together.







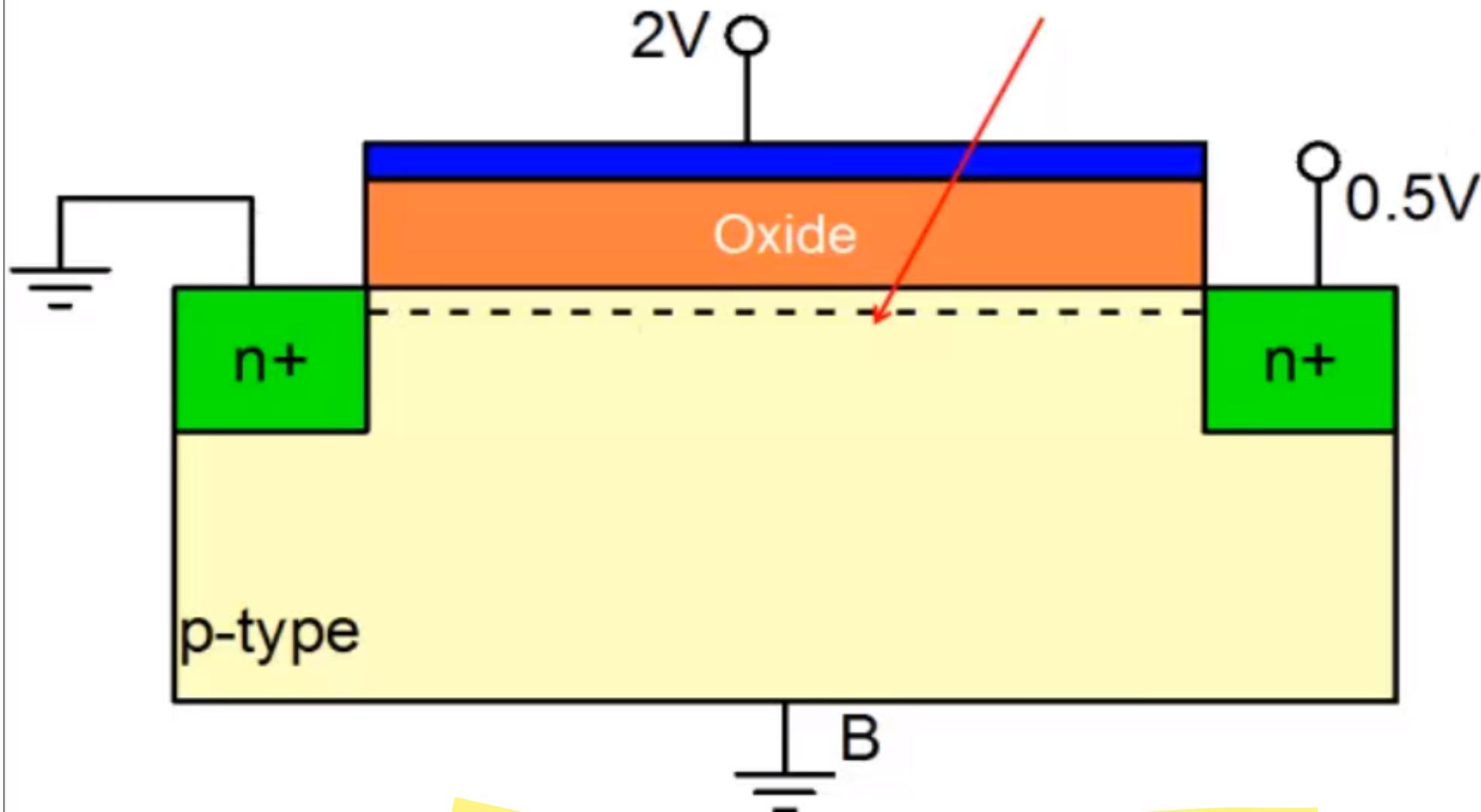
Operation of the MOSFET



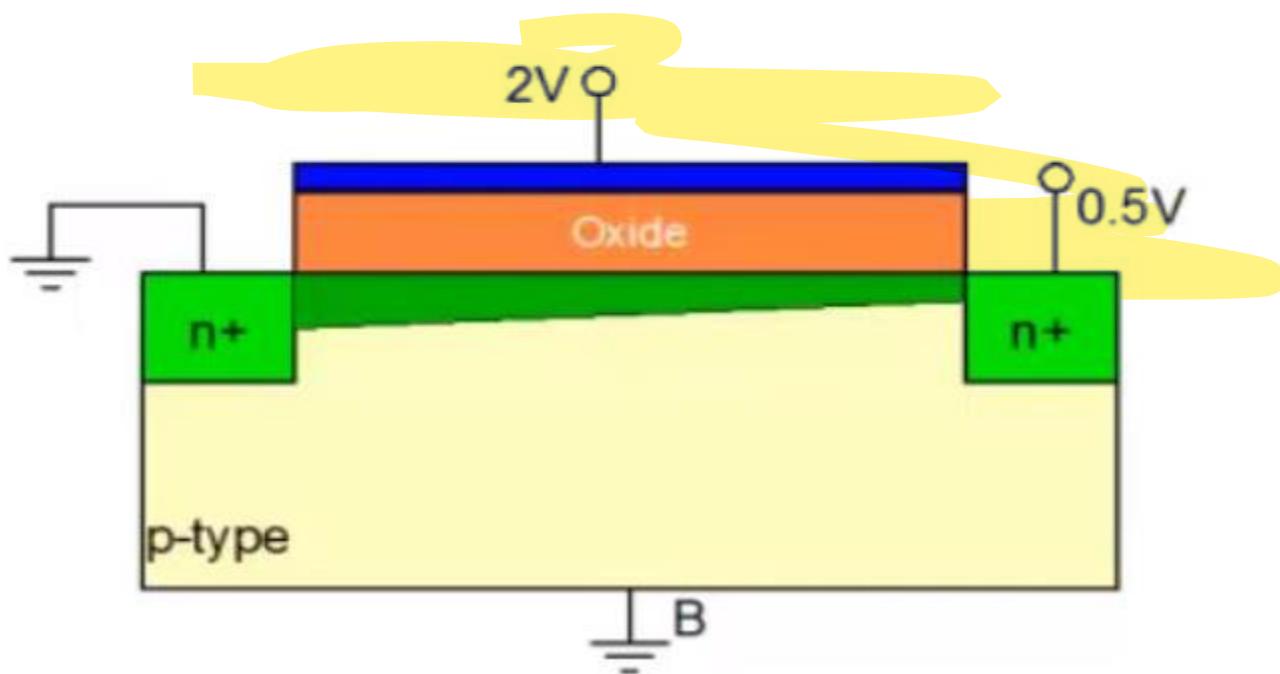
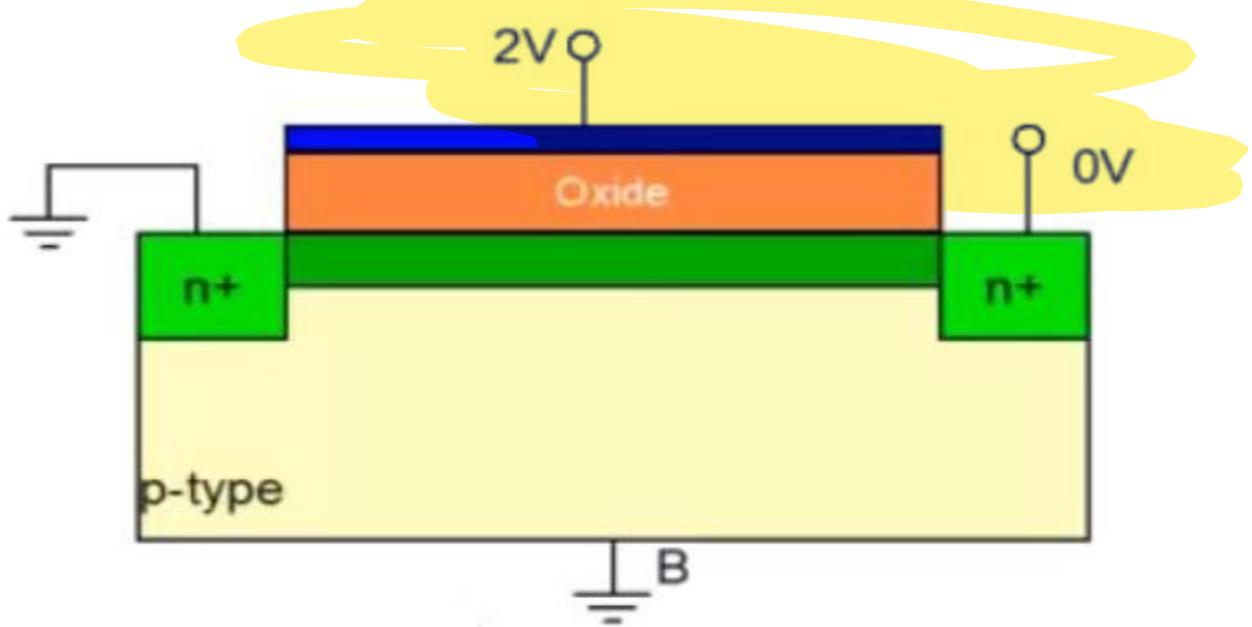
$$C'_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

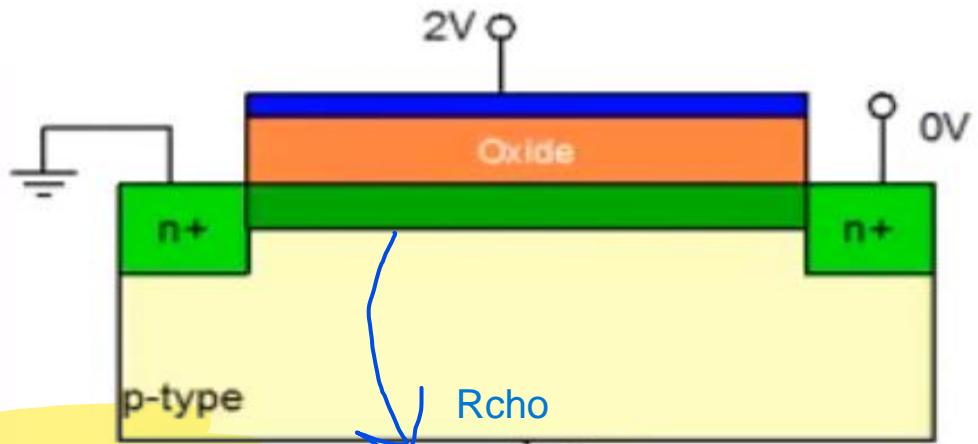
Inversion charge/area : $Q_{inv} = -C_{ox}(V_{GS} - V_{THN})$

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x))$$



When a positive drain voltage is applied, current flows from drain to source and inversion charge density decreases from source to drain end.





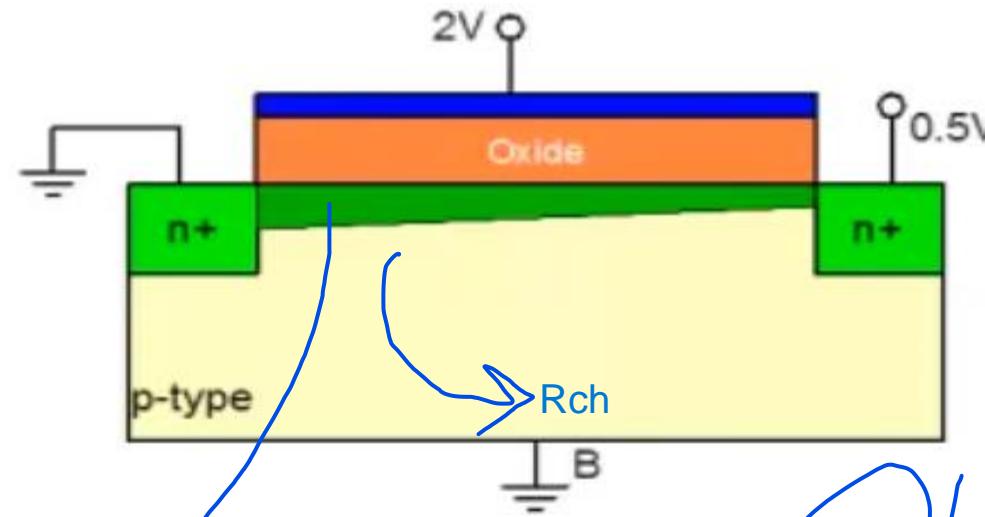
$$R = \rho \times l / A$$

$$dR_{ch} = \frac{1}{q\mu n(x)} \frac{dx}{W \times t}$$

$$R_{ch} \propto \frac{1}{\int Q_{inv} dx}$$

$$I_{DS} = \frac{V_{DS}}{R_{cho}} = 0$$

As drain voltage increases, channel resistance also increases causing drain current to depart from linear behavior



$$R_{ch} > R_{cho}$$

here as VDS increases, so does the Resistance, so do we end up with a linear behaviour? Not actually.

don't confuse the thickness with the thickness of the depletion layer.

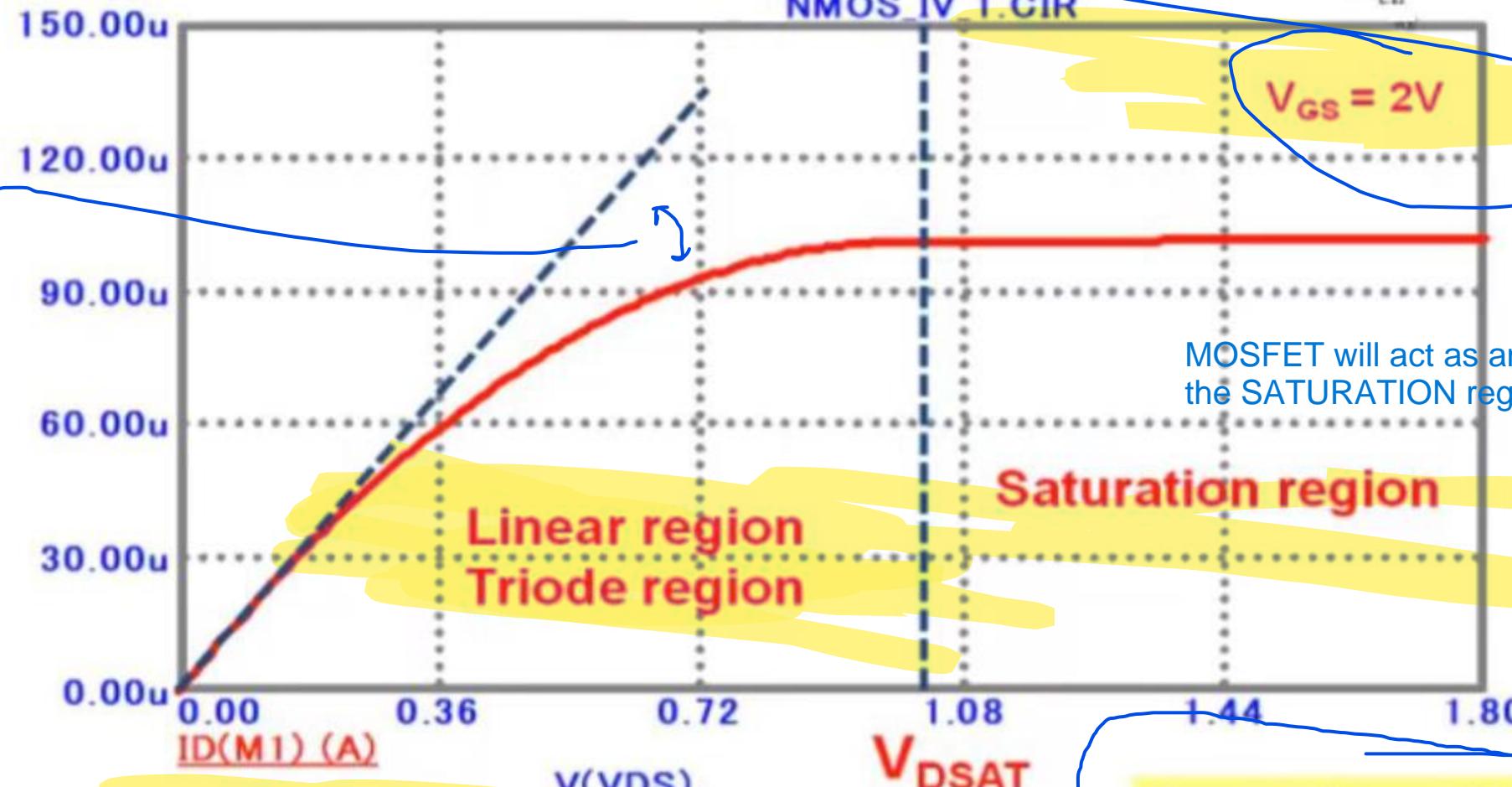
The thickness represents the density of the electrons and not the thickness of the depletion layer. the depletion layer is anyways very thin in practice, so you can consider it to be a sheet.

$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$

linear and triode is the same thing

$$I_{DS} = \frac{V_{DS}}{R_{ch}} > 0$$

departure from linear behavior



MOSFET will act as an amplifier in the SATURATION region.

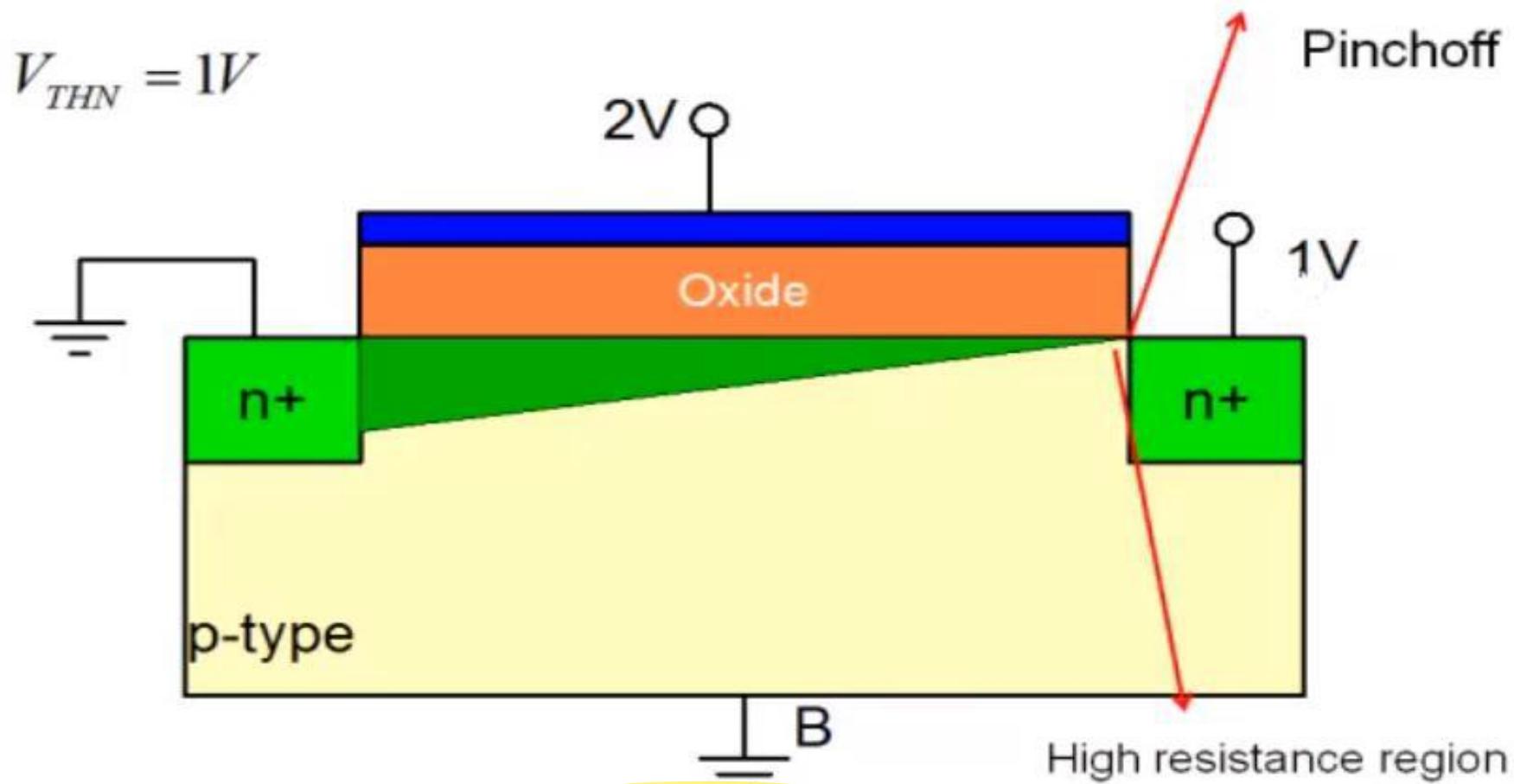
Saturation region

Linear region
Triode region

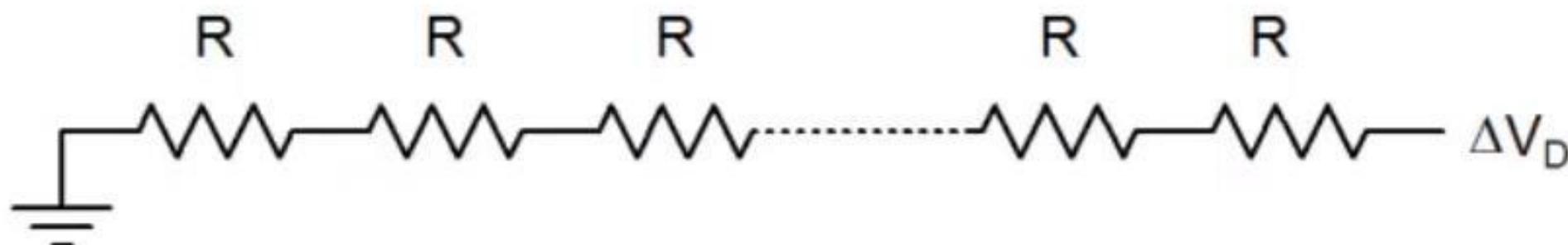
$$V_{DSAT} = V_{GS} - V_{THN}$$

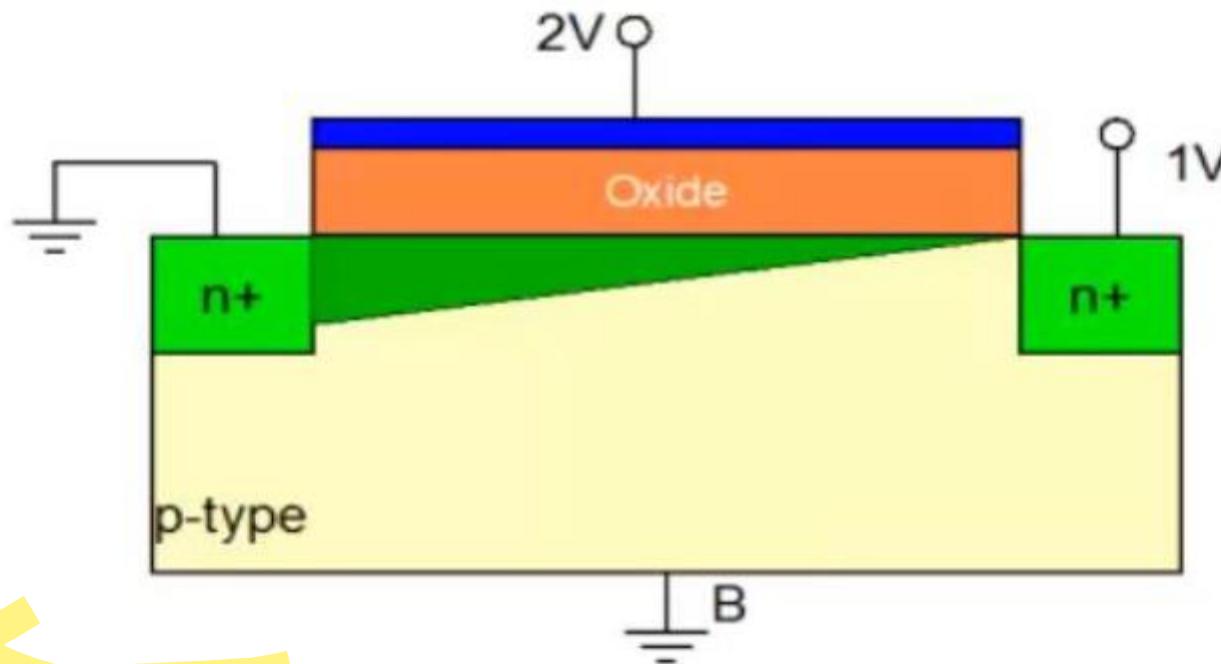
Note that **Saturation in MOSFET is analogous to forward active mode in BJT** and linear region is analogous to saturation in BJT.

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2 - 1 - 1) = 0$$



Any further increase in drain bias is absorbed in a small region next to the drain and rest of channel is not much affected and thus current becomes constant.



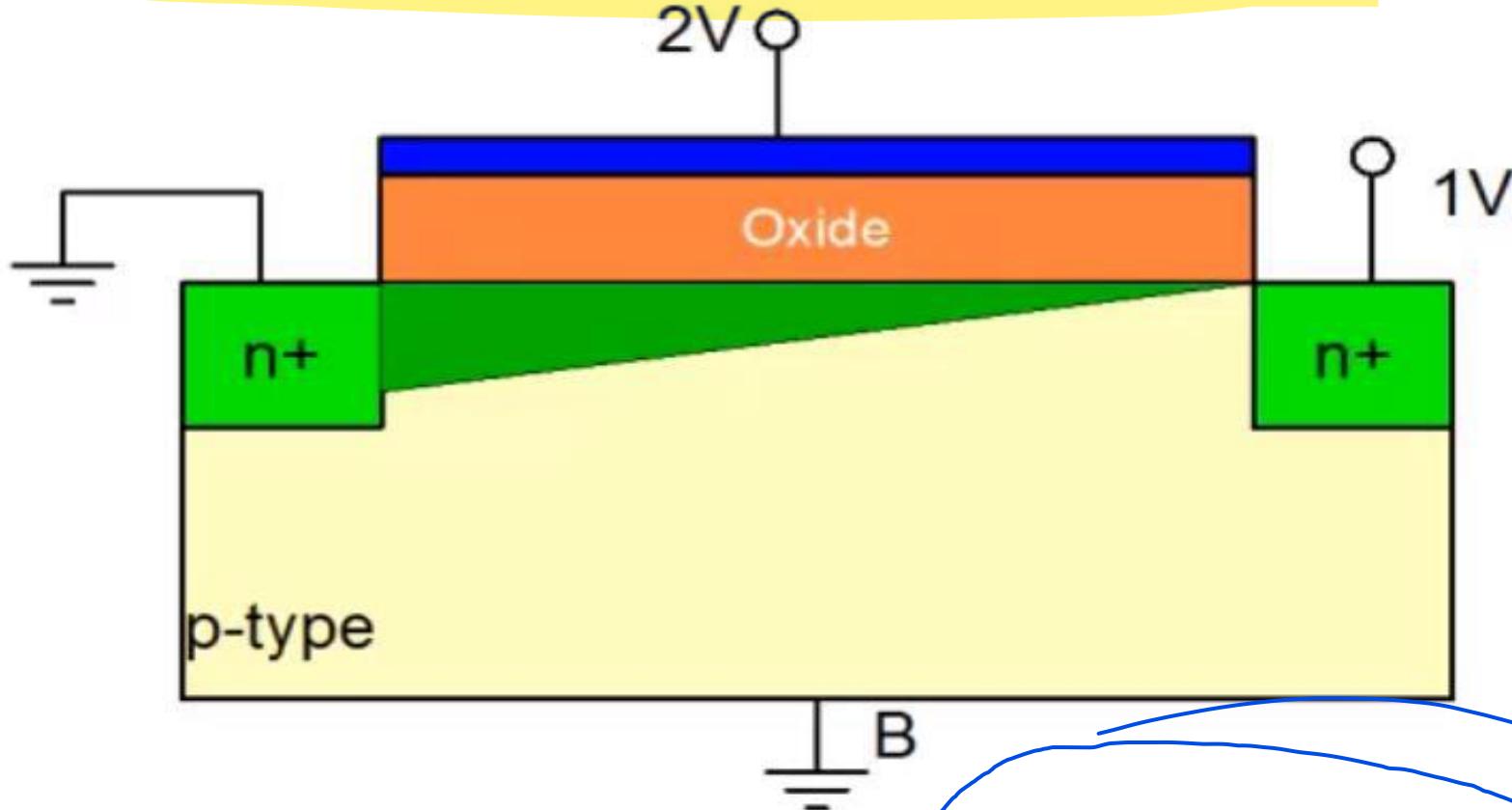


After pinchoff or saturation, drain current does not change much with drain voltage but is still very sensitive to gate voltage. MOSFET can now **AMPLIFY** signals



$$\frac{\partial I_{DS}}{\partial V_{GS}} \gg \frac{\partial I_{DS}}{\partial V_{DS}}$$

The voltage at which pinchoff occurs is the drain-saturation voltage V_{DSAT}
or we can say that the voltage at the pinchoff point is equal to V_{dsat}



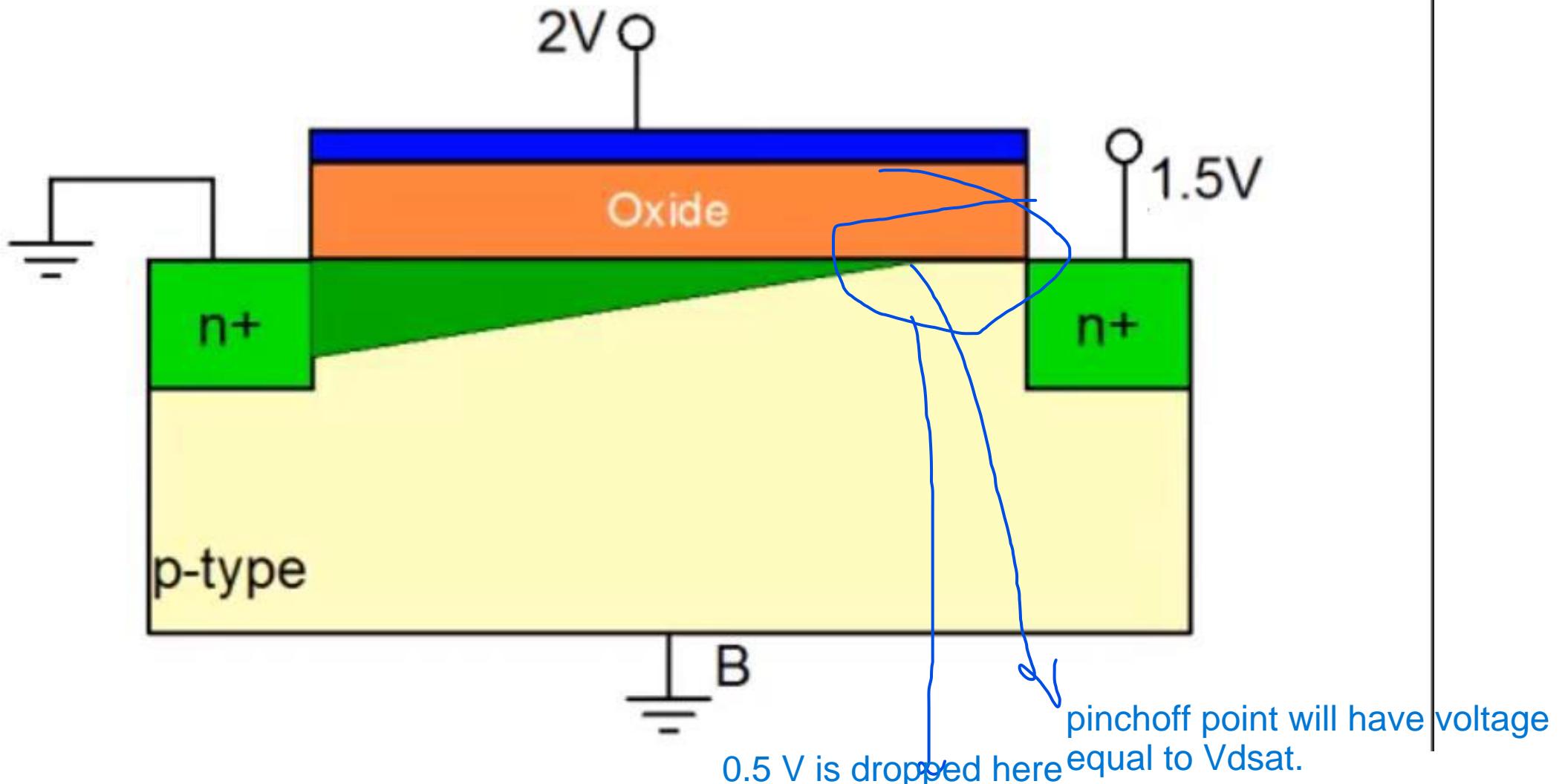
$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V_{DSAT}) \approx 0$$

$$V_{DSAT} = V_{GS} - V_{THN}$$

This is a very simple picture. In short channel MOSFETs especially, saturation is a more complicated phenomenon.,

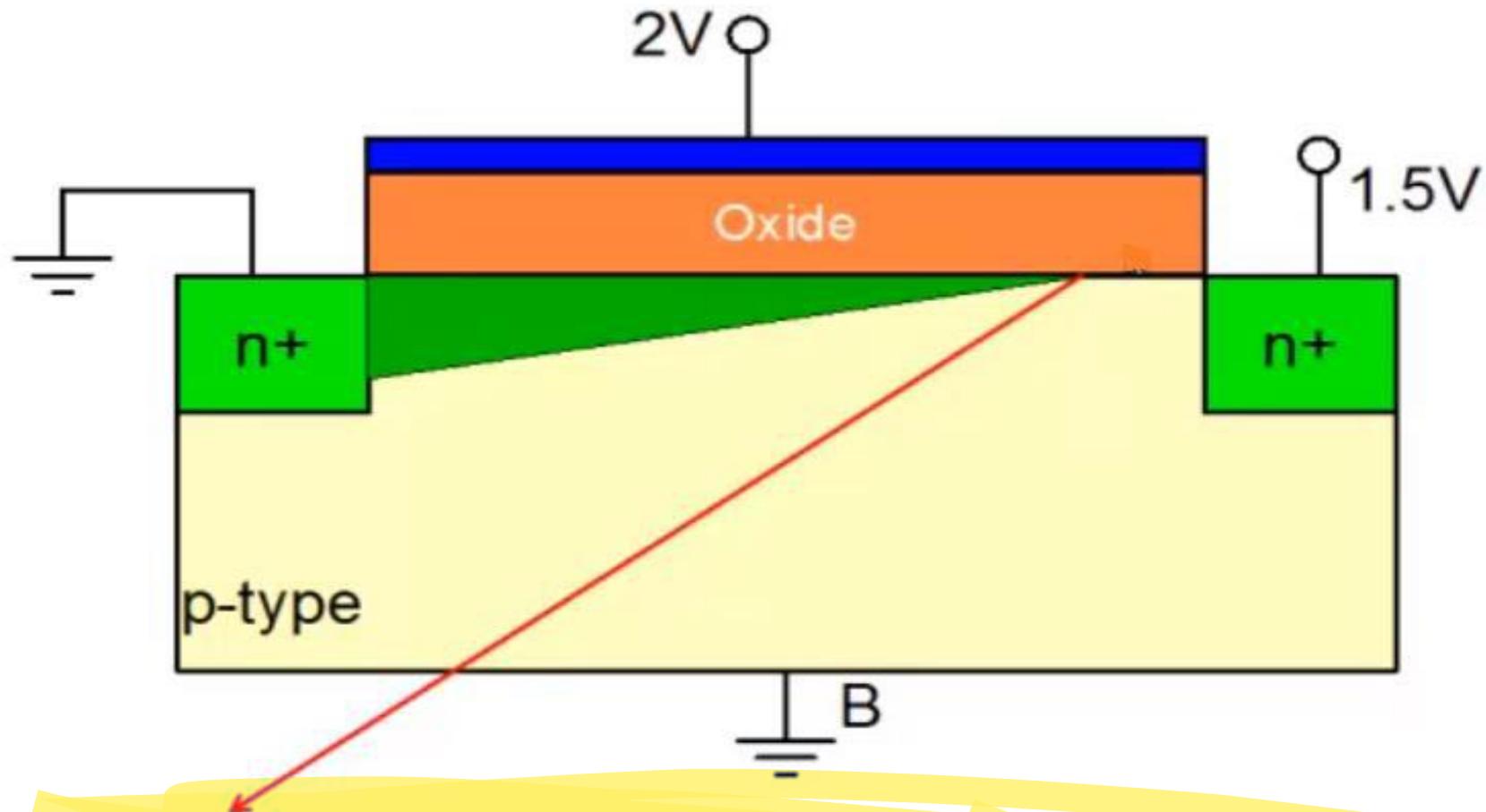
For voltages larger than saturation voltage

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2 - 1 - 1) = 0$$



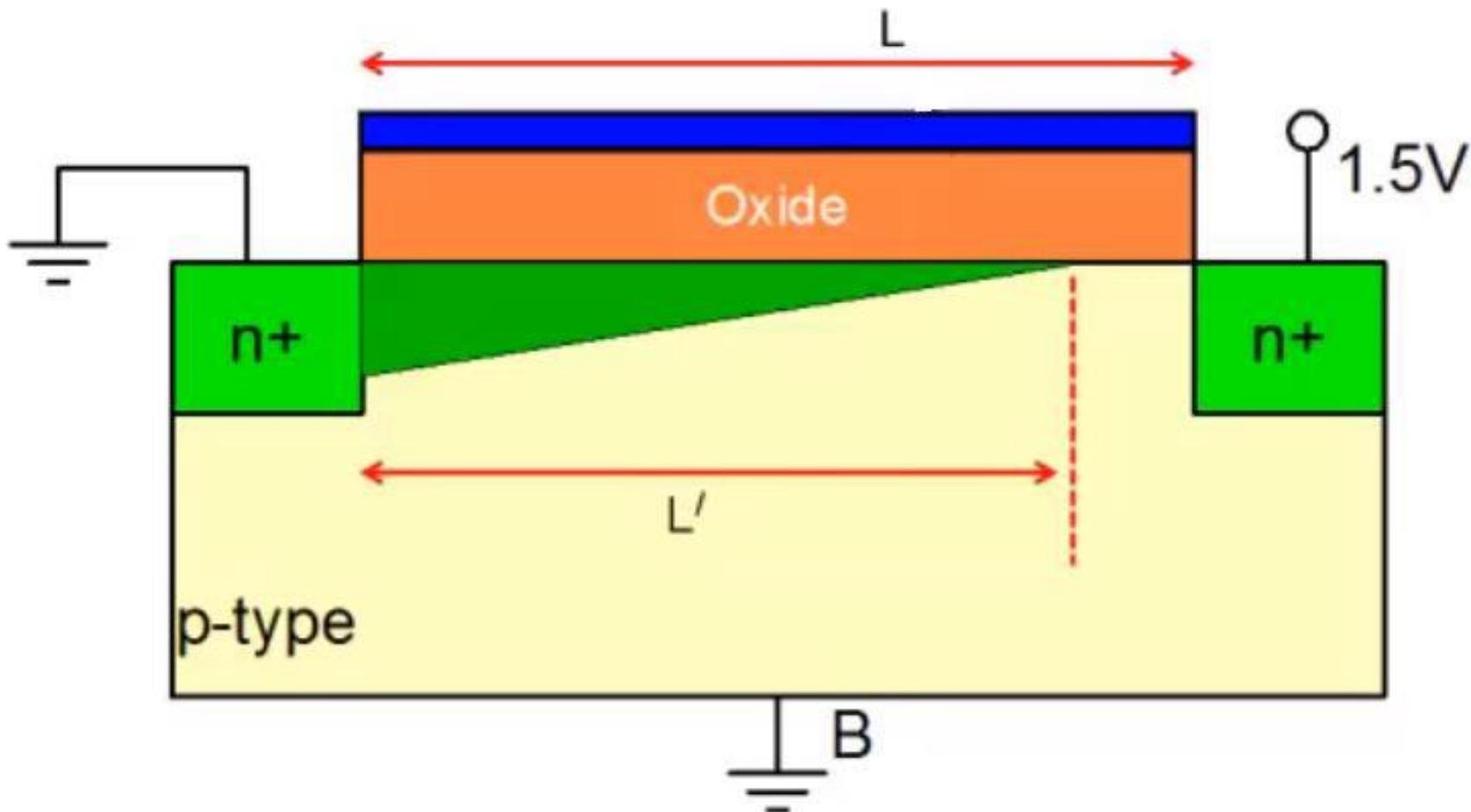
For voltages larger than saturation voltage

$$Q_{DN}(x) = -C_{ox}(V_{GS} - V_{THN} - V(x)) \cong -C_{ox}(2 - 1 - 1) = 0$$

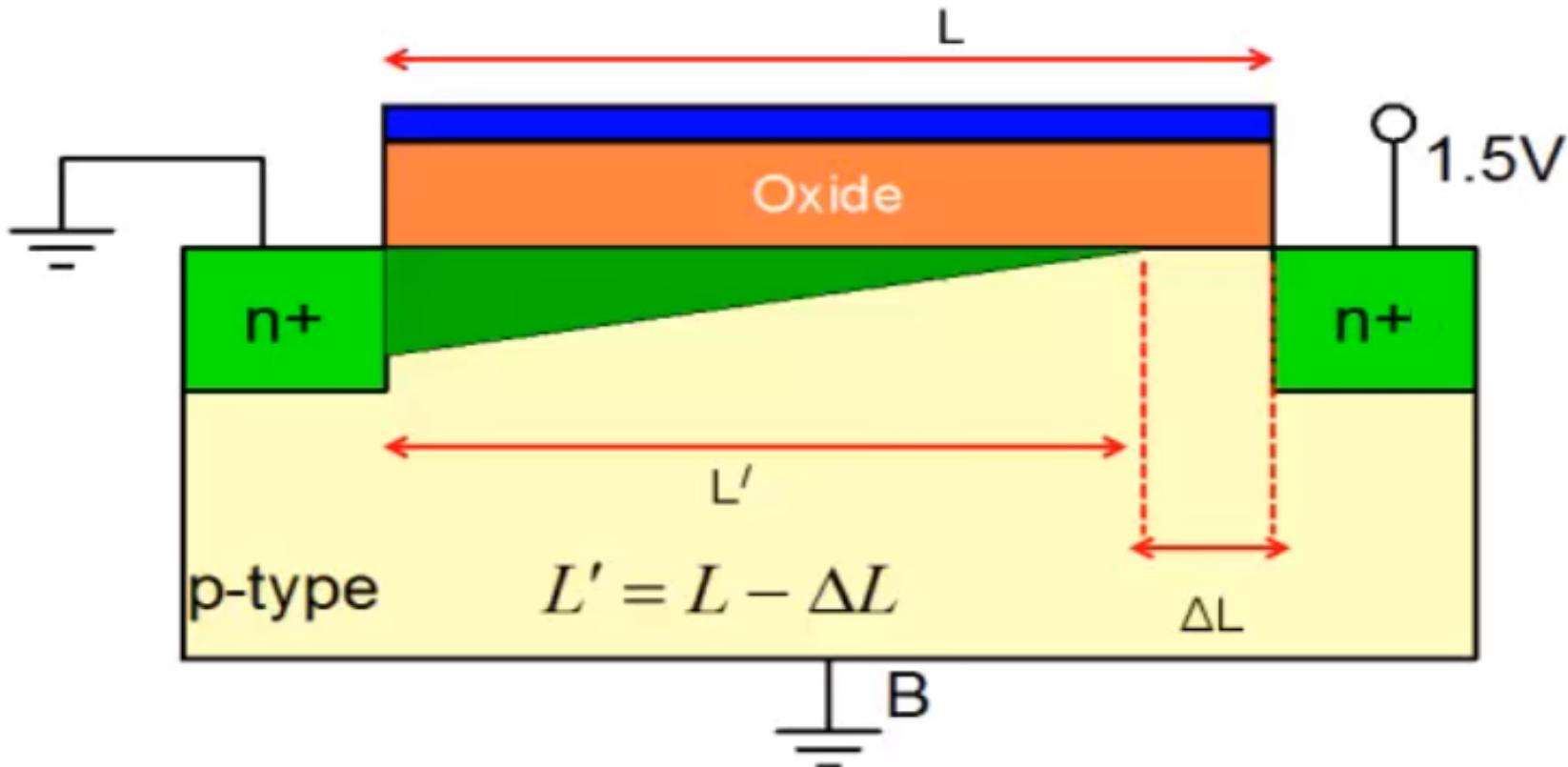


Pinchoff point moves left towards the source end. Voltage is $V_{DSAT} = 1V$

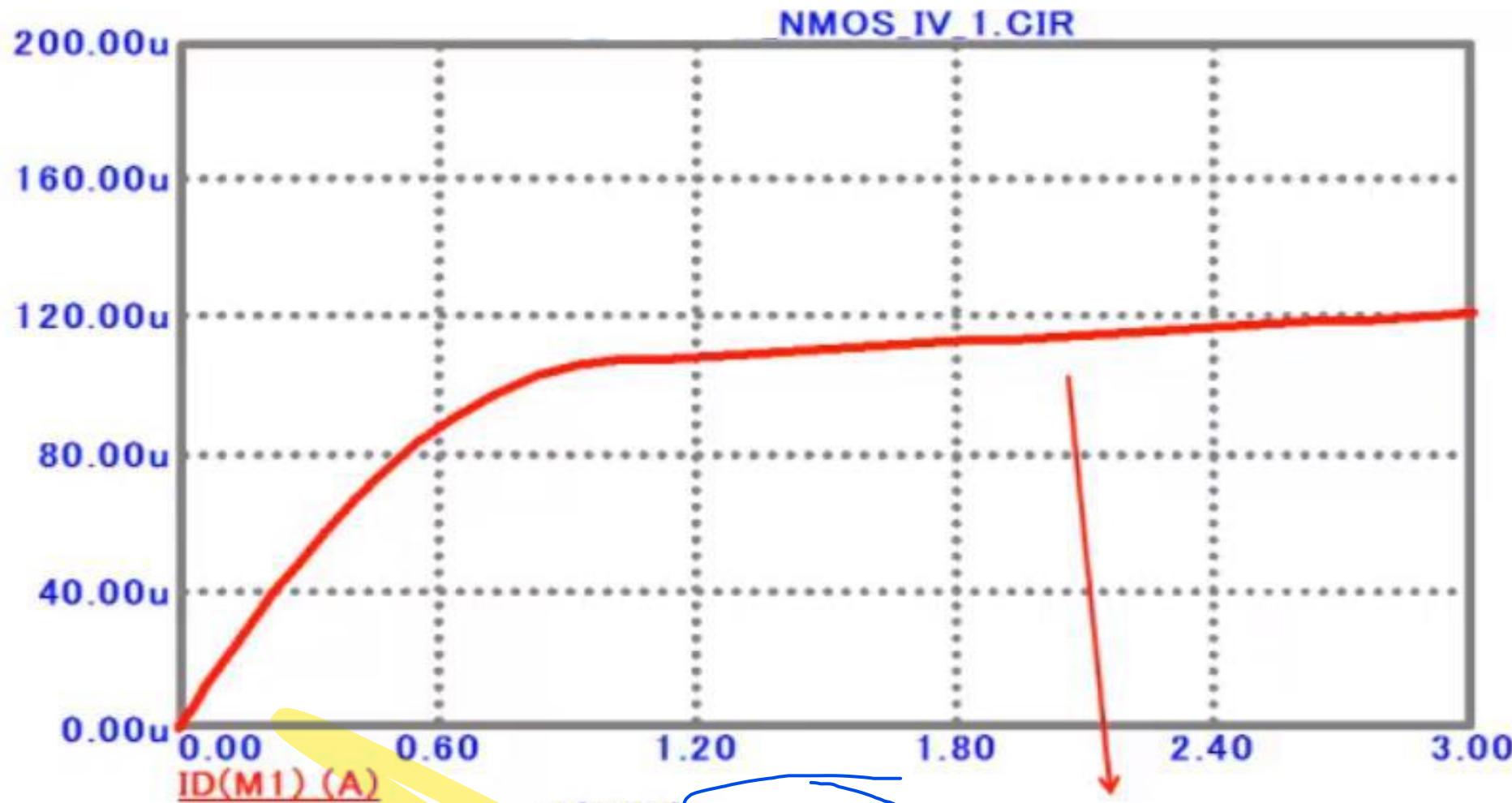
Channel Length Modulation



Channel Length Modulation



Effective channel length decreases as voltage increases beyond V_{DSAT} . As a result current increases a little with voltage



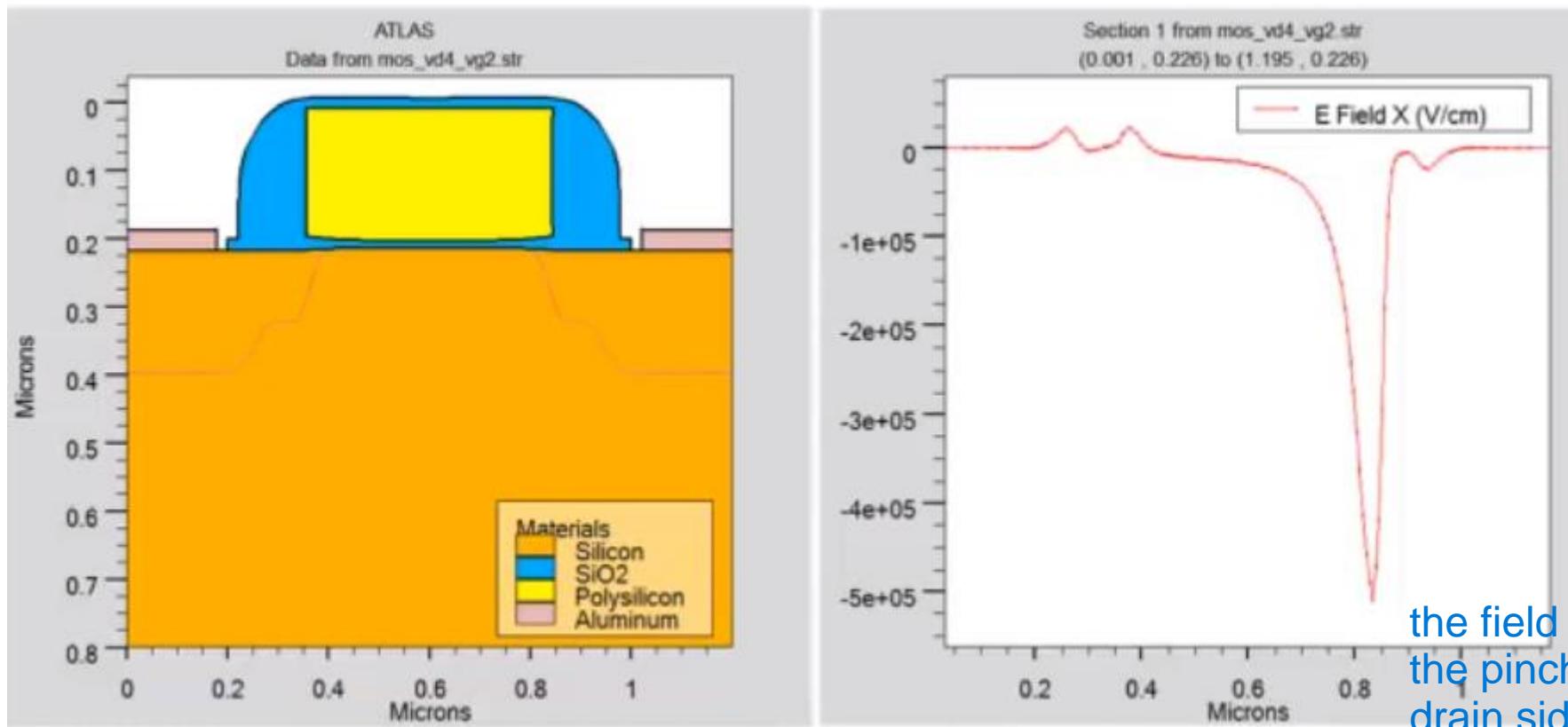
$I_D(M1)$ (A)

$V(V_{DS})$

$$I_{DSAT} \times (1 + \lambda \times V_{DS})$$

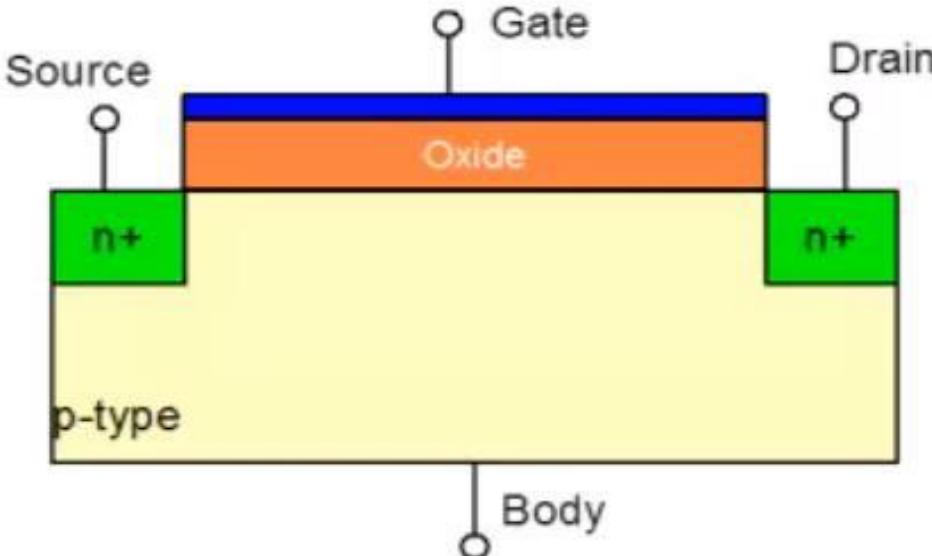
λ : channel length modulation parameter

current when
voltage is equal
to V_{DSAT}



the field is very high from the pinchoff point to the drain side.

Threshold Voltage



if $V_{SB} = 0$, V_{TH} is equal to V_{TH0}

$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \quad V_{THNO} = 1V$$

γ = body parameter Units : \sqrt{V}

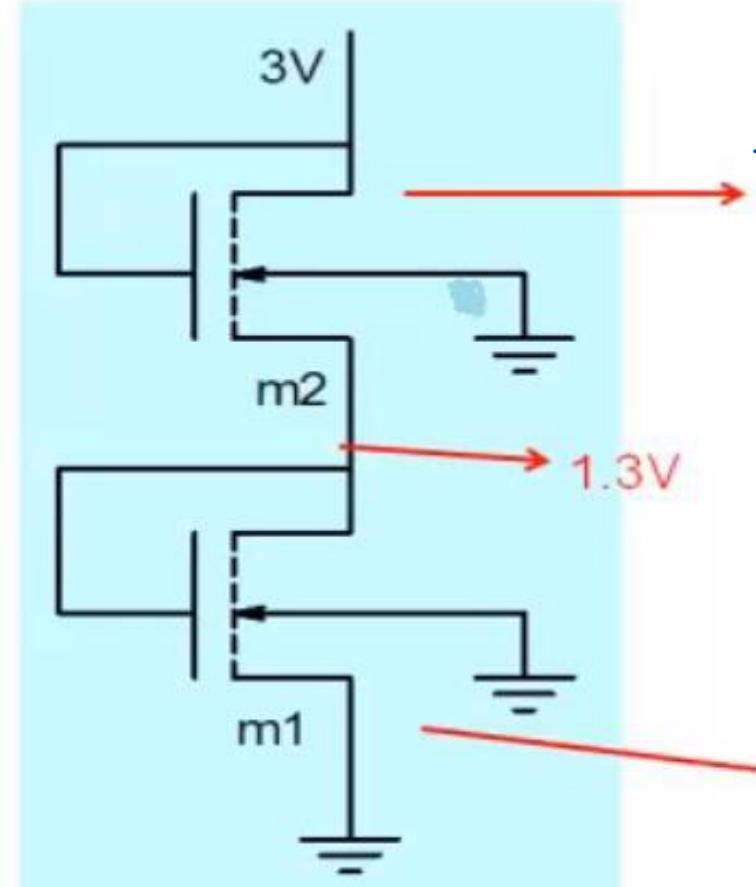
$$\gamma = 0.7 V^{1/2}$$

Surface potential : $2\phi_F$

$$2\phi_F = 0.7V$$

$$V_{THNO} = 1V; \gamma = 0.7 V^{1/2}; 2\phi_F = 0.7V$$

$$V_{THN} = V_{THN0} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$$



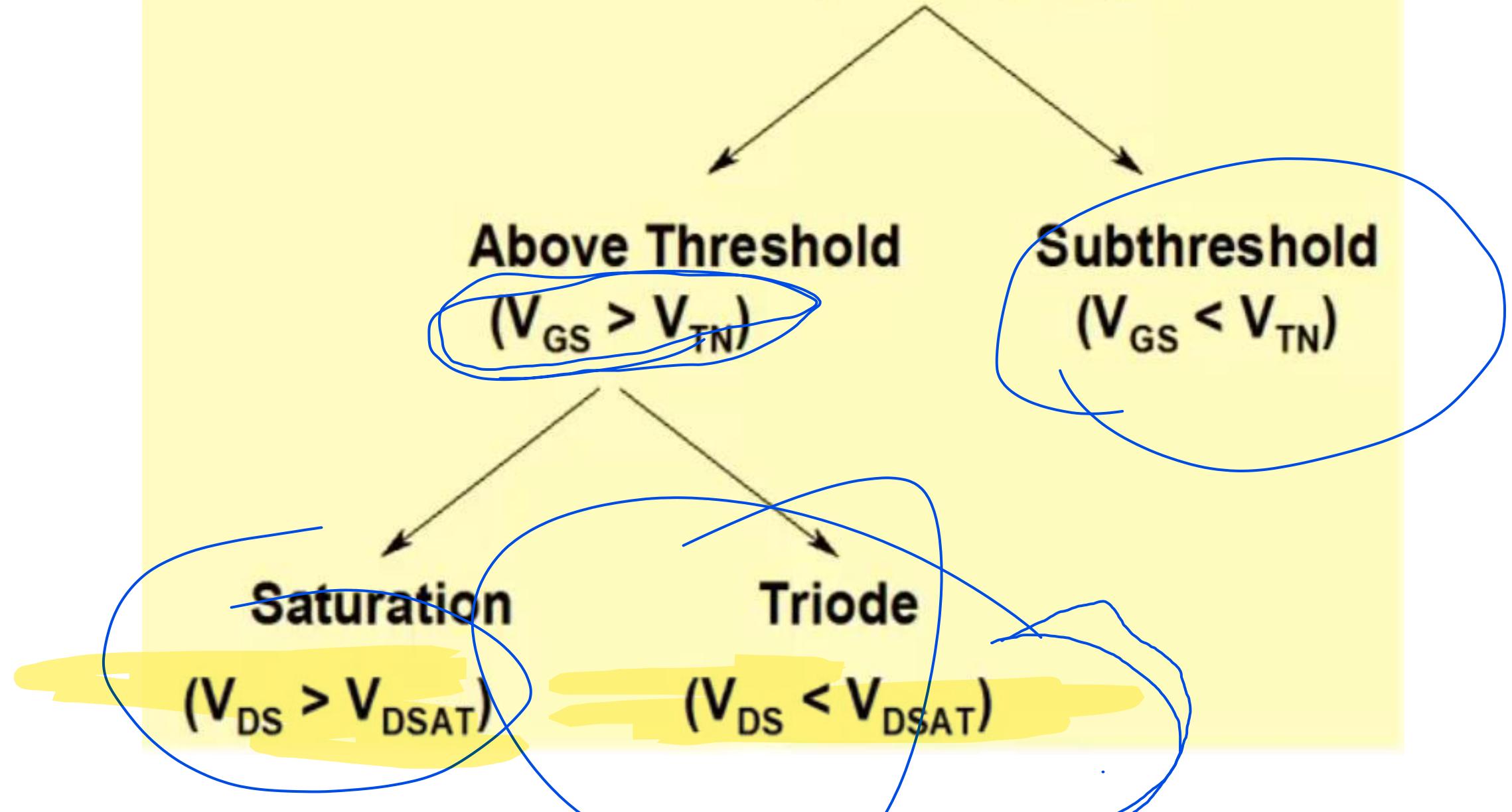
$$V_{SB2} = 1.3V; V_{THN2} = 1.4V$$

$$= 0.4V$$

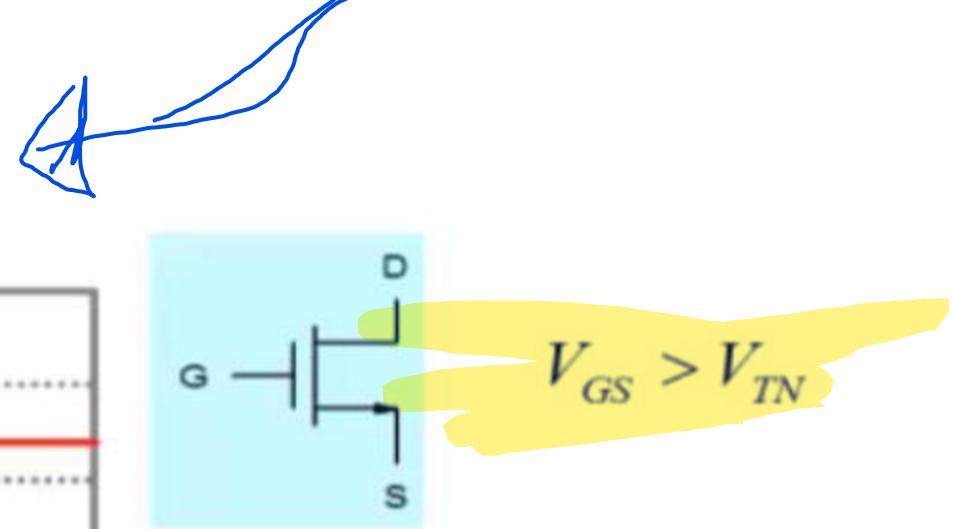
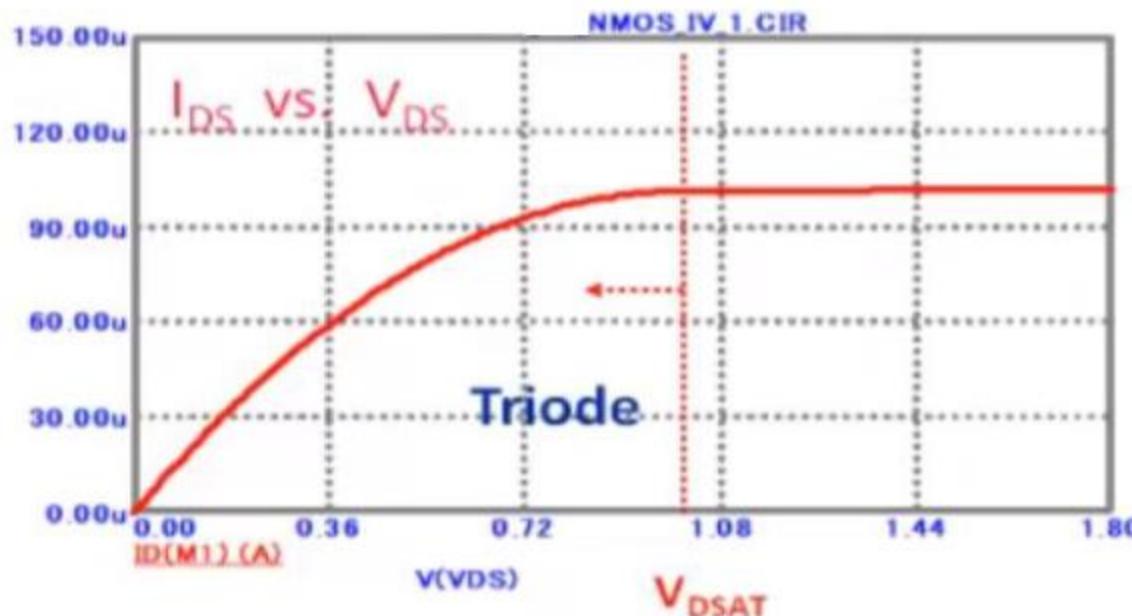
$$= 1 + 0.4V$$

$$V_{THN1} = V_{THN0} = 1V$$

MOS Operating Regions



dc Model: Triode (or Linear)



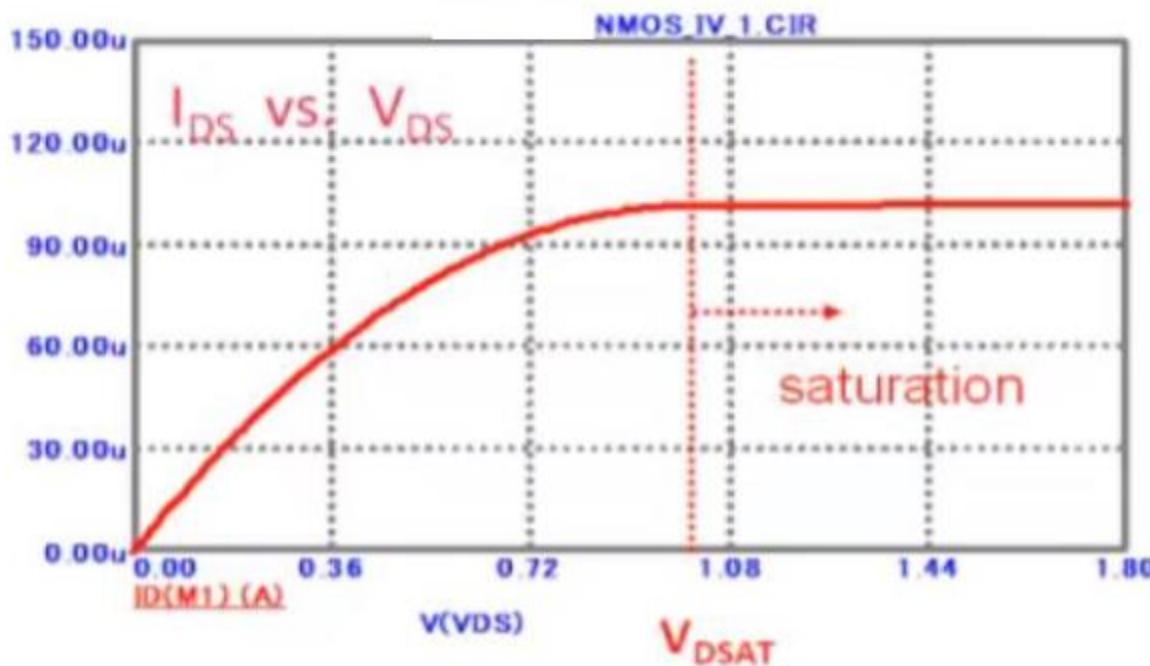
$$V_{DS} < V_{Dsat} = V_{GS} - V_{TN}$$

$$I_{DS} = \beta_N \left\{ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

$$\beta_N = kP_N \cdot \frac{W}{L}$$

$$kP_N = \mu_n C_{ox'} : \text{(TransConductance parameter } \frac{\mu A}{V^2} \text{)}$$

DC Model: Saturation Region



$$V_{GS} > V_{THN}$$

$$V_{DS} \geq V_{GS} - V_{THN}$$

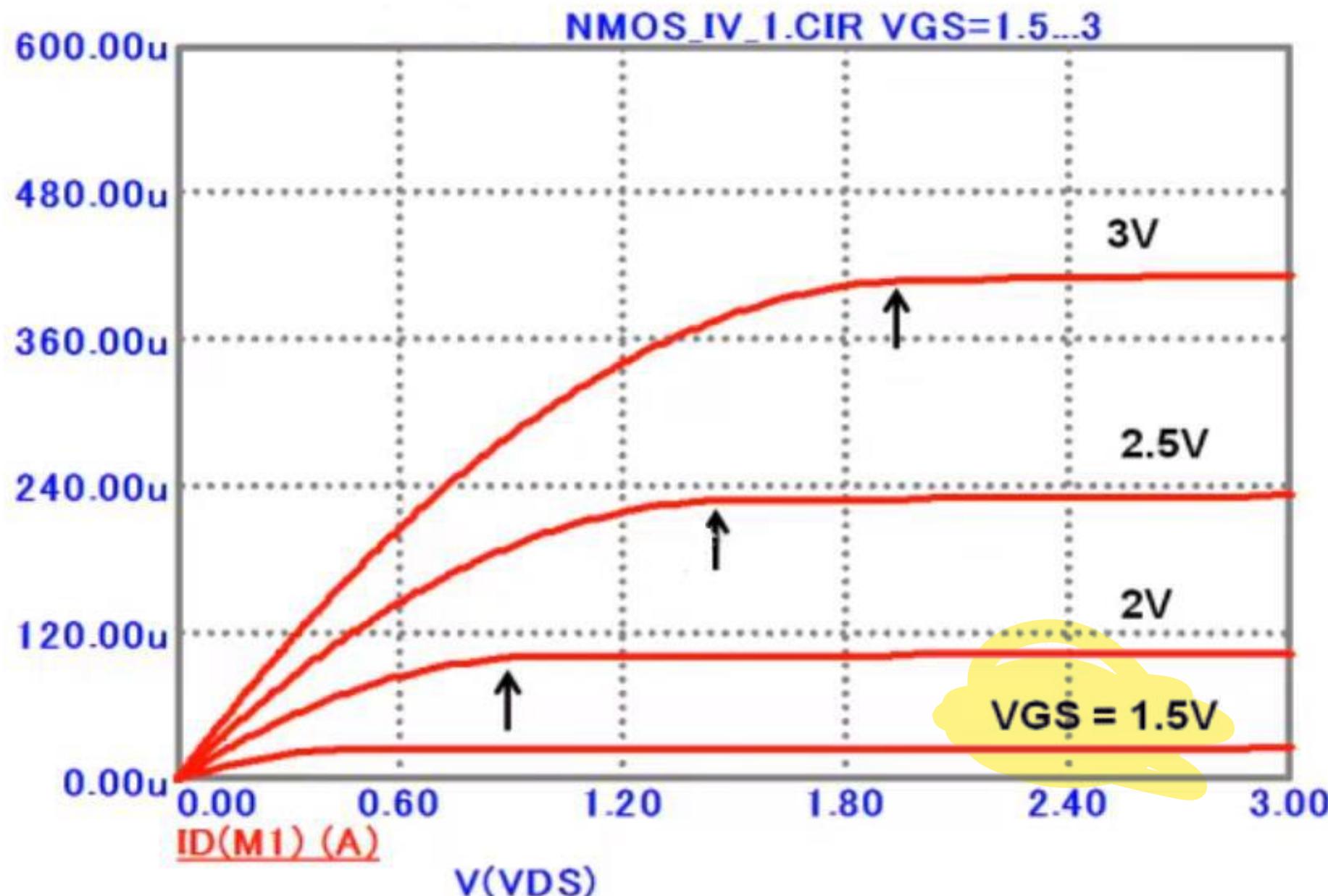
i.e. $V_{GS} - V_{THN} - V_{DS} \leq 0$ checks out for saturation region

$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}]$$

λ_n is the channel length modulation parameter

Note that unlike BJT, V_{DSAT} is not only larger but also dependent on applied gate-source voltage

Output Characteristics of MOSFET



dc model parameters

$$P_N = \mu_N C_{ox} W$$

Linear : $I_{DS} = \beta_N \left\{ (V_{GS} - V_{THN}) V_{DS} - \frac{V_{DS}^2}{2} \right\}$

$$\beta_N = k P_N \cdot \frac{W}{L}$$

Saturation : $I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}]$

$$\lambda_n$$

channel length modulation

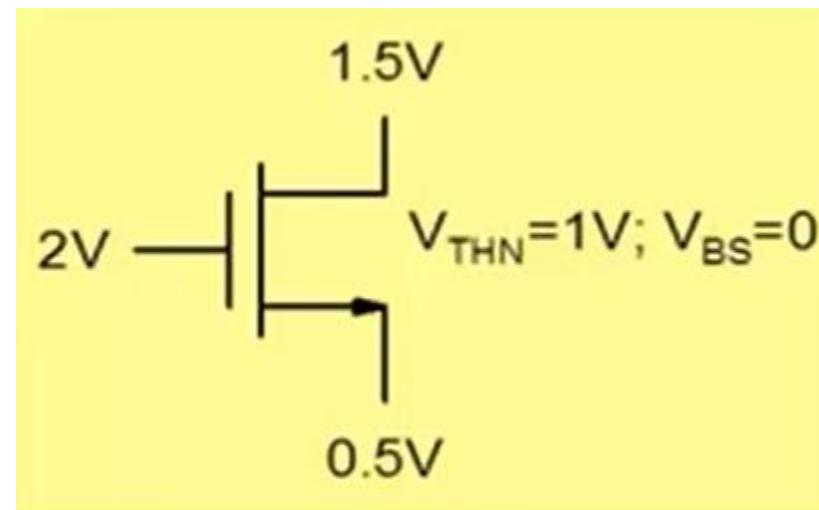
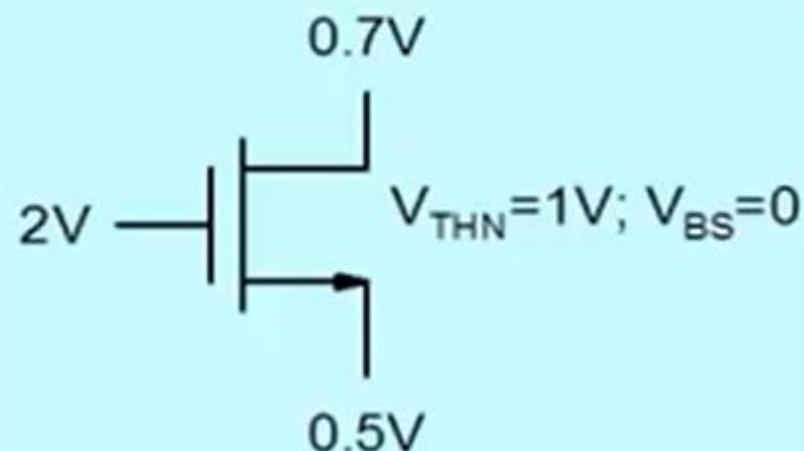
$$V_{THN} = V_{THN0} + \gamma (\sqrt{2\phi_F} + V_{SB} - \sqrt{2\phi_F})$$

$$V_{THNO} = 1V; \gamma = 0.7 V^{1/2}; 2\phi_F = 0.7V;$$

$$K P_N = 100 \mu A / V^2; L = 1 \mu m; \lambda = 0.01 V^{-1}$$

L is usually fixed, W is determined by designer

Which mode is the transistor operating in ?



$$V_{GS} = 1.5 ; V_{DS} = 0.2$$

$$V_{DSAT} = V_{GS} - V_{THN} = 0.5$$

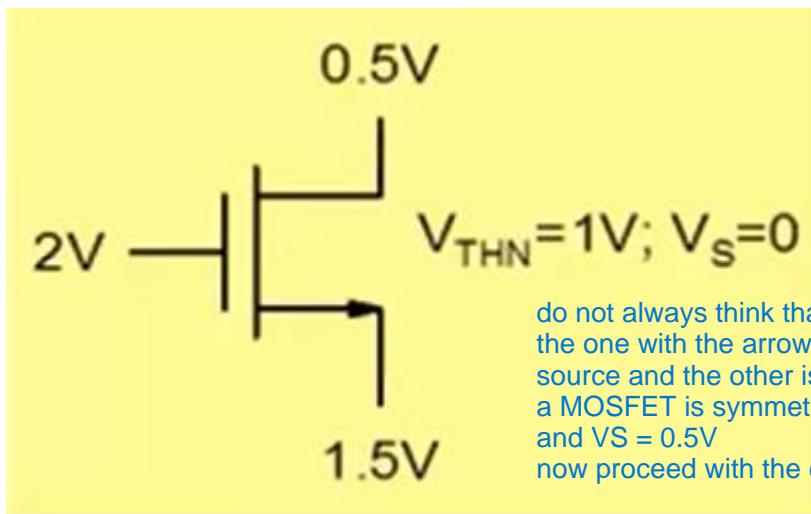
$V_{DS} < V_{DSAT} \Rightarrow Linear$

$$V_{DSAT} = 0.5 ; V_{DS} = 1V$$

$V_{DS} > V_{DSAT}$

Saturation

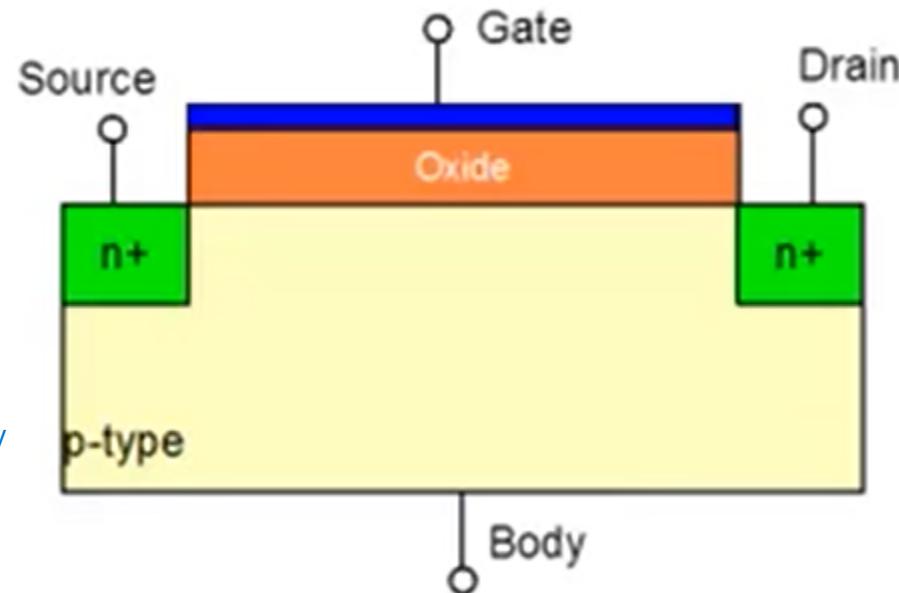
Which mode is the transistor operating in ?



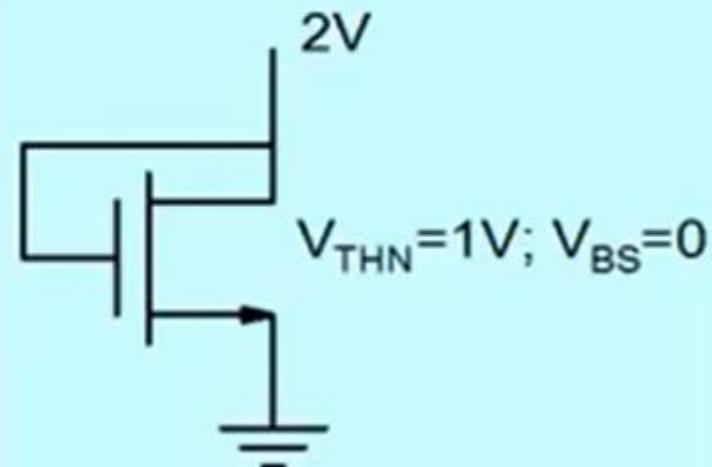
$$V_{GS} = 0.5; V_{DS} = -1V$$

$$V_{DSAT} = V_{GS} - V_{THN} = 0.5$$

$V_{DS} > V_{DSAT} \Rightarrow saturation$



$$V_{GS} = 1.5; V_{DS} = 1V$$



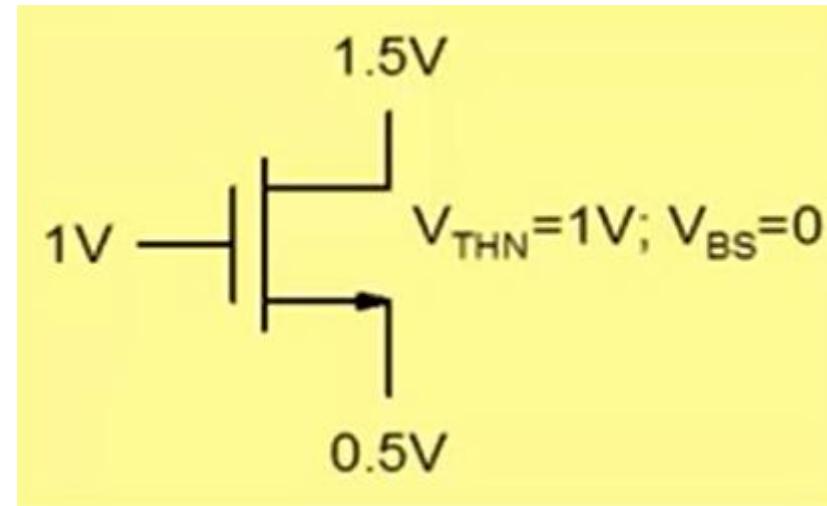
$$V_{GS} = 2 ; V_{DS} = 2$$

Saturation

$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}]$$

$$I_X \cong \frac{\beta_N}{2} (V_X - V_{THN})^2$$

Diode with a turn-on voltage of V_{THN}



$$V_{GS} = 0.5V < V_{THN}$$

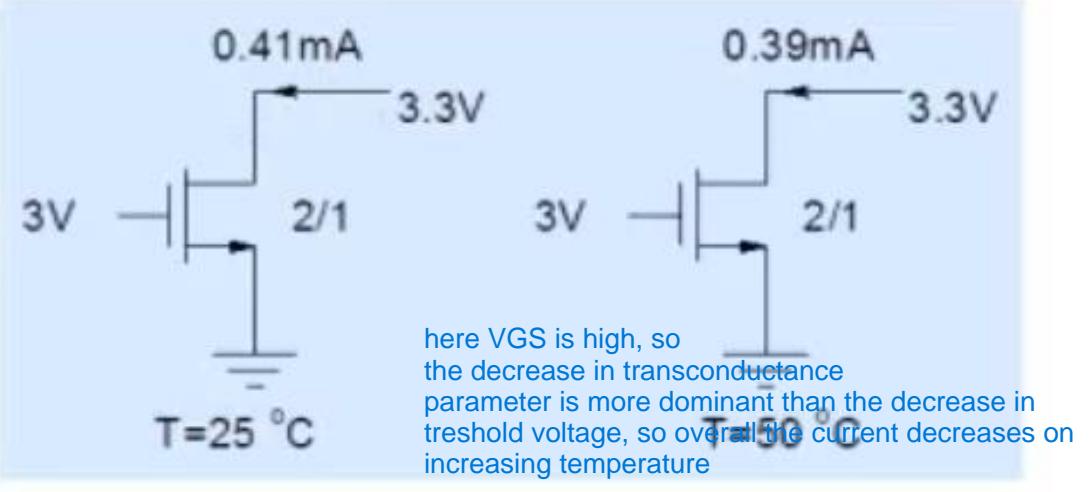
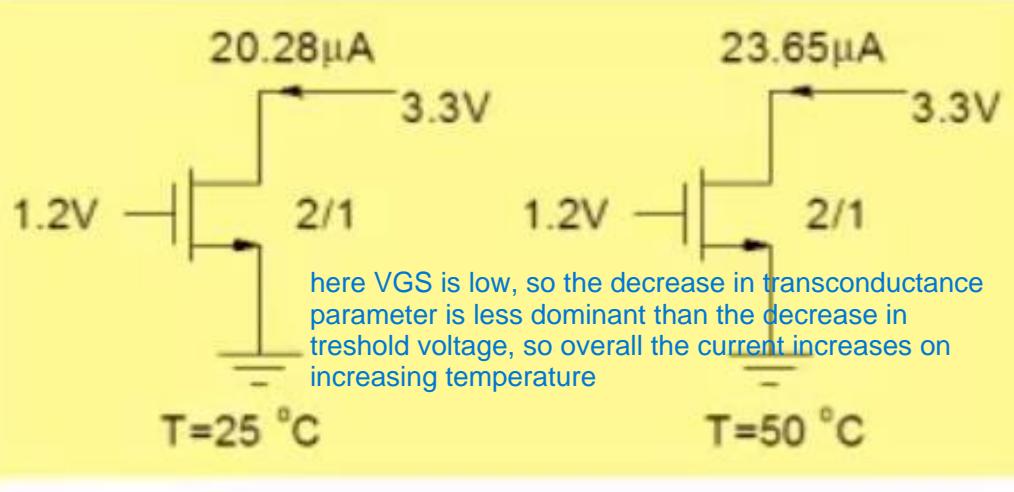
Transistor is in sub-threshold mode of operation

Temperature dependence

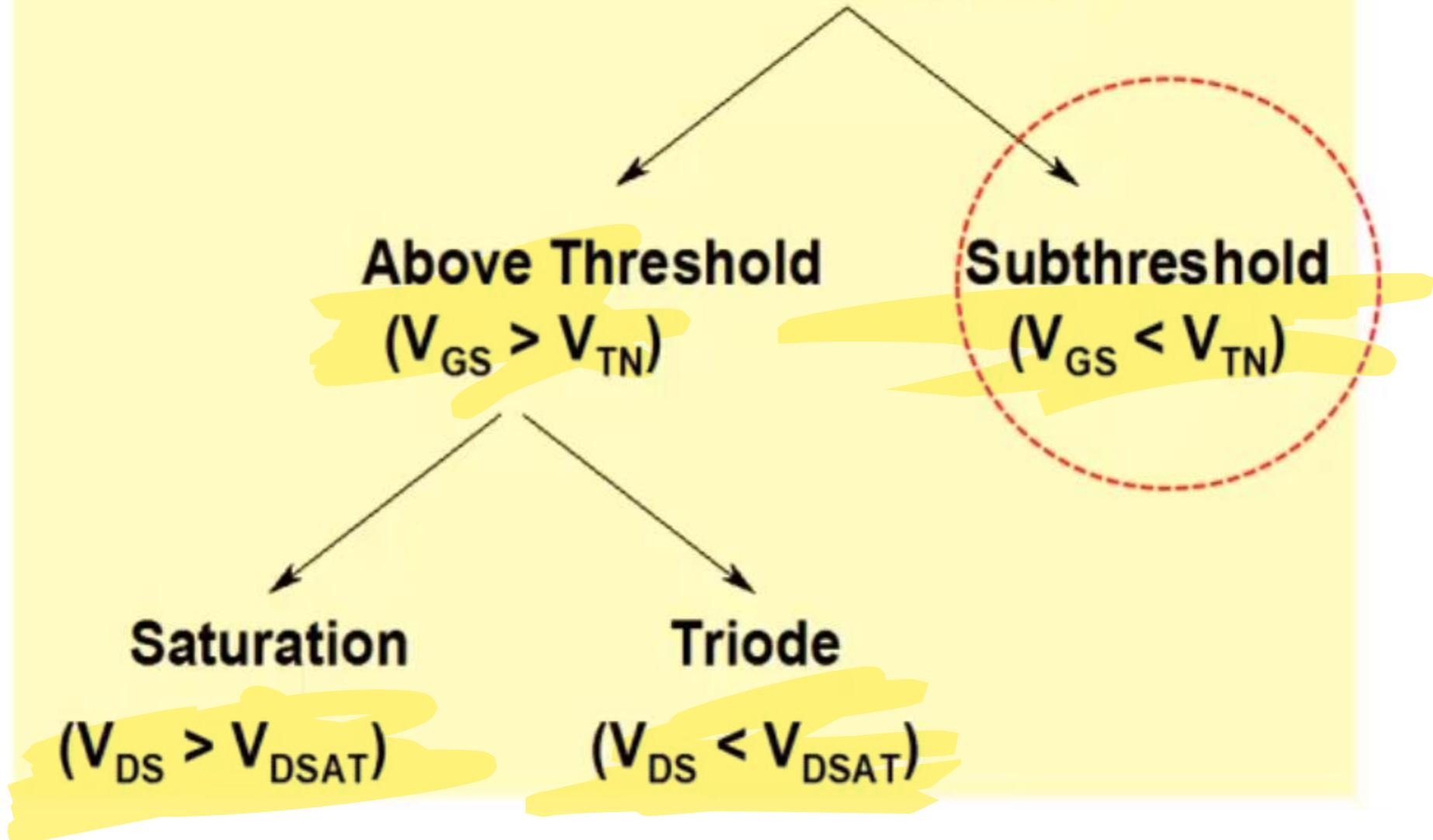
$$I_{DS} = \frac{KP_N}{2} \times \frac{W}{L} \times (V_{GS} - V_{THN})^2$$

Increase in temperature causes both transconductance parameter KP_N and threshold voltage V_{THN} to decrease

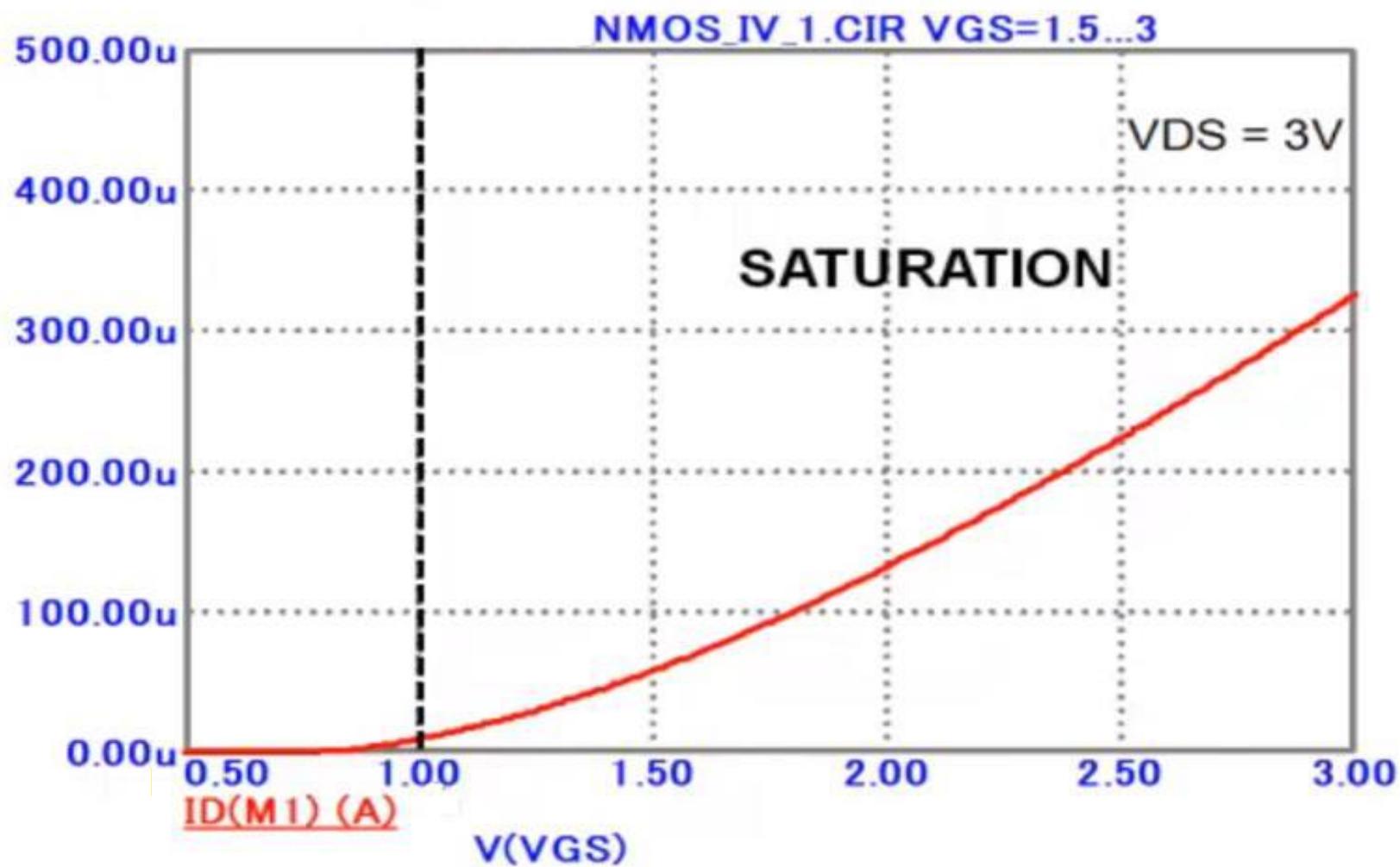
Although both KP_N and V_{THN} decrease with temperature, the former causes a decrease in current while the latter causes an increase in current.



MOS Operating Regions



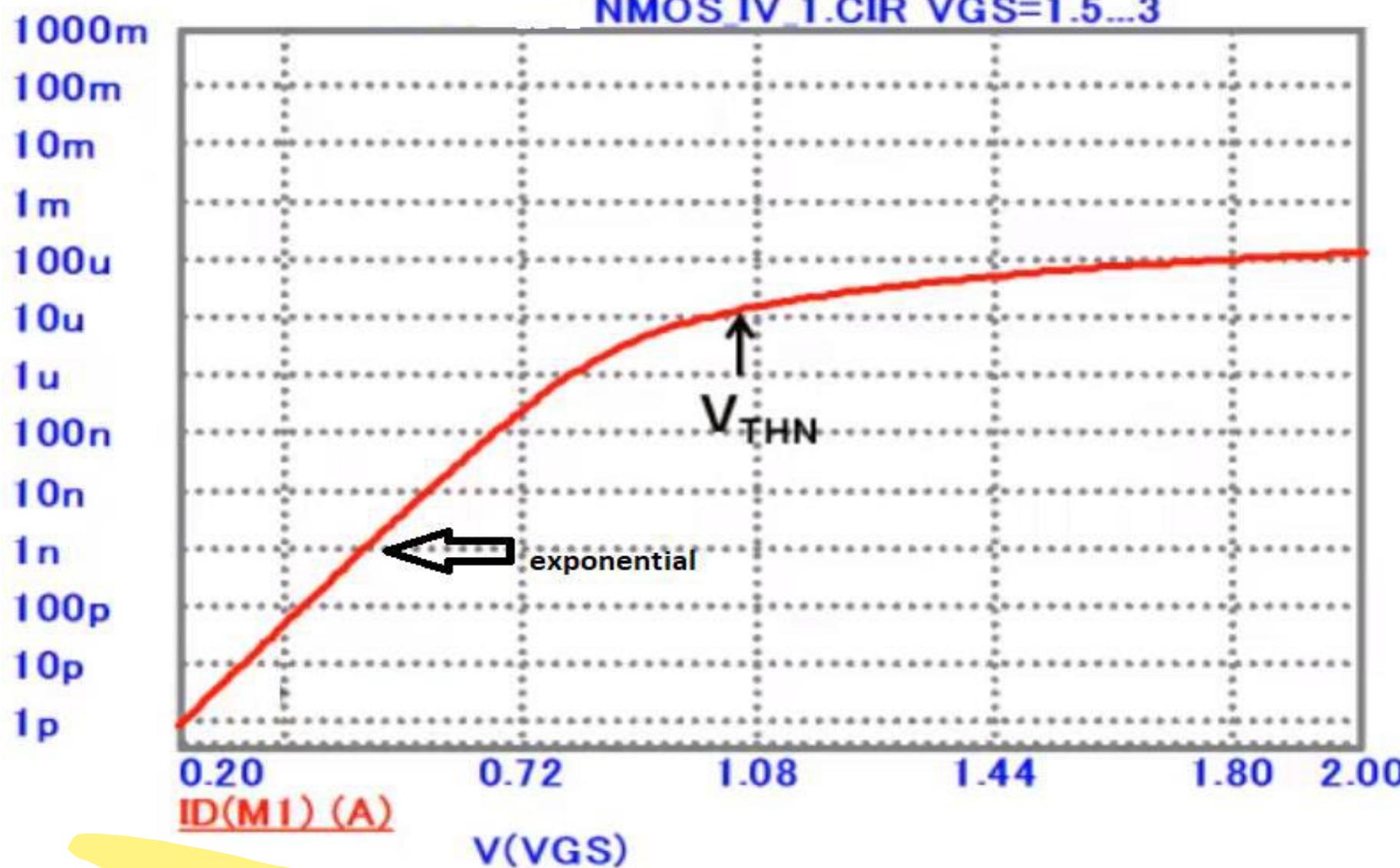
Transfer characteristics of NMOS



Current is very small until gate-source voltage exceeds threshold voltage
 V_{THN}

current vs V_{GS}

NMOS_IV_1.CIR VGS=1.5...3



-Logscale
-Ignoring leakages

$$I_D \propto e^{\frac{qV_{GS}}{N'kT}}$$

current varies exponentially with V_{GS}

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{I_{DS}}{nV_T}$$

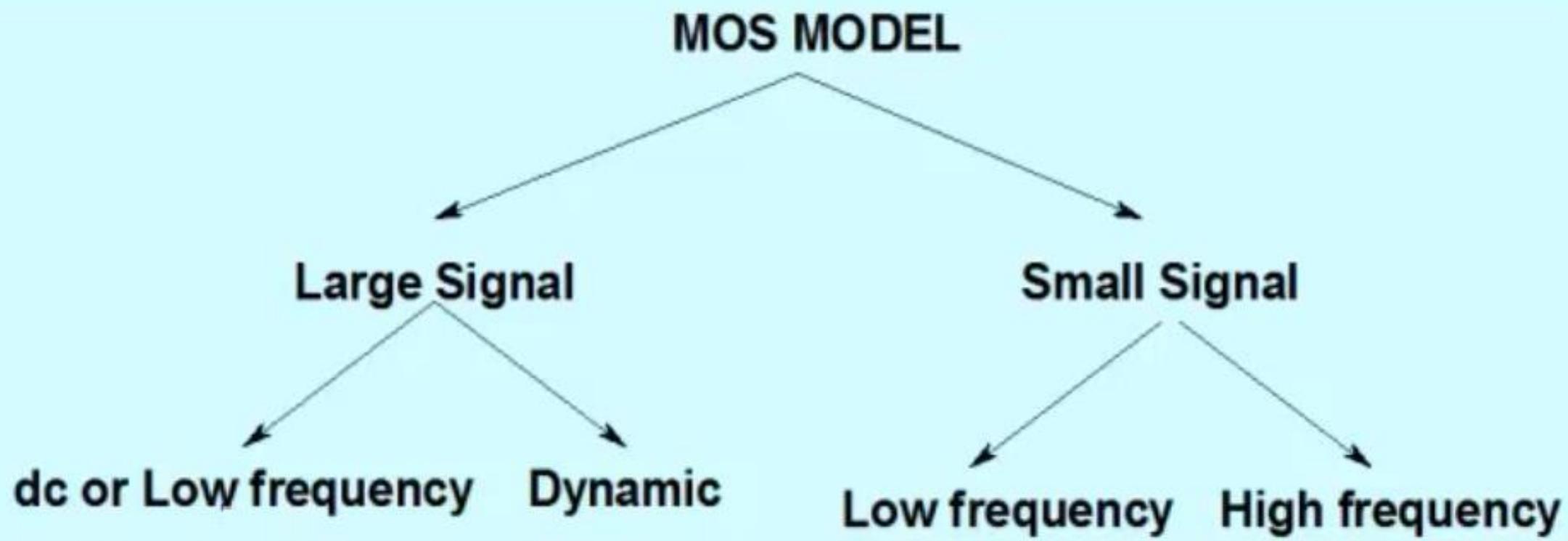
- In subthreshold region, MOS acts like a BJT

$$BJT: \quad I_{C_{\Delta}} = I_S e^{V_{BE}/V_T}$$

$$MOS: \quad I_{DS} = I_S e^{V_{GS}/\eta V_T}$$

- The advantage of MOS is that it offers almost infinite input impedance. Its disadvantage is that current levels are low.

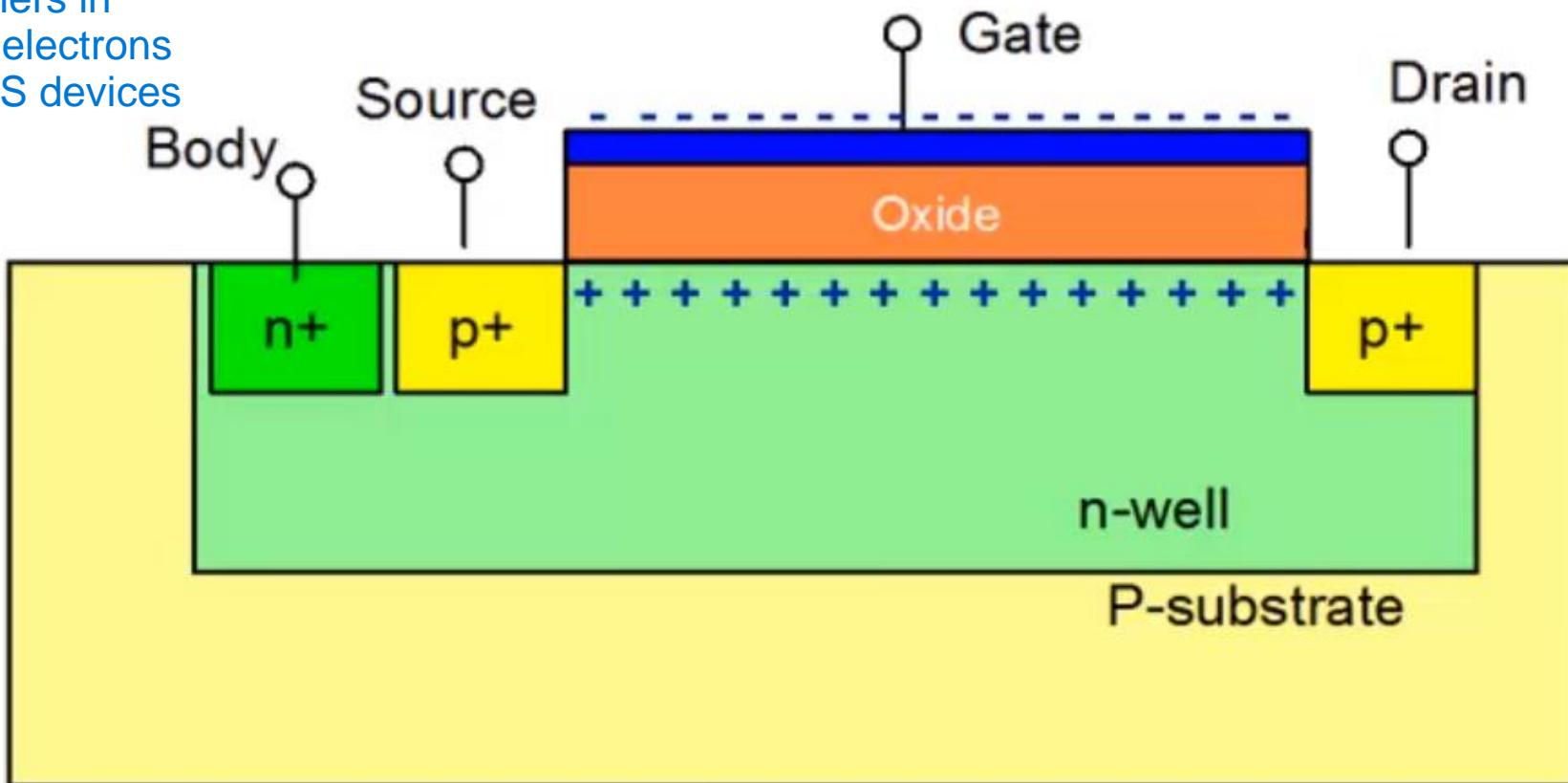
MOS models : The classification of models can be done on the basis of magnitude and frequency of applied voltages



PMOS

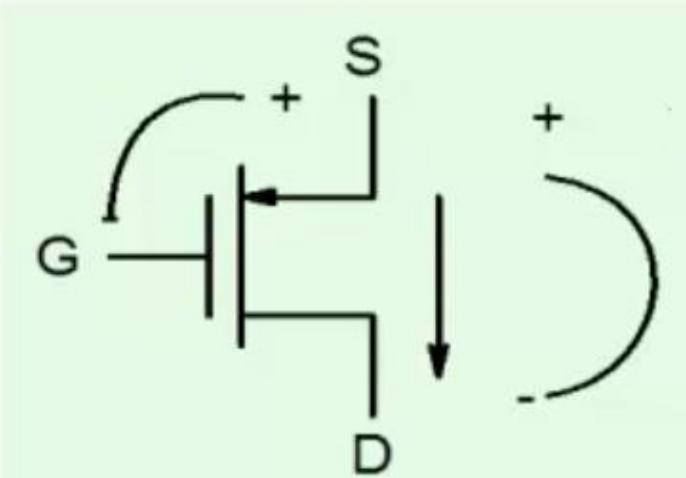
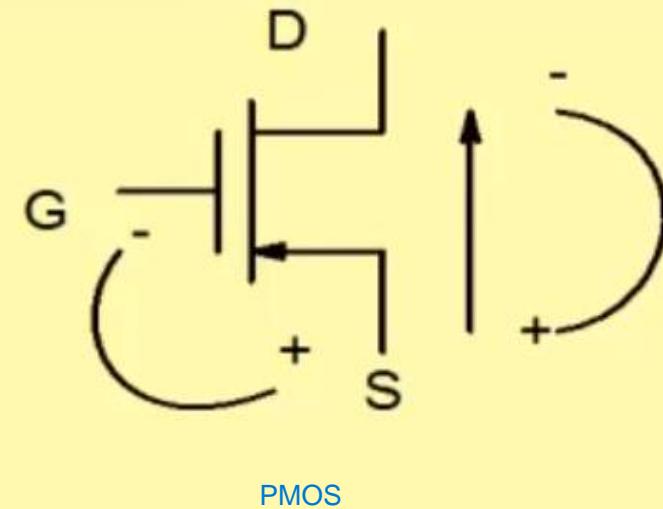
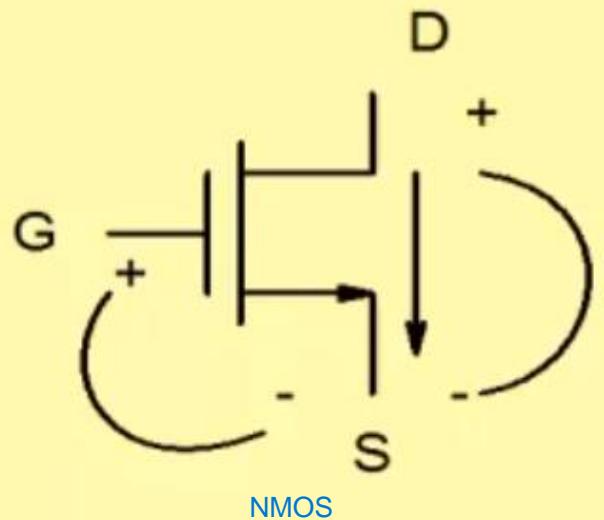
The majority of carriers in NMOS devices are electrons while those in PMOS devices are holes

so here in PMOS, source is higher than the drain, so the holes flow from the source and go to the drain.



V_{GS} is negative ; Threshold voltage V_{TP} is negative

V_{DS} is negative ; I_{DS} is negative



$$V_{GSN} \rightarrow V_{SGP}$$

$$I_{DSN} \rightarrow I_{SDP}$$

$$V_{DSN} \rightarrow V_{SDP}$$

Transformations

in NMOS: everything has S in the second parameter, like V_GS, V_DS, V_BS etc
in PMOS: everything has S in the first parameter, like V_SG, V_SD, V_SB etc-

$$V_{GSN} \rightarrow V_{SGP}$$

$$V_{DSN} \rightarrow V_{SDP}$$

$$V_{BSN} \rightarrow V_{SBP}$$

$$V_{THN} \rightarrow -V_{THP}$$

$$I_{DSN} \rightarrow I_{SDP}$$

$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{THN})^2 [1 + \lambda_n V_{DS}] \rightarrow$$

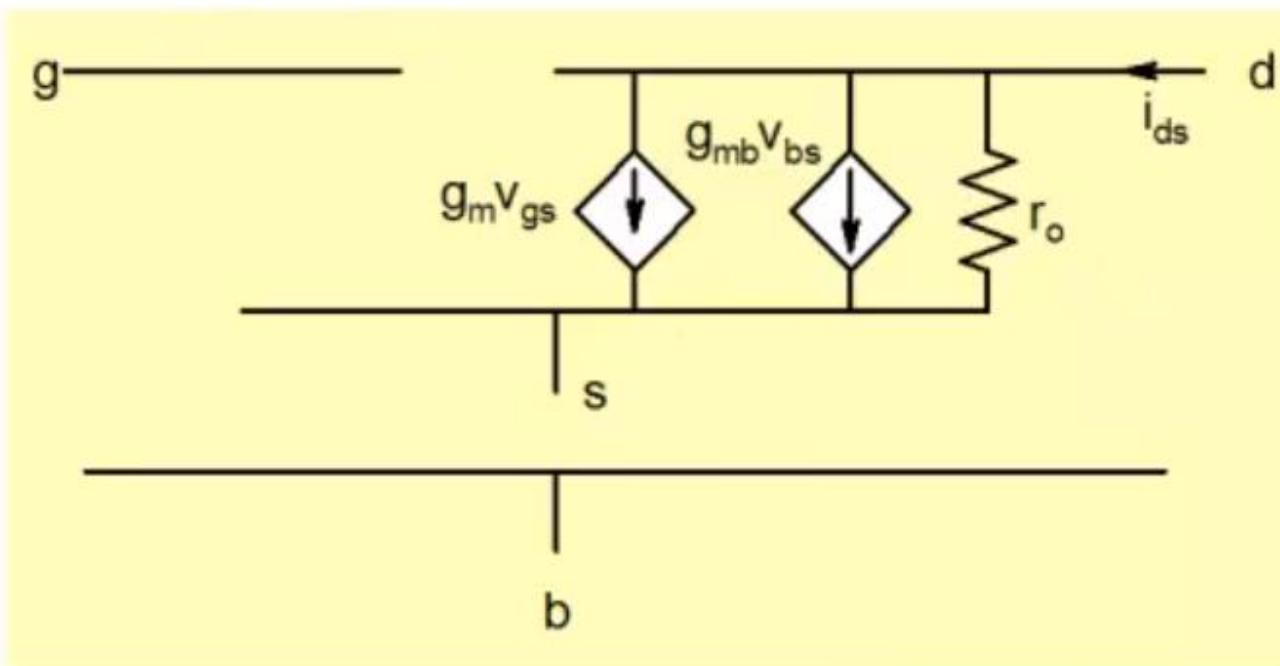
$$I_{SD} = \frac{\beta_P}{2} (V_{SG} + V_{THP})^2 [1 + \lambda_p V_{SD}]$$

$$i_{sd} = g_m v_{sg} + g_{mb} v_{sb} + \frac{v_{sd}}{r_o}$$

$$i_{ds} = g_m v_{gs} + g_{mb} v_{bs} + \frac{v_{ds}}{r_o}$$
 same as NMOS

this is the current in MOSFET for a low frequency small signal model

Small Signal Model



in the small signal model
the output current
linearly depends on all the other voltages, in this
case, since we have a 4 terminal device, it
depends on the 3 voltages, V_{BS} , V_{GS} , and V_{DS}

$$g_m = \frac{2I_{SDQ}}{V_{SGQ} + V_{THP}}$$

$$r_o = \frac{1}{\lambda_p I_{SDQ}}$$

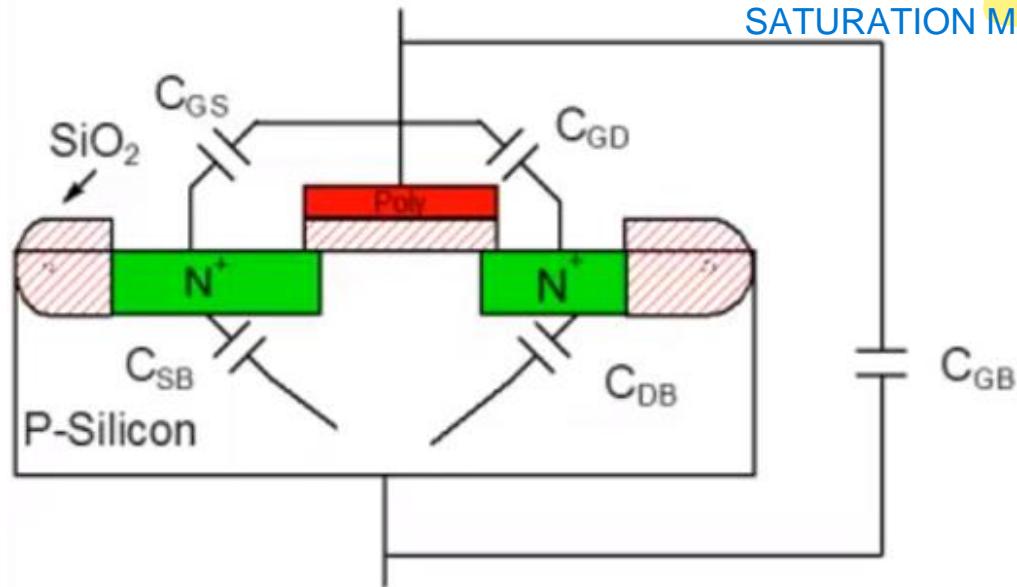
in digital electronics, we are not concerned with
small signal model, because we deal with large
transitions: $0 \rightarrow 1$ or $1 \rightarrow 0$, so we need to look at the
large signal model and not this.

here Q is the bias point. remember, small signal
model is always calculated around a bias point.

Capacitance Model

Saturation

- There are five distinct components of capacitance as illustrated below



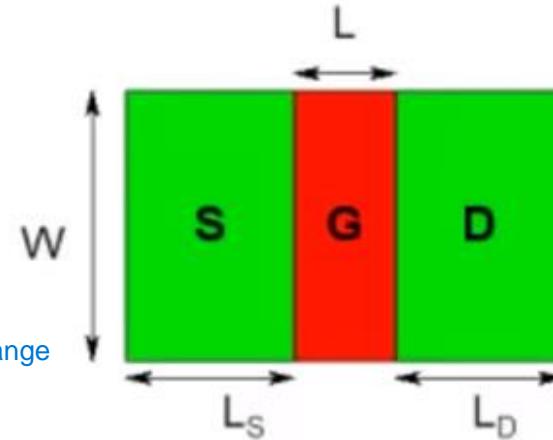
THIS IS
ONLY FOR
SATURATION MODE

unit is cap/length

C_GD has capacitance due to overlap part but no capacitance due to channel charge (considering saturation) due to pinchoff.

the channel doesn't enter the saturation region

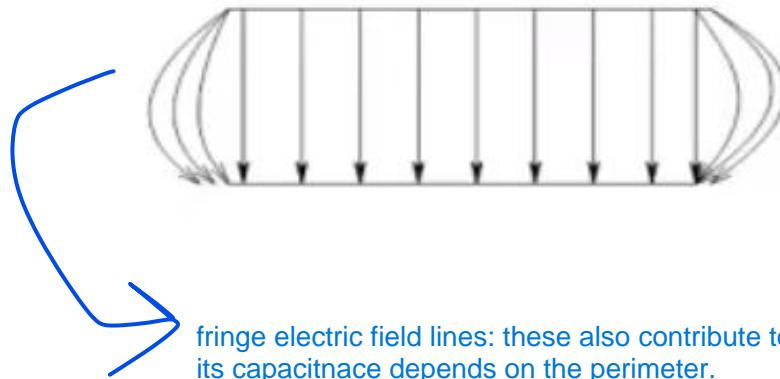
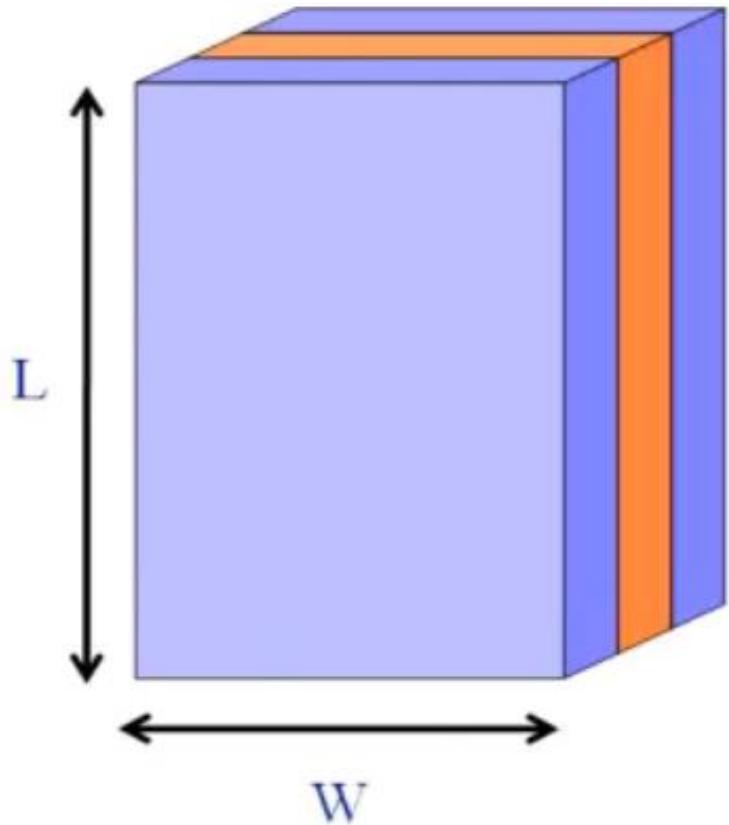
cap/length



The C_GS and C_GD capacitance depends upon the region of operation of the MOSFET, it changes from linear to saturation etc-

Meanwhile C_{SB} and C_{DB} are just capacitance of a diode in REverse bias and thus don't change when Gate or drain voltage is changed as long as the diodes are reverse biased.

Capacitances: Area and Perimeter Components

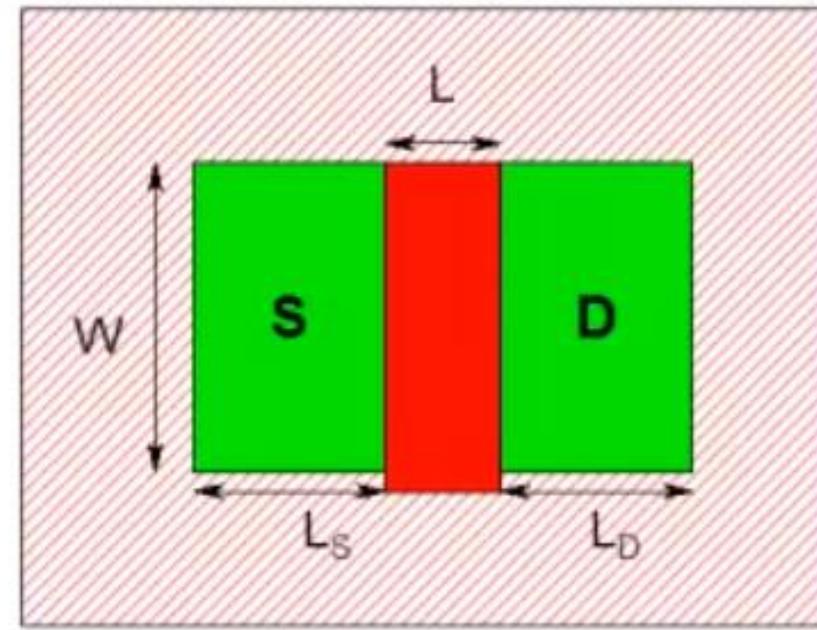
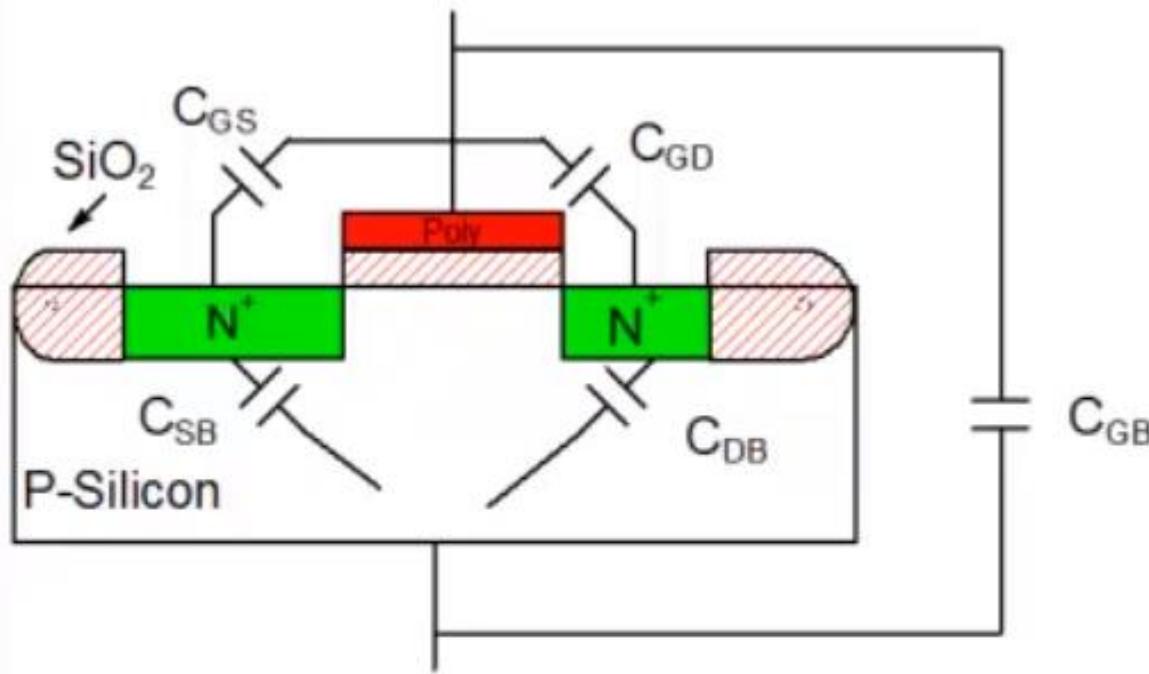


fringe electric field lines: these also contribute towards the capacitance.
its capacitance depends on the perimeter.

$$C = \frac{\epsilon}{d} \times W \times L + C_p \times (2L + 2W)$$

regular capacitance

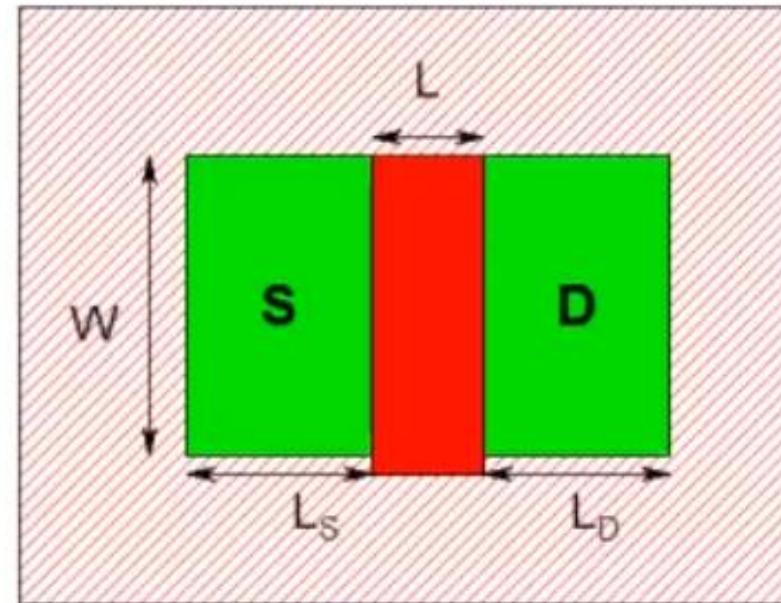
capacitance due to fringe fields, as you can see it depends on perimeter: $2L+2W$



$$C_{sb} = \frac{C_j \cdot A_s}{\left(1 + \frac{V_{SB}}{P_B}\right)^{M_j}} + \frac{C_{jsw} \cdot P_S}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_S = 2L_S + W, \quad A_s = W \cdot L_S$$

$$C_{db} = \frac{C_{jsw} \cdot P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j \cdot A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}} \quad P_D = 2L_D + W$$

$C_{gb} = C_{GBO} \cdot L \sim$ often negligible



IN triode it is 1/2 whereas in saturation it was 2/3

Triode/Linear Region

$$C_{gs} = \frac{1}{2} C_{ox'} \cdot W \cdot L + C_{GSO} \cdot W$$
$$C_{gd} = \frac{1}{2} C_{ox'} \cdot W \cdot L + C_{GDO} \cdot W$$

this was not there in saturation because of pinch off

C_{sb} = same as before

C_{db} = same as before

C_{gb} = same as before

Assuming $V_{DS} \sim 0$

Cutoff/OFF condition: $V_{GS} < V_{TH}$

Cutoff Region

$$C_{gs} = C_{GSO} \cdot W$$

$$C_{gd} = C_{GDO} \cdot W$$

in cutoff no capacitance due to the depletion region as there is no depletion region that has formed

C_{sb} = same as before

C_{db} = same as before

$$C_{gb} = C_{GBO} \cdot L + C_{ox'} \cdot W \cdot L$$

Assuming Tr. is in accumulation

Summary

$$C_{gs} \equiv \frac{2}{3} C_{ox'} W \cdot L + C_{gso} W \quad C_{gd} = C_{GDO} \cdot W$$

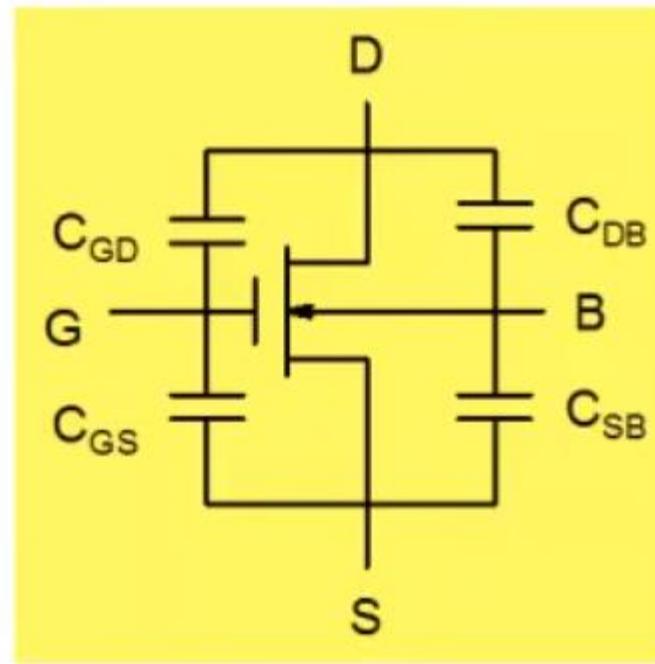
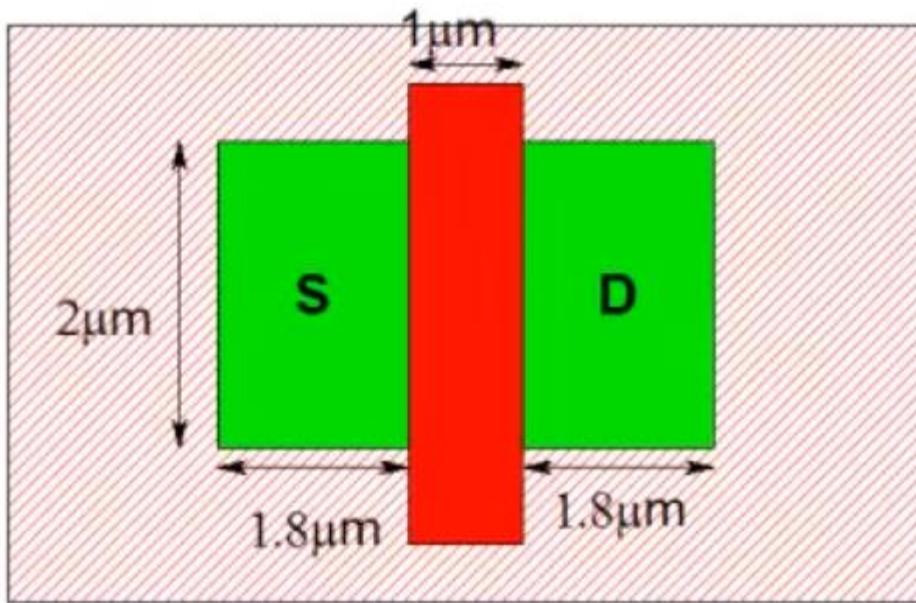
$$C_{sb} = \frac{C_j \cdot A_s}{\left(1 + \frac{V_{SB}}{P_B}\right)^{M_J}} + \frac{C_{jsw} \cdot P_S}{\left(1 + \frac{V_{SB}}{P_{BSW}}\right)^{M_{jsw}}}, \quad P_S = 2L_S + W, \quad A_s = W \cdot L_S$$

$$C_{db} = \frac{C_{jsw} \cdot P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j \cdot A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_J}} \quad P_D = 2L_D + W$$

The capacitance model presented herein requires 10 parameters:

$$C_{GSO}, C_{GDO}, C_{GBO}, C'_{OX}, C_J, PB, M_J, C_{JSW}, P_{BSW}, M_{JSW}$$

Typical Values of Capacitances



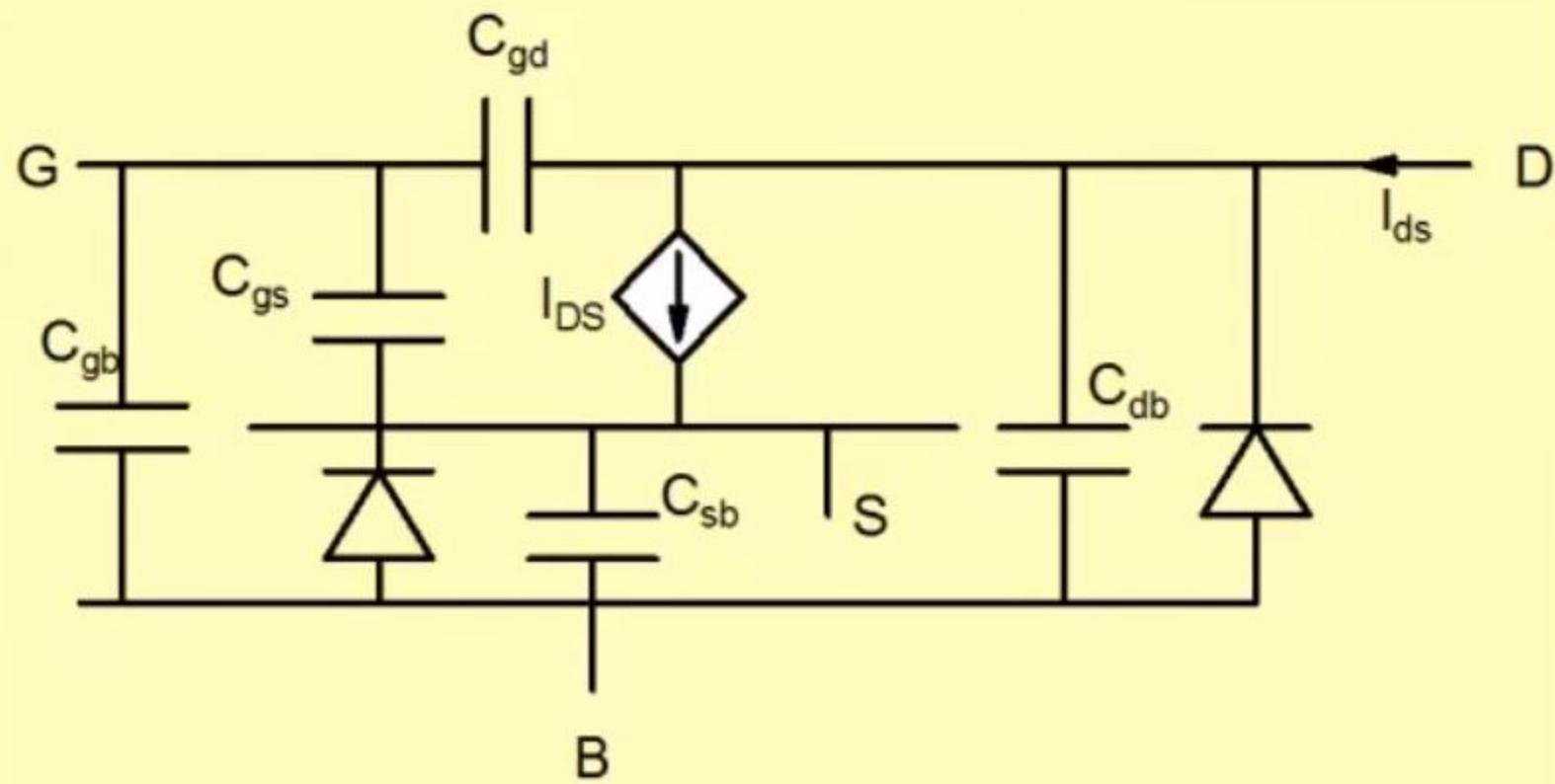
$$C_{gs} = 4.1 \text{ fF}; C_{gd} = 0.43 \text{ fF}$$

$$C_{sb} = 4.47 \text{ fF}$$

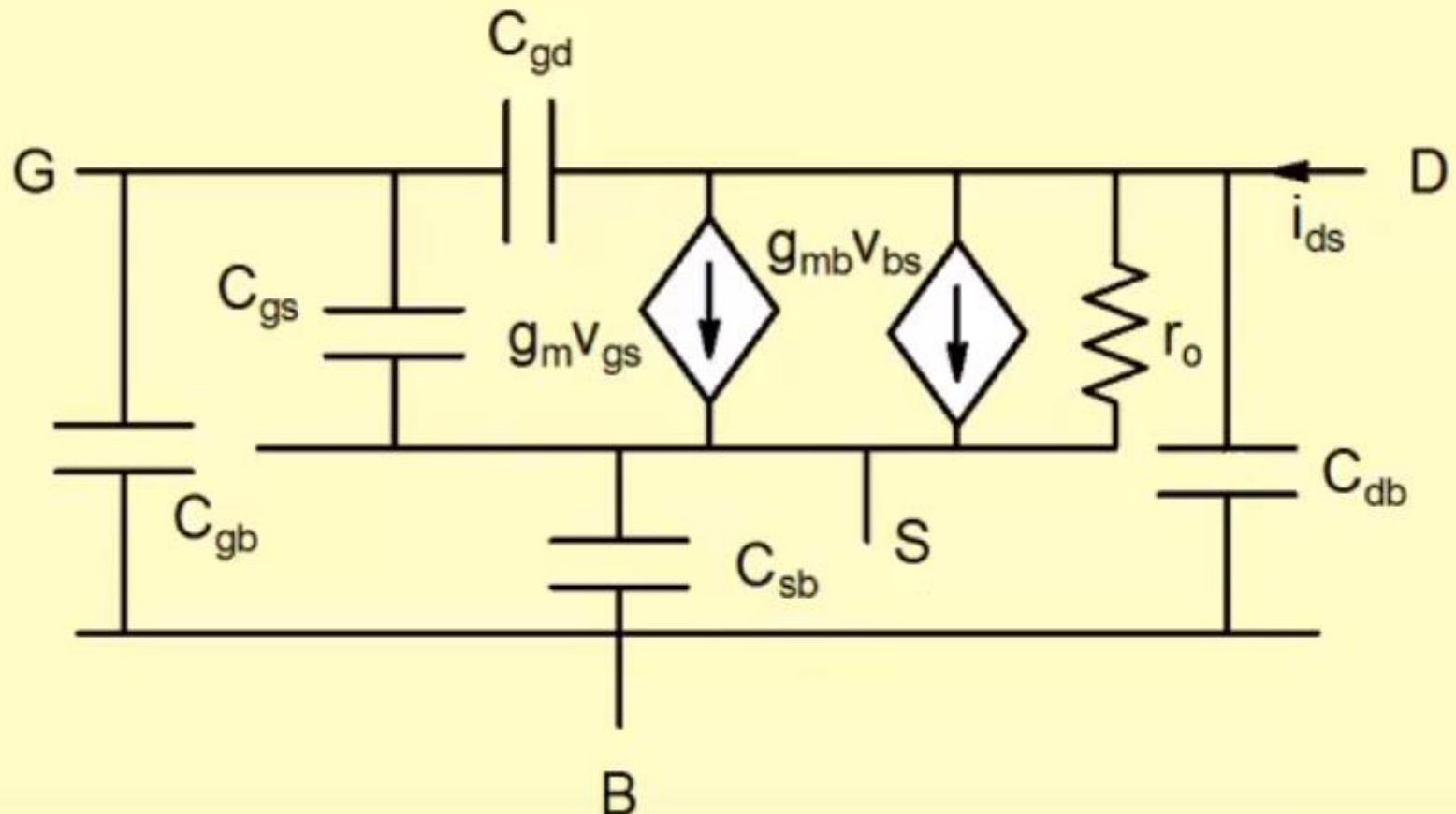
$$C_{db} = 2.75 \text{ fF}$$

$$V_{SB} = 0; V_{DS} = 2 \text{ V}$$

Complete Large Signal Model



High Frequency Small Signal Model



- We have so far discussed simple MOS models which are suitable for ‘hand-analysis’ of circuits. For more accurate prediction of circuit characteristics using circuit simulation more accurate MOS models are required.
- SPICE and its various variants are the most popular circuit simulation tool. In SPICE, there are a number of MOS models that are available including Level-1, level-2, Level-3, BSIM1, BSIM2, BSIM3, BSIM4 etc.
- Level-1 model is the simplest and is basically similar to the large signal model that we have described earlier. A popular model for submicron devices is BSIM3 model.

* **SPICE- Simulation Program with Integrated Circuit Emphasis**

* **BSIM- Berkeley Short-channel IGFET Model**

BSIM3 : Berkeley Short Channel IGFET (Insulated gate Field Effect) Model

$$I_{ds} = \frac{I_{ds0}(V_{ds\text{eff}})}{1 + \frac{R_{ds}I_{ds0}(V_{ds\text{eff}})}{V_{ds\text{eff}}}} \left(1 + \frac{V_{ds} - V_{ds\text{eff}}}{V_A} \right) \left(1 + \frac{V_{ds} - V_{ds\text{eff}}}{V_{ASCBE}} \right)$$

$$I_{ds0} = \frac{W_{\text{eff}}\mu_{\text{eff}}C_{\text{ox}}V_{gsteff}(1 - A_{\text{bulk}} \frac{V_{ds\text{eff}}}{2(V_{gsteff} + 2v_t)})V_{ds\text{eff}}}{L_{\text{eff}}[1 + V_{ds\text{eff}} / (E_{\text{sat}}L_{\text{eff}})]}$$

$$V_A = V_{A_{\text{sat}}} + (1 + \frac{P_{\text{vag}}V_{gsteff}}{E_{\text{sat}}L_{\text{eff}}})(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}})^{-1}$$

$$V_{ACLM} = \frac{A_{\text{bulk}}E_{\text{sat}}L_{\text{eff}} + V_{gsteff}}{P_{CLM}A_{\text{bulk}}E_{\text{sat}}} (V_{ds} - V_{ds\text{eff}})$$

Introduction

Latest Models

Nano-CMOS

Post-Silicon

Interconnect

Reliability

Contact



LATEST MODELS

Typical SPICE model files for each future generation are available here.

Attention: By using a **PTM** file, you agree to acknowledge both the URL of **PTM**: <http://ptm.asu.edu/> and the related publications in all documents and publications involving its usage.

New!

June 01, 2012:

PTM releases a new set of models for multi-gate transistors (**PTM-MG**), for both HP and LSTP applications. It is based on [BSIM-CMG](#), a dedicated model for multi-gate devices.

Acknowledgement: PTM-MG is developed in collaboration with ARM.

Please start from [models](#) and [param.inc](#).

- 7nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 10nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 14nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 16nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)
- 20nm PTM-MG [HP NMOS](#), [HP PMOS](#), [LSTP NMOS](#), [LSTP PMOS](#)

The entire package is also available here: [PTM-MG](#)

November 15, 2008:

PTM releases a new set of models for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect.

- 16nm PTM LP model: [V2.1](#)
- 22nm PTM LP model: [V2.1](#)
- 32nm PTM LP model: [V2.1](#)
- 45nm PTM LP model: [V2.1](#)

September 30, 2008:

PTM releases a new set of models for high-performance applications (PTM HP), incorporating high-k/metal gate and stress effect.

- 16nm PTM HP model: [V2.1](#)
- 22nm PTM HP model: [V2.1](#)

BSIM Group

About

News

Models

Publications

Members

Links

BSIM4, as the extension of BSIM3 model, is a physics-based, accurate, scalable, robust technology development. It is developed by the BSIM Research Group in the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California, Berkeley. All suggestions for model improvements are charted by the Compact Model Coalition (CMC).

BSIM4 has been used for the 0.13 um, 90 nm, 65 nm, 45/40 nm, 23/28 nm, and 22/20nm technology nodes.

See BSIM3, a predecessor of BSIM4, [here](#).

BSIM-CMG
BSIM-IMG
BSIM-SOI
BSIM-BULK
BSIM4

Physical effects into sub-100nm regime. It is a SPICE model for circuit simulation and CMOS

Latest Release

BSIM4 4.8.1 was released on Feb. 15, 2017.

We would like to thank CMC members for testing beta models and providing valuable feedbacks during model development.

Download [BSIM4 4.8.1](#) model package, including

- Model code in C

* PTM Low Power 16nm Metal Gate / High-K / Strained-Si

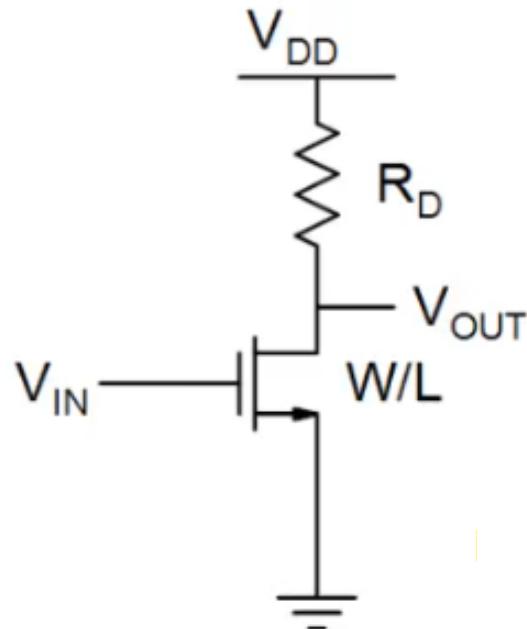
* nominal Vdd = 0.9V

.model nmos nmos level = 54

+version = 4.0	binunit = 1	paramchk= 1	mobmod = 0
+capmod = 2	igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	
+tnom = 27	toxe = 1.2e-009	toxp = 9e-010	toxm = 1.2e-009
+dtox = 3e-010	epsrox = 3.9	wint = 5e-009	lint = 0
+ll = 0	wl = 0	lln = 1	wln = 1
+lw = 0	ww = 0	lwn = 1	wwn = 1
+lw1 = 0	wwl = 0	xpart = 0	toxref = 1.2e-009
+vth0 = 0.68191	k1 = 0.4	k2 = 0	k3 = 0
+k3b = 0	w0 = 2.5e-006	dvt0 = 1	dvt1 = 2
+dvt2 = 0	dvt0w = 0	dvt1w = 0	dvt2w = 0
+dsub = 0.1	minv = 0.05	voffl = 0	dvtp0 = 1e-011
+dvtp1 = 0.1	lpe0 = 0	lpeb = 0	xj = 5e-009
+ngate = 1e+023	ndep = 7e+018	nsd = 2e+020	phin = 0
+cdsc = 0	cdscb = 0	cdscd = 0	cit = 0
+voff = -0.1014	nfactor = 1.6	eta0 = 0.0095	etab = 0
+vfb = -0.55	u0 = 0.028	ua = 6e-010	ub = 1.2e-018
+uc = 0	vsat = 200000	a0 = 1	ags = 0
+a1 = 0	a2 = 1	b0 = 0	b1 = 0
+keta = 0.04	dwg = 0	dwb = 0	pclm = 0.02
+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = -0.005	drout = 0.5
+pvag = 1e-020	delta = 0.01	pscbe1 = 8.14e+008	pscbe2 = 1e-007
+fprout = 0.2	pdits = 0.01	pditsd = 0.23	pditsl = 2300000
+rsh = 5	rdsw = 170	rsw = 75	rdw = 75
+rdswmin = 0	rdwmin = 0	rswmin = 0	prwg = 0
+prwb = 0	wr = 1	alpha0 = 0.074	alpha1 = 0.005
+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002
+egidl = 0.8	aiebacc = 0.012	biebacc = 0.0028	ciebacc = 0.002

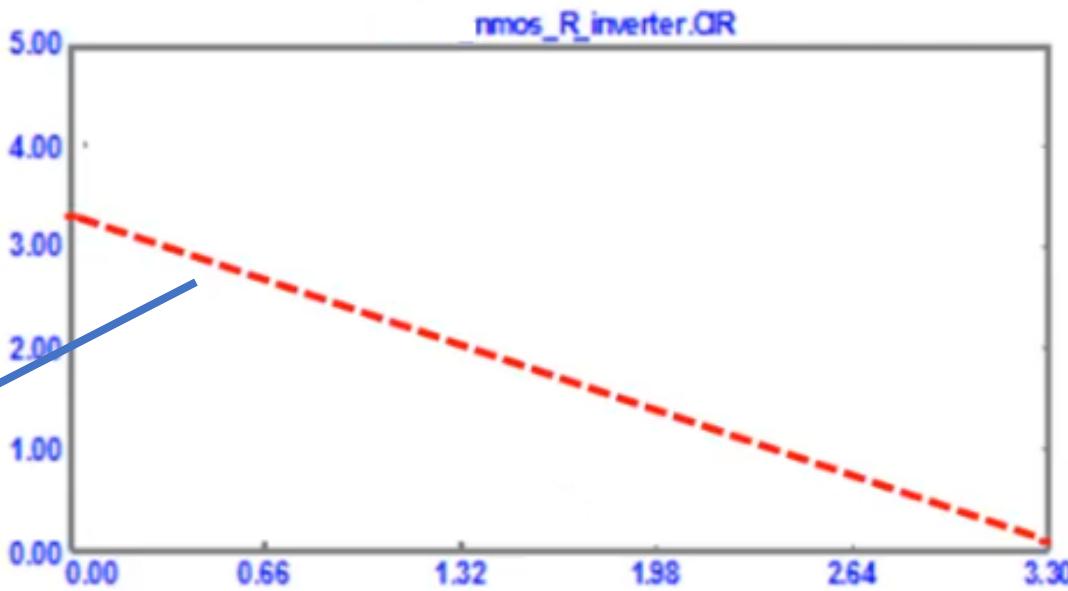
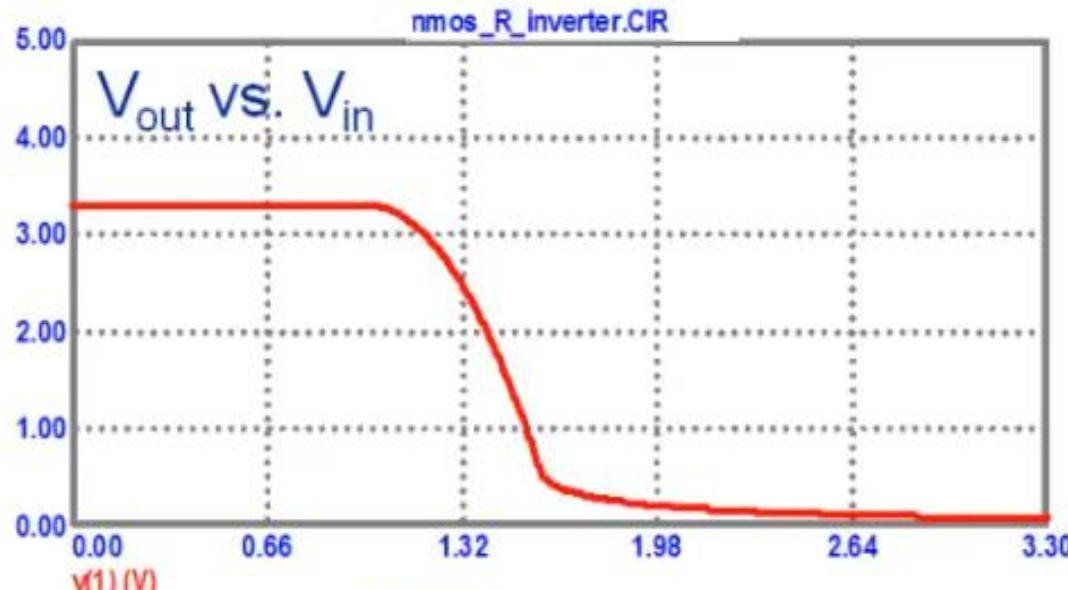
Circuit Design

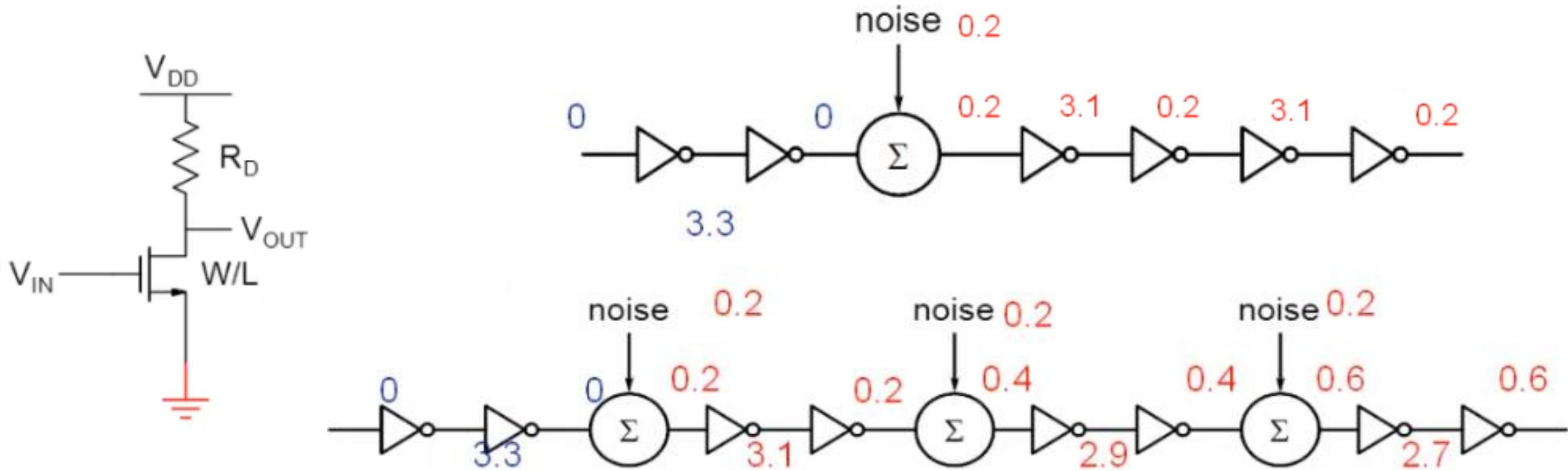
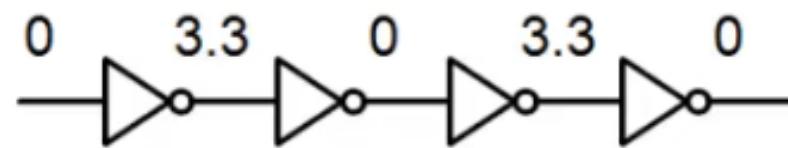
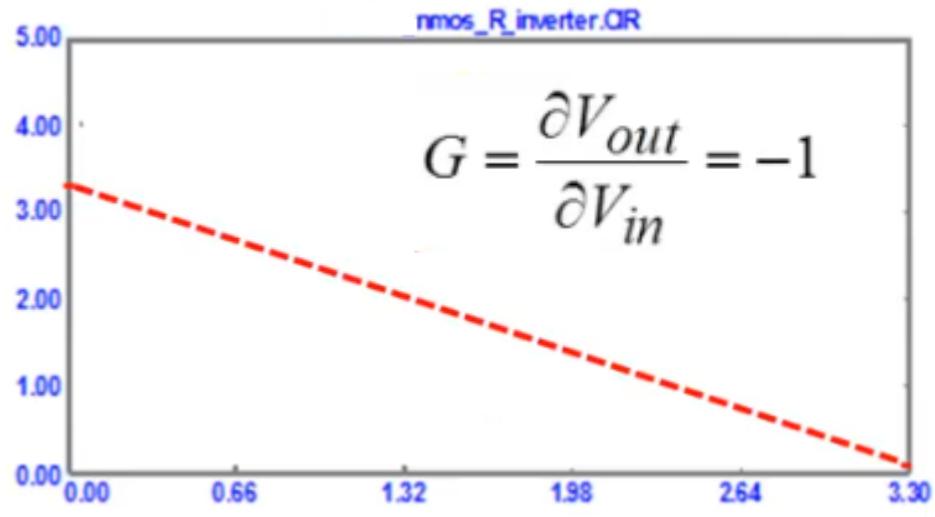
Inverter with Resistive Load



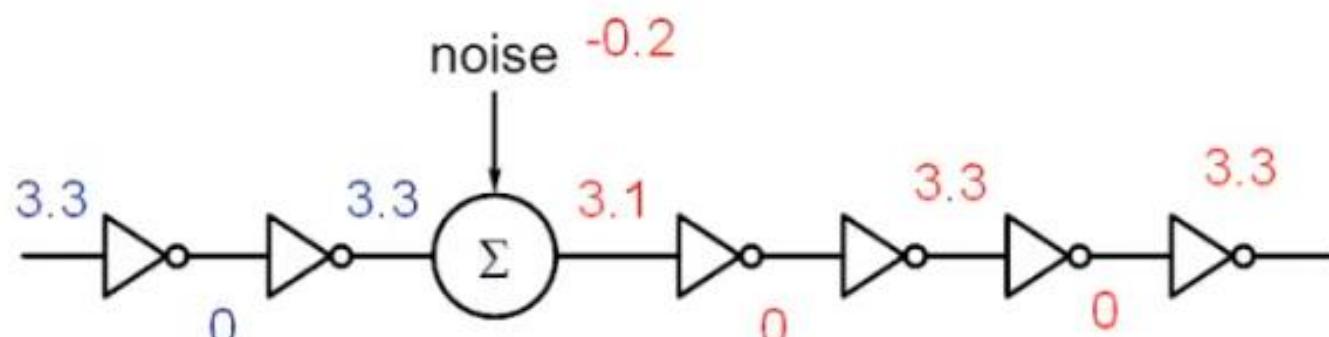
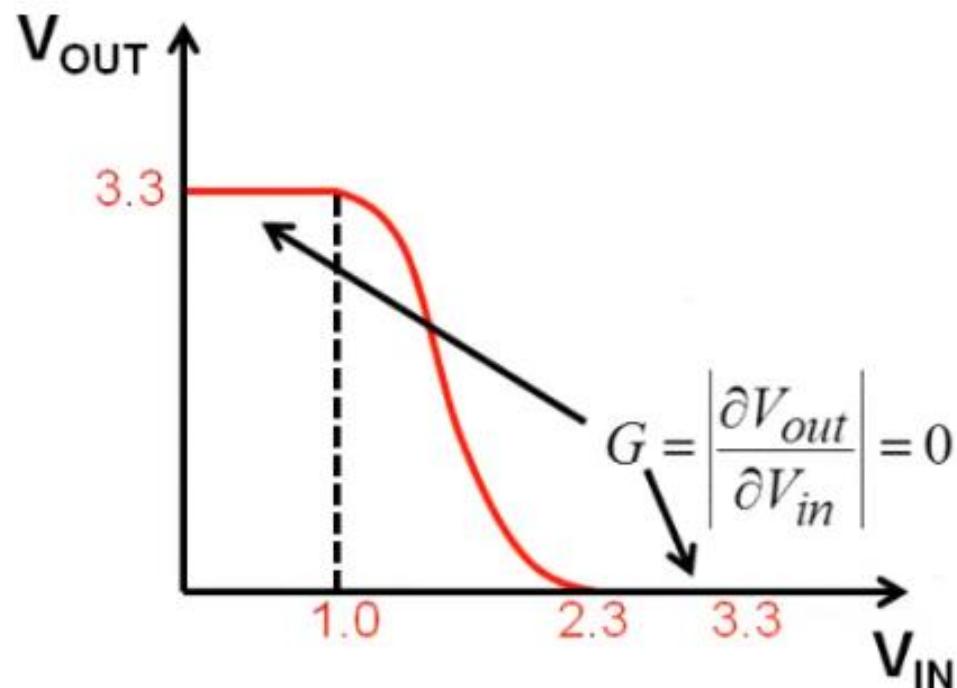
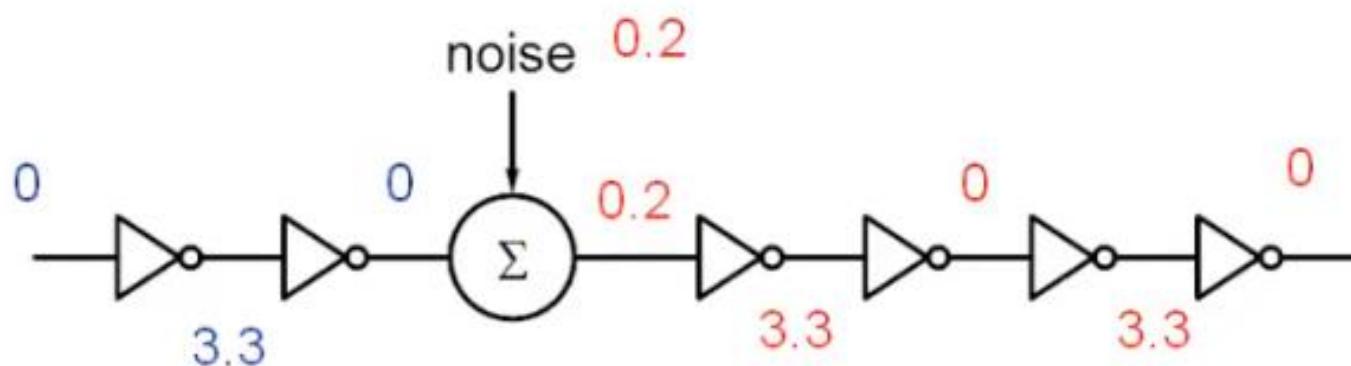
1. Area
2. Delay
3. Power
4. ...

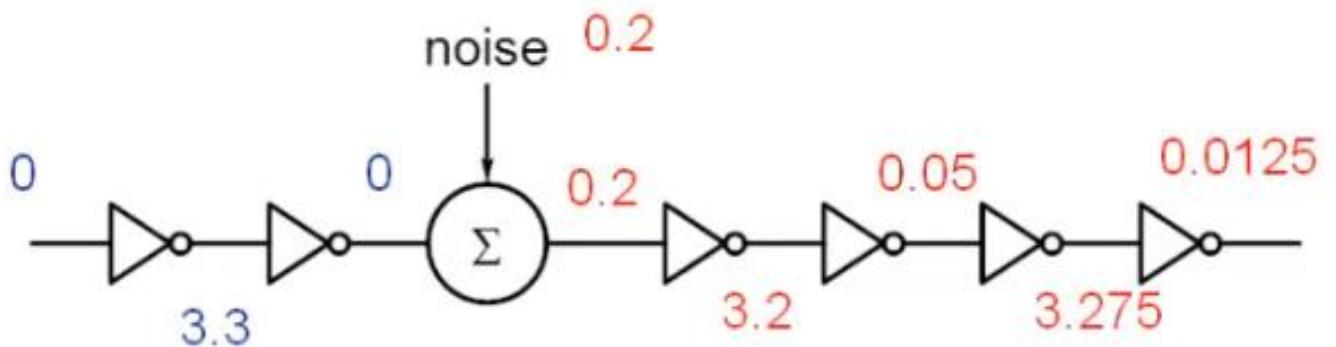
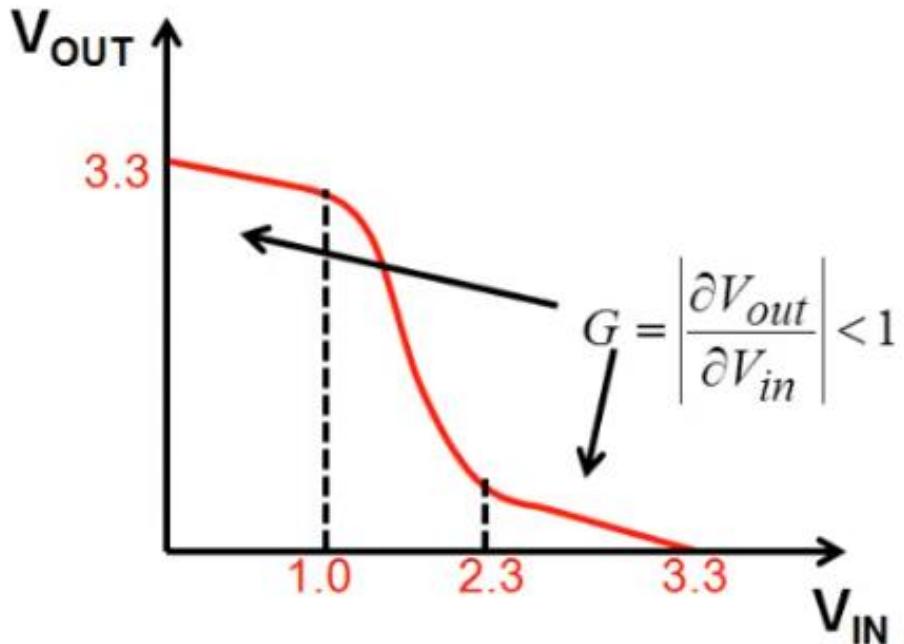
Is this a good inverter ?





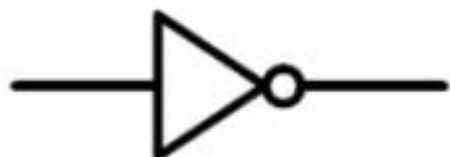
Systems that we design should be robust in presence of noise



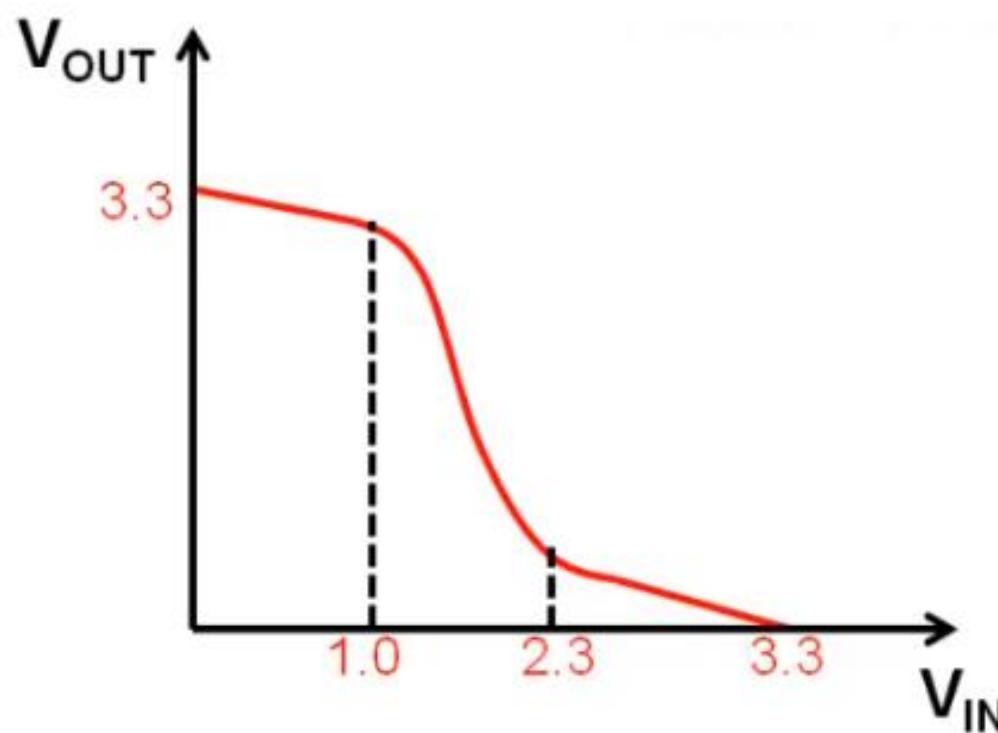


There must be a region
with Gain greater than
unity

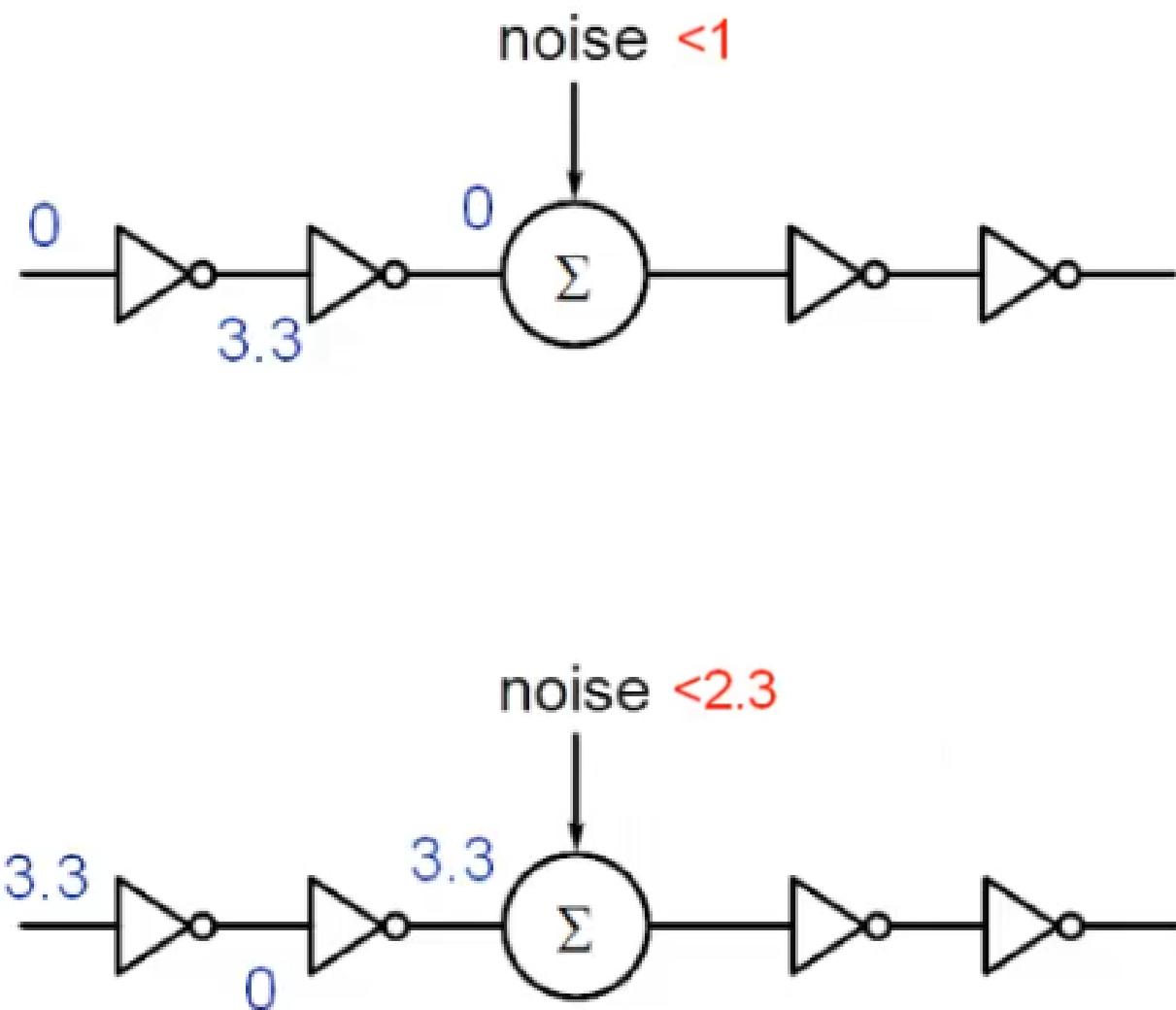
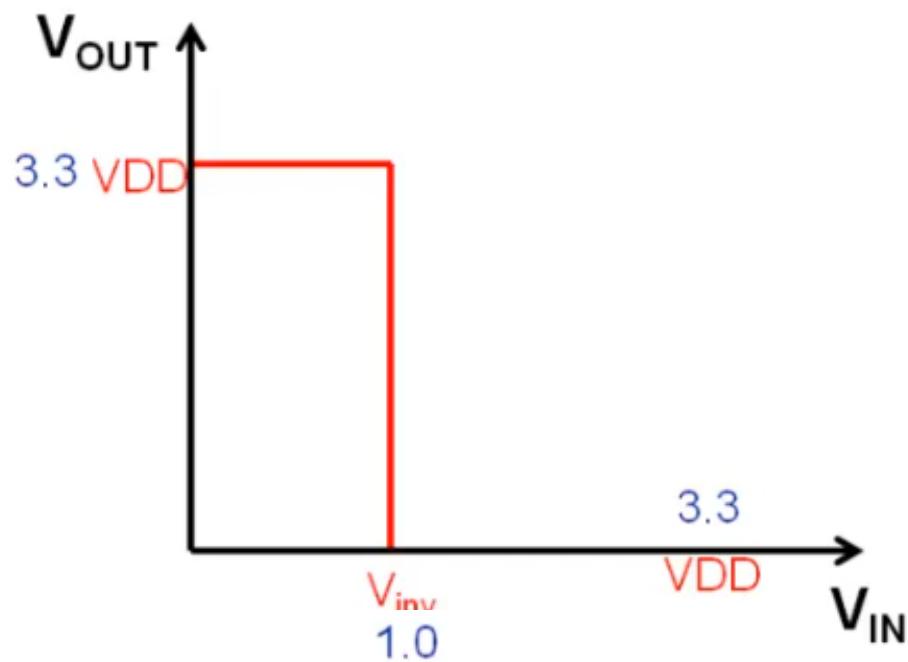
To build an inverter, we need an element that can provide gain
i.e. a transistor



1. Area
2. Delay
3. Power
4. Noise margin

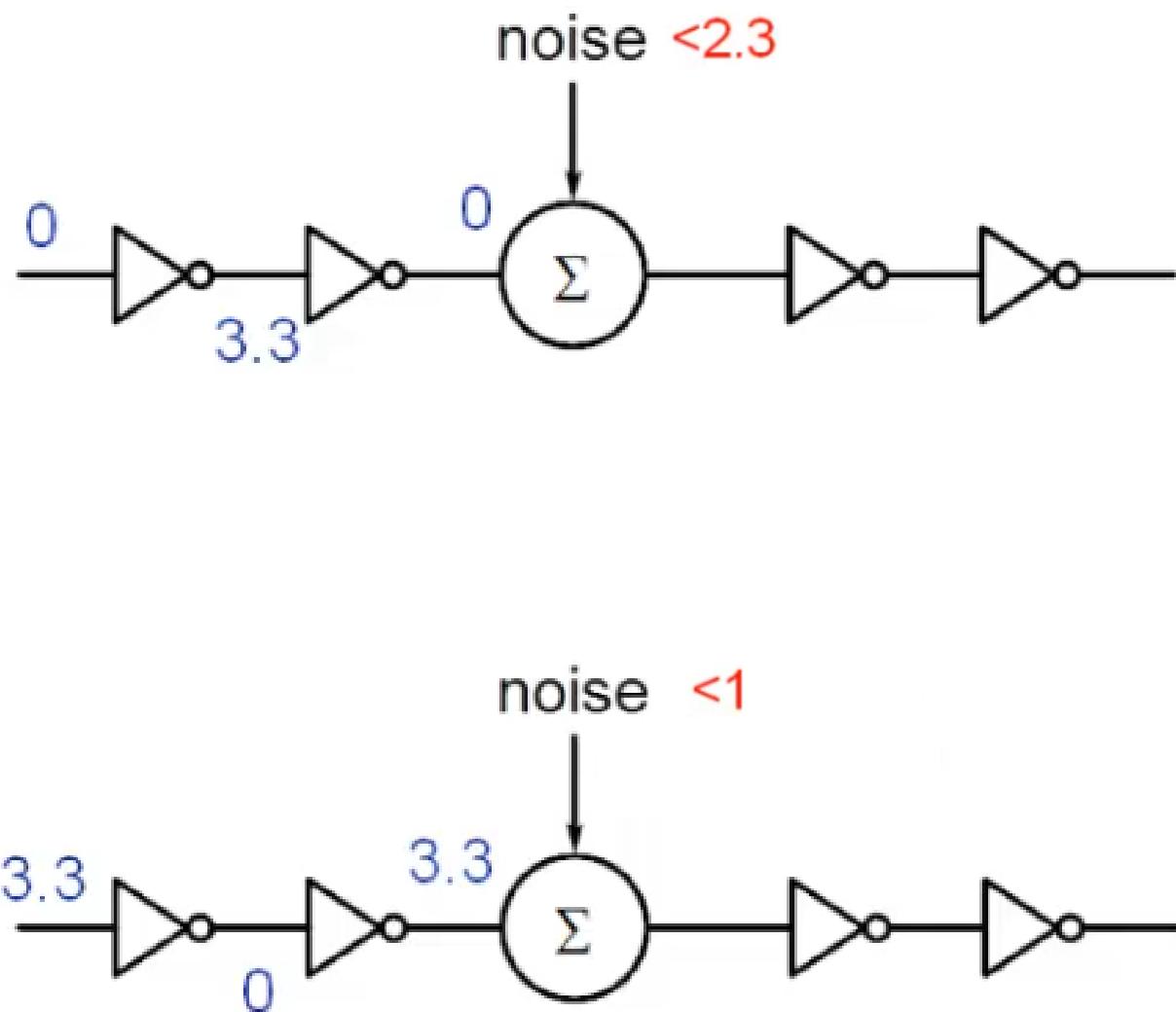
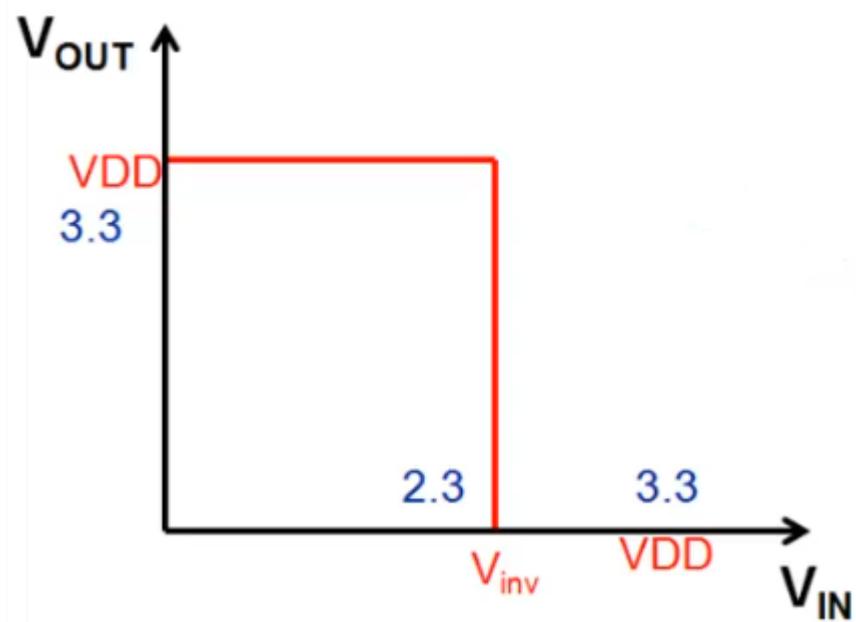


Inverter Threshold Voltage

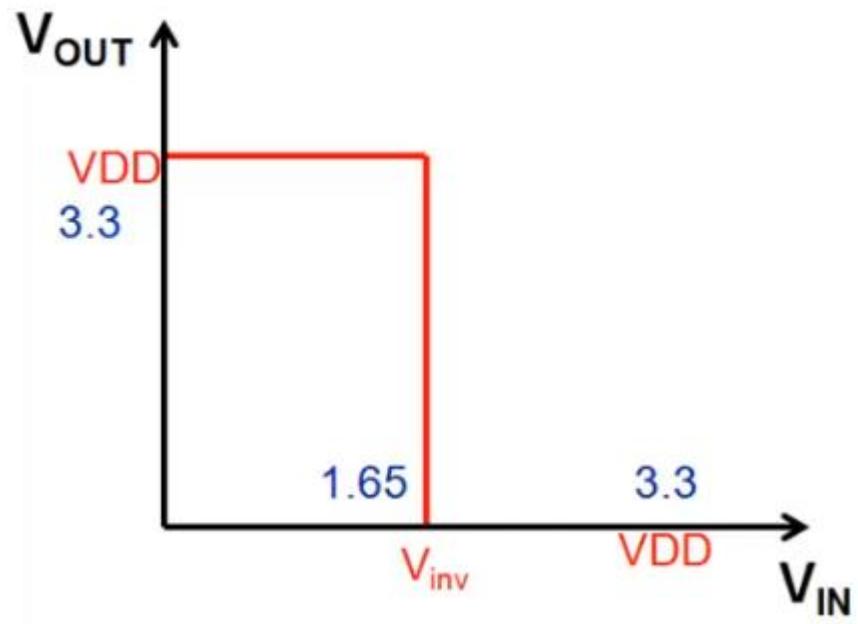


Asymmetrical characteristics

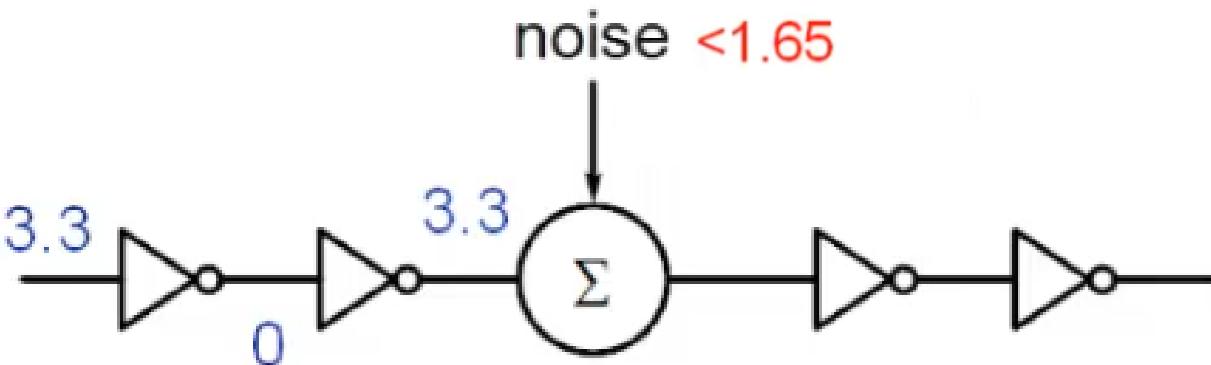
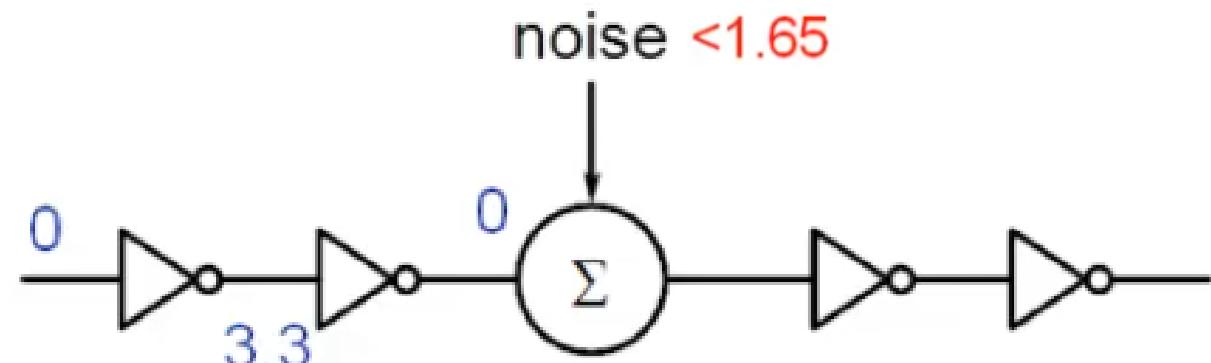
Inverter Threshold Voltage



Asymmetrical characteristics

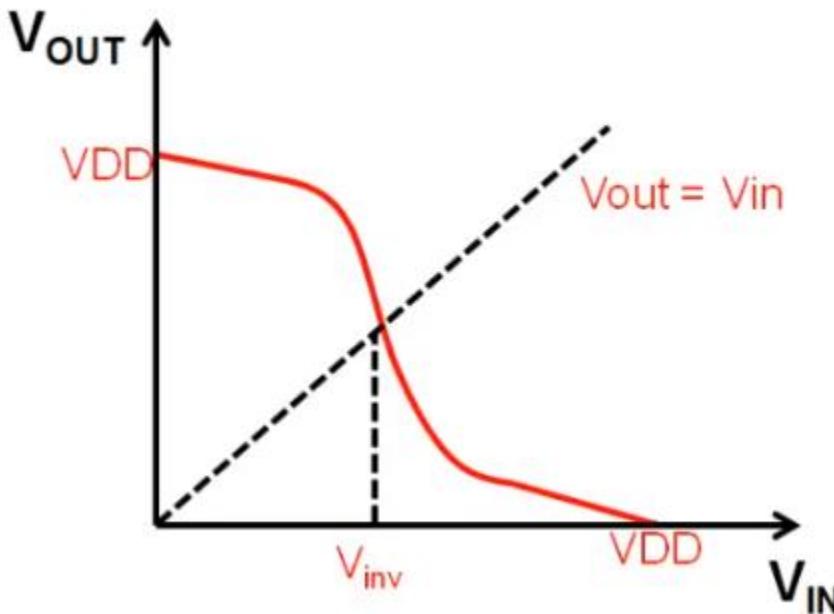


$$V_{inv} = 0.5V_{DD}$$



symmetrical characteristics

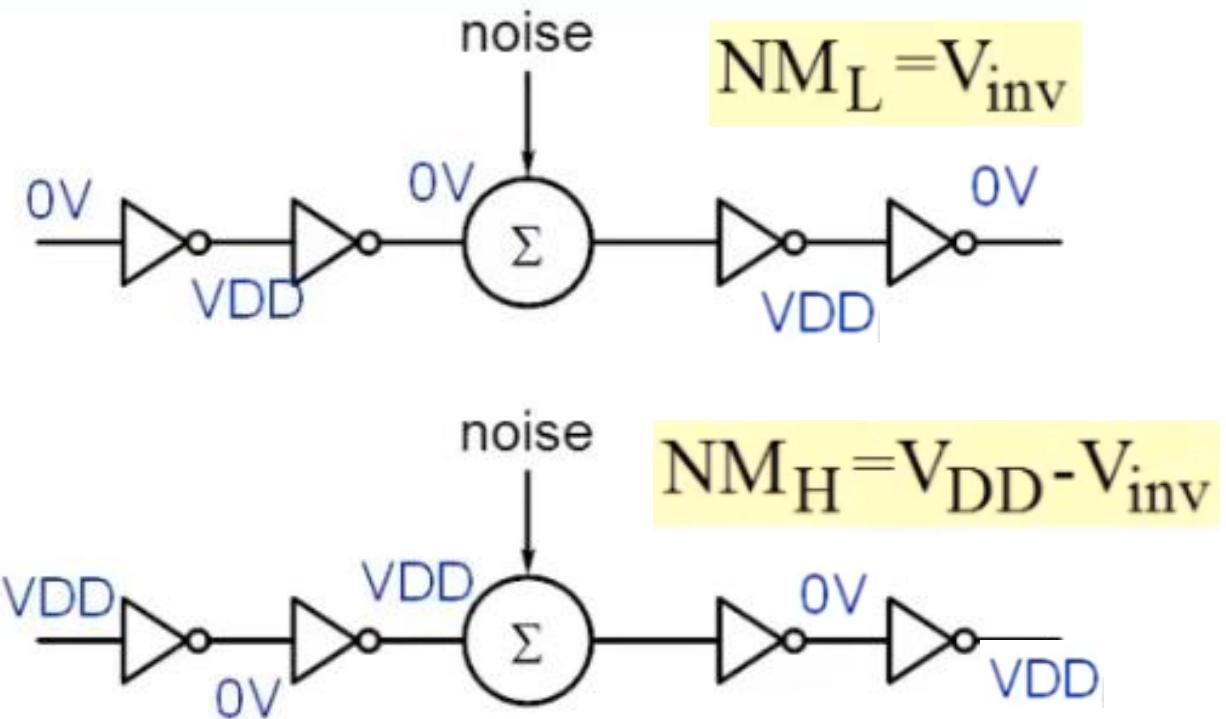
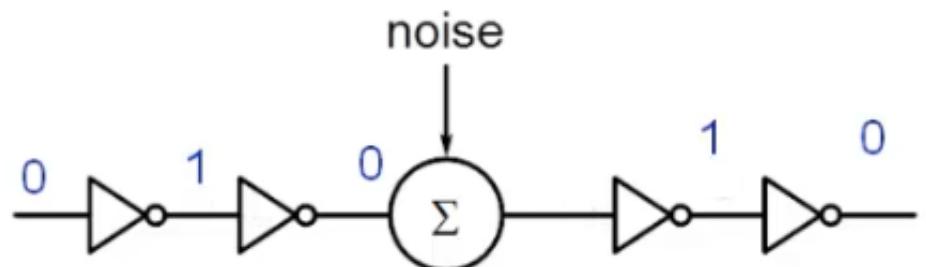
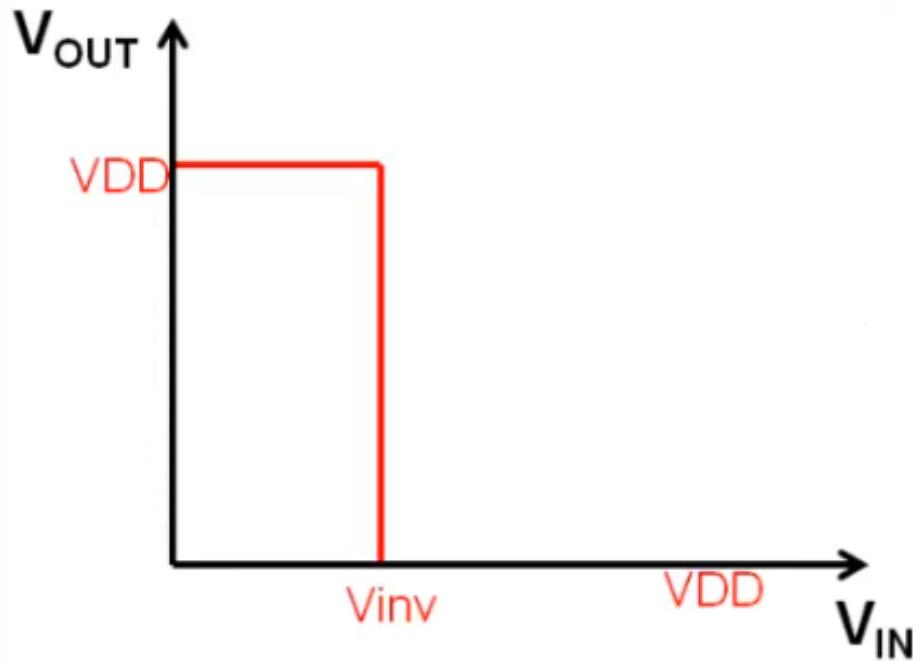
Inverter Threshold Voltage



For $V_{in} > V_{inv}$, the output is closer to “0”

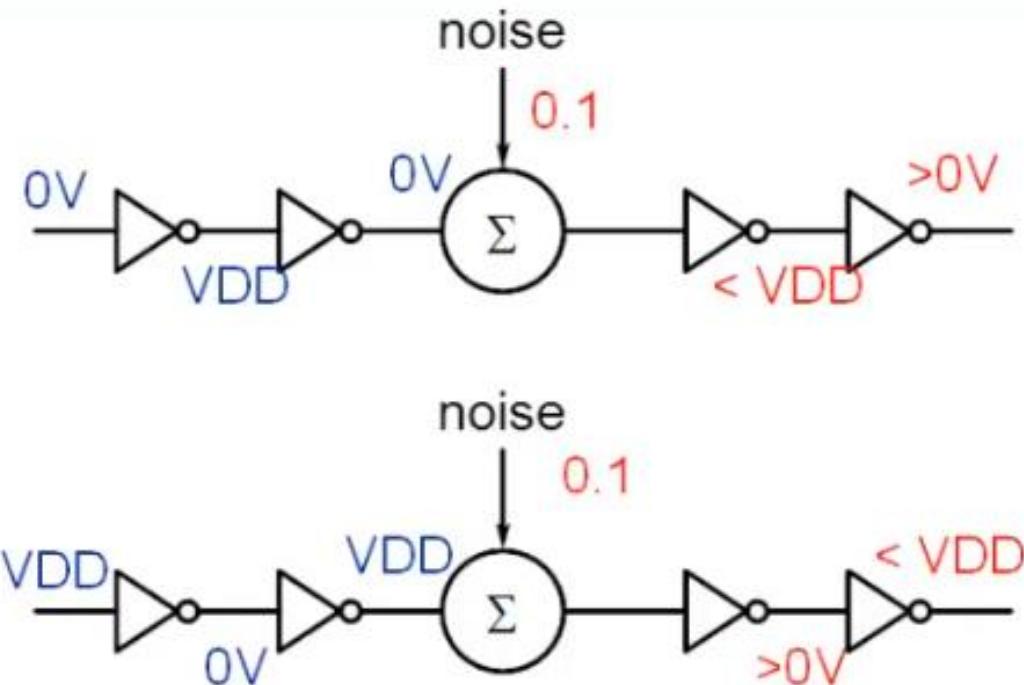
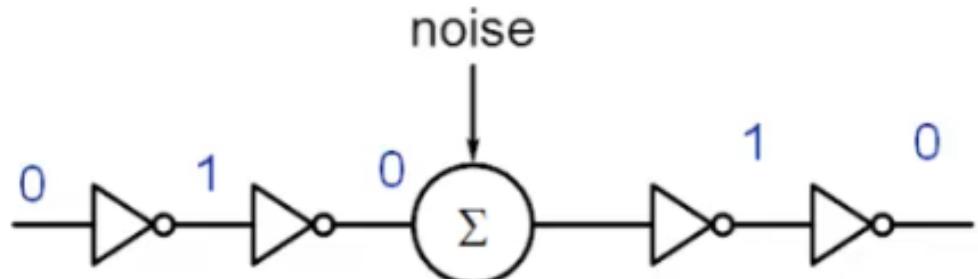
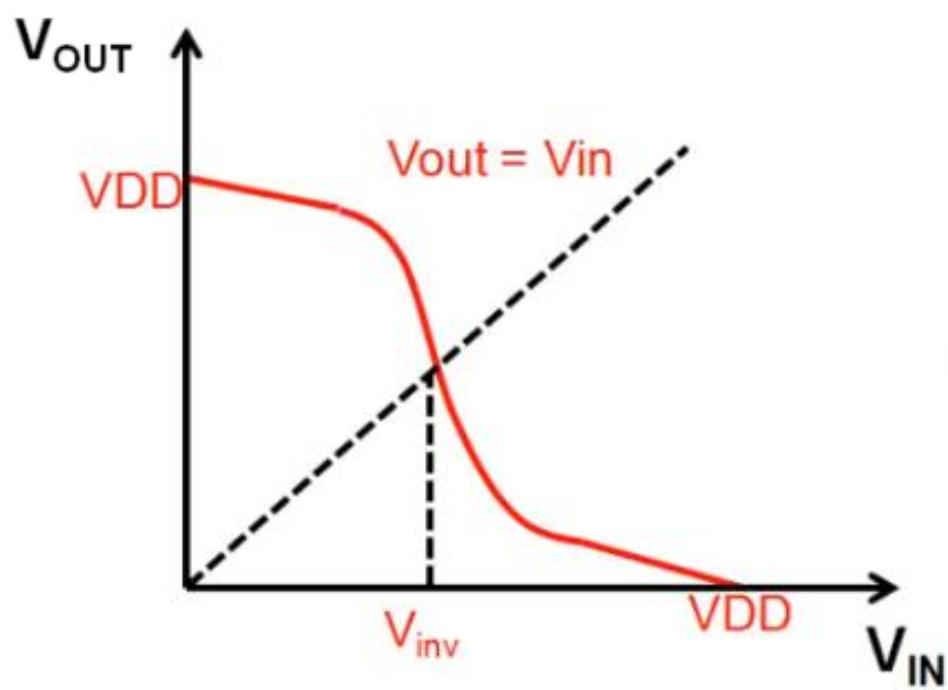
$$V_{inv} = 0.5V_{DD}$$

Noise Margins

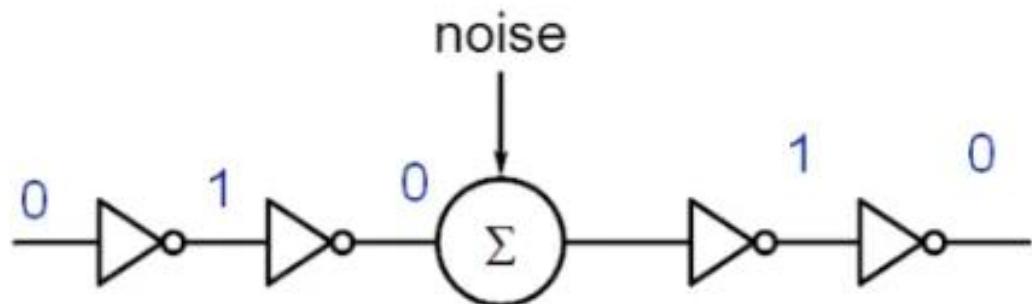
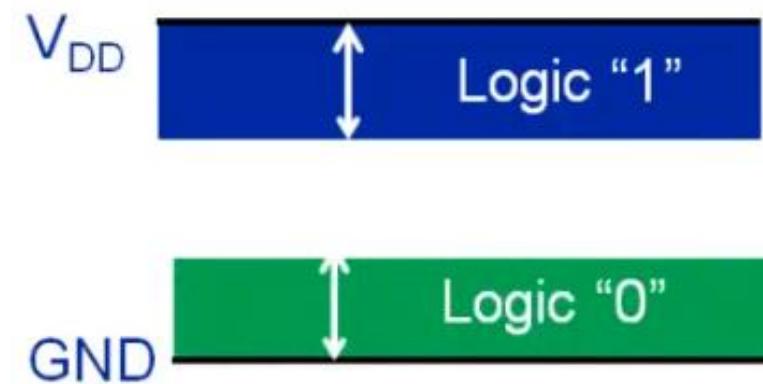
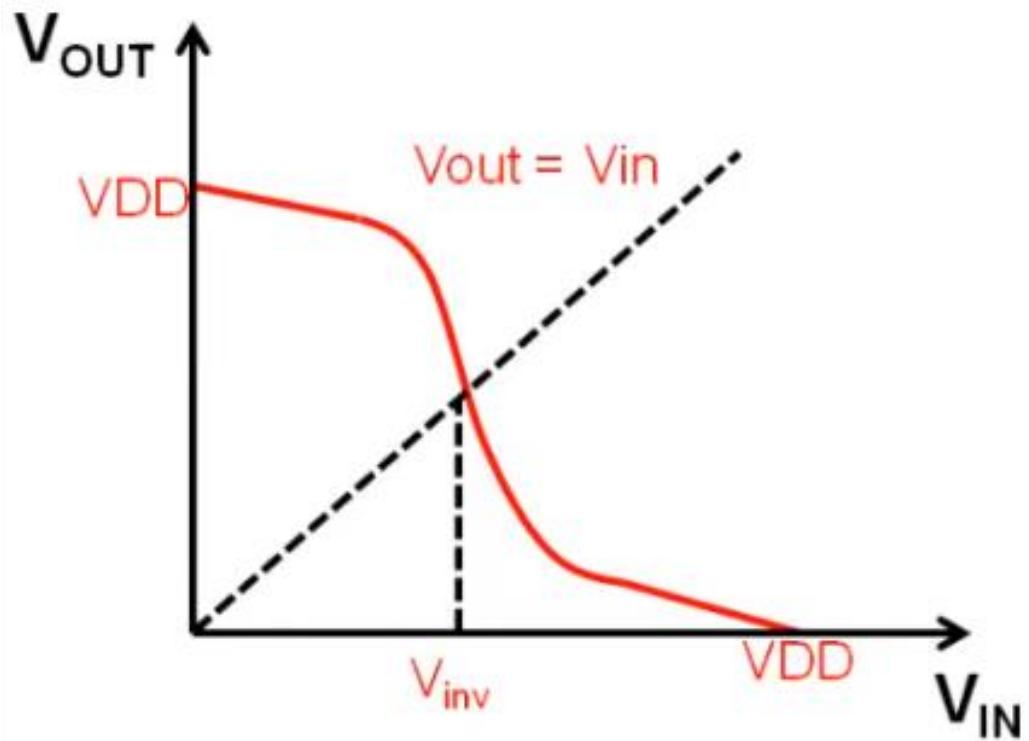


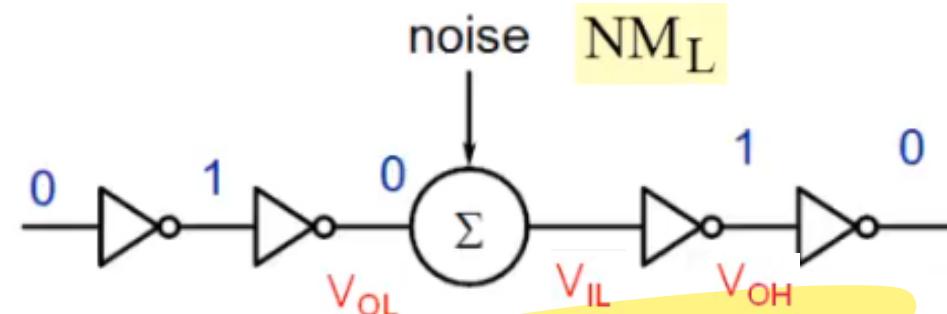
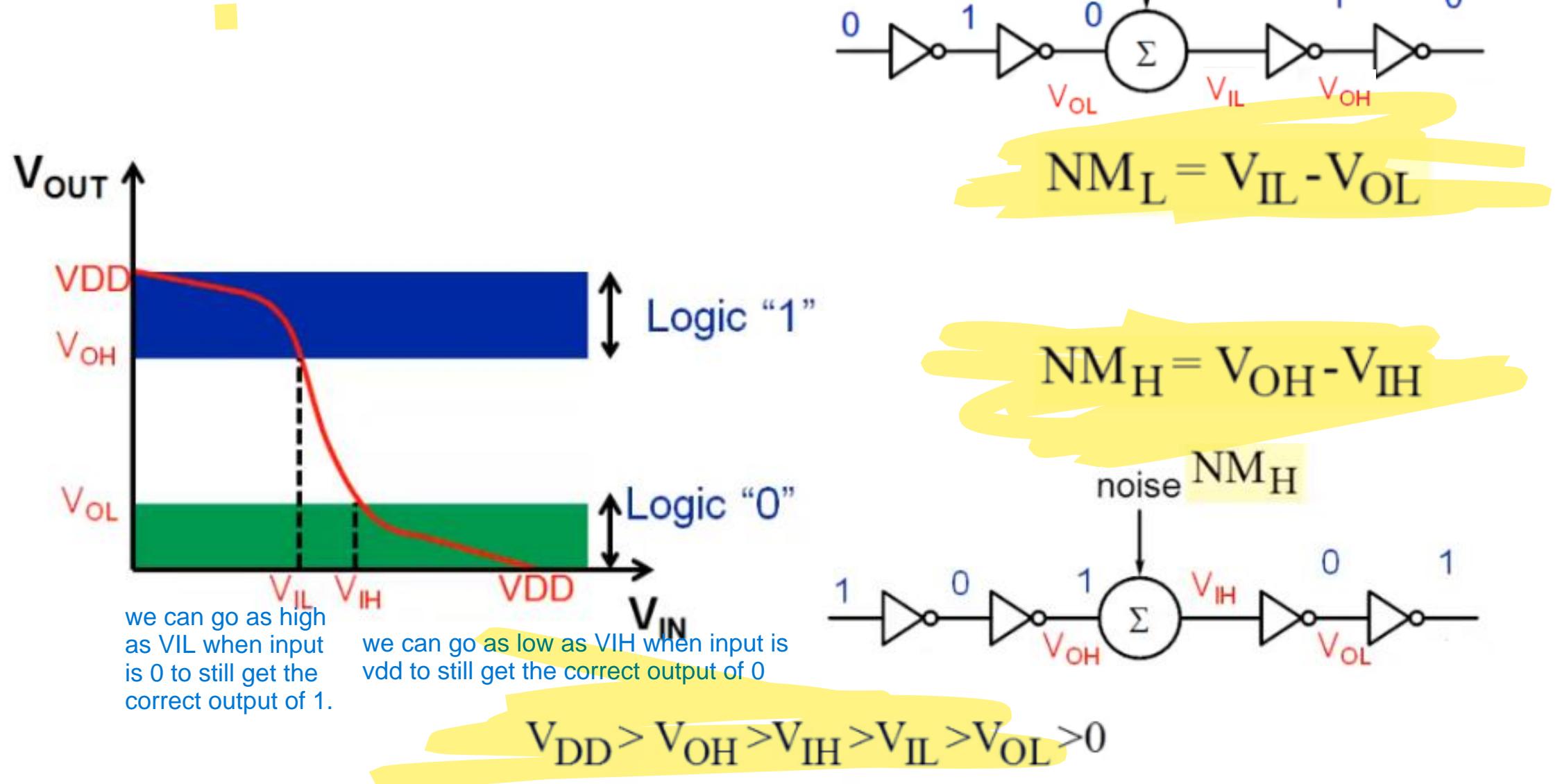
Logical correctness

Noise Margins



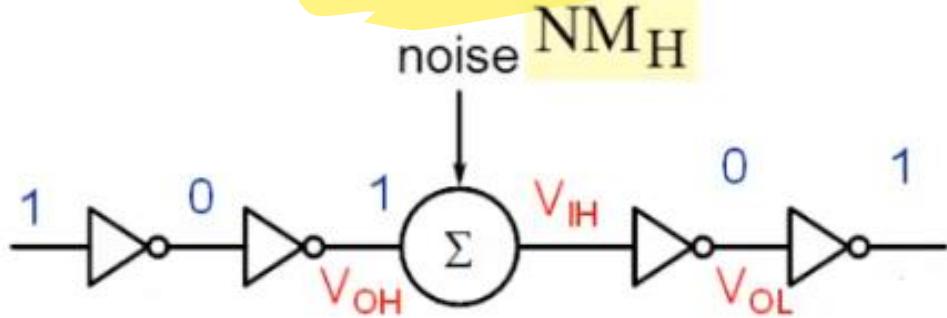
Need proper definition of logic levels in terms of voltages



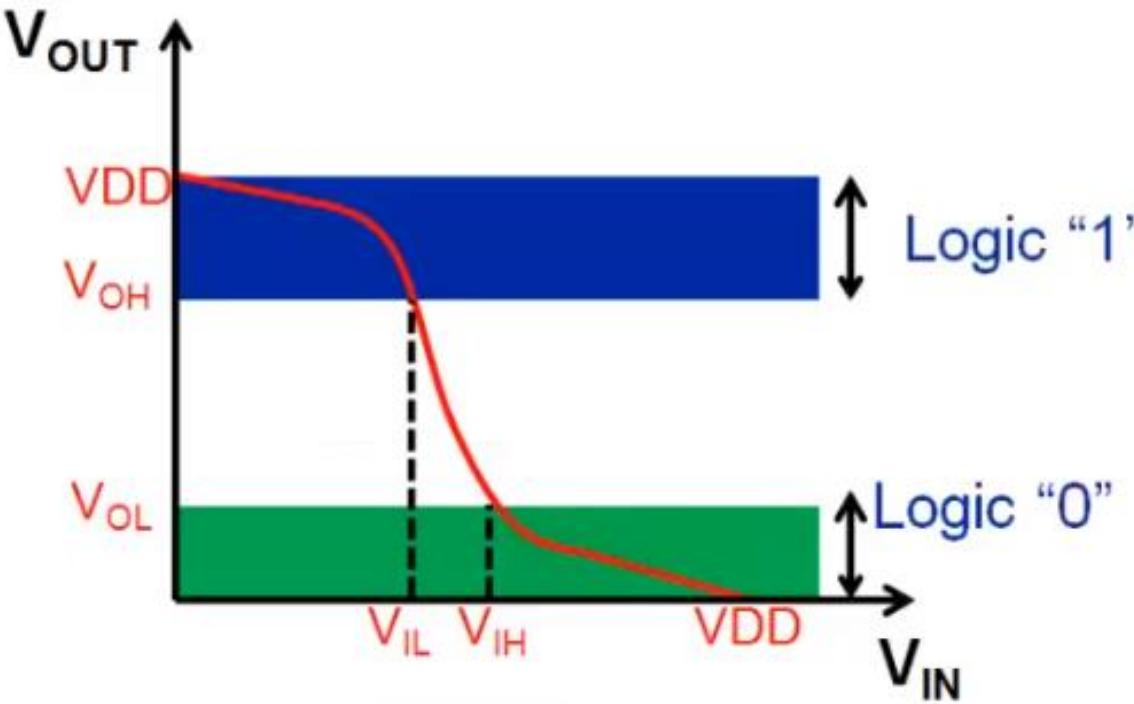


$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

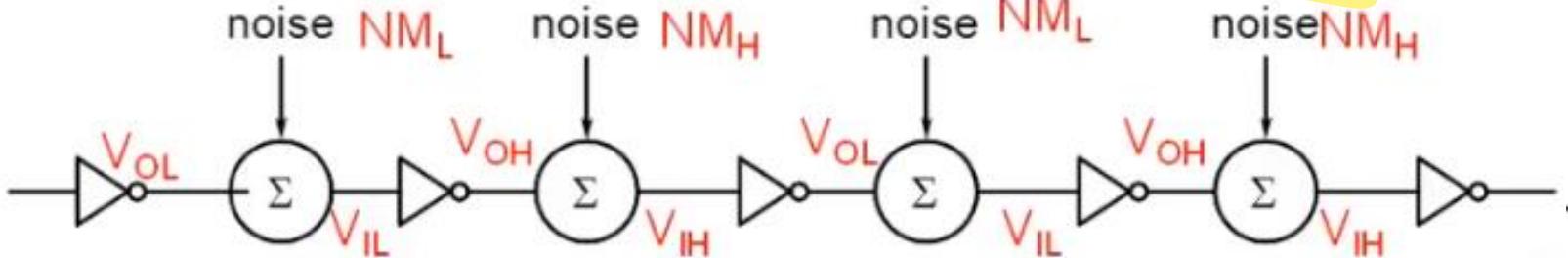


Noise Margins



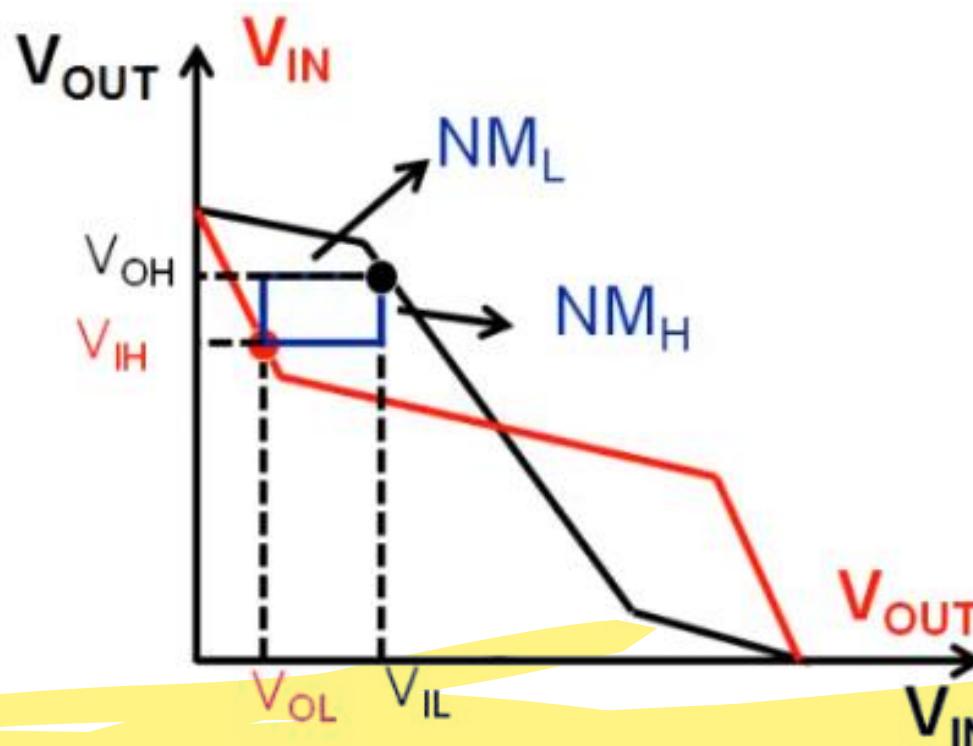
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$



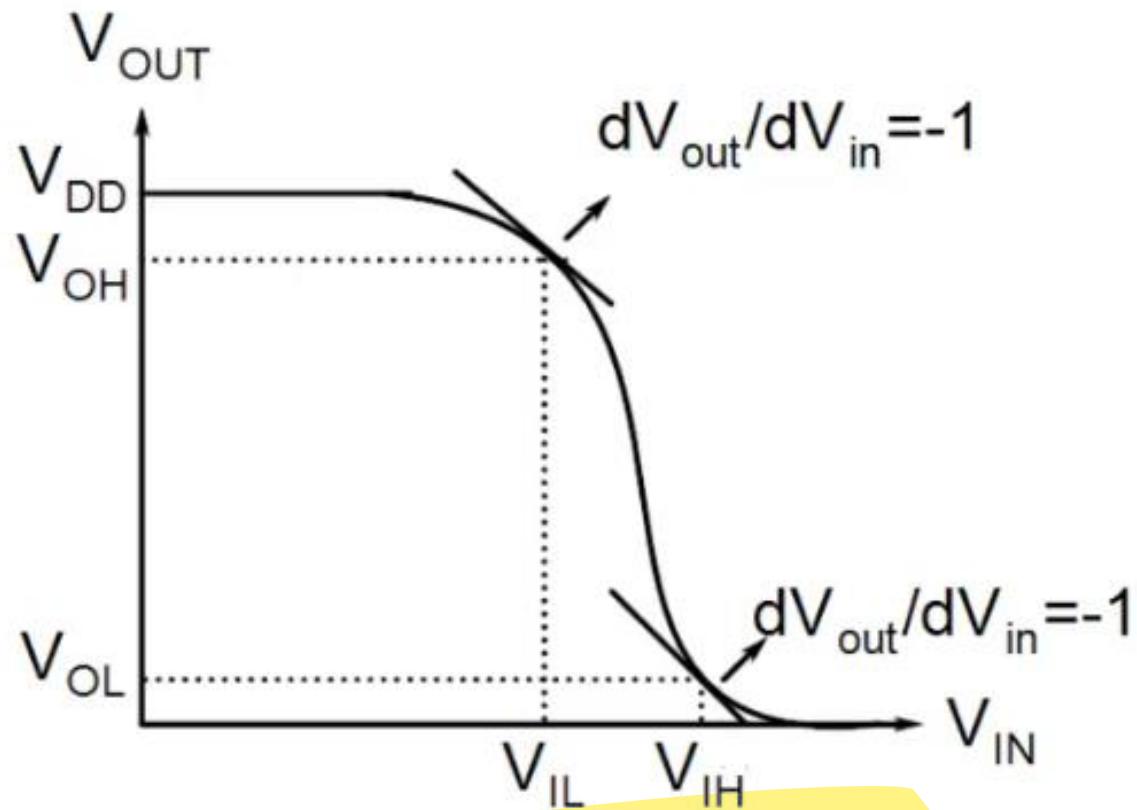
How do we find these threshold values?

Maximize $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$



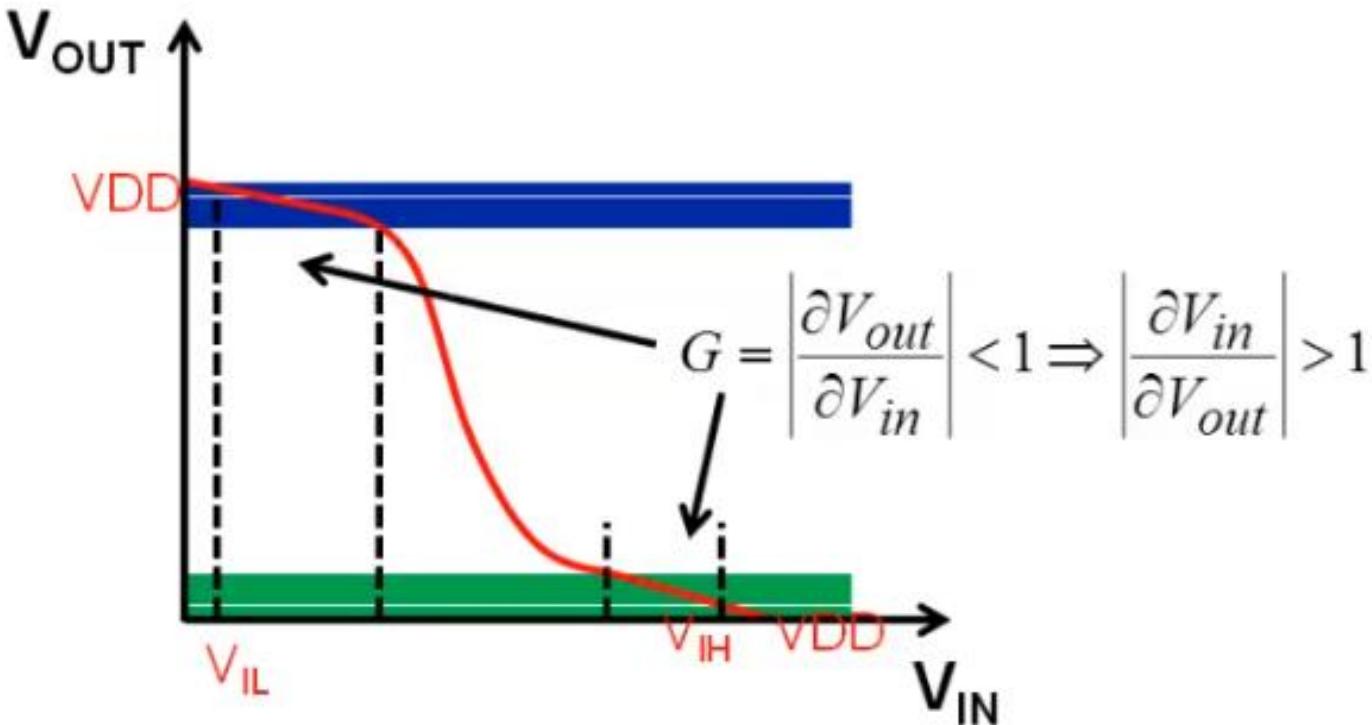
For $NM_H = NML$, find the biggest square that can be accommodated

Alternative Method For finding threshold values?



-valid high and low logic levels should be defined as bands with one determined by the unity-Gain points on VTC

How do we find these threshold values?



$$\uparrow NM_L = V_{IL} - V_{OL}$$

$$\uparrow NM_H = V_{OH} - V_{IH}$$

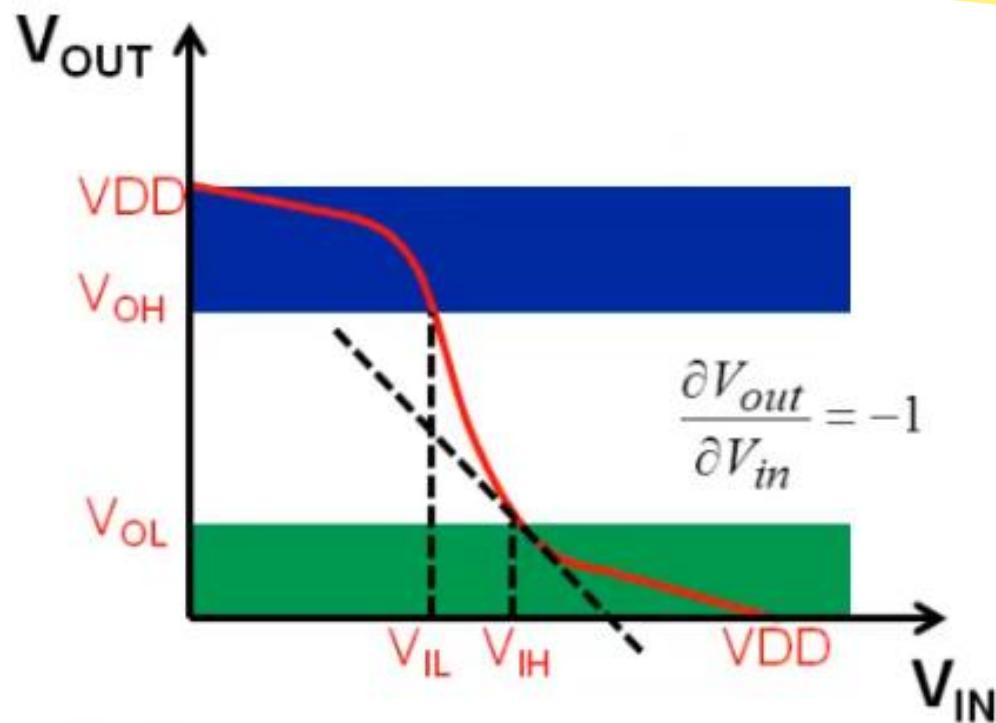
Both noise margins are very small

$$NM_L = V_{IL} - V_{OL} \quad \text{increase } \delta V_{OL} = -\delta V_{OH} \quad \Rightarrow \delta V_{IL} = -\delta V_{IH}$$

$$\delta(NM_L) = \delta V_{IL} - \delta V_{OL}$$

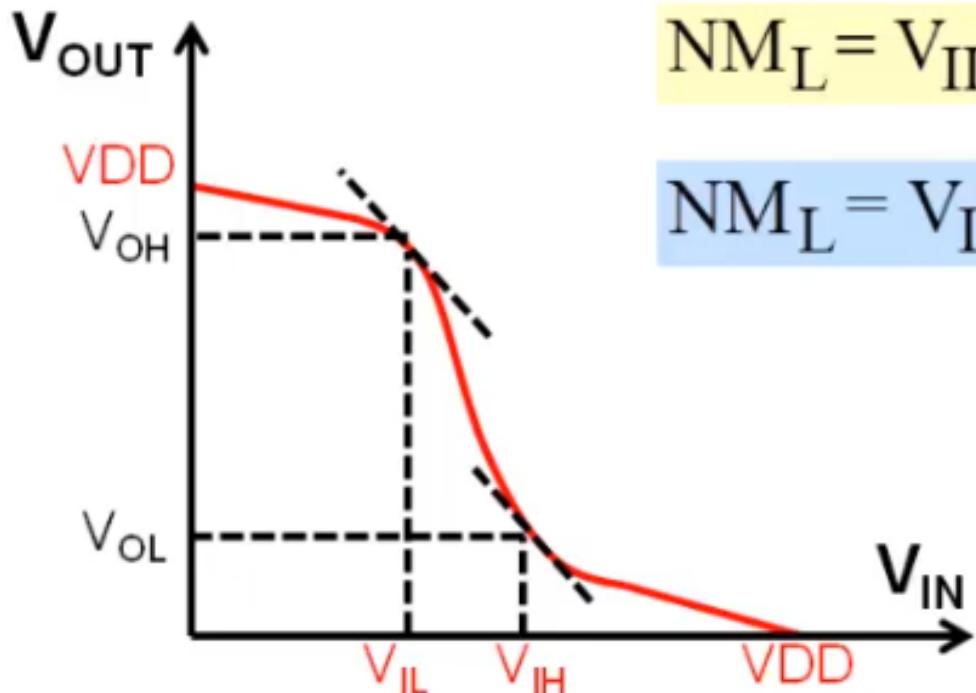
$$\delta(NM_L) = \left(\frac{\delta V_{IL}}{\delta V_{OL}} - 1 \right) \times \delta V_{OL}$$

$$\frac{\delta(NM_L)}{\delta V_{OL}} = \begin{pmatrix} 1 \\ -\frac{\delta V_{OL}}{\delta V_{IH}} - 1 \end{pmatrix}$$



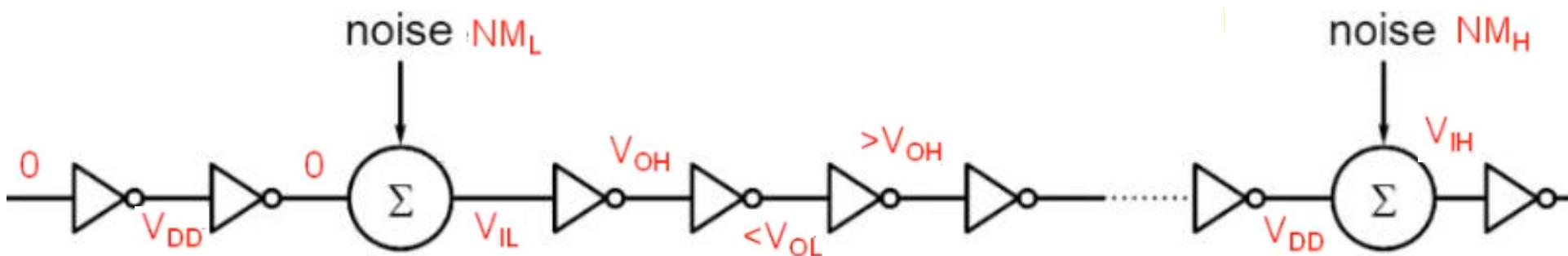
As long as $-\frac{\partial V_{out}}{\partial V_{in}} < 1$ NM_L improves

Noise Margins: Alternative definition

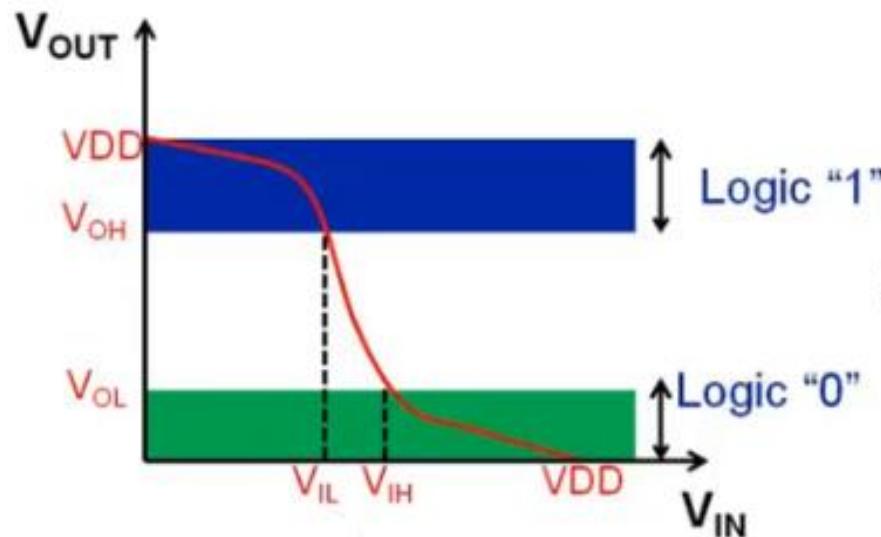


$$NM_H = V_{OH} - V_{IH}$$

$$NM_H = V_{DD} - V_{IH}$$

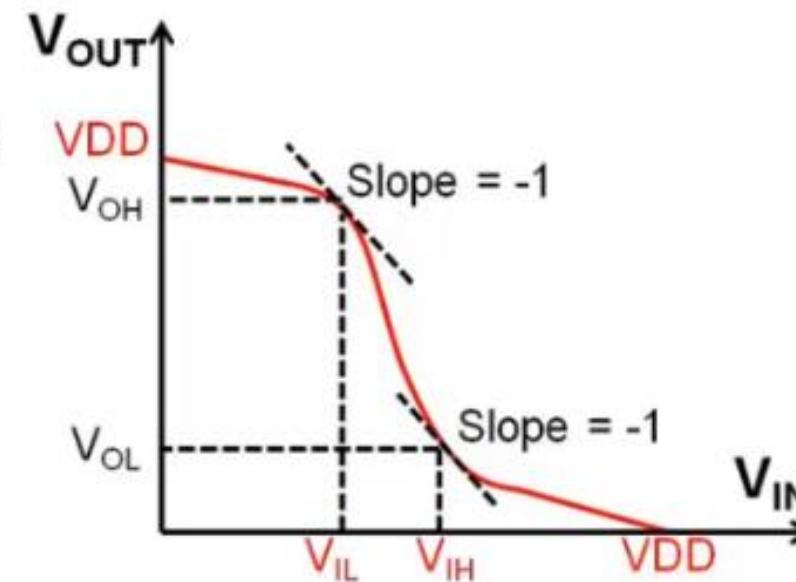
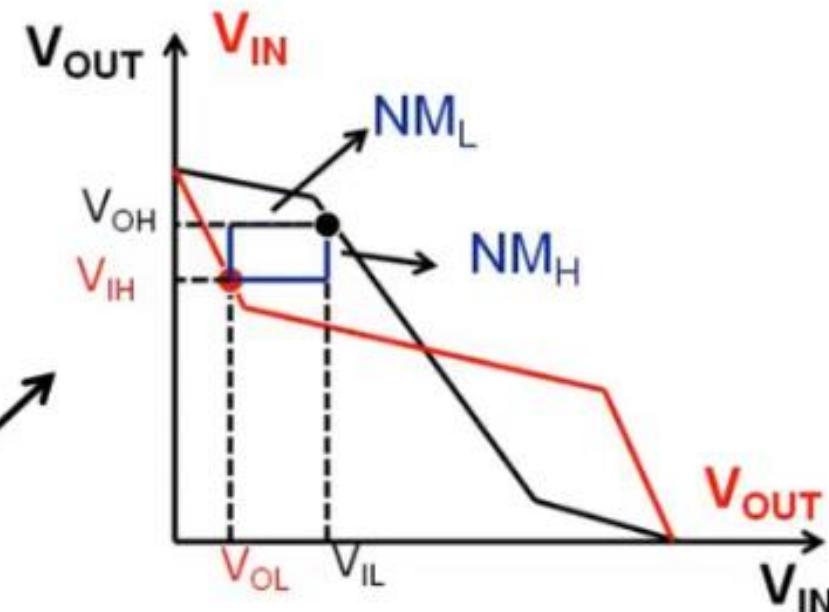


Noise Margin: Summary



$$NM_L = V_{IL} - V_{OL}$$

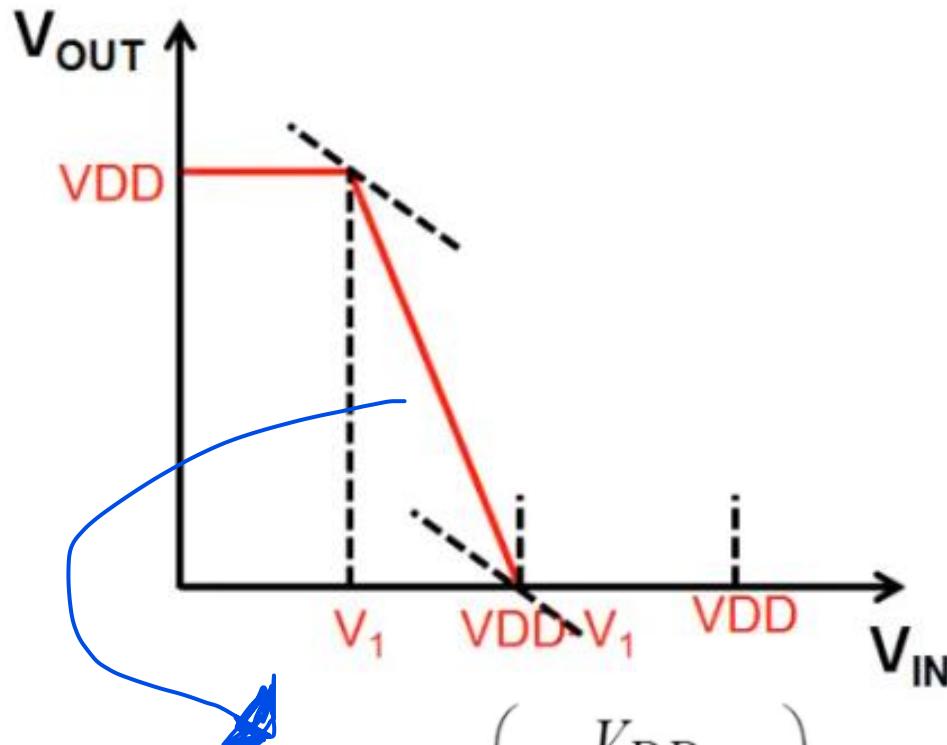
$$NM_H = V_{OH} - V_{IH}$$



Example-1

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$



$$G_{max} = \left(\frac{V_{DD}}{V_{DD} - 2V_1} \right)$$

G_{max} is the gain of this region

noise margin here

maximum possible margin

$$V_{OH} = V_{DD}; V_{IL} = V_1$$

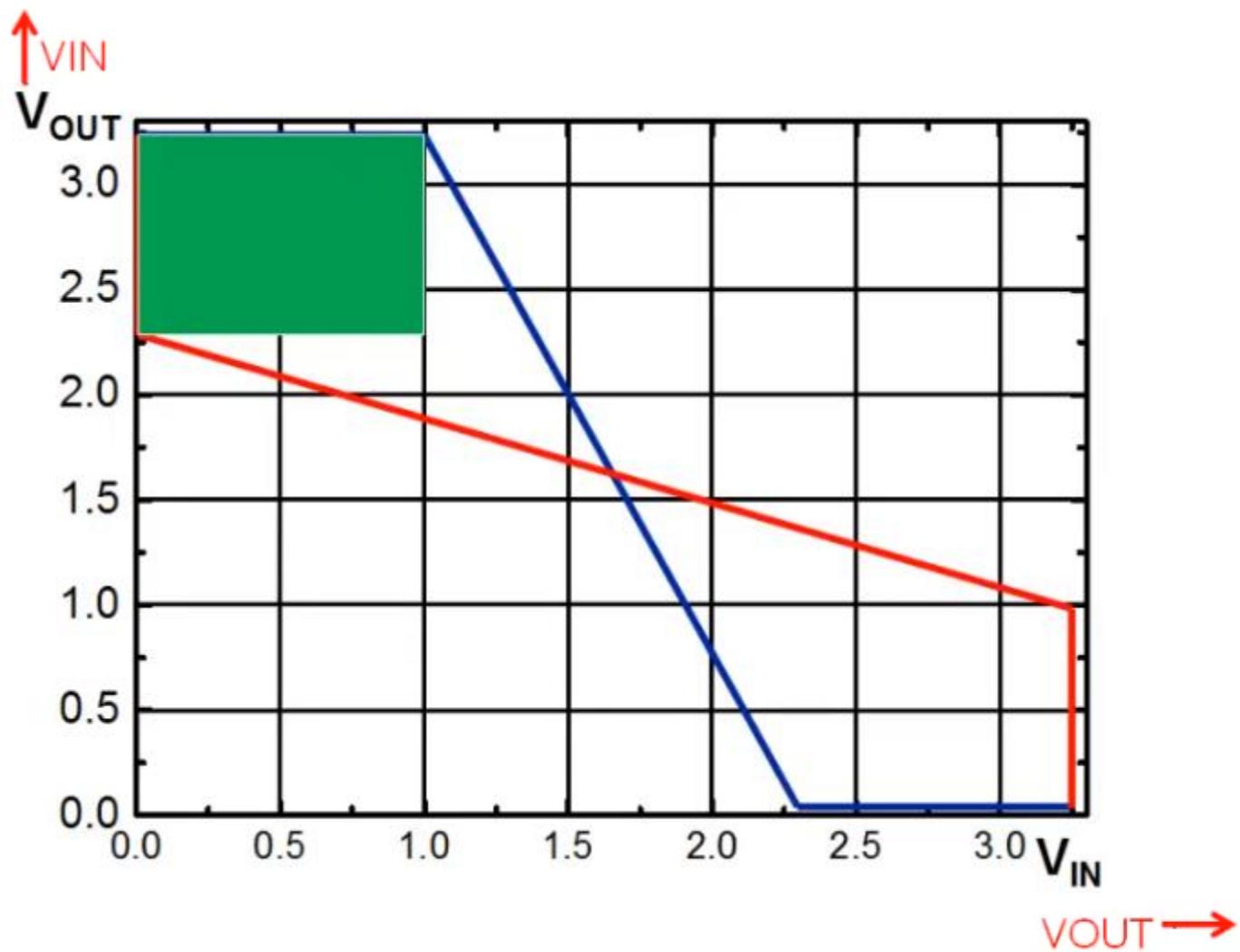
$$V_{OL} = 0; V_{IH} = V_{DD} - V_1$$

$$NM_H = NM_L = V_1$$

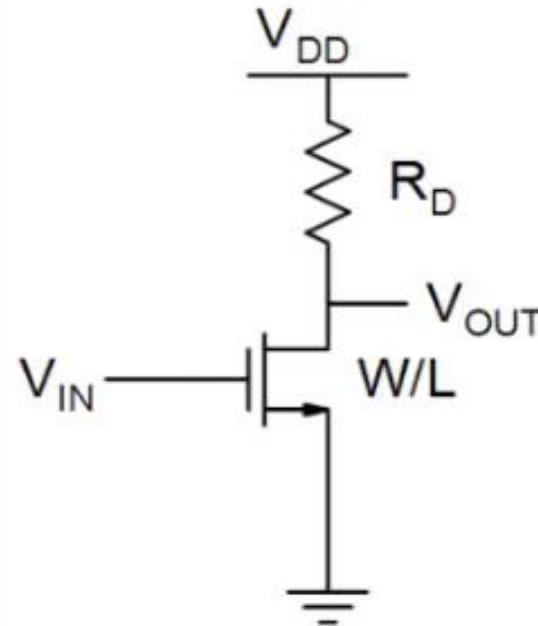
$$\frac{V_1}{V_{DD}} = 0.5 \left(1 - \frac{1}{G_{max}} \right)$$

$$\frac{NM_H}{0.5V_{DD}} = \left(1 - \frac{1}{G_{max}} \right)$$

more the G_{max} , more noise margin the system has in this case



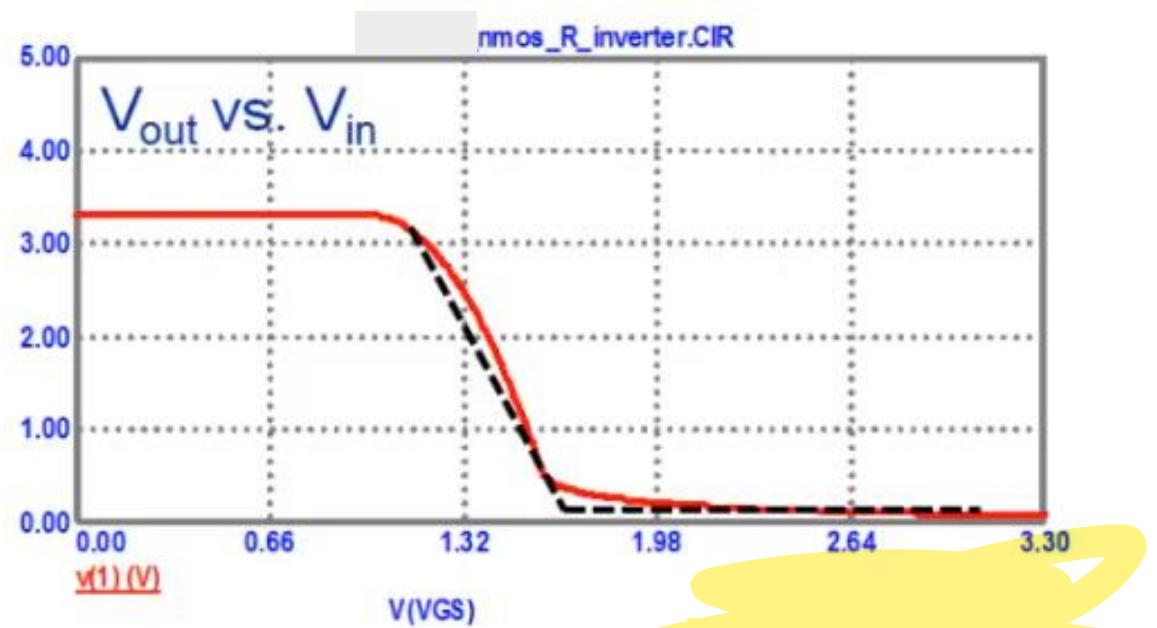
Inverter with Resistive Load



1. Area
2. Delay
3. Power
4. Noise Margins

$$V_{DD} = 3.3V$$

$$KP_N = 100 \mu A/V^2; V_{THN} = 1V$$



Step 1. $V_{OH} = V_{DD}; V_{OL} > 0$

Step 2.

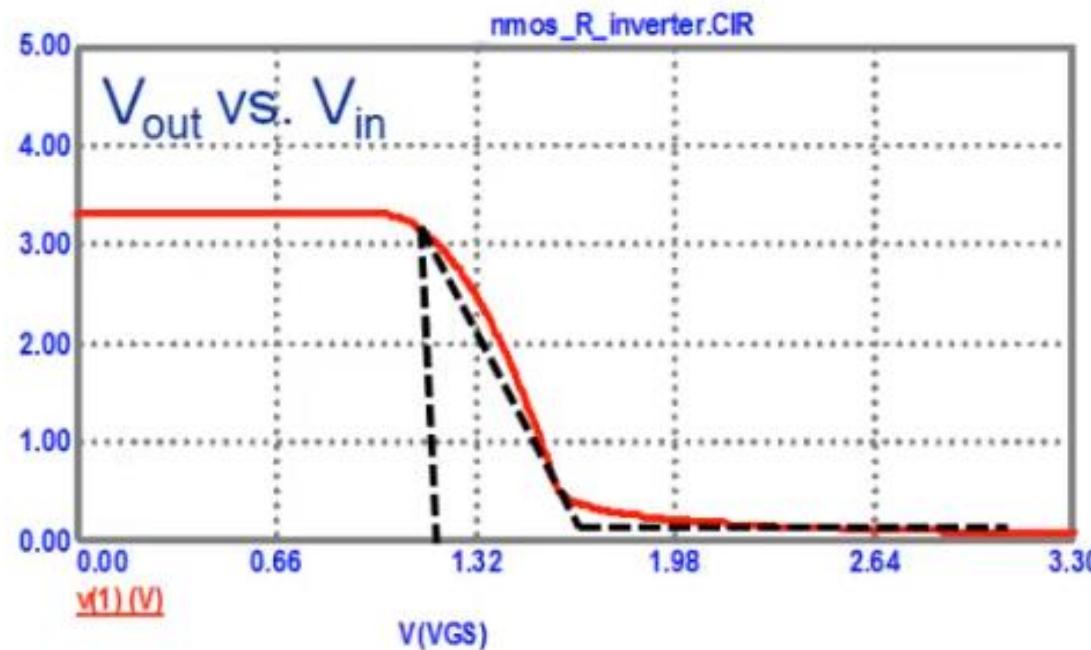
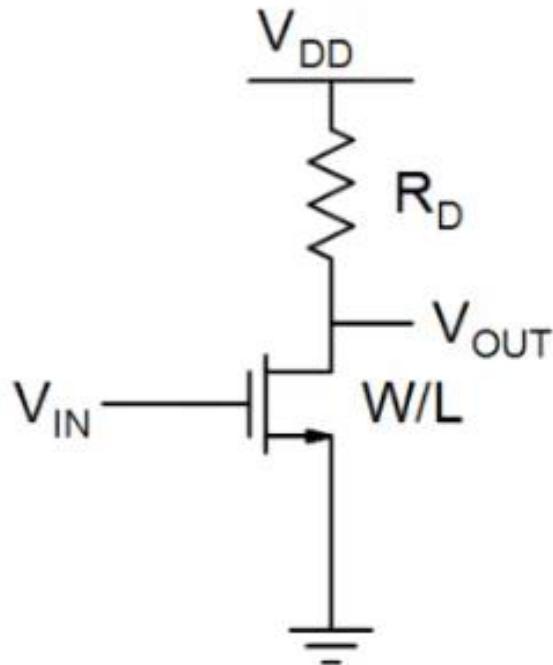
$$I_{DS} \approx \frac{V_{DD}}{R_D} \approx \beta_N \times (V_{DD} - V_{THN}) \times V_{OL}$$

Assumptions: $V_{DD}-V_{OL}$ is approx V_{DD} only
 V_{OL}^2 is neglected

$$\Rightarrow V_{OL} = \left(\frac{V_{DD}}{V_{DD} - V_{THN}} \right) \times \frac{1}{KP_N} \times \frac{1}{(W/L) \times R_D}$$

$$W/L = 4\lambda/2\lambda; R_D = 72k \Rightarrow V_{OL} \sim 0.1V$$

Inverter with Resistive Load



$$K_P N = 100 \mu A / V^2; V_{THN} = 1V$$

$$V_{DD} = 3.3V$$

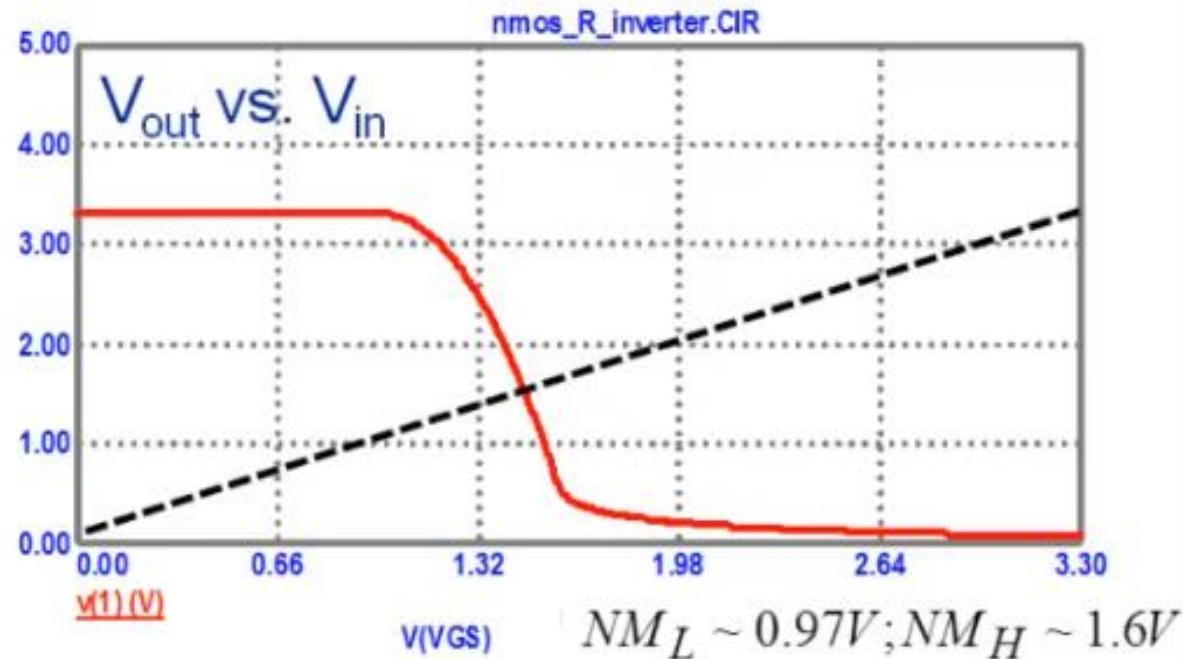
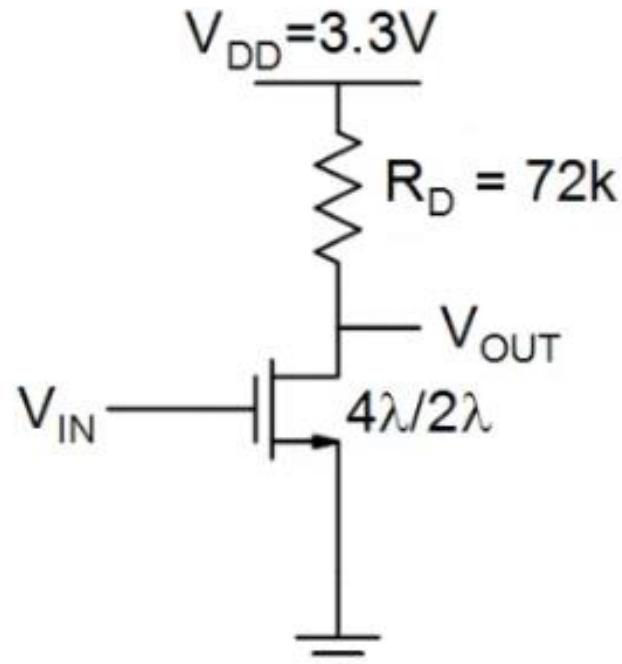
$$\frac{\partial V_{out}}{\partial V_{in}} = -1 \quad \rightarrow \quad V_{IL} \sim 1.07V$$

$$V_{IL} \sim V_{THN} = 1V$$

$$NM_L = V_{IL} - V_{OL} \sim 0.97V$$

$$\frac{NM_L}{0.5V_{DD}} = \frac{0.97}{1.65} = 0.59$$

$$V_{IH} \sim 1.7 \Rightarrow NM_H = V_{DD} - V_{IH} \sim 1.6V$$



$$V_{out} = V_{in}$$

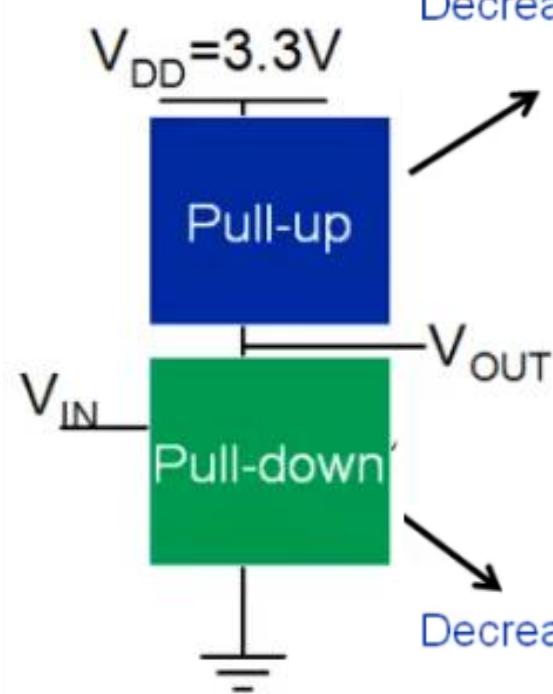
Transistor in saturation

$$I_{DS} = \left(K_P N \times \frac{W}{L} \right) \times \frac{(V_{out} - V_{THN})^2}{2} = \frac{V_{DD} - V_{out}}{R_D}$$

For $R_D = 72k$, $V_{out} = V_{in} = V_{inv} = 1.5V$

Shift characteristics to right to improve NM_L

1. Decrease R_D
2. Decrease W/L



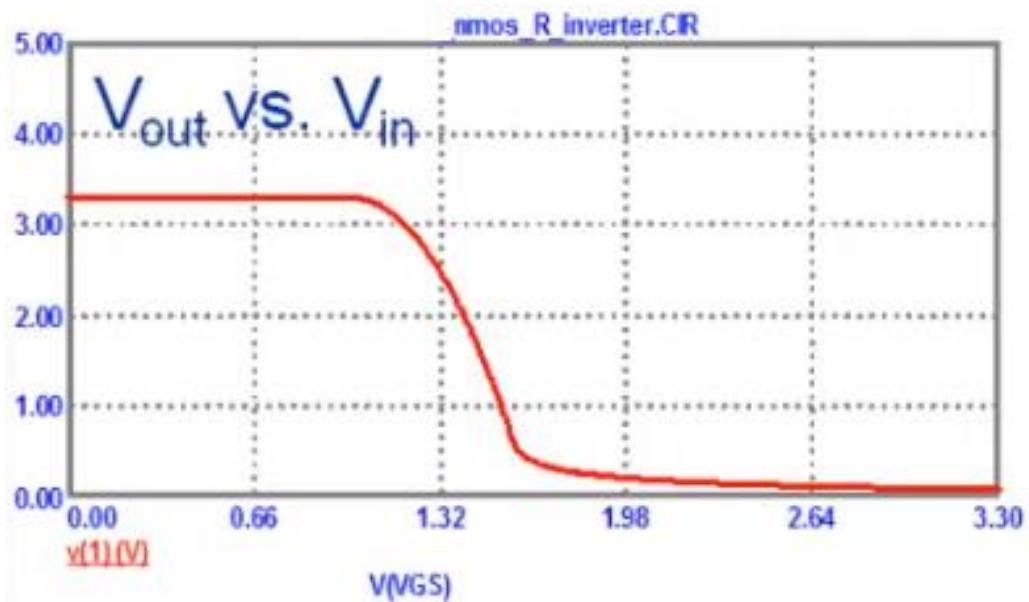
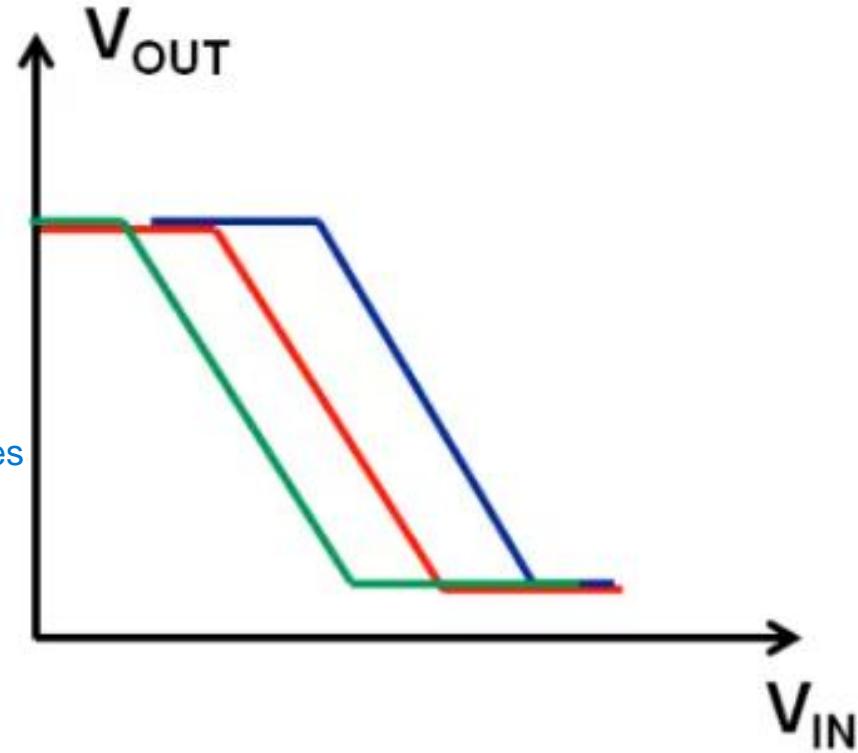
Decrease pull-up resistance

in a MOSFET, when you decrease W/L, Id decreases that means the resistance of the MOSFET increases.

To shift characteristics to the right:

1. decrease pull up resistance: so that effect of pull up block is more and it keeps the VTC close to VDD for longer time and thus shifting VTC to right
2. increase pull down resistance: so that pull down effect decreases and VTC takes longer time to reach GND thus shifting VTC to the right.

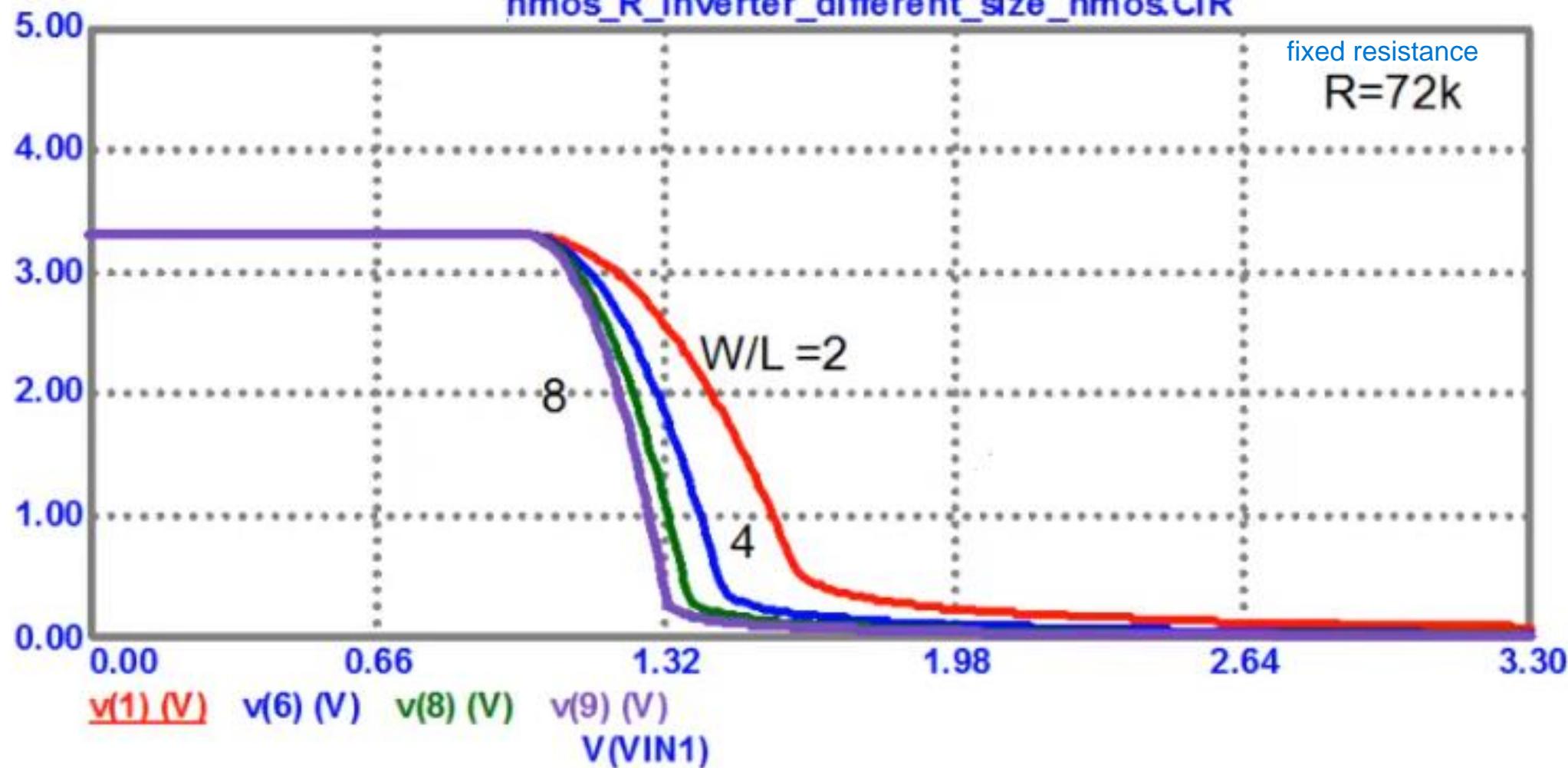
Decrease pull-down resistance



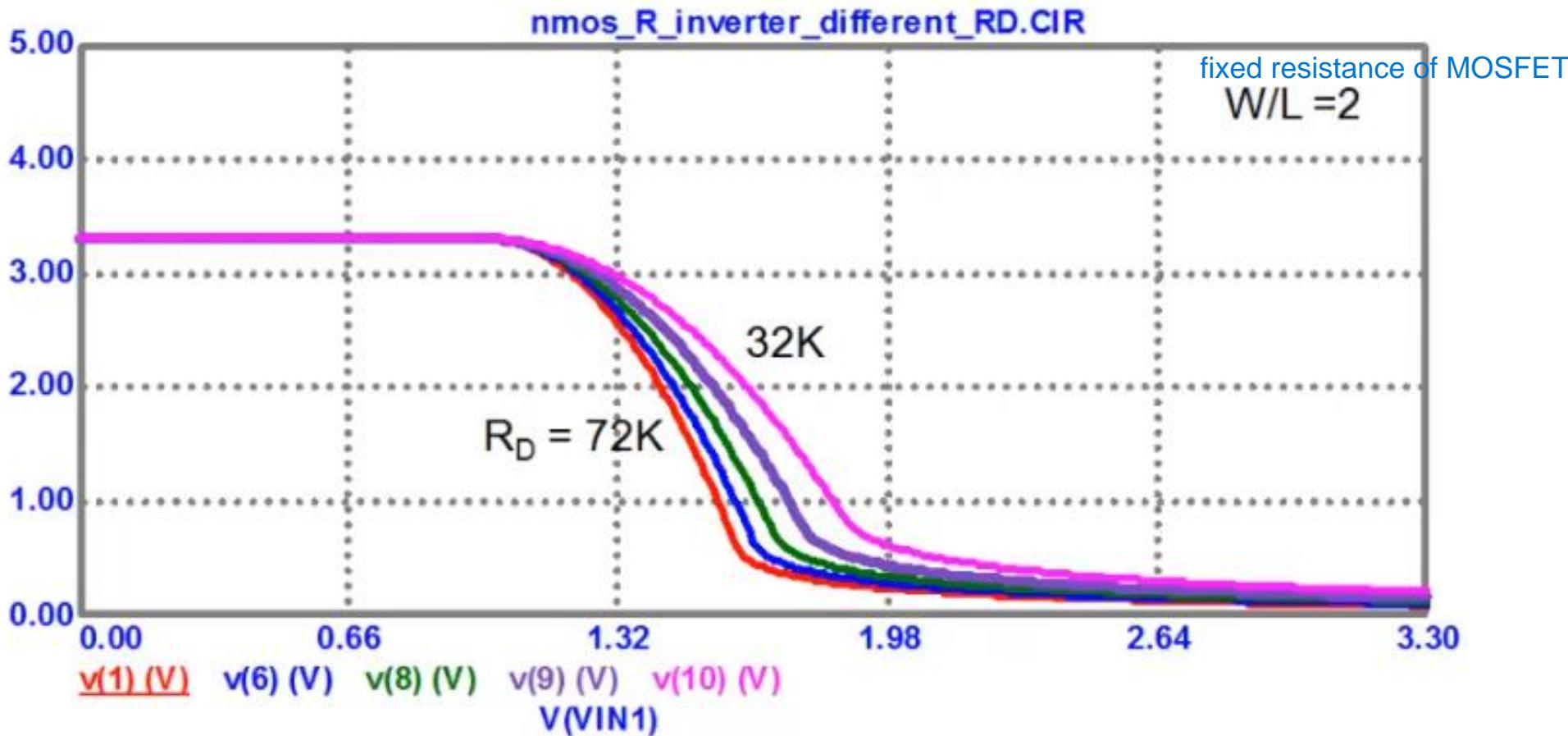
Shift characteristics to right to improve NM_L

1. Decrease R_D
2. Decrease W/L

nmos_R_inverter_different_size_nmos.CIR



Decreasing the pull down resistor shifts characteristics left



$$R_D = 72k \Rightarrow V_{OL} = 0.1V; V_{OH} = 3.3V$$

$$V_{IL} = 1.07V; V_{IH} = 1.7V$$

$$NM_L \sim 0.97V; NM_H \sim 1.6V$$

$$V_{inv} = 1.5V$$

$$R_D = 32k \Rightarrow V_{OL} = 0.22V; V_{OH} = 3.3V$$

$$V_{IL} = 1.16V; V_{IH} = 2V$$

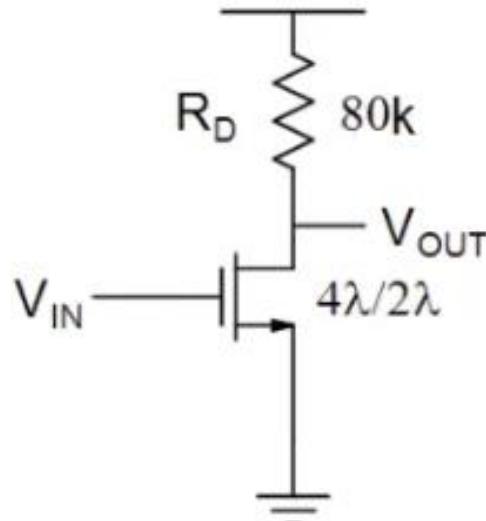
$$NM_L \sim 0.94V; NM_H \sim 1.3V$$

$$V_{inv} = 1.72V$$

here NML did not increase so NMH decrease doesn't really matter but at least size decreased when we went from 72k to 32k

$$V_{DD} = 3.3V$$

$$NM_L \sim 0.97V; NM_H \sim 1.6V$$

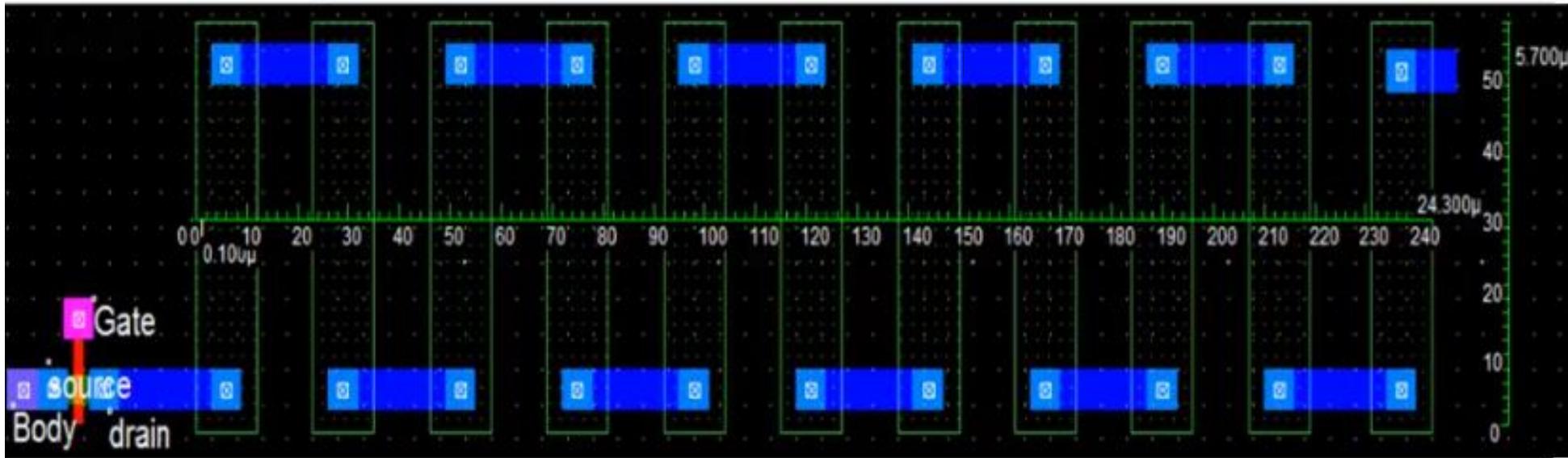


$$R_D = 10k$$

$$W/L = 4\lambda/2\lambda; R_D = 10k \Rightarrow V_{OL} \sim 0.72V$$

$$NM_L = V_{IL} - V_{OL} \sim 0.28V$$

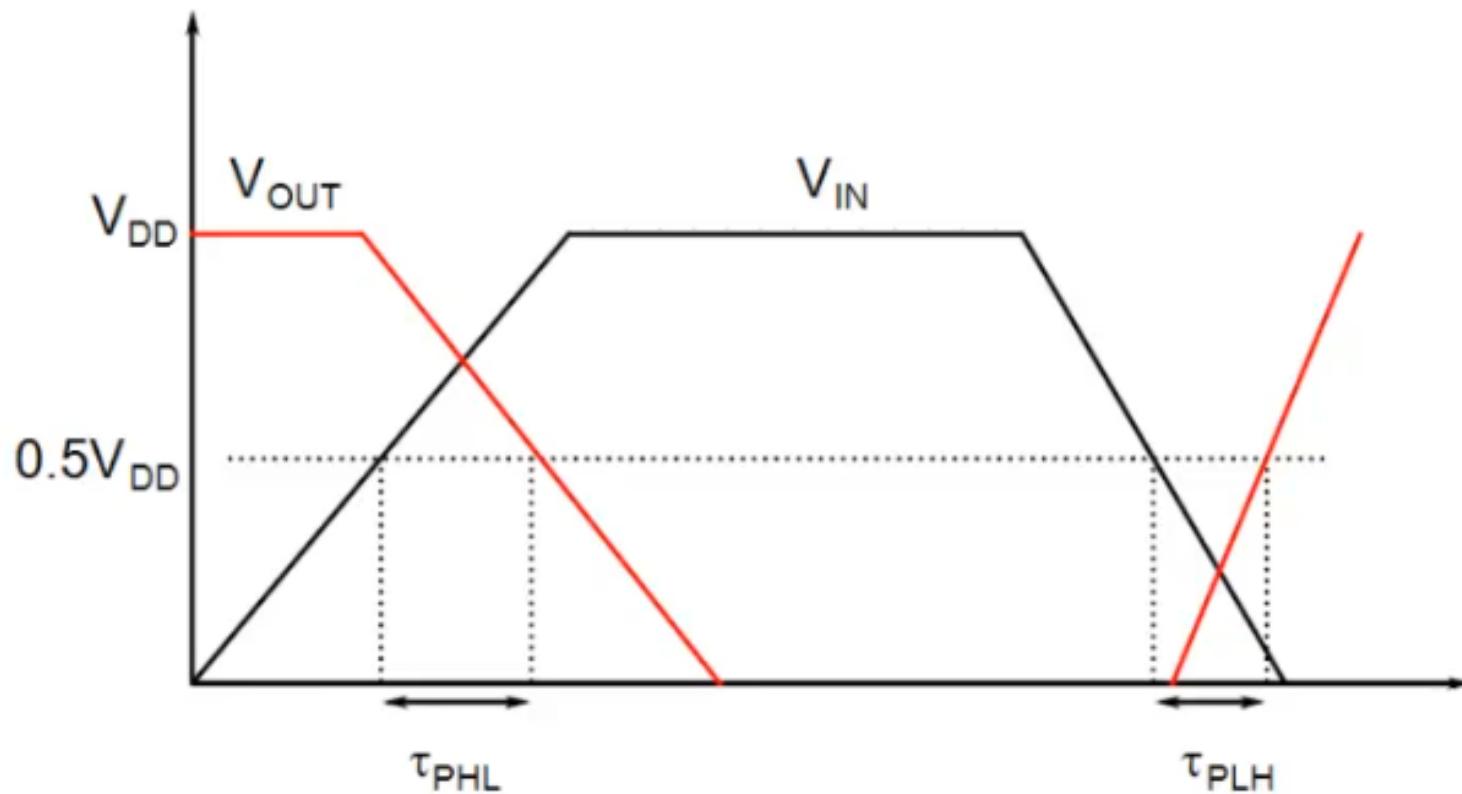
1. Area
2. Delay
3. Power
4. Noise Margins



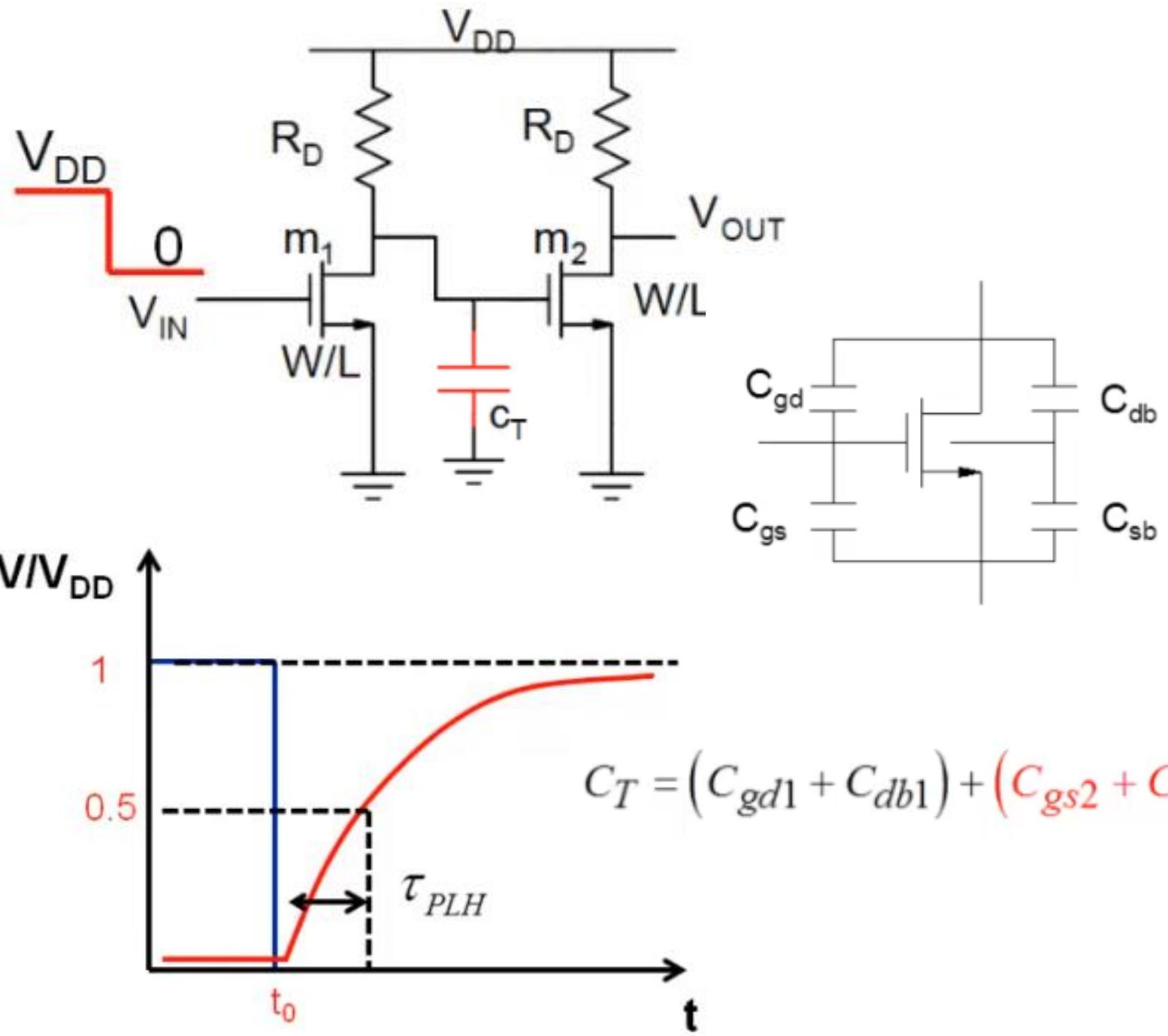
$$\frac{A_{RD}}{A_{tr1}} \sim 35$$

area of 72k Ohm resistance is aprx 35 times the area of the transistor.
so reducing the value of the resistance decreases the area occupied by a lot.

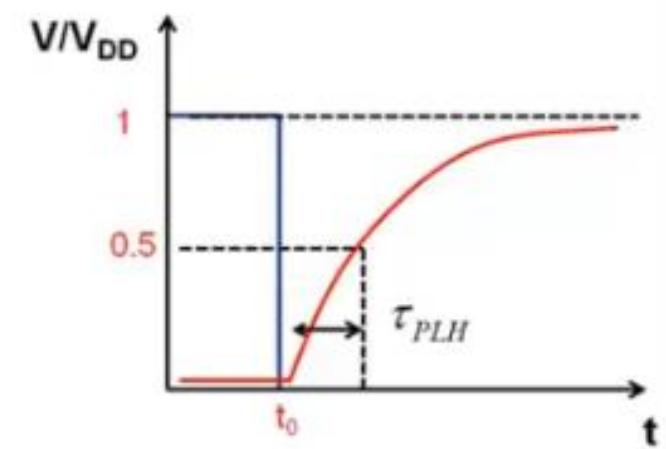
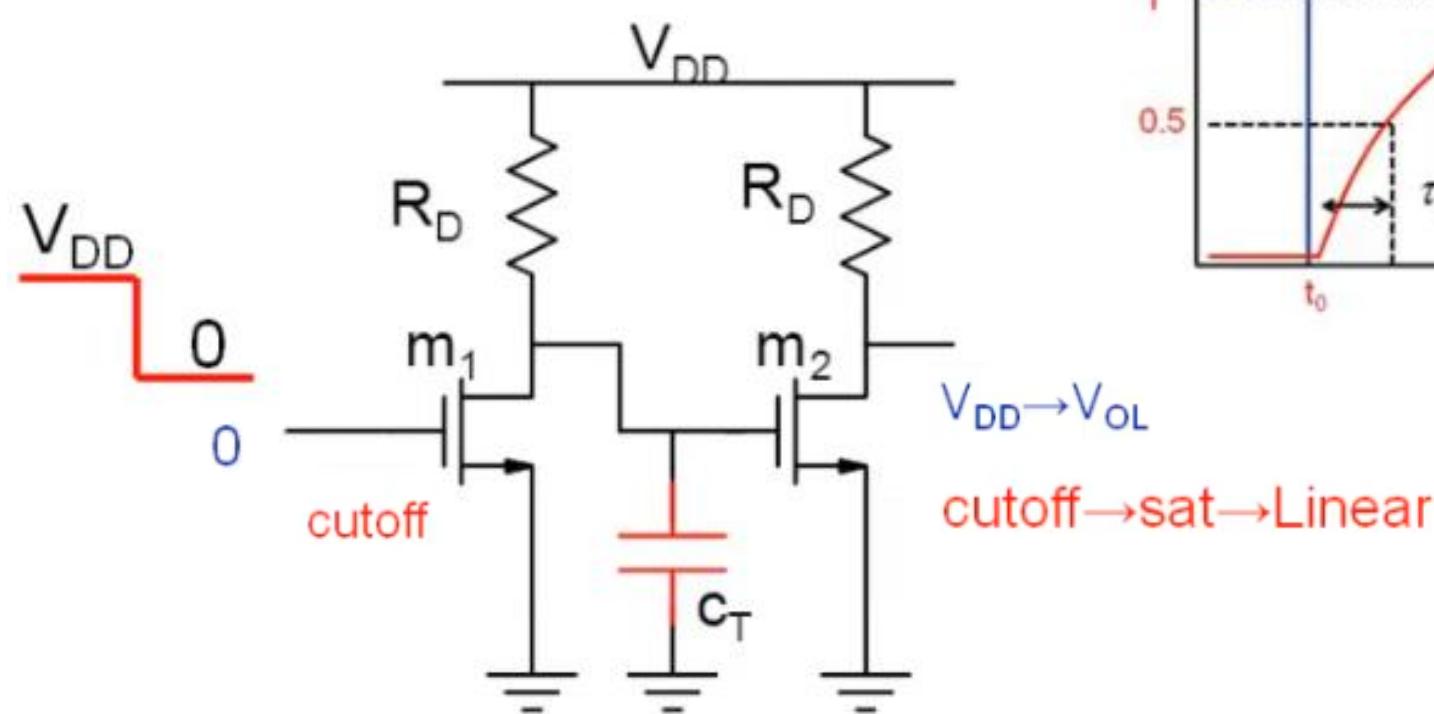
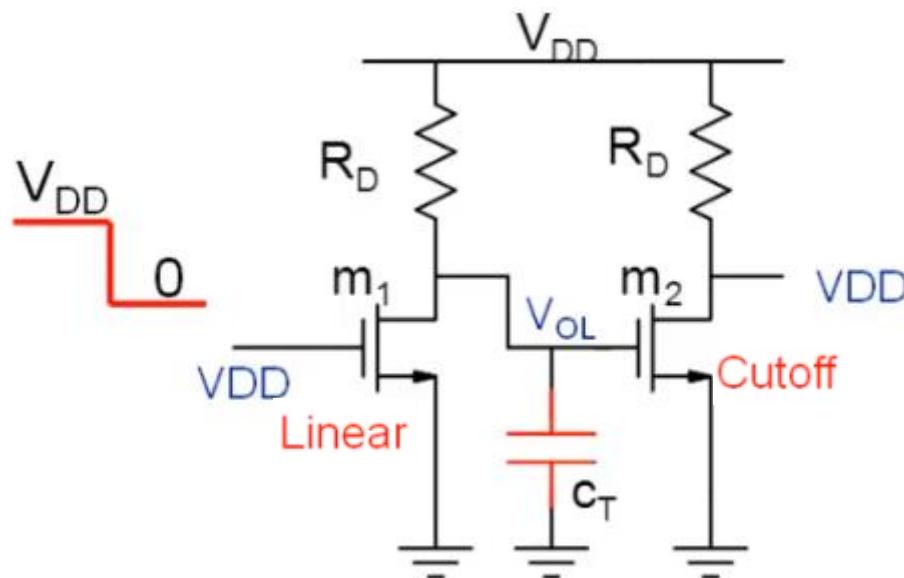
Propagation Delay

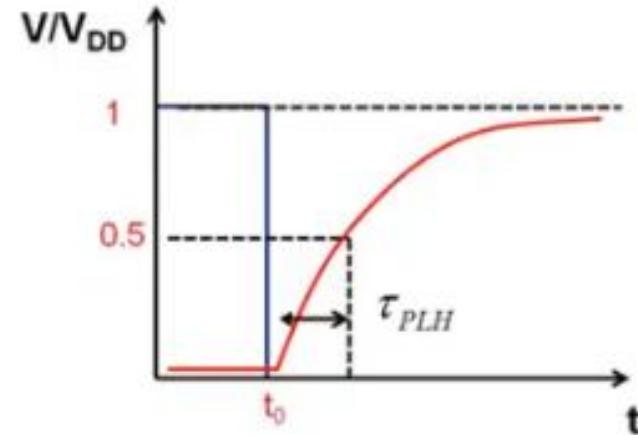
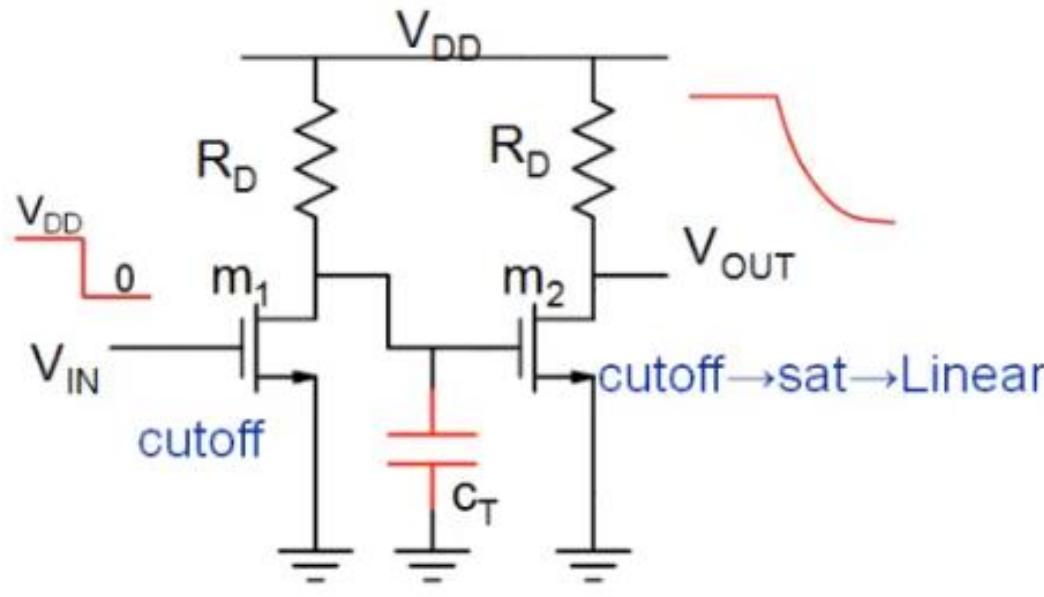


$$\tau_R ; \tau_F ; \tau_{PHL} ; \tau_{PLH}$$



Parameter	NMOS	PMOS
$V_{THNO}(V)$	0.69	-0.869
λ (for $L = 1\mu m$)	0.015	0.065
γ	0.696	0.456
$K_P(\mu A/V^2)$	100	40
$CGSO(pF)$	281	252
$CGDO(pF/m)$	281	252
$CJ(\mu F/m^2)$	467.7	932
PB	0.9	0.92
MJ	0.5	0.466
$CJSW(pF/m)$	616.95	181
$MJSW$	0.235	0.5



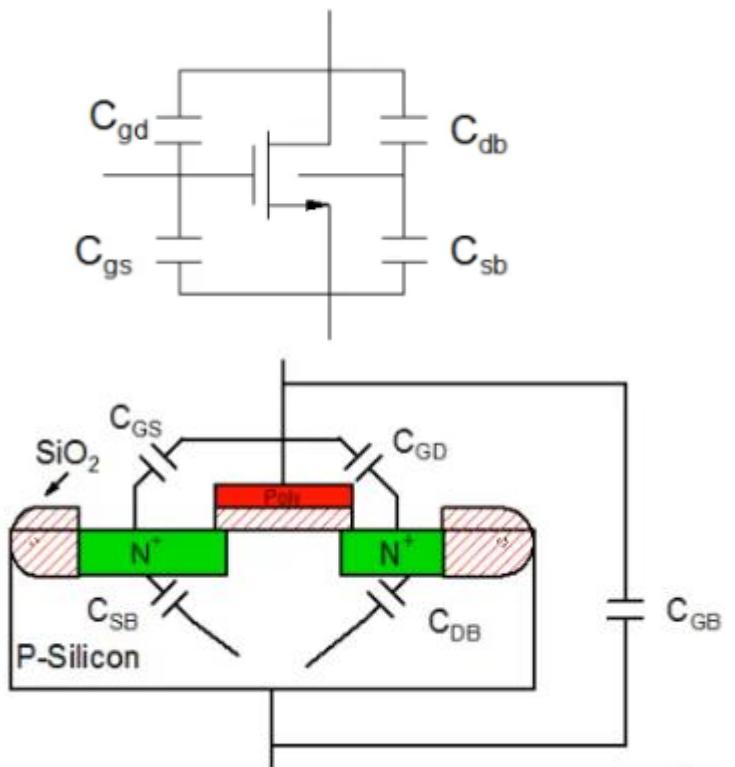


$$C_T = (C_{gd1} + C_{db1}) + (C_{gs2} + C_{gd2})$$

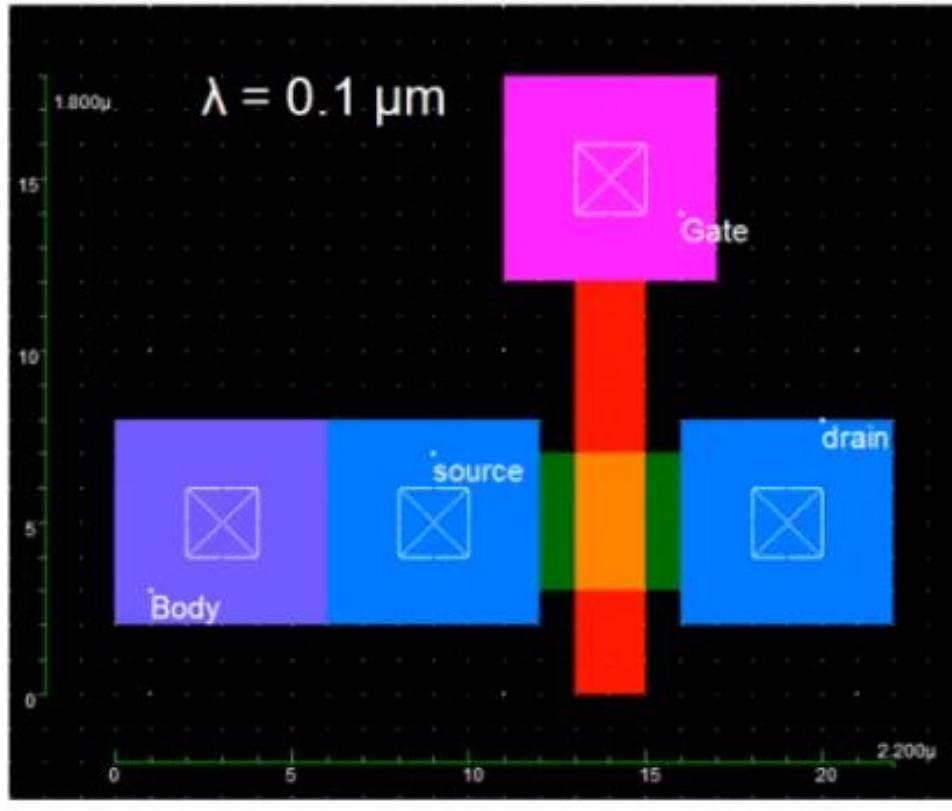
$$C_{gd1} = C_{GDO} \cdot W_1 \quad C_{gd2} = C_{GDO} \cdot W_2$$

$$C_{db1} = \frac{C_{jsw} \cdot P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j \cdot A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}}$$

$V_{DB} = 0 \rightarrow 0.5VDD$



$$C_{gs1} \approx (C_{gso} \cdot W) \rightarrow \frac{2}{3} C_{ox'} \cdot W \cdot L + C_{gso} \cdot W$$



$$A_D = 4 \times 1 + 6 \times 6 = 40;$$

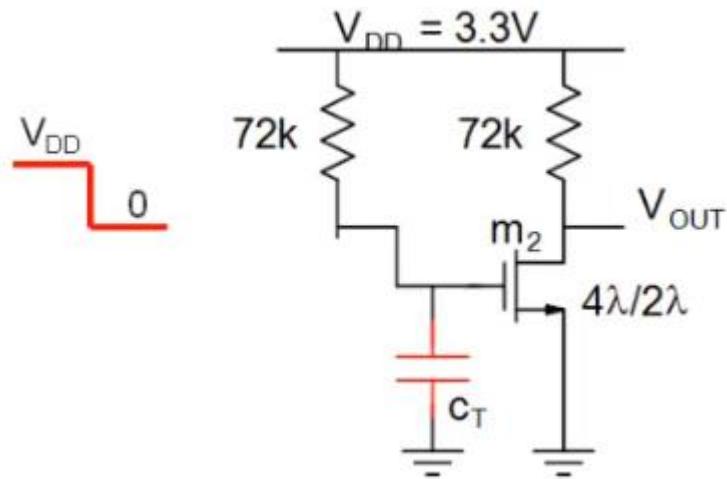
$$P_D = 2 \times (1 + 1 + 6) + 6 = 22$$

$$V_{DB} = 0$$

$$C_{db1} = \frac{C_{jsw} \cdot P_D}{\left(1 + \frac{V_{DB}}{P_{BSW}}\right)^{M_{jsw}}} + \frac{C_j \cdot A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}} = 5.7 \text{ fF}$$

$\sim 4 \text{ fF}$

1.7 fF

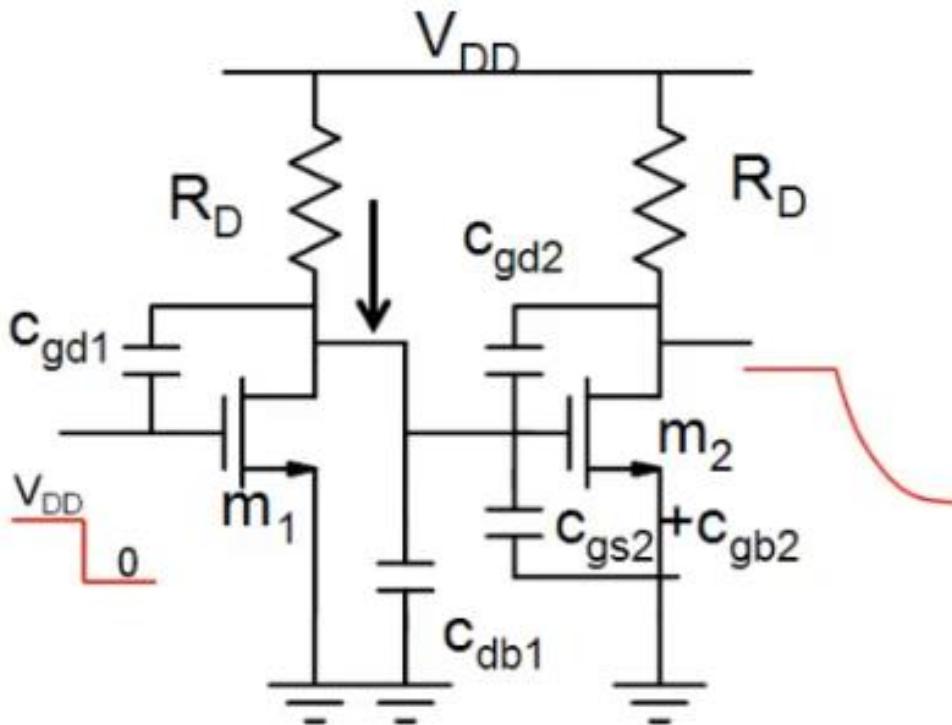


$$C_T = (C_{gd1} + C_{db1}) + (C_{gs2} + C_{gd2})$$

$$C_{To} = 8.5 \text{ fF}$$

$$\begin{aligned}\tau_{PLH} &\cong 0.693 \times R_D \times \tilde{C}_T \\ &= 424 \text{ ps}\end{aligned}$$

$\tau_{PLH} \cong 137 \text{ ps}$ if C_{db} is not considered



M1 : linear \rightarrow cutoff

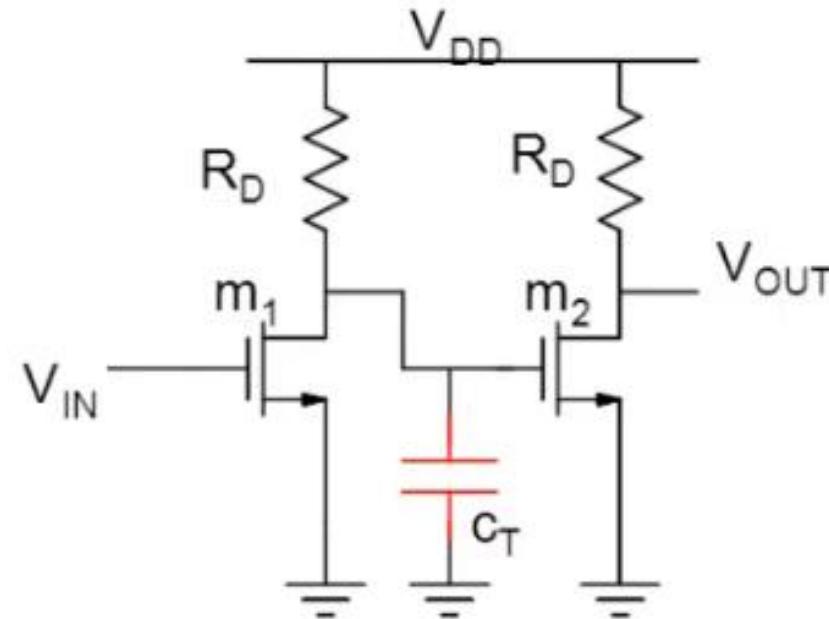
$$C_T = (C_{gd1} + C_{db1}) + (C_{gs2} + C_{gd2} + C_{gb2})$$

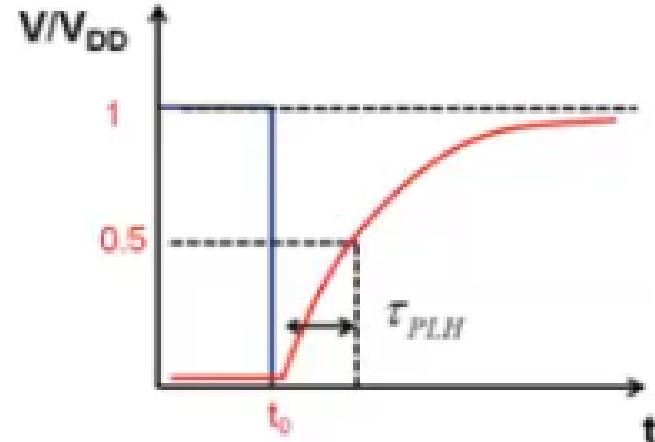
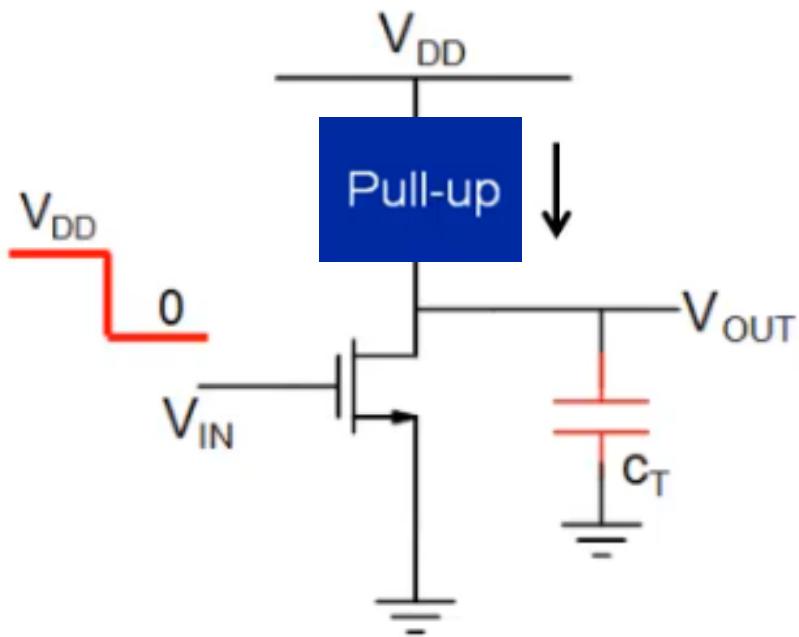
M2: cutoff \rightarrow sat \rightarrow Linear

$$I = \sum \frac{dQ_j}{dt}$$

$$I = C_{gd1} \times \frac{d(V_{D1} - V_{G1})}{dt} + C_{gd2} \times \frac{d(V_{D1} - V_{D2})}{dt} + C_{db1} \times \frac{dV_{D1}}{dt} + (C_{gs2} + C_{gb2}) \times \frac{dV_{D1}}{dt}$$

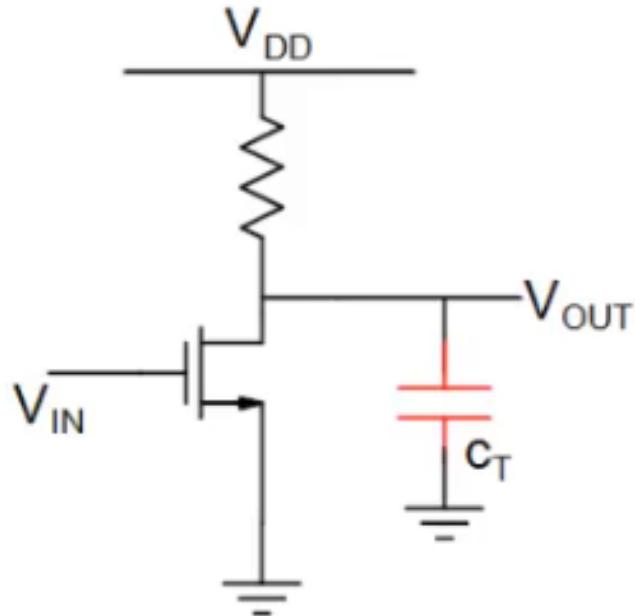
$$I = \left(C_{gd1} \times \left(1 - \frac{dV_{G1}}{dV_{D1}} \right) + C_{gd2} \times \left(1 - \frac{dV_{D2}}{dV_{D1}} \right) + C_{db1} + C_{gs2} + C_{gb2} \right) \times \frac{dV_{D1}}{dt}$$



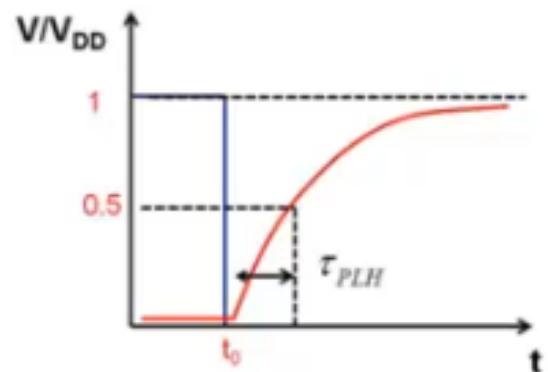


$$I_{pu} = C_T \times \frac{dV_{out}}{dt} \quad | \quad \tau_{plh} = \int_0^{0.5V_{DD}} \frac{C_T}{I_{pu}} \times dV_{out}$$

$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$



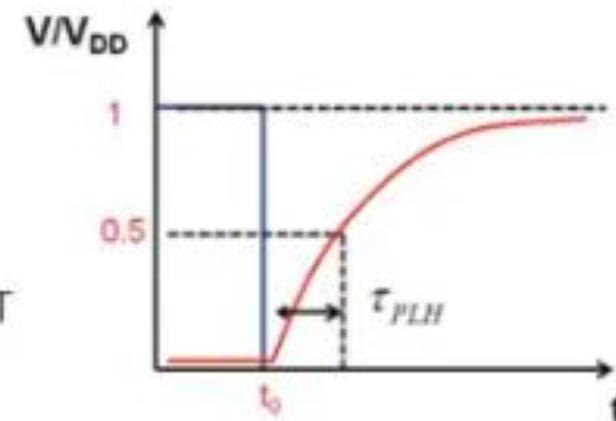
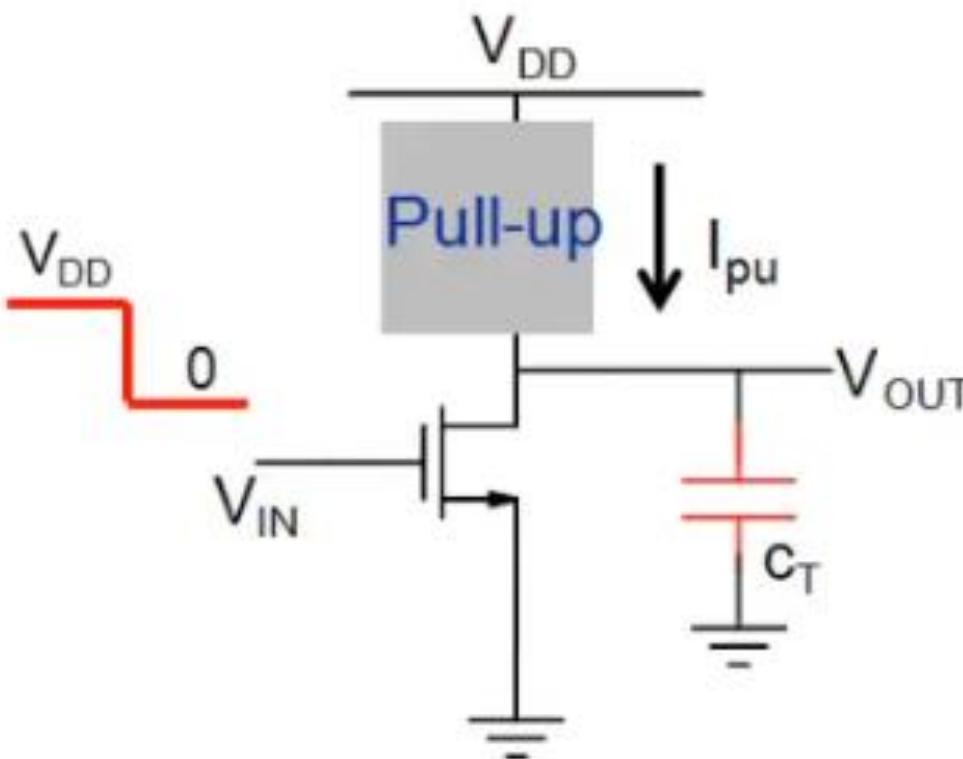
$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$



$$I_{pu} = \frac{V_{DD}}{R_D} \rightarrow \frac{0.5V_{DD}}{R_D}$$

$$\tilde{I}_{pu} \cong 0.75 \frac{V_{DD}}{R_D}$$

$$\tau_{plh} \cong 0.67 \times R_D \tilde{C}_T$$

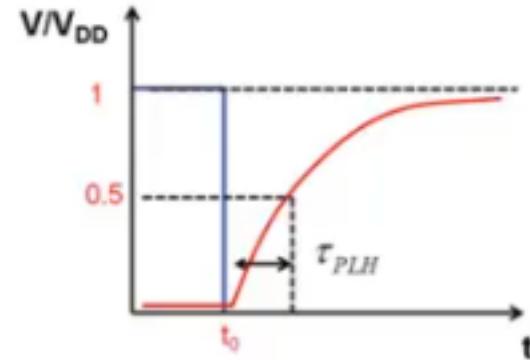
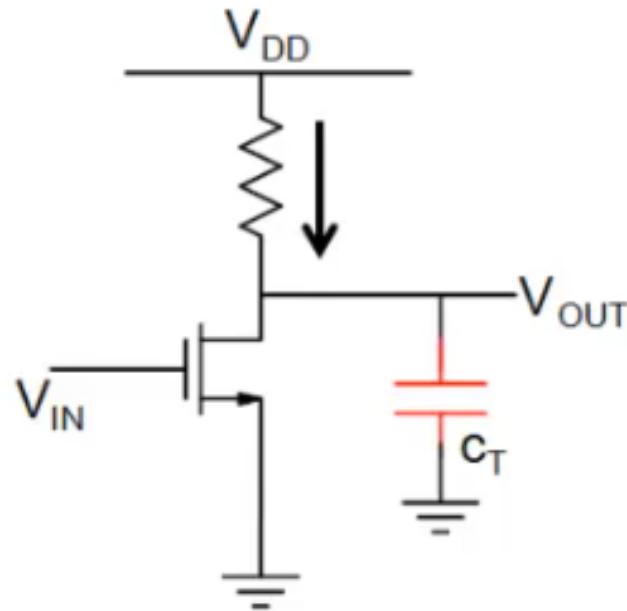


$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

$$I_{pu} \propto V_{DD}^m; m > 1 \quad P_{diss} \propto V_{DD}$$

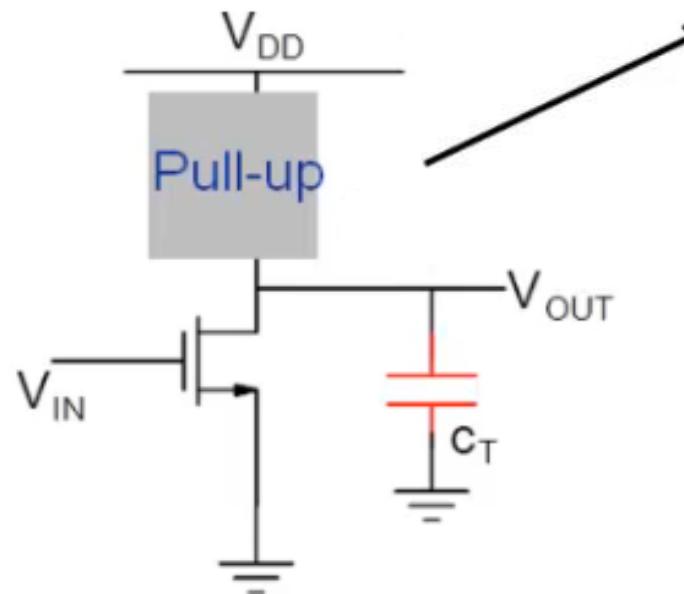
In general delay decreases with increase in supply voltage

There is a power delay tradeoff



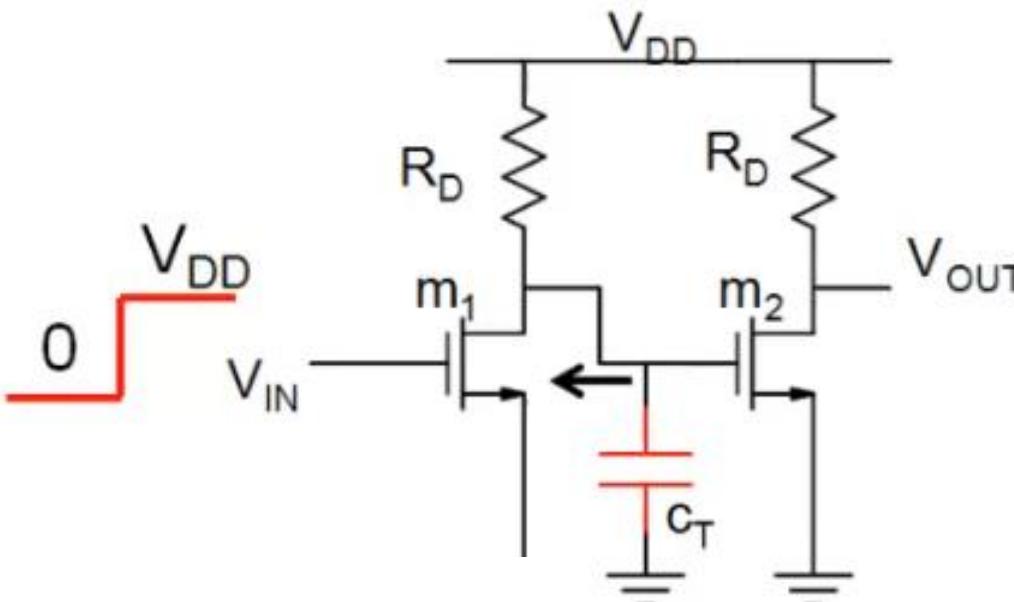
$$I_{pu} = \frac{V_{DD}}{R_D} \rightarrow \frac{0.5V_{DD}}{R_D}$$

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$



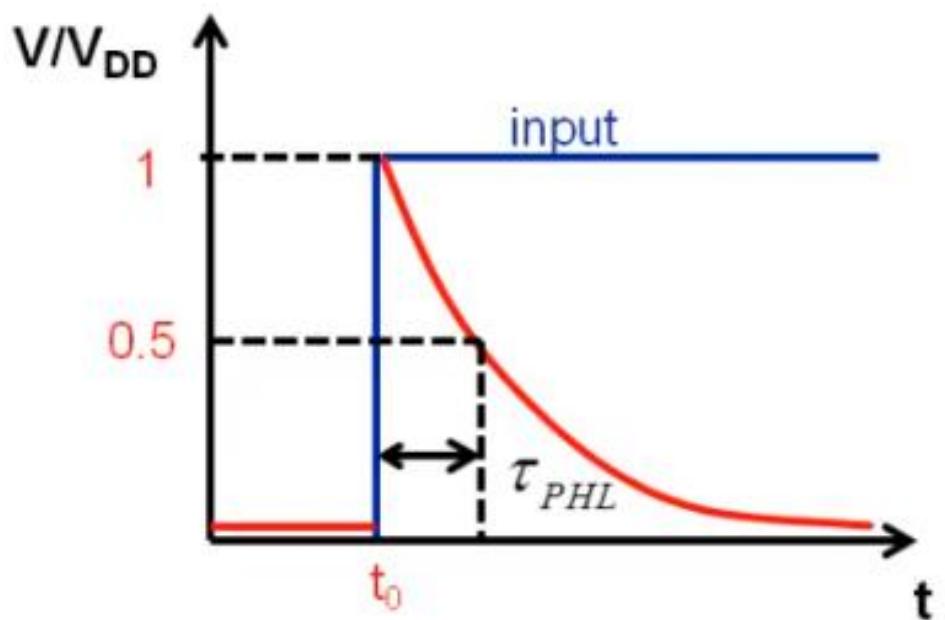
Ideally should be like a current source which switches on during charging.

High to Low delay propagation Delay



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{dis.}}$$

$$I_{dis.} = I_{DS1} - \frac{V_{DD} - V_{D1}}{R_D}$$

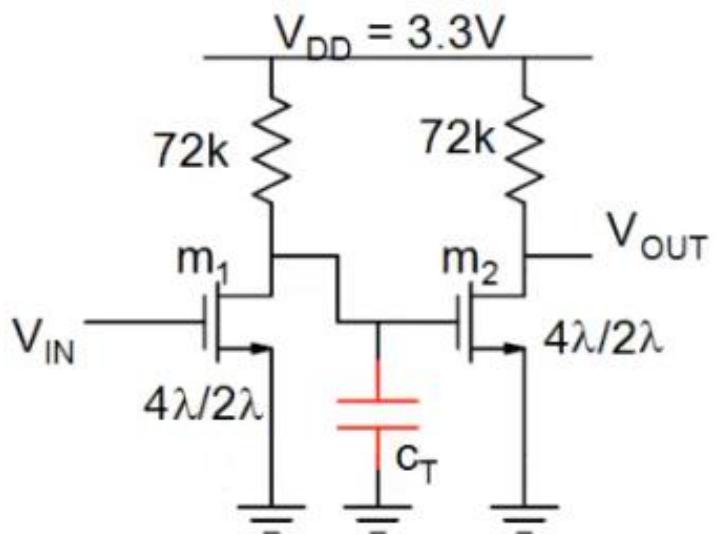


M1 : sat (3.3 → 2.3)
lin. (2.3 → 1.65)

$$I_{DS}(t=0) = \left(K_P N \times \frac{W}{L} \right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

$$I_{DS}(t=\tau_{phl}) = \left(K_P N \times \frac{W}{L} \right) \times \left((V_{DD} - V_{THN}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{4} \right) - \frac{V_{DD}}{2R_D}$$

High to Low delay propagation Delay



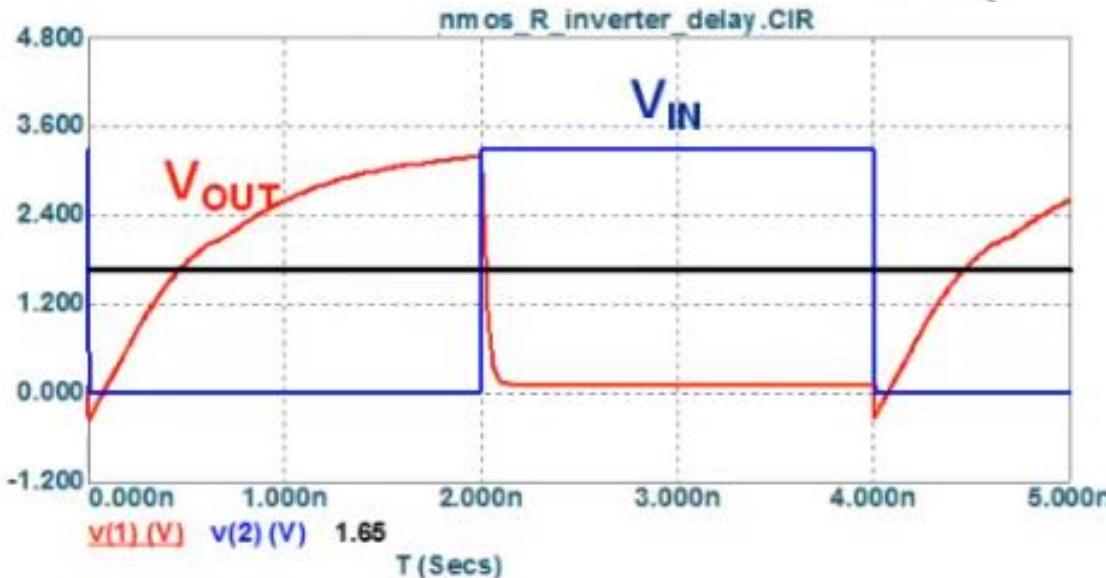
$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{dis.}} \quad \sim 39 \text{ ps}$$

$$\tau_{PLH} \cong 424 \text{ ps}$$

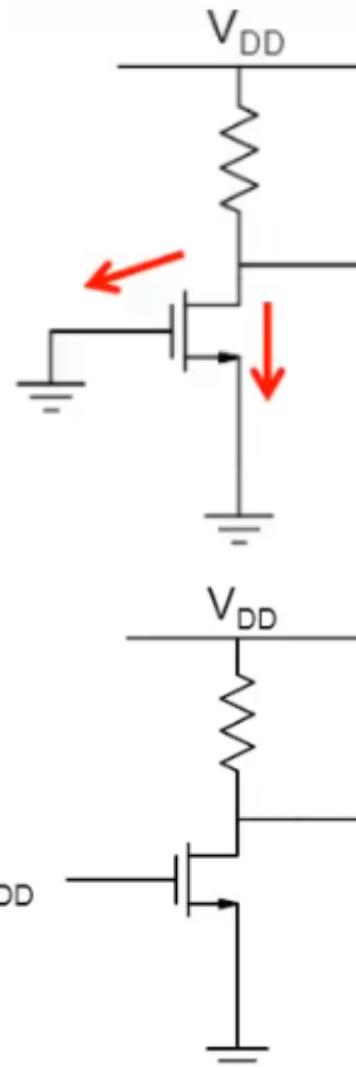
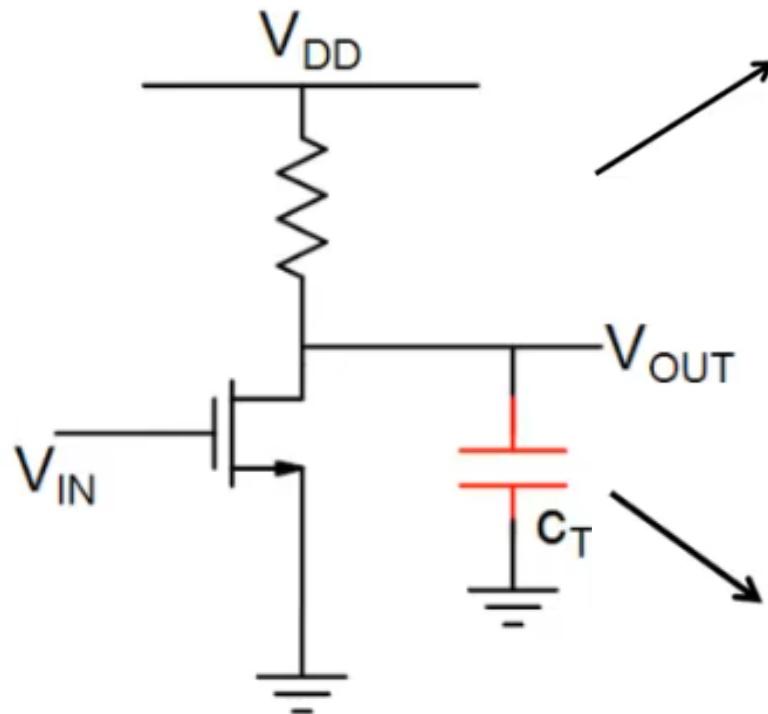
$$I_{dis.} = I_{DS1} - \frac{V_{DD} - V_{D1}}{R_D}$$

$$I_{DS}(t=0) = \left(KP_N \times \frac{W}{L} \right) \times \frac{(V_{DD} - V_{THN})^2}{2} \quad 0.53 \text{ mA}$$

$$I_{DS}(t=\tau_{phl}) = \left(KP_N \times \frac{W}{L} \right) \times \left((V_{DD} - V_{THN}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{4} \right) - \frac{V_{DD}}{2R_D} \quad 0.19 \text{ mA}$$

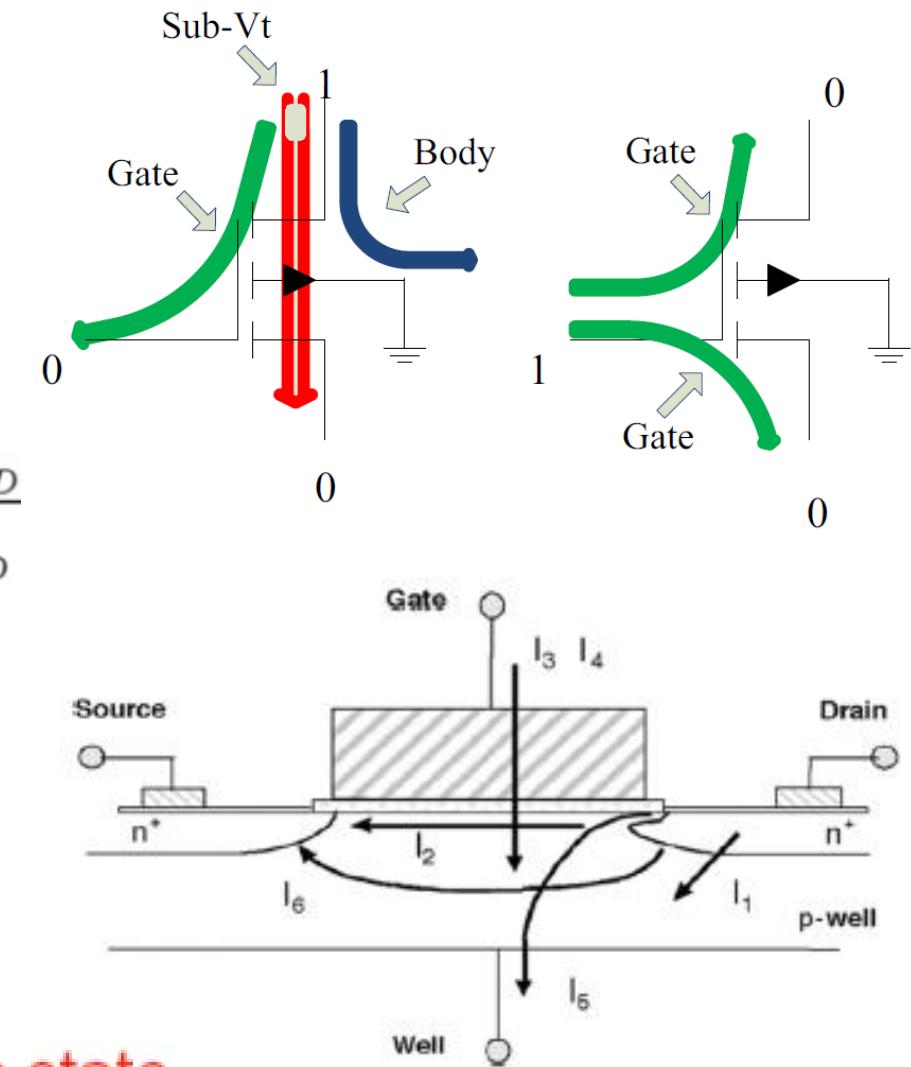


Power dissipation



$$P = V_{DD} \times I_{leakage}$$

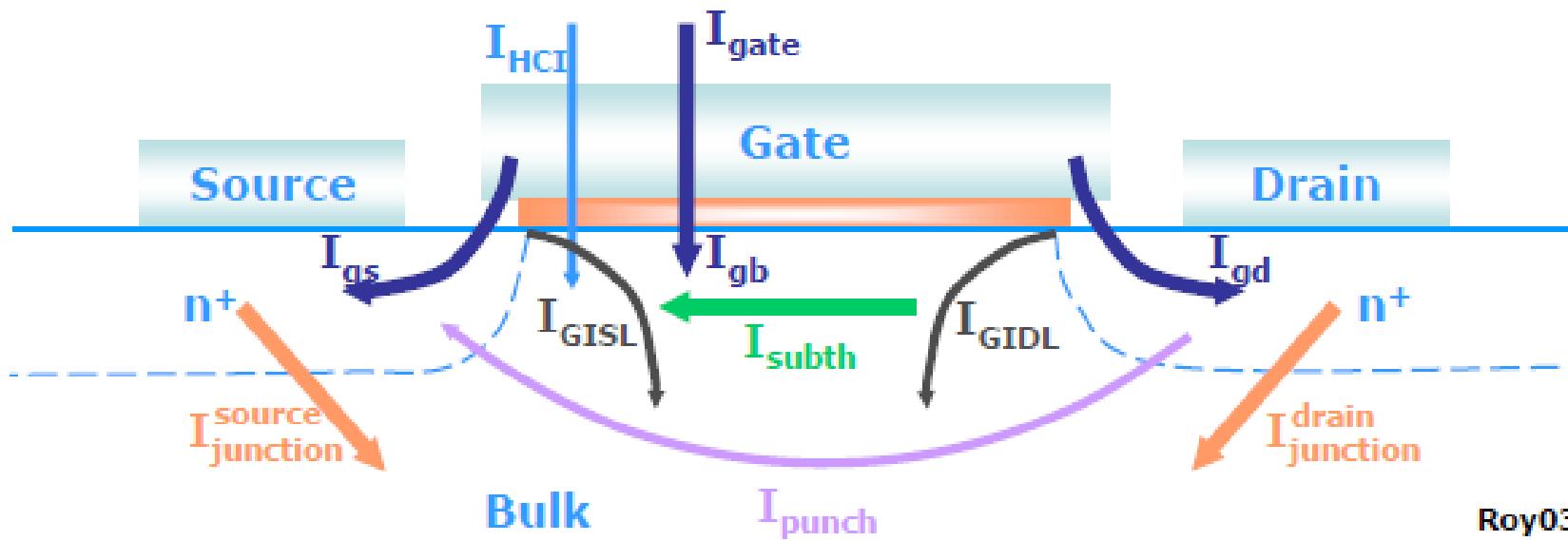
$$P \sim \frac{V_{DD}^2}{R_D}$$



1. Static
2. Dynamic

Energy should be drawn only to change the state

- If channel is locking:
 - subthreshold current (I_{subth})
 - gate tunnelling to S/D (I_{gate})
 - pn-junction leakage (I_{junction})
 - gate induced drain leakage (I_{GIDL})
 - depletion punchthrough (I_{punch})
- If channel is conducting:
 - gate tunnelling (I_{gate})
 - pn-junction leakage (I_{junction})
- If channel is switching:
 - hot carrier injection (I_{HCI})



Roy03

Long Channels
($L > 1\mu\text{m}$)

Leakages are very small.

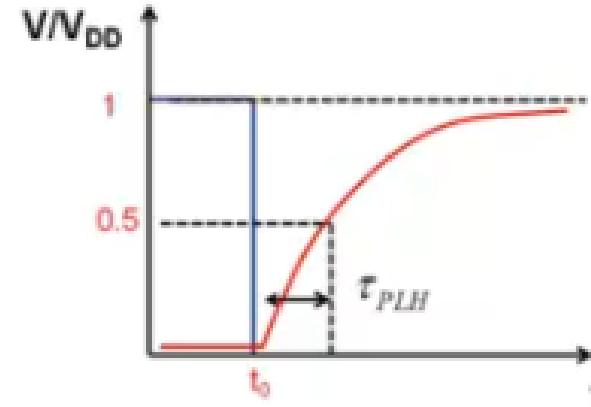
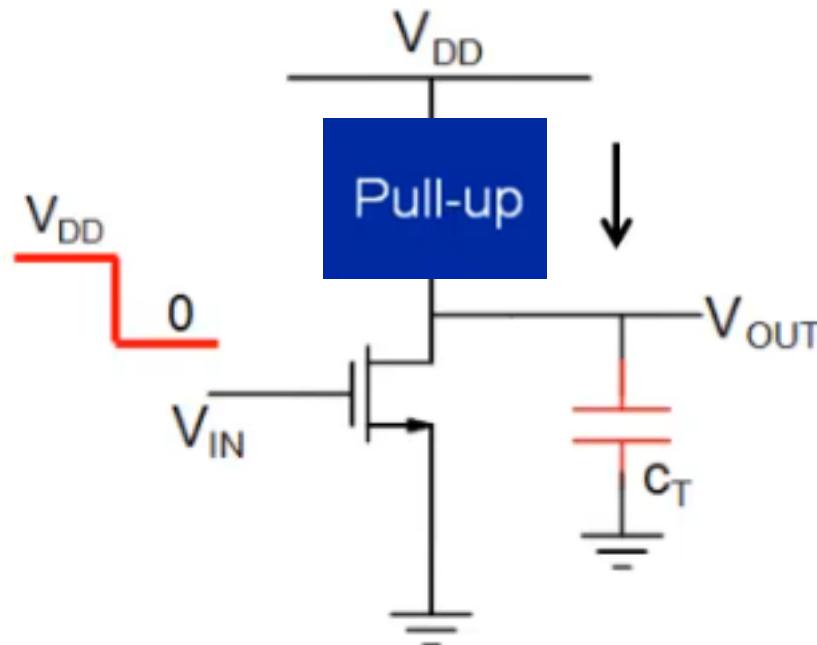
Short Channels
 $L > 180\text{nm}$
 $t_{\text{ox}} > 3\text{nm}$

Sub-threshold leakage

Very Short Channels
 $L > 90\text{nm}$
 $t_{\text{ox}} > 2\text{nm}$

Sub-threshold leakage +
Gate leakage

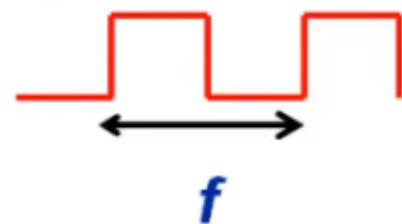
Nano scale Channels
 $L < 90\text{nm}$
 $t_{\text{ox}} < 2\text{nm}$
Sub-threshold leakage +
Gate leakage + Junction
leakage / BTBT



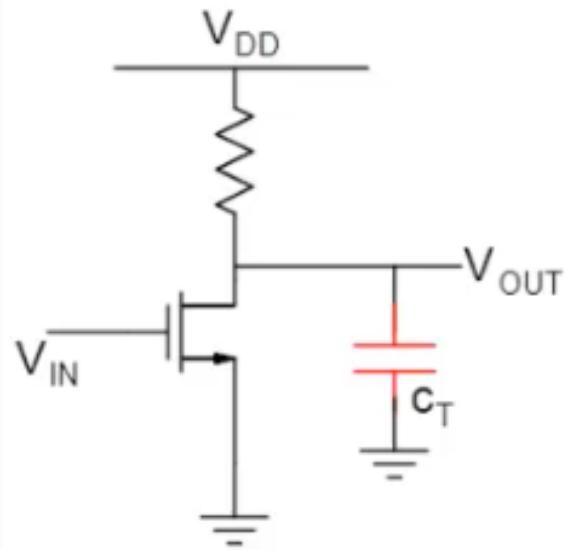
$$E_{\text{supply}} = \int V_{DD} \times I_{pu} dt = C_T \times V_{DD}^2$$

Half of it is dissipated in the resistor and the other half is stored in capacitor

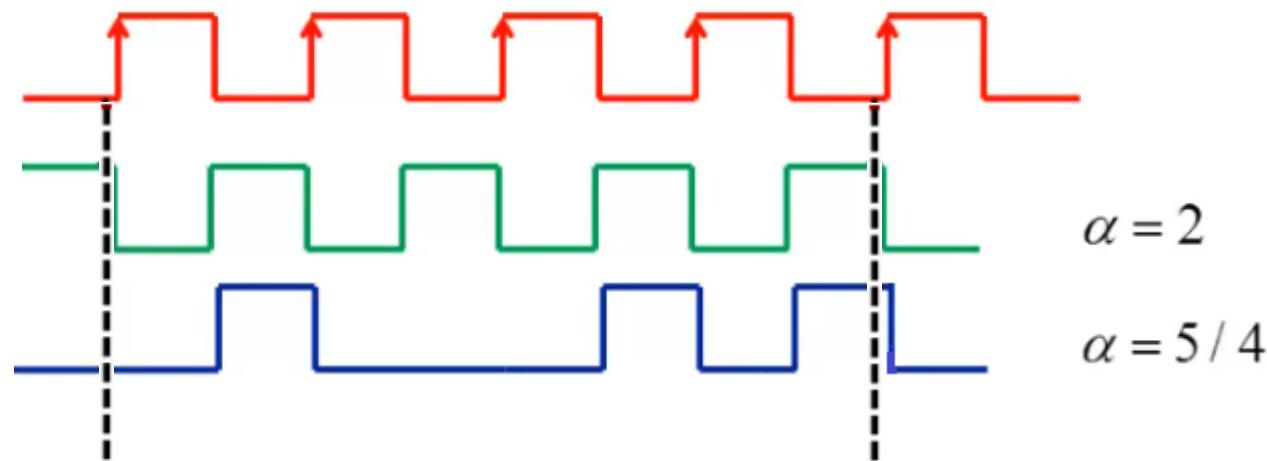
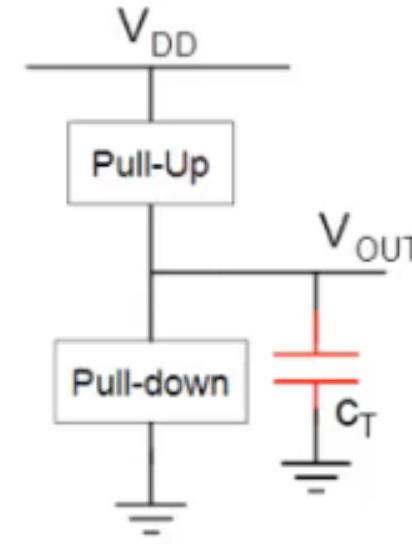
When the inverter switches back to zero, the energy stored on capacitor is also dissipated



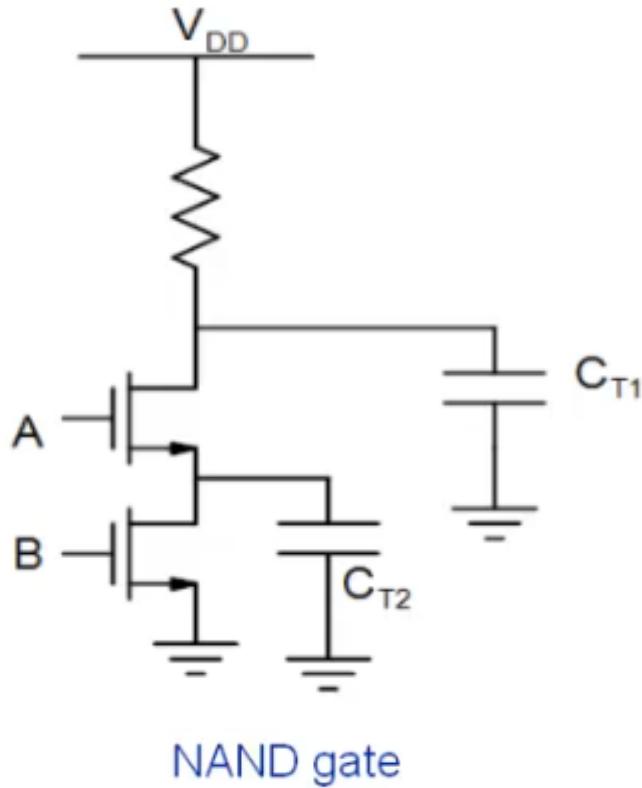
$$P_{\text{dynamic}} = \frac{0.5C_T \times V_{DD}^2 + 0.5C_T \times V_{DD}^2}{T} = C_T \times V_{DD}^2 \times f$$



$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$



$$P_{dynamic} = \sum (0.5C_j \times V_j^2) \times f \times \alpha_j$$

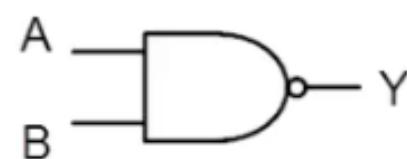


Suppose $B=1$ and A switches with clock frequency

$$P_{dynamic} \approx (0.5C_{T1} \times V_{DD}^2) \times f \times 2$$

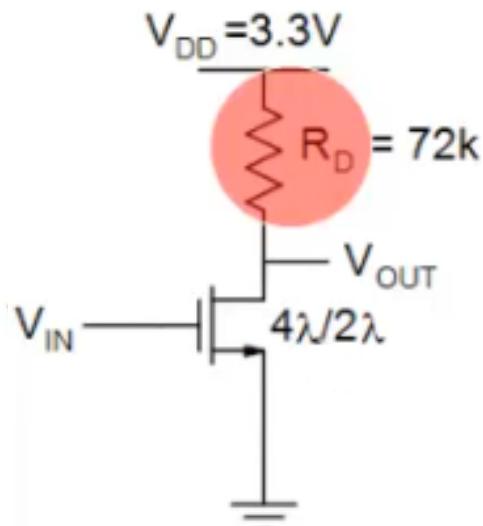
Suppose $A=1$ and B switches with clock frequency

$$P_{dynamic} \approx (0.5C_{T1} \times V_{DD}^2) \times f \times 2 + (0.5C_{T2} \times V_{DD}^2) \times f \times 2$$

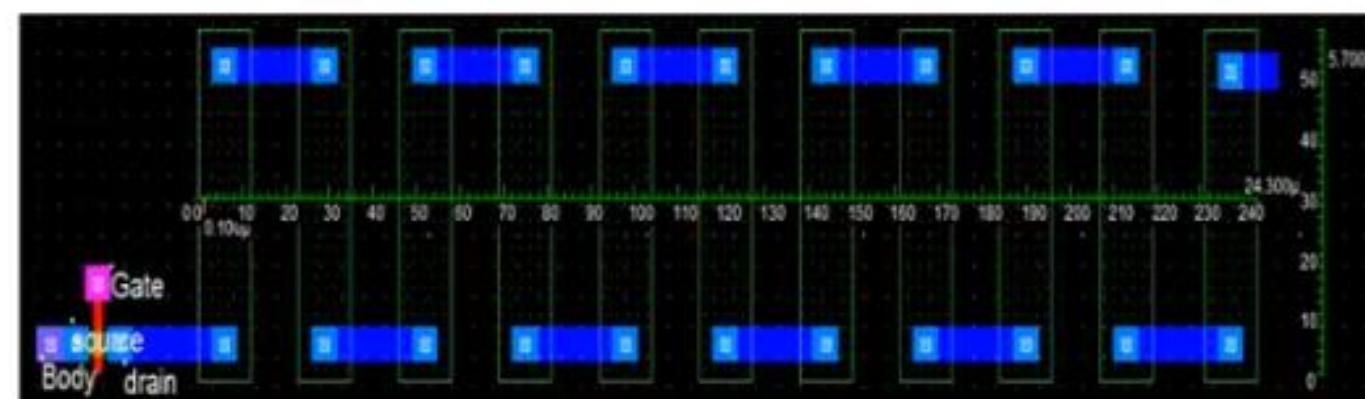
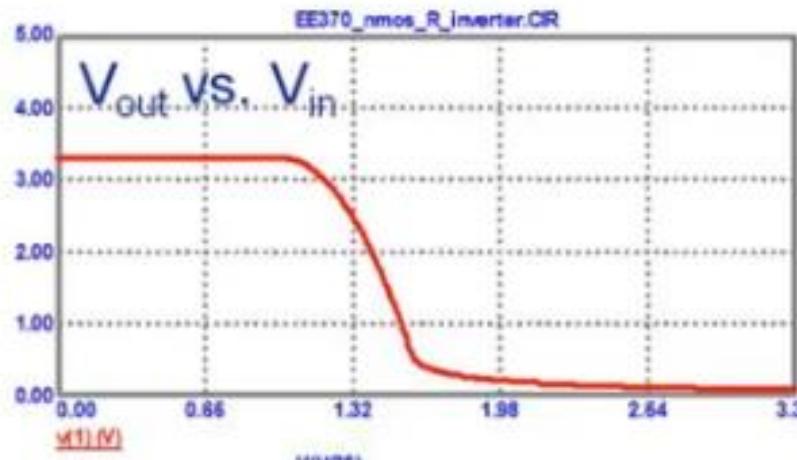


What about delays?

Summary



1. Noise Margins
2. Area
3. Delay
4. Power



$$\tau_{PLH} \approx 424 \text{ ps}; \tau_{PHL} \approx 39 \text{ ps}$$

$$\tau_{PLH} \approx 0.693 \times R_D \times \tilde{C}_T$$

$$R_D = 72k \Rightarrow V_{OL} = 0.1V; V_{OH} = 3.3V$$

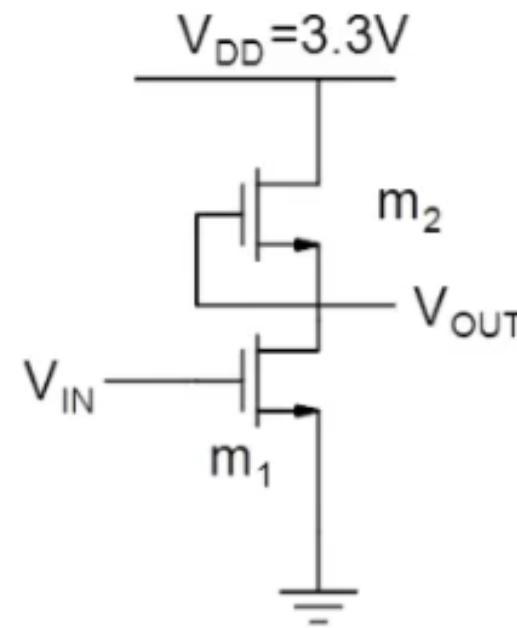
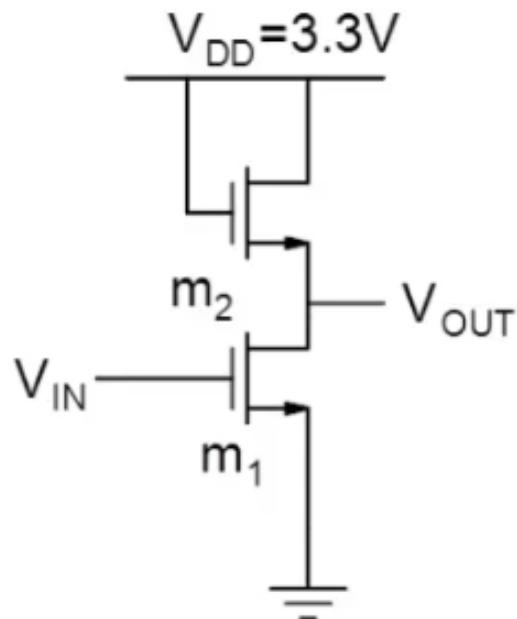
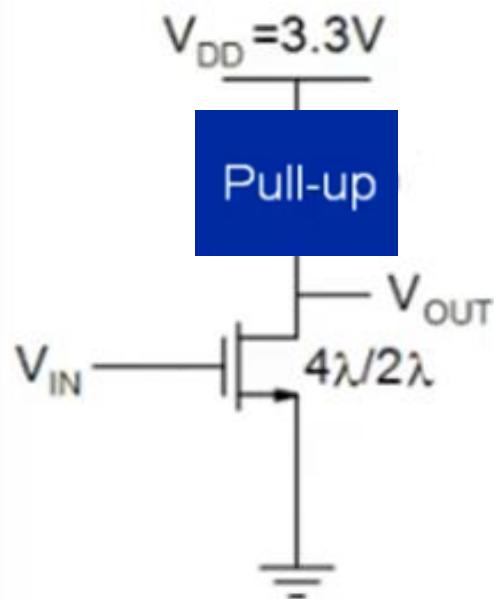
$$V_{IL} = 1.07V; V_{IH} = 1.7V$$

$$NM_L \sim 0.97V; NM_H \sim 1.6V$$

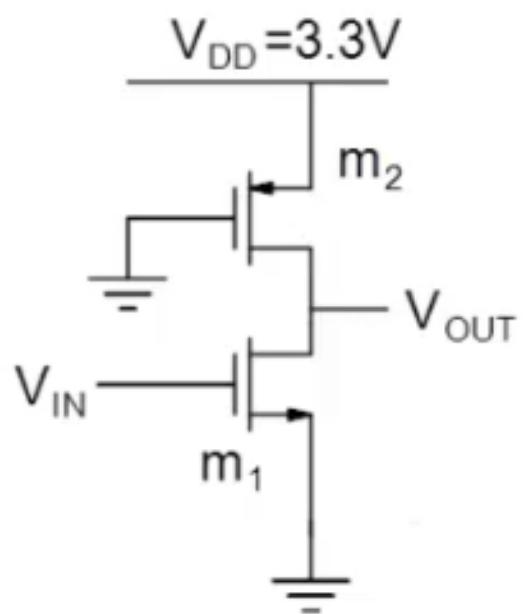
$$V_{inv} = 1.5V$$

$$P_{static} \sim \frac{V_{DD}^2}{R_D}$$

$$P_{dynamic} = C_T \times V_{DD}^2 \times f$$

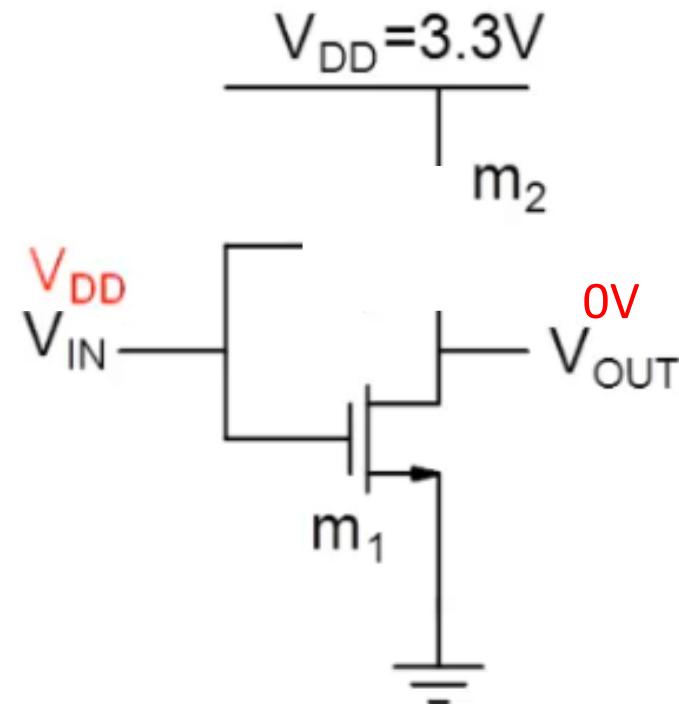
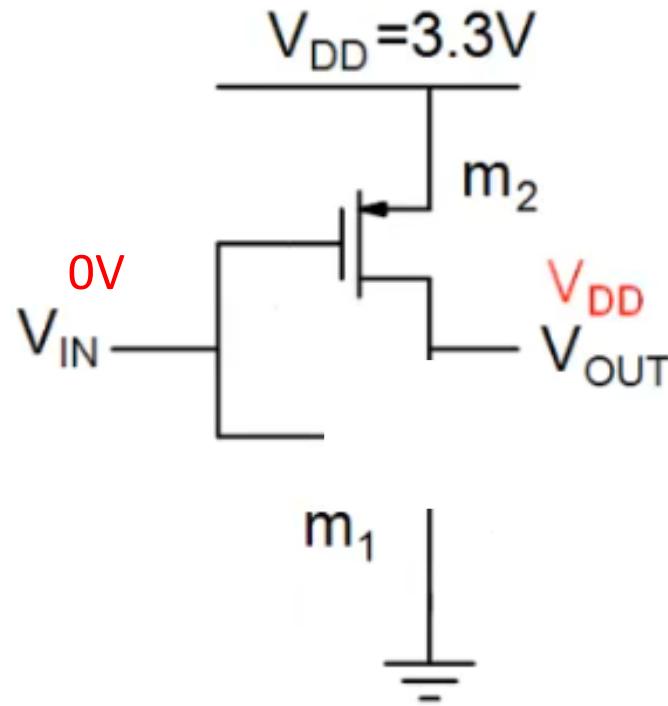


Make m_2 depletion mode



They all have static power dissipation
when output is low.

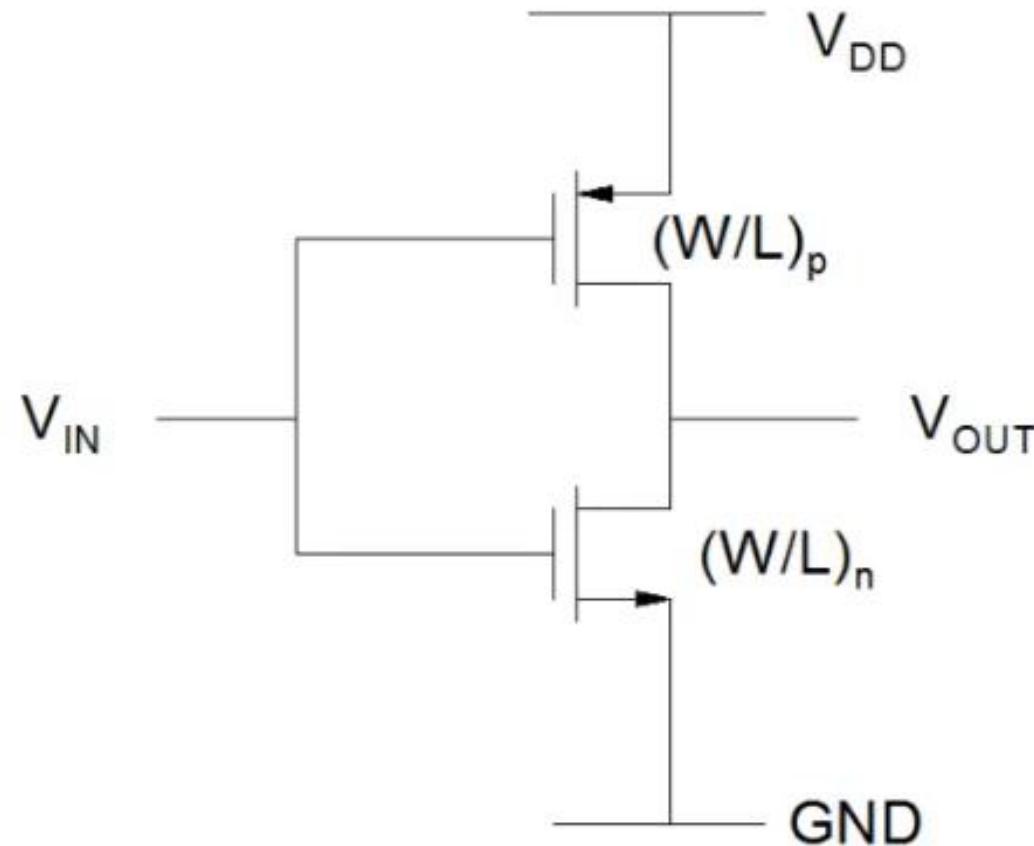
Pseudo-NMOS logic



Logic “1” is V_{DD} and “logic “0” is GND independent of size of transistors.

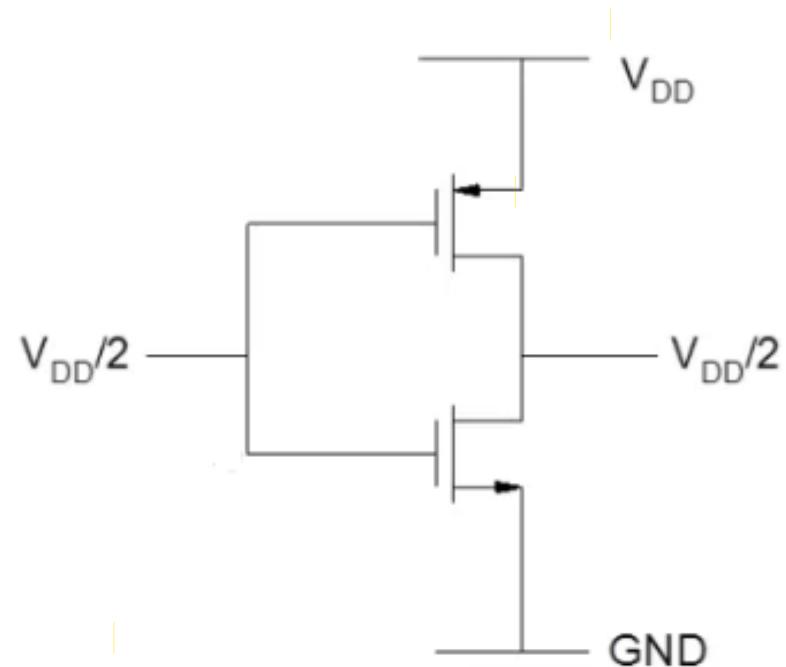
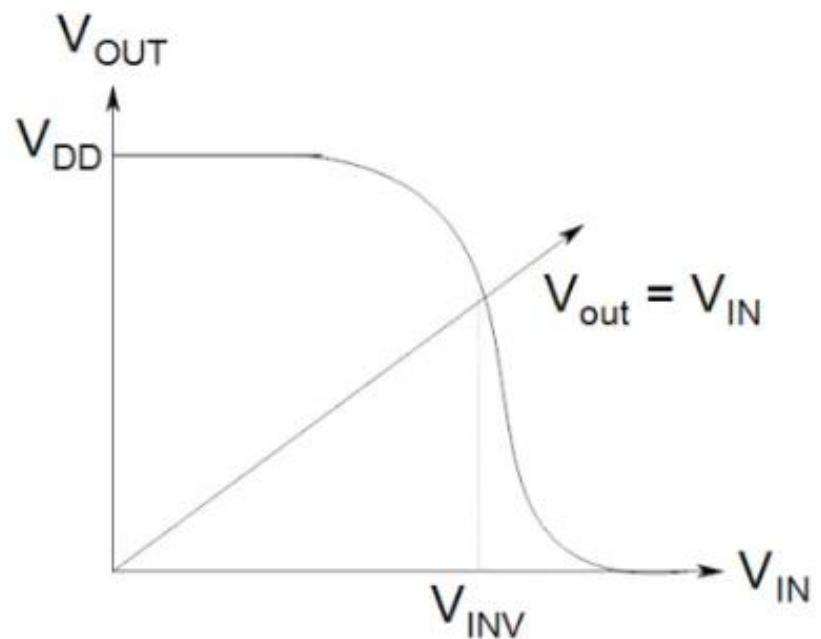
There is “no” static power dissipation in the circuit

CMOS Inverter



How should we size to obtain symmetrical VTC ?

CMOS Inverter : VTC



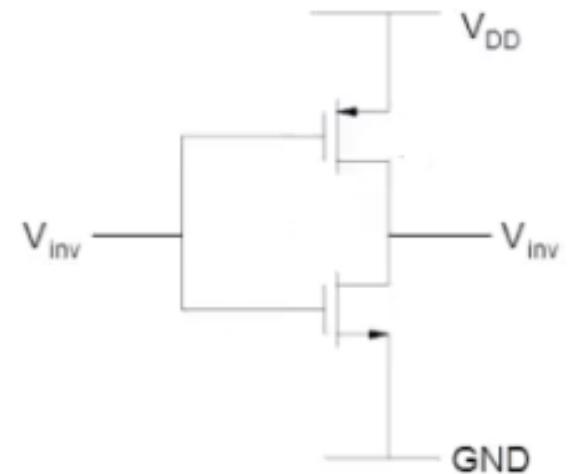
Both NMOS and PMOS are in saturation region

CMOS Inverter : VTC

$$I_{DSN} = I_{SDP}$$

$$\frac{\beta_N}{2}(V_{inv} - V_{THN})^2 = \frac{\beta_P}{2}(V_{SGP} + V_{THP})^2$$

$$V_{SGP} = V_{DD} - V_{inv}$$



$$\beta_N = W_N / L_N K P_N$$

$$\beta_P = W_p / L_p K P_p$$

$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

$$\beta_R = \frac{\beta_N}{\beta_P} = \left(\frac{W_N / L_N}{W_P / L_P} \right) \times \left(\frac{K P_N}{K P_P} \right)$$

CMOS Inverter : VTC

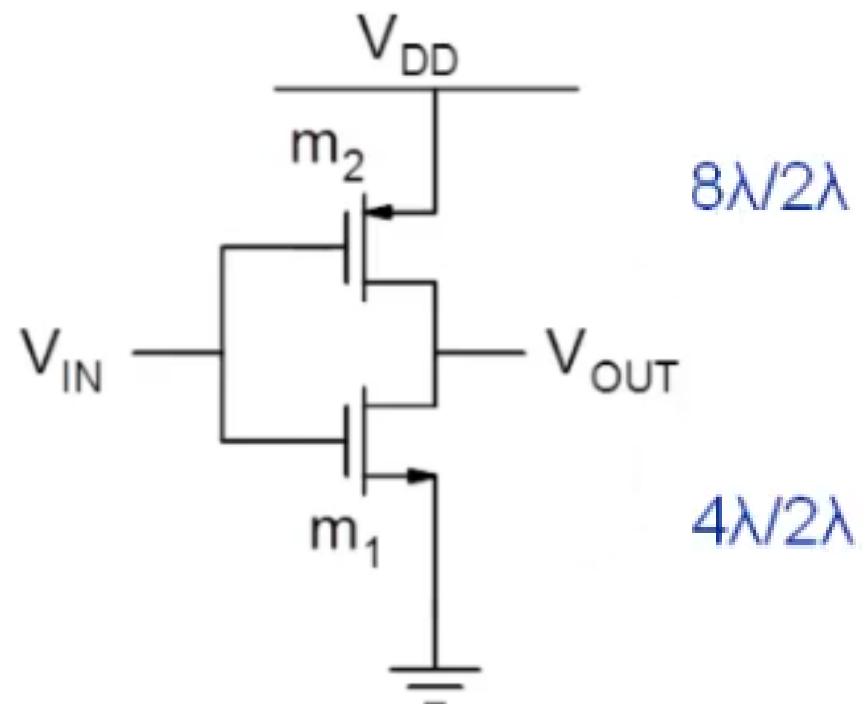
$$V_{INV} = \frac{V_{THN} + \frac{1}{\sqrt{\beta_R}}(V_{DD} + V_{THP})}{1 + \frac{1}{\sqrt{\beta_R}}}$$

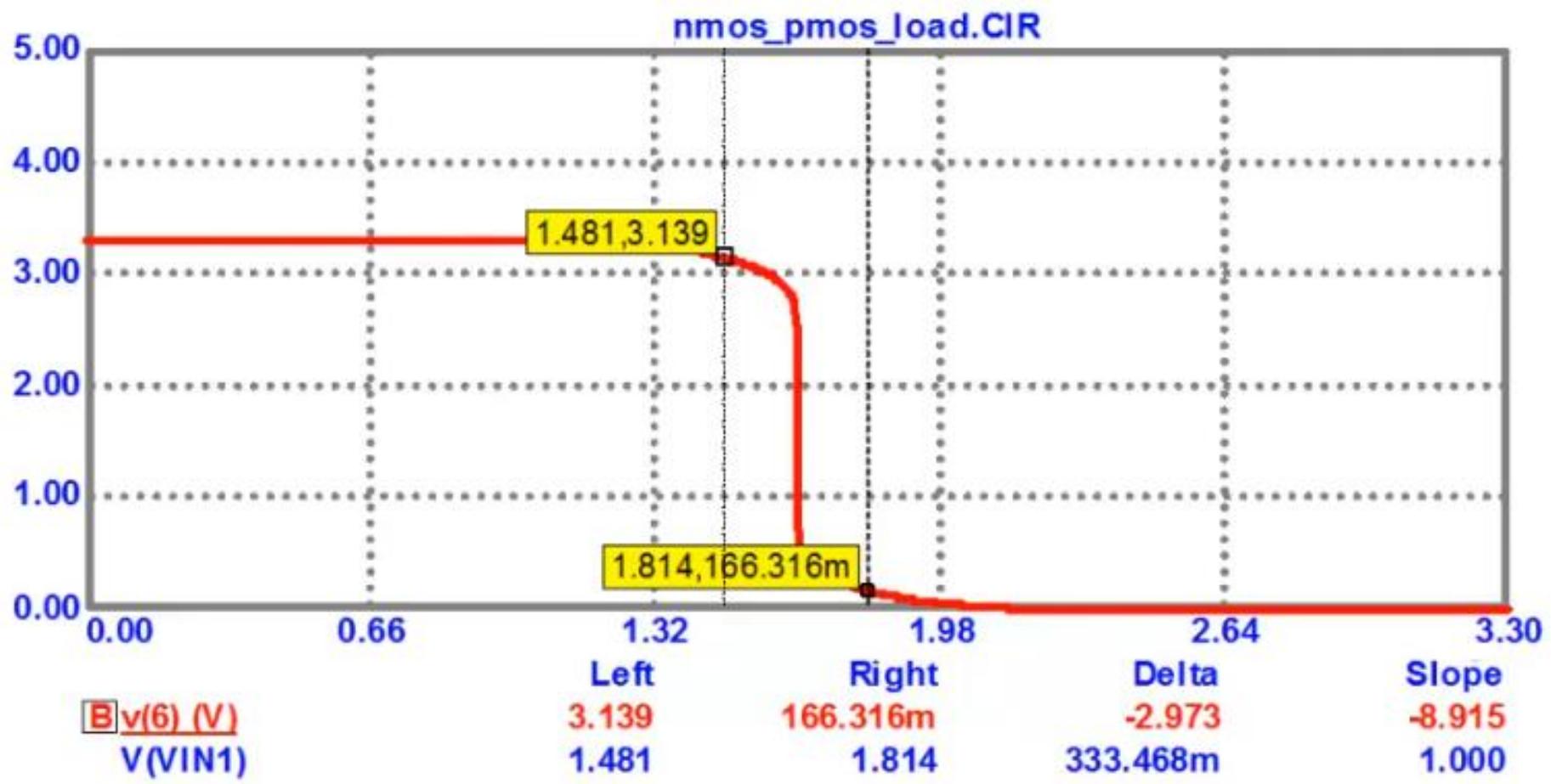
$$V_{INV} = 0.5V_{DD}$$

$$\beta_R = \frac{0.5V_{DD} + V_{THP}}{0.5V_{DD} - V_{THN}}$$

$$\Rightarrow \beta_R = 1$$

$$\frac{W_P/L_P}{W_N/L_N} = \frac{KP_N}{KP_P} \quad 2.0$$





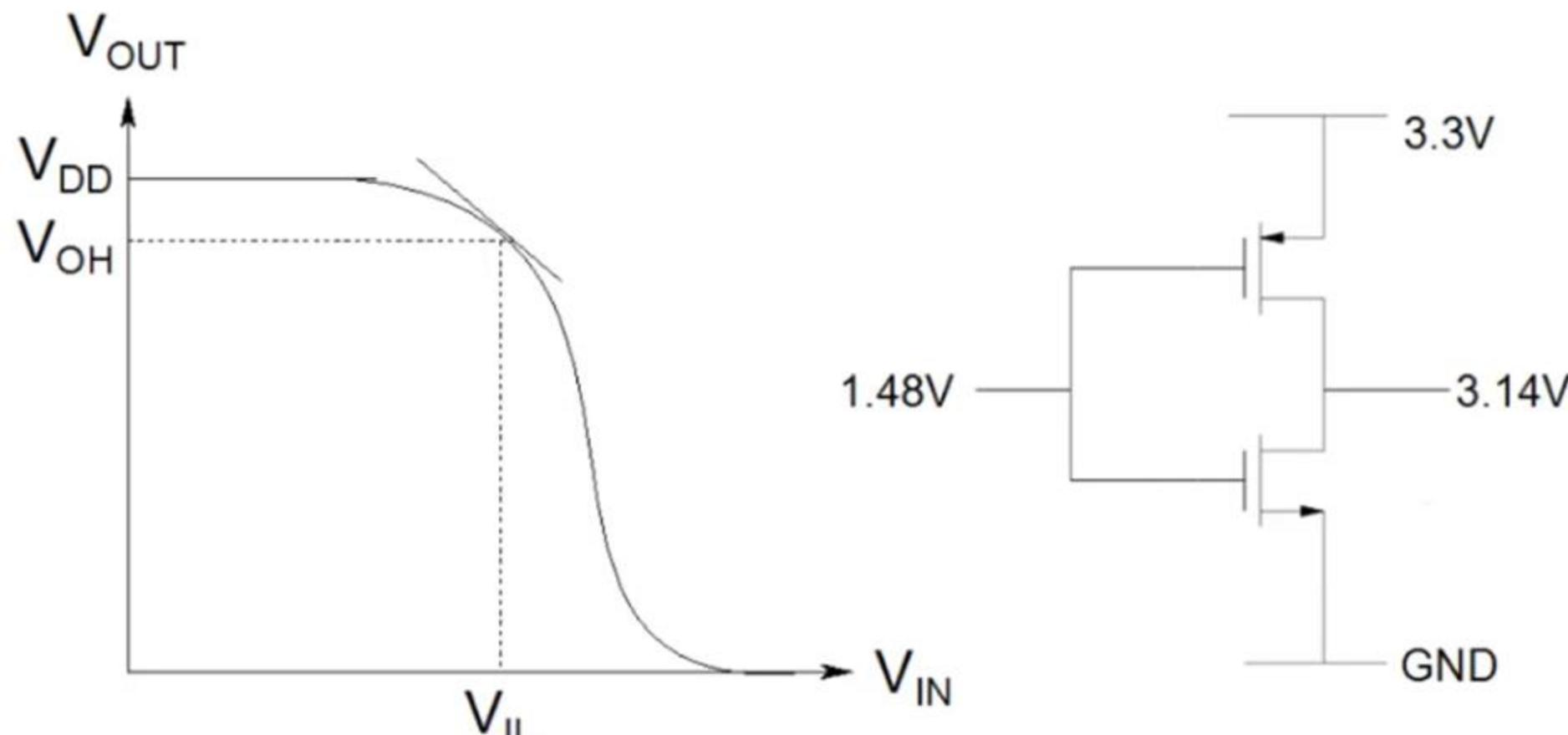
$$V_{IL} = 1.48V; v_{ol} = 0V$$

$$V_{IH} = 1.814V; v_{oh} = 3.3V$$

$$NM_H = 1.48V; NM_L = 1.48V$$

$$\frac{NM_H}{0.5V_{DD}} = 0.9$$

CMOS Inverter : V_{IH} ; V_{IL}



At V_{IL} , PMOS in Linear and NMOS in Saturation

CMOS Inverter : V_{IH} ; V_{IL}

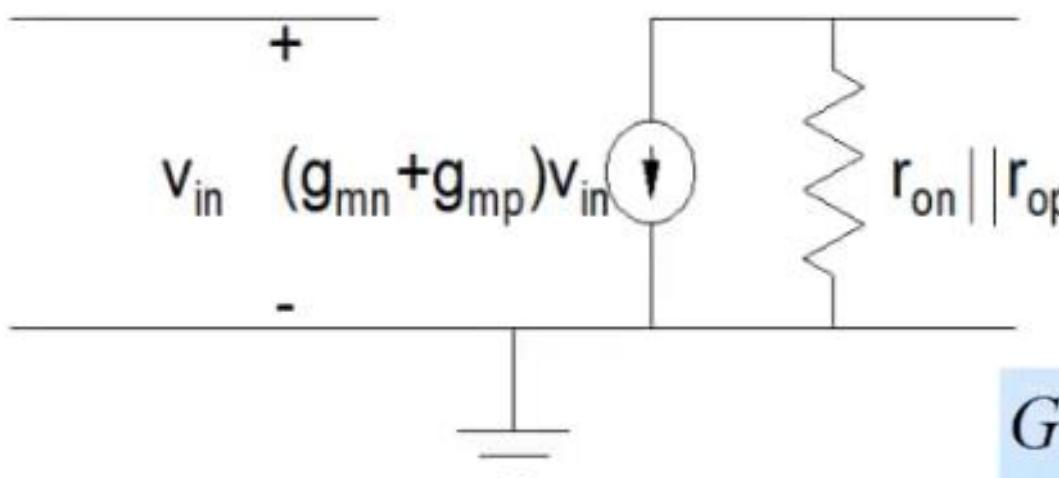
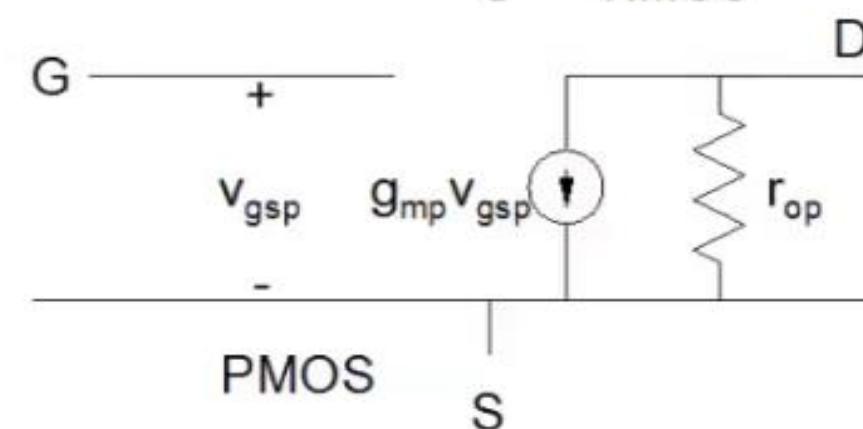
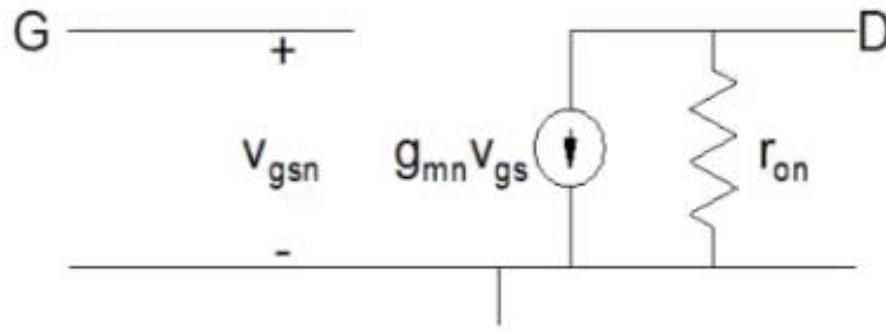
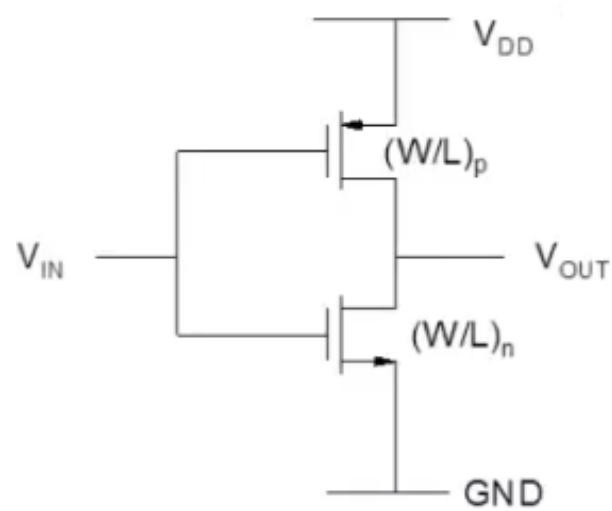
W_P/W_N	V_{INV}	V_{IH}	V_{IL}	V_{OH}	V_{OL}
1	1.53	1.67	1.34	3.16	0.177
2	1.65	1.81	1.48	3.14	0.166
3	1.7	1.9	1.575	3.12	0.148

CMOS Inverter : V_{IL}

$$\frac{\beta_N}{2}(V_{IL} - V_{THN})^2 = \beta_P((V_{DD} - V_{IL} + V_{THP})(V_{DD} - V_{OUT}) - 0.5(V_{DD} - V_{OUT})^2)$$

- Gain of inverter is Unity

CMOS Inverter : V_{IH} ; V_{IL}



$$G = -(g_{MN} + g_{MP}) \times r_{ON} \parallel r_{OP}$$

CMOS Inverter : V_{IL}

$$G = -(g_{MN} + g_{MP}) \times r_{ON} \parallel r_{OP} = -1$$

$$\Rightarrow (g_{MN} + g_{MP}) \times r_{OP} \cong 1$$

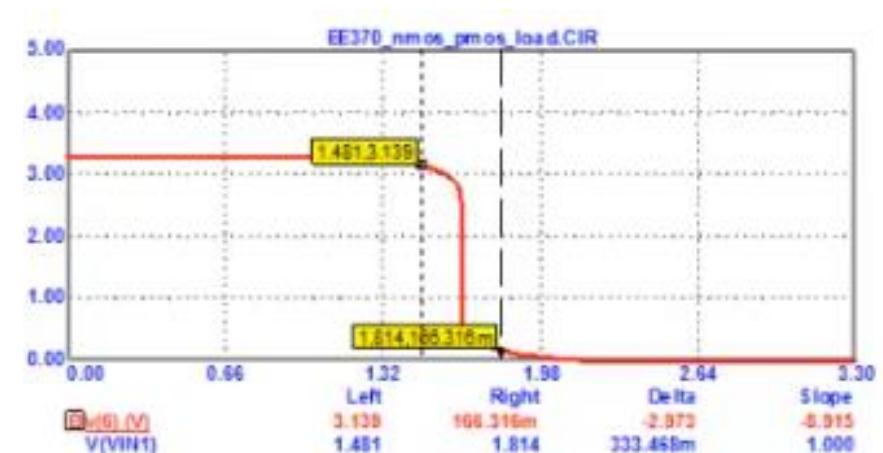
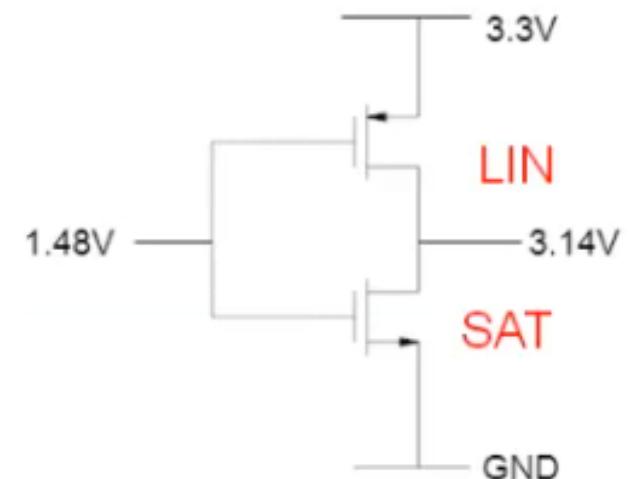
$$g_{mn} = \beta_N \times (V_{IL} - V_{THN}) ; \quad g_{mp} = \beta_P \times (V_{DD} - V_{OUT})$$

$$r_{op} = \frac{1}{\beta_P \times (V_{DD} - V_{IL} + V_{THP} + V_{DD} - V_{OUT})}$$

$$\frac{\beta_N}{2} (V_{IL} - V_{THN})^2 =$$

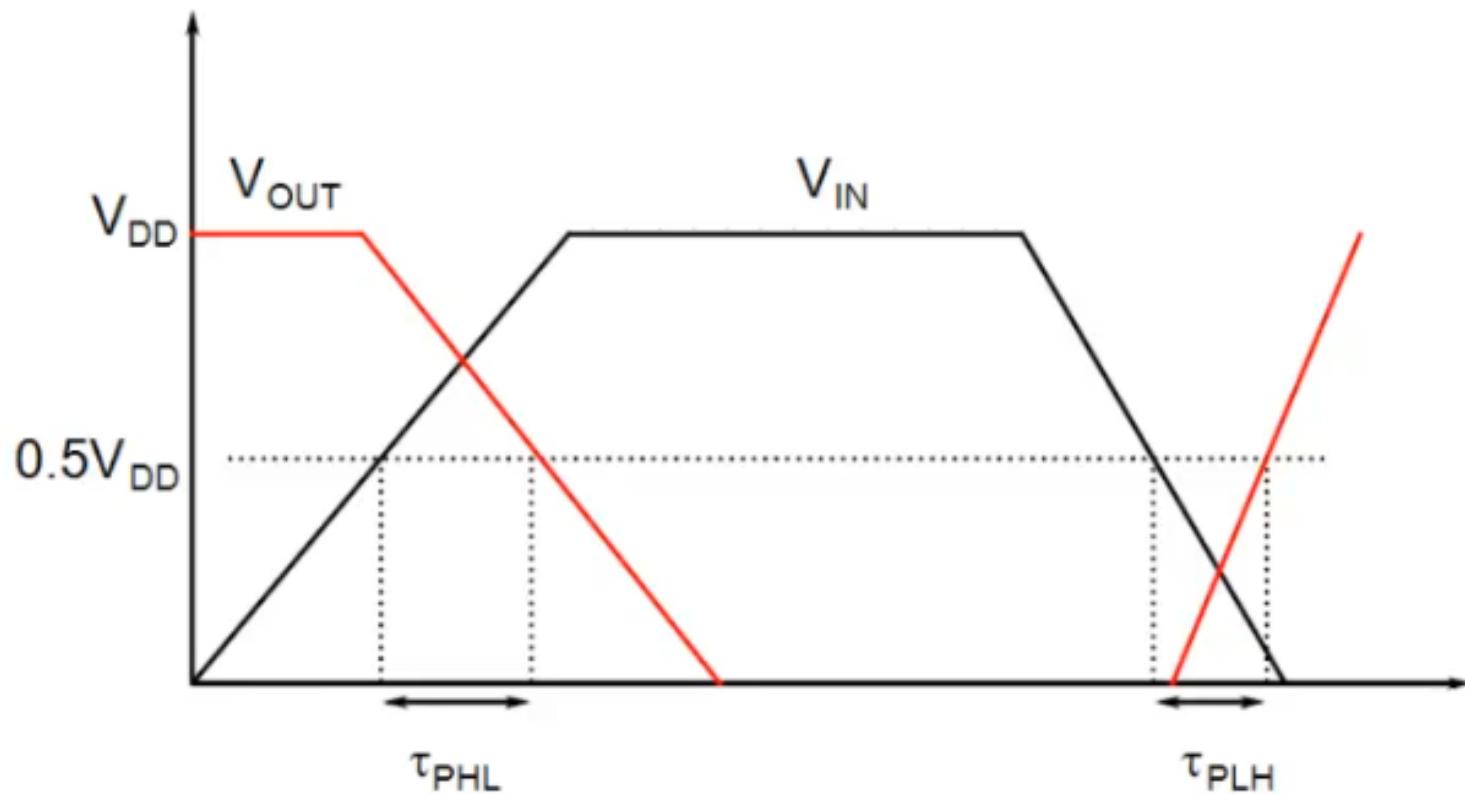
$$\beta_P ((V_{DD} - V_{IL} + V_{THP})(V_{DD} - V_{OUT}) - 0.5(V_{DD} - V_{OUT})^2)$$

$$V_{IL} \sim V_{inv} - \delta V; \quad V_{IH} \sim V_{inv} + \delta V$$



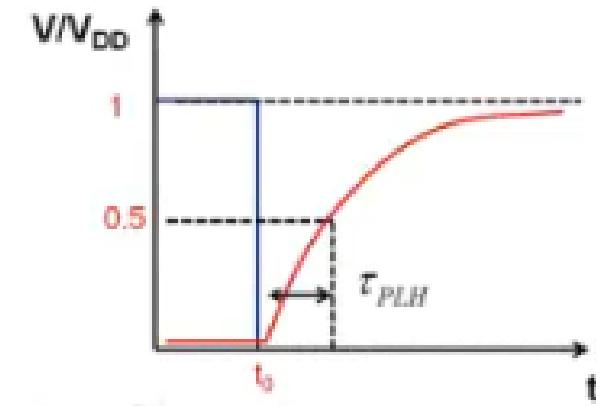
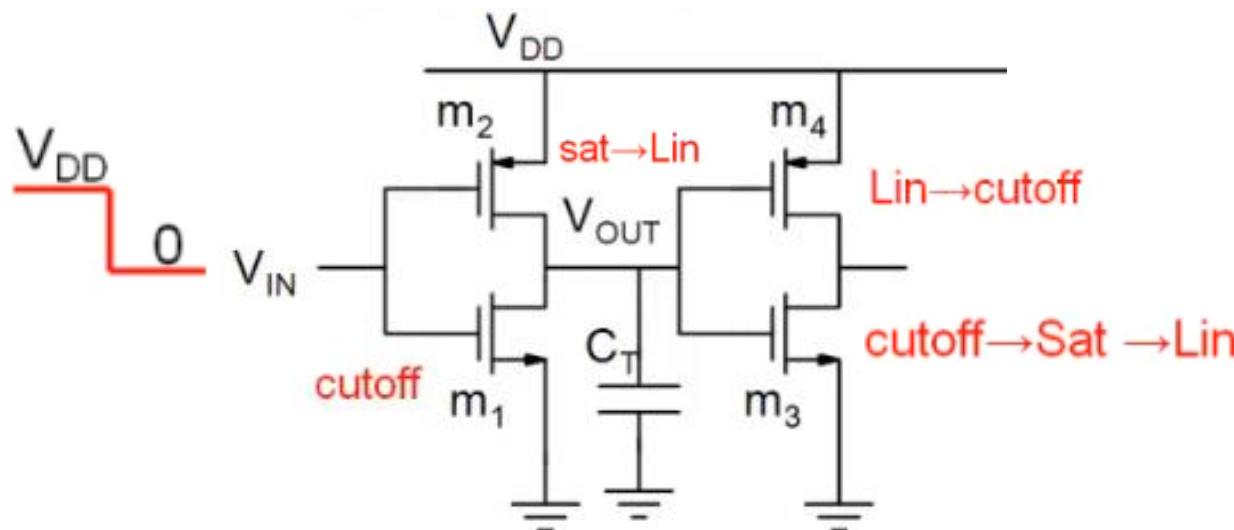
$$\delta V \sim 0.17V$$

CMOS: Propagation Delay



$$\tau_R ; \tau_F ; \tau_{PHL} ; \tau_{PLH}$$

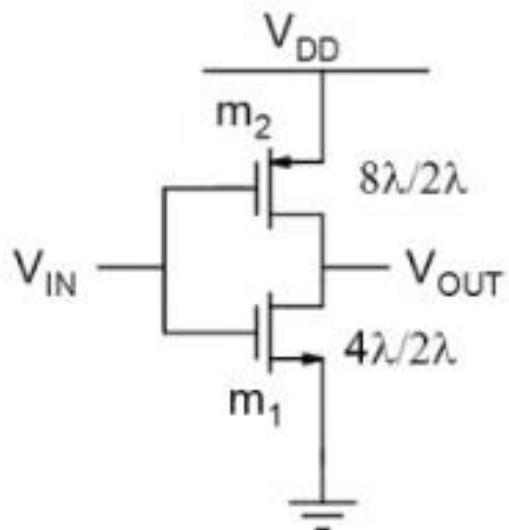
Low to high propagation delay



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$\tau_{phh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu}}$$

$$C_T = \left(C_{gdn1} + C_{dbn1} + C_{gdp2} + C_{dbp2} \right) + \\ \left(C_{gsn3} + C_{gdn3} + C_{gbn3} + C_{gsp4} + C_{gdp4} + C_{gbp4} \right)$$

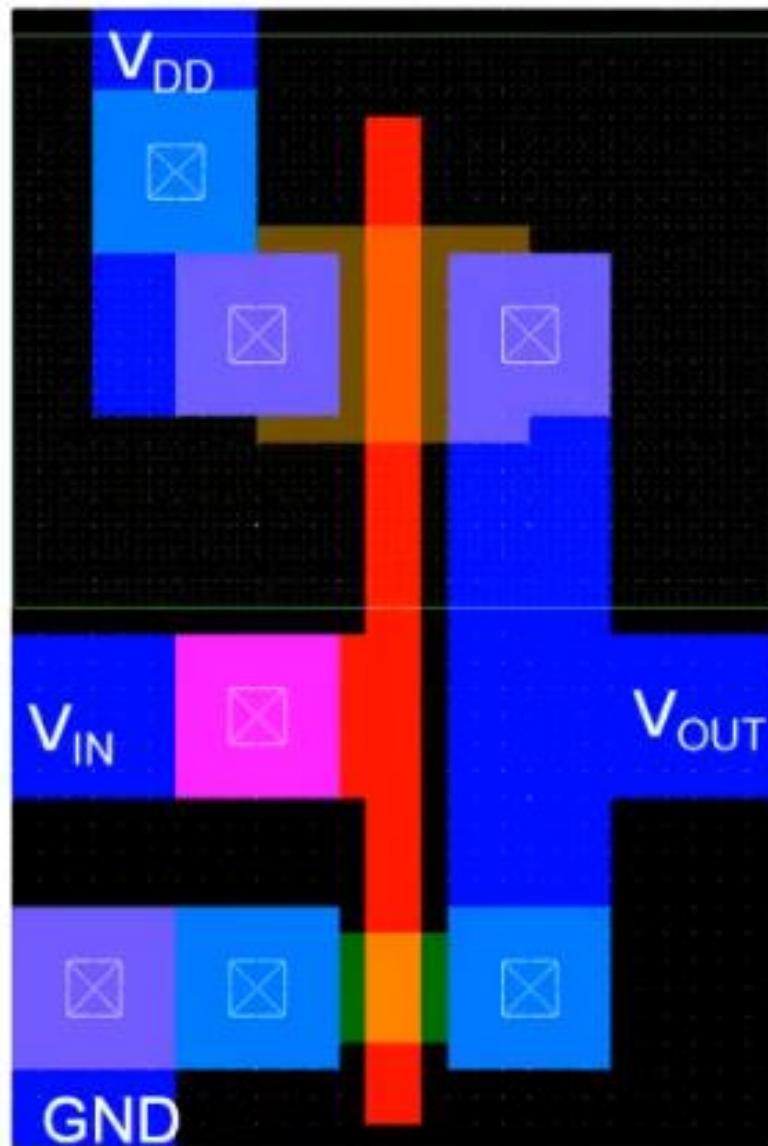


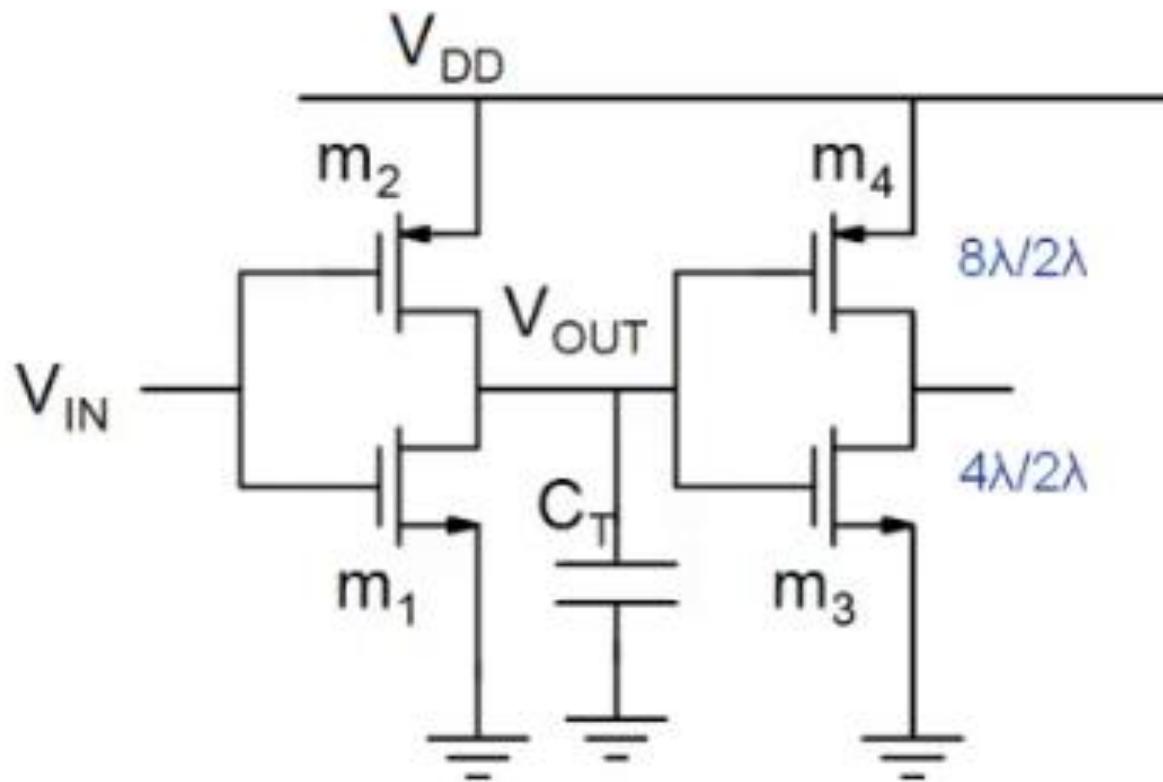
$$A_{D1} = 4 \times 1 + 6 \times 6 = 40;$$

$$P_{D1} = (1 + 1 + 6) \times 2 + 6 = 22$$

$$A_{D2} = 8 \times 4 + 3 \times 6 = 50;$$

$$P_{D2} = (4 + 1 + 3) \times 2 + 6 = 22$$

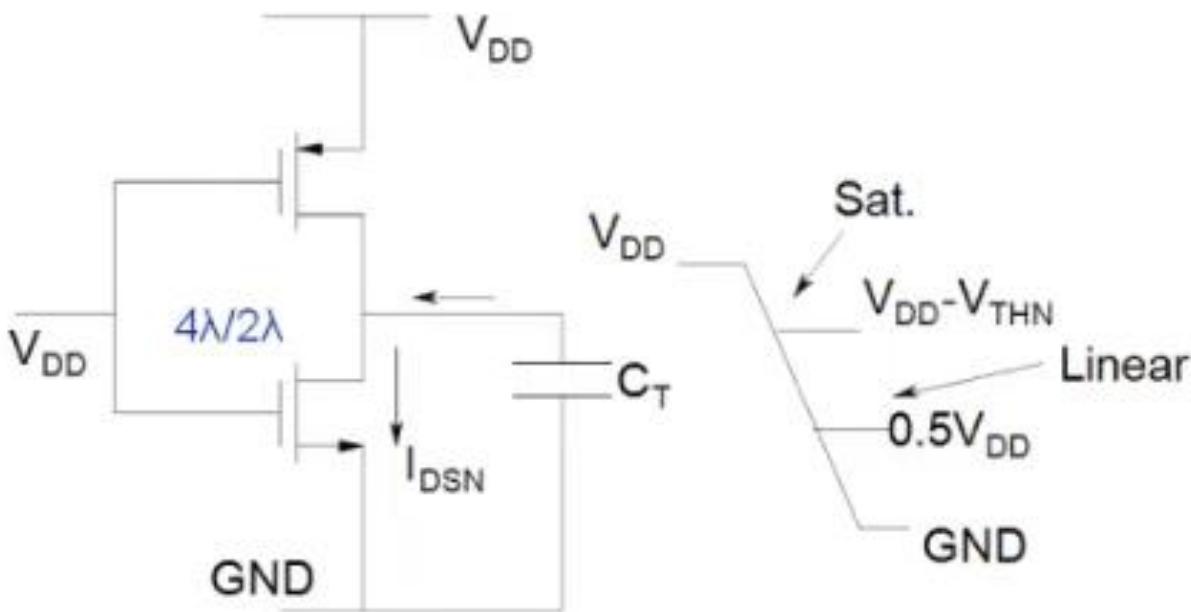




$$C_T = \left(C_{gdn1} + C_{dbn1} + C_{gdp2} + C_{dbp2} \right) + \left(C_{gsn3} + C_{gdn3} + C_{gbn3} + C_{gsp4} + C_{gdp4} + C_{gbp43} \right)$$

~0.3fF ~6fF ~0.6fF ~6fF
 $\sim 2.0\text{fF}$ $\sim 5\text{fF}$
 $\sim 13+7\text{fF}$

Delay Analysis :



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}} \quad \tau_{phl} \sim 65 \text{ ps}$$

42+23

$$I_{DS}(t=0) = \left(K_P N \times \frac{W_N}{L_N} \right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

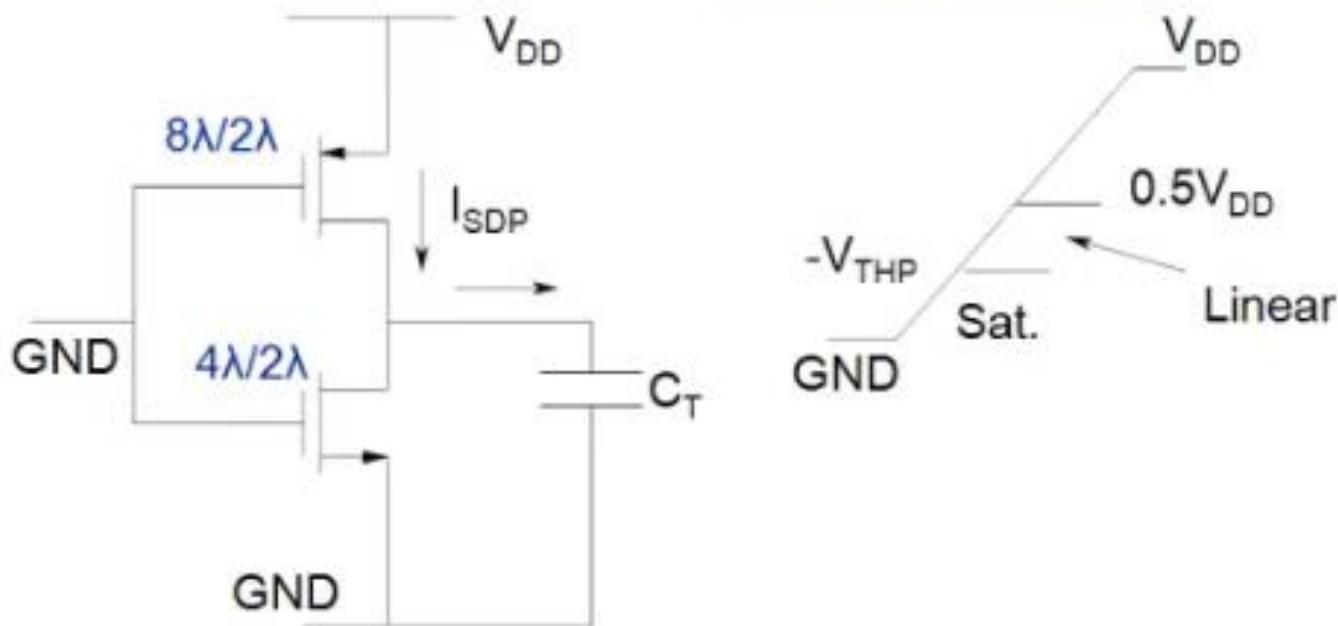
$$I_{DS}(t=\tau_{phl}) = \left(K_P N \times \frac{W_N}{L_N} \right) \times \left((V_{DD} - V_{THN}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right)$$

$\sim 0.53 \text{ mA} \rightarrow \tilde{I}_{pd} \sim 0.5 \text{ mA}$

$\sim 0.487 \text{ mA}$

Delay Analysis :

$$\tau_{plh} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu.}} \quad \tau_{plh} \sim 65 \text{ ps}$$

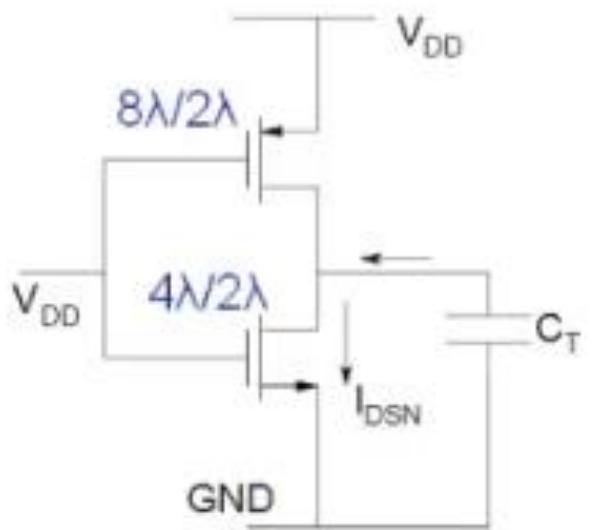


$$I_{SDP}(t=0) = \left(K_P \times \frac{W_P}{L_P} \right) \times \frac{(V_{DD} + V_{THP})^2}{2} \quad \sim 0.53 \text{ mA}$$

$$I_{SDP}(t=\tau_{plh}) = \left(K_P \times \frac{W_P}{L_P} \right) \times \left((V_{DD} + V_{THP}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right) \quad \sim 0.487 \text{ mA}$$

$\tilde{I}_{pu} \sim 0.5 \text{ mA}$

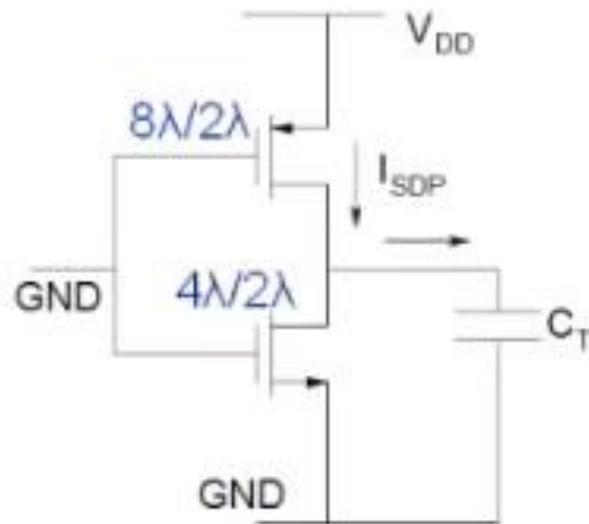
$\tilde{I}_{pu} \sim 0.487 \text{ mA}$



$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

$$I_{DS}(t=0) = \left(K P_N \times \frac{W_N}{L_N} \right) \times \frac{(V_{DD} - V_{THN})^2}{2}$$

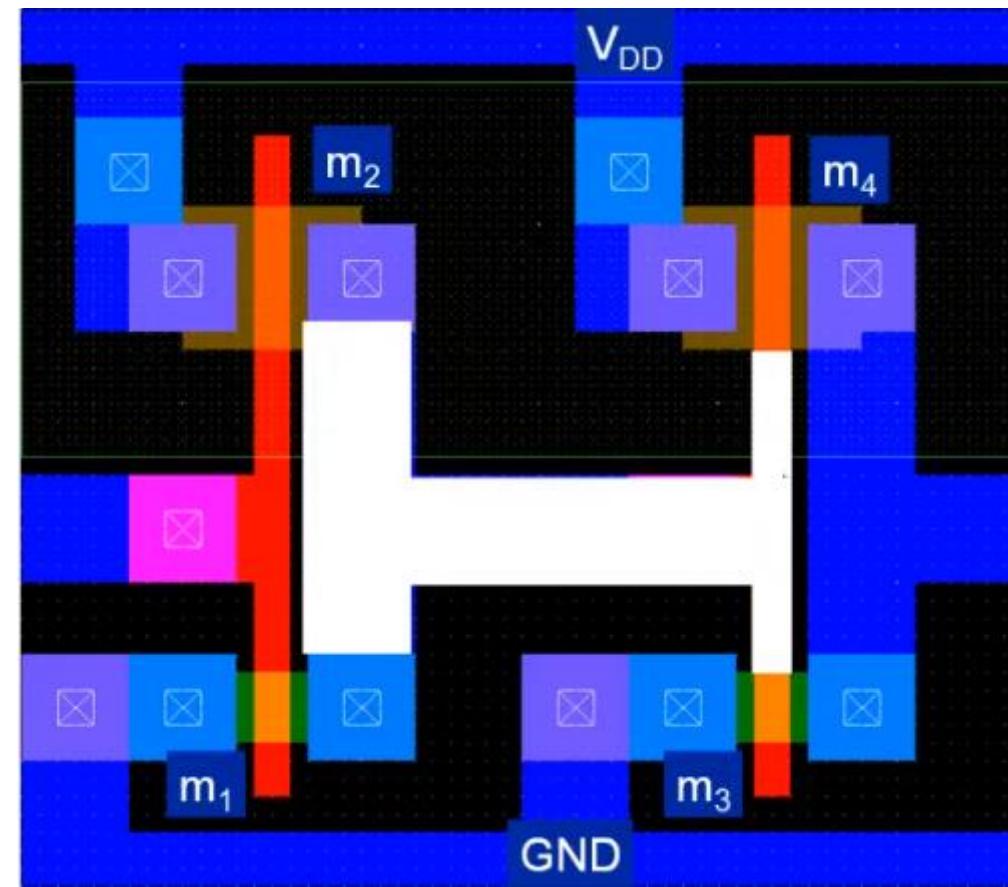
$$I_{DS}(t = \tau_{phl}) = \left(K P_N \times \frac{W_N}{L_N} \right) \times \left((V_{DD} - V_{THN}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right)$$

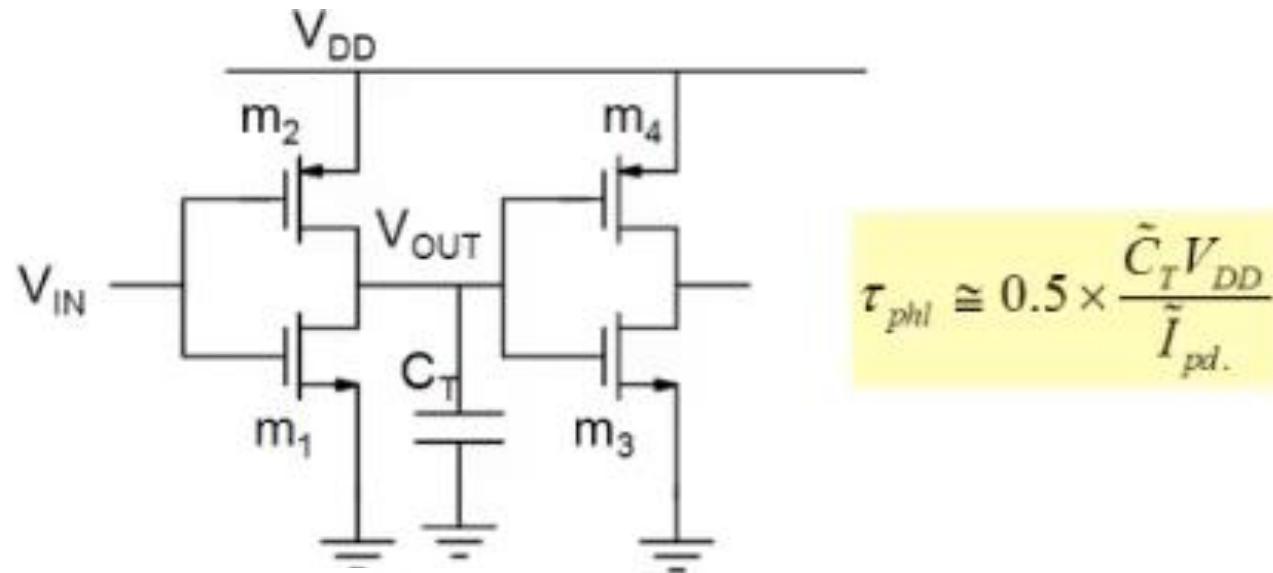


$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pu.}}$$

$$I_{SDP}(t=0) = \left(K P_P \times \frac{W_P}{L_P} \right) \times \frac{(V_{DD} + V_{THP})^2}{2}$$

$$I_{SDP}(t = \tau_{phl}) = \left(K P_P \times \frac{W_P}{L_P} \right) \times \left((V_{DD} + V_{THP}) \frac{V_{DD}}{2} - \frac{V_{DD}^2}{8} \right)$$





$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_T V_{DD}}{\tilde{I}_{pd.}}$$

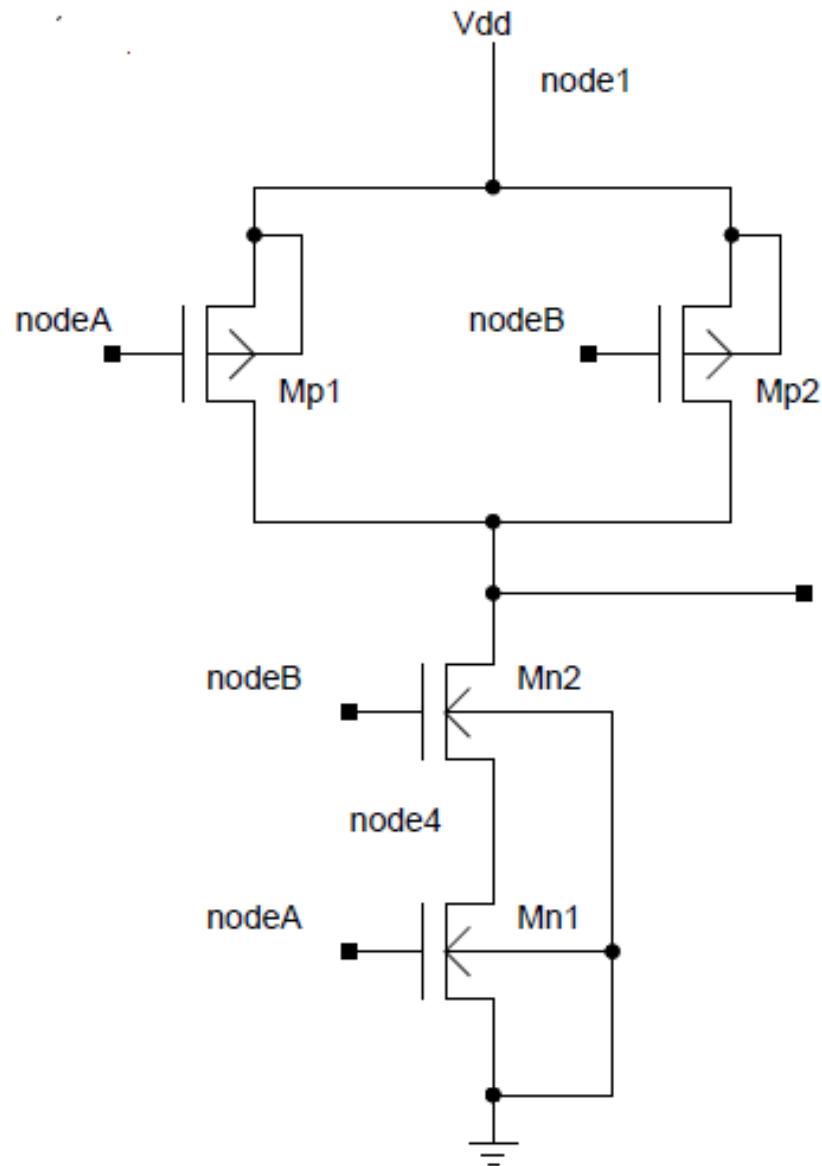
$\sim 13\text{fF}$

$\sim 7\text{fF}$

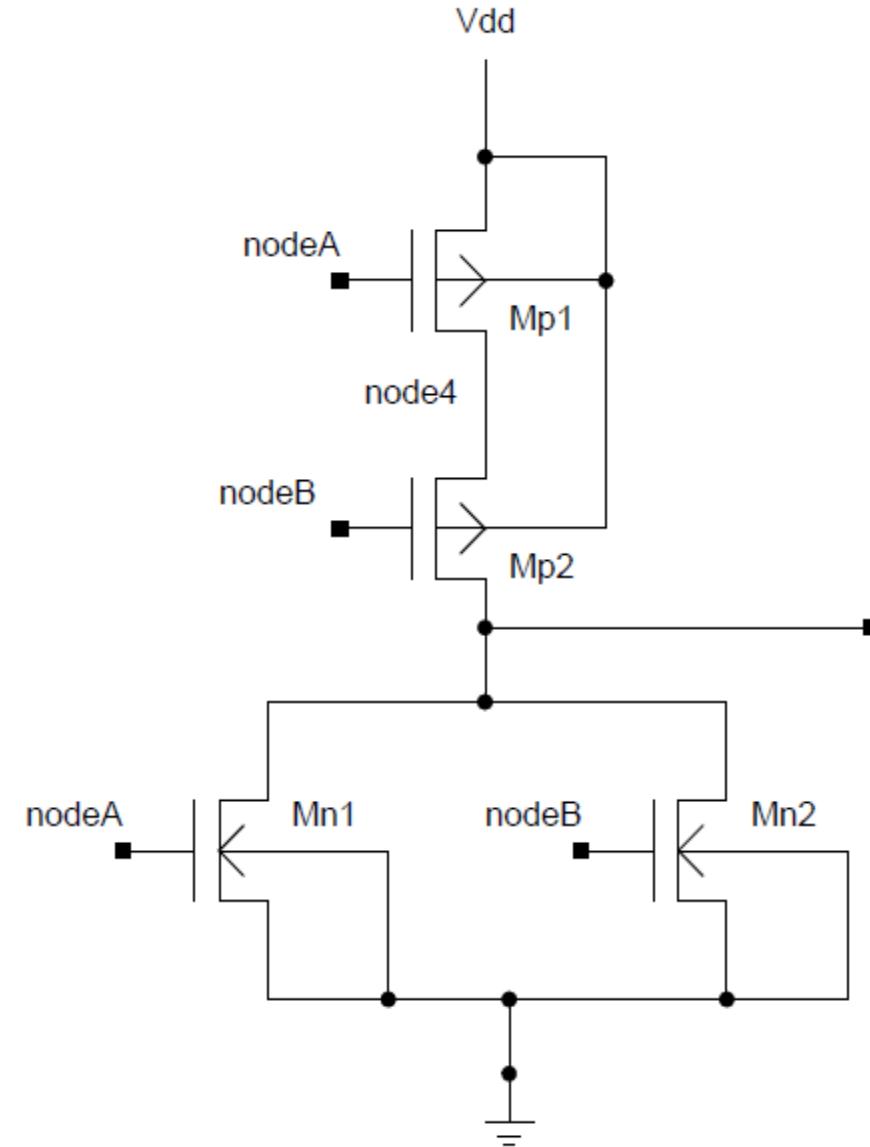
$$\tau_{phl} \cong 0.5 \times \frac{\tilde{C}_m V_{DD}}{\tilde{I}_{pd.}} + 0.5 \times \frac{\tilde{C}_L V_{DD}}{\tilde{I}_{pd.}}$$

$$\tau_{phl} (ps) \cong 42 + a \times C_L (fF); a = 3.25$$

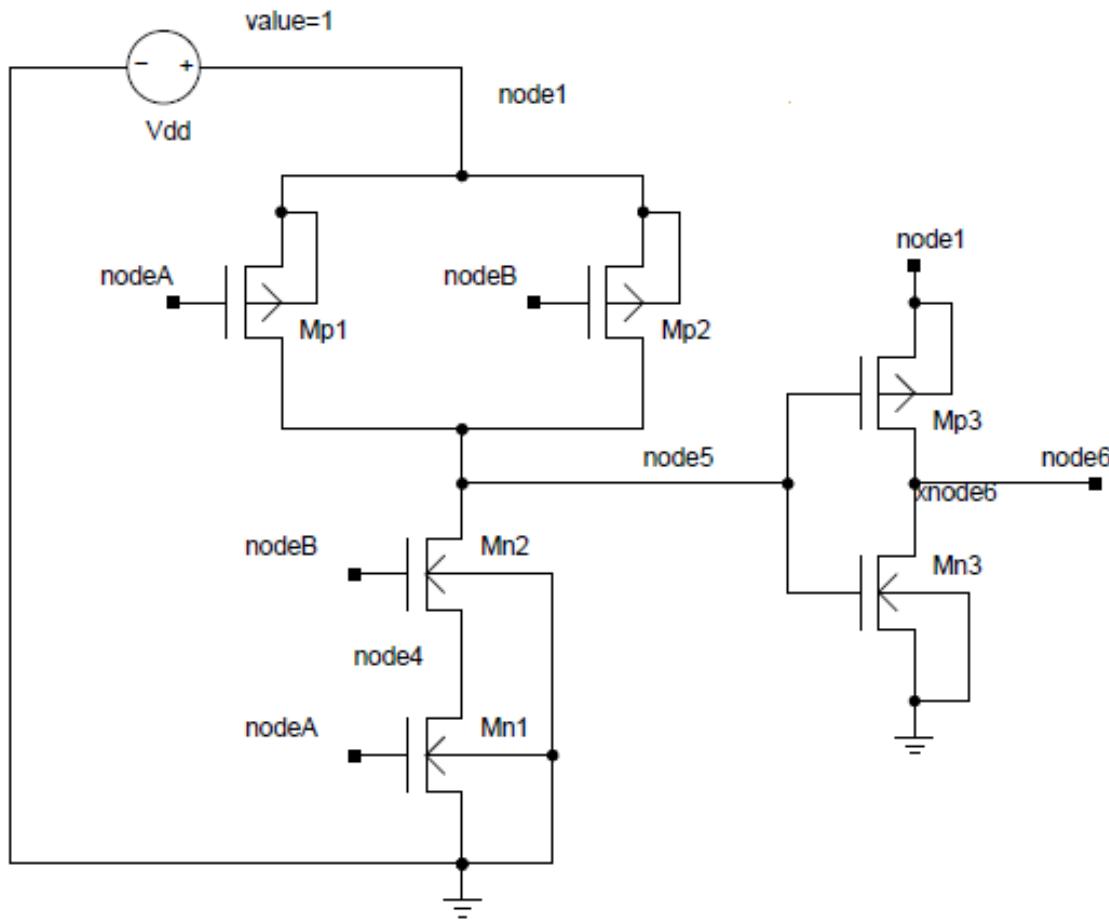
ps/fF or ns/pF



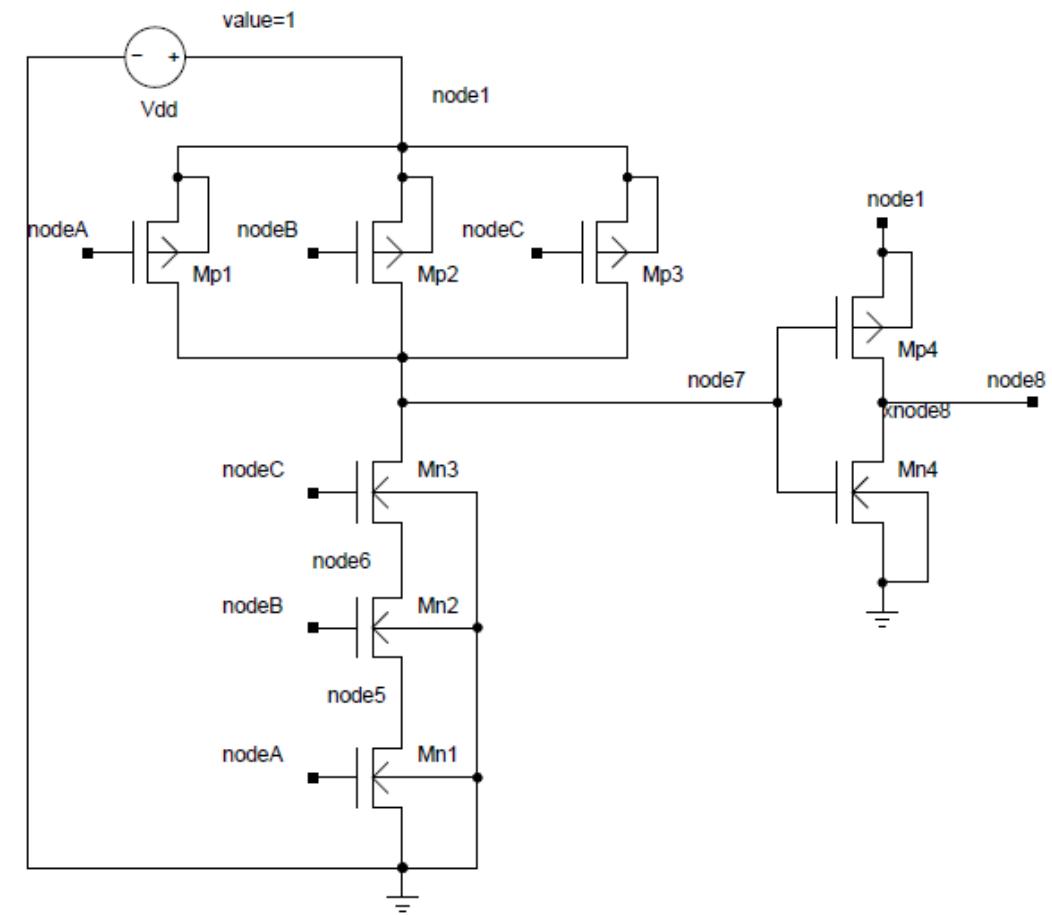
NAND2



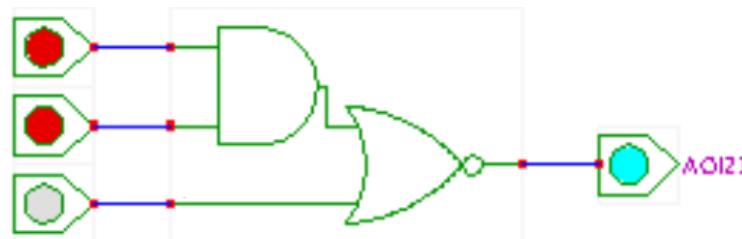
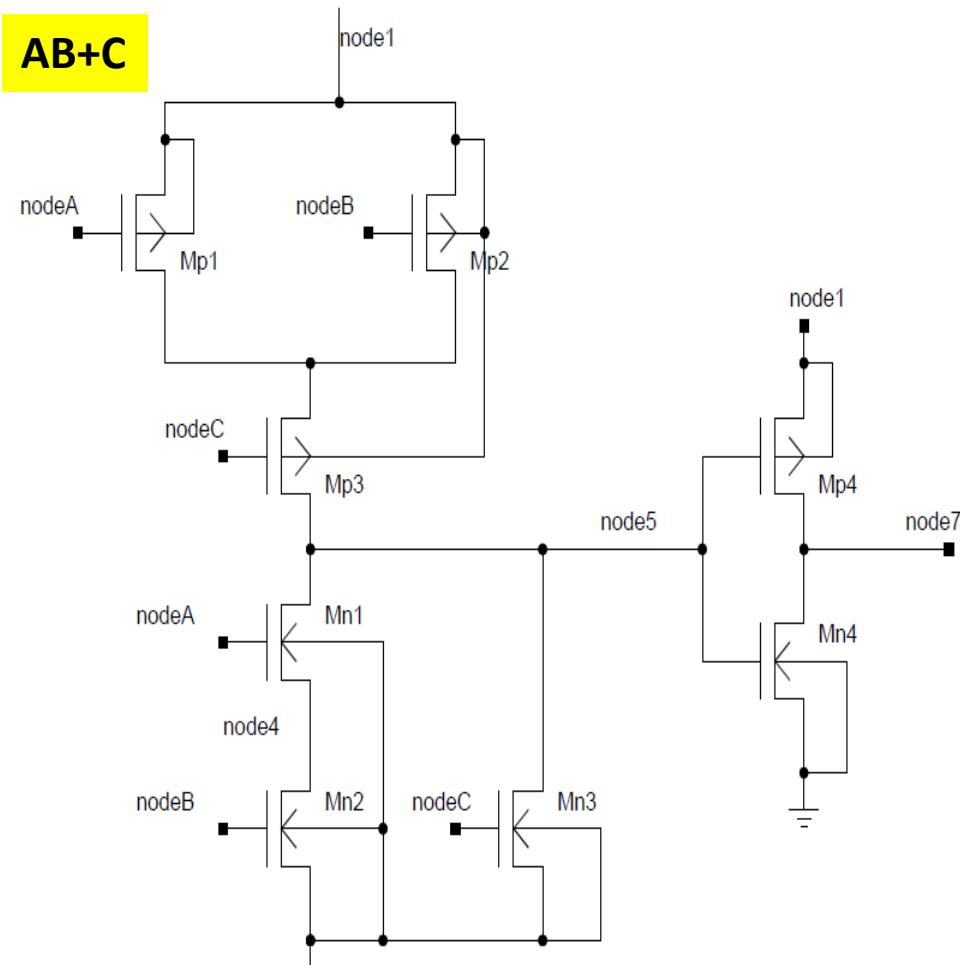
NOR2



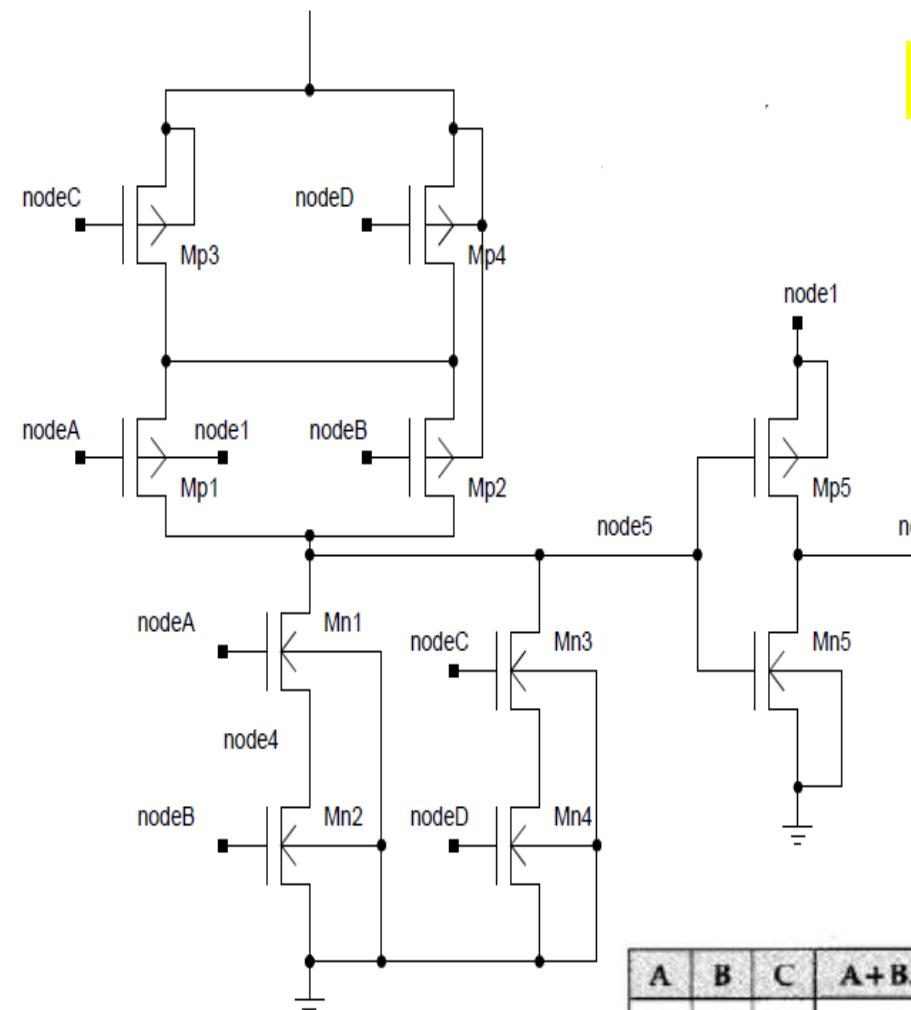
AND2



AND3

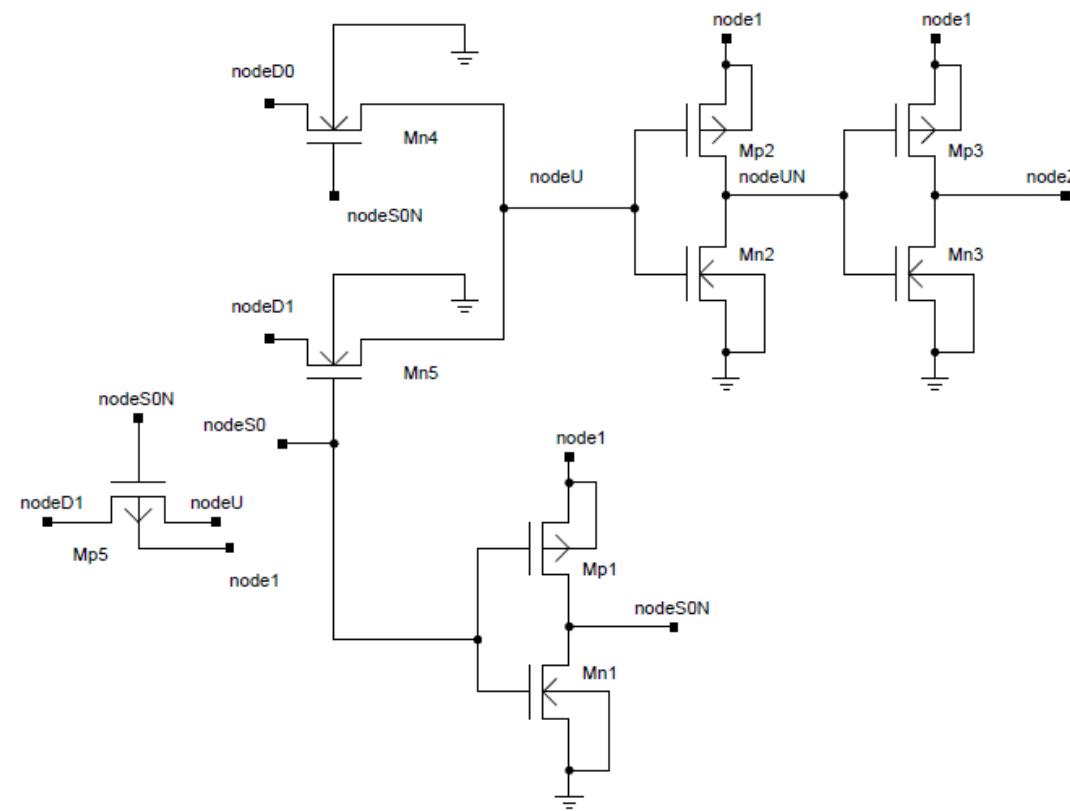
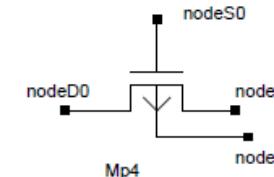
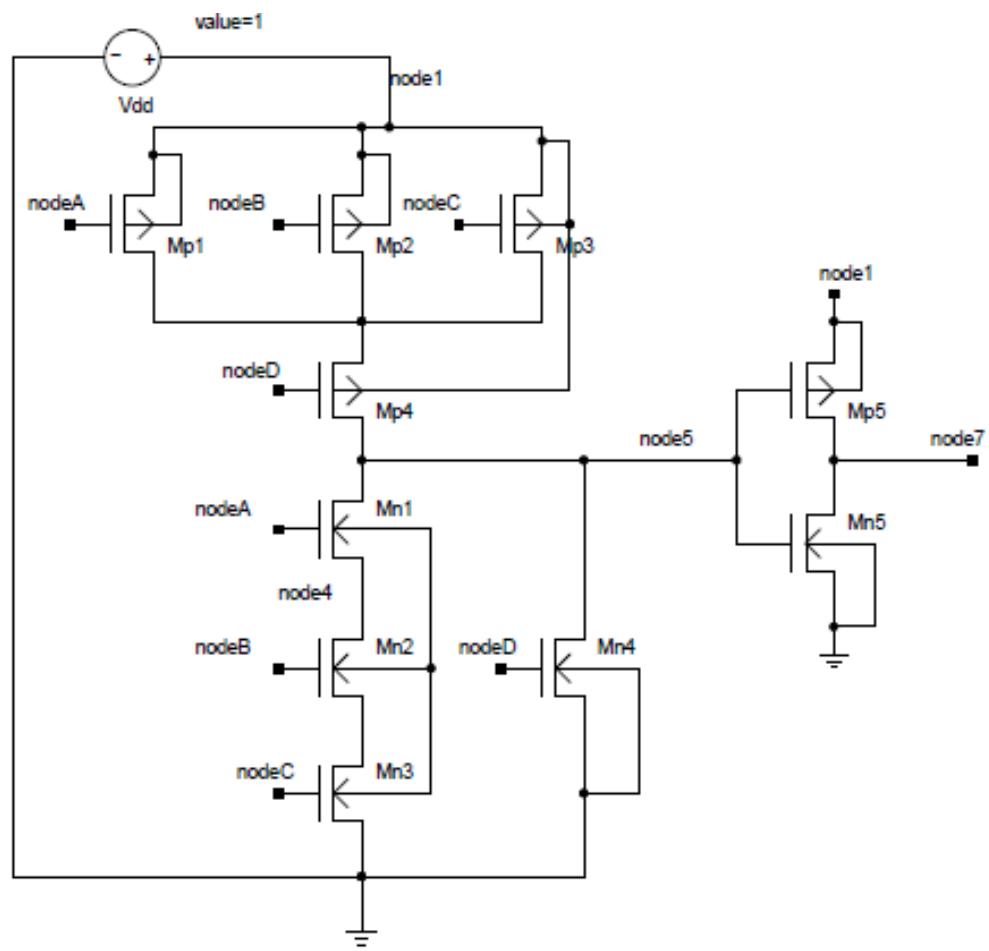
AB+C**AO12****Design****ABC+DE**

OAI21 (Or-And-Invert)

**AO22**

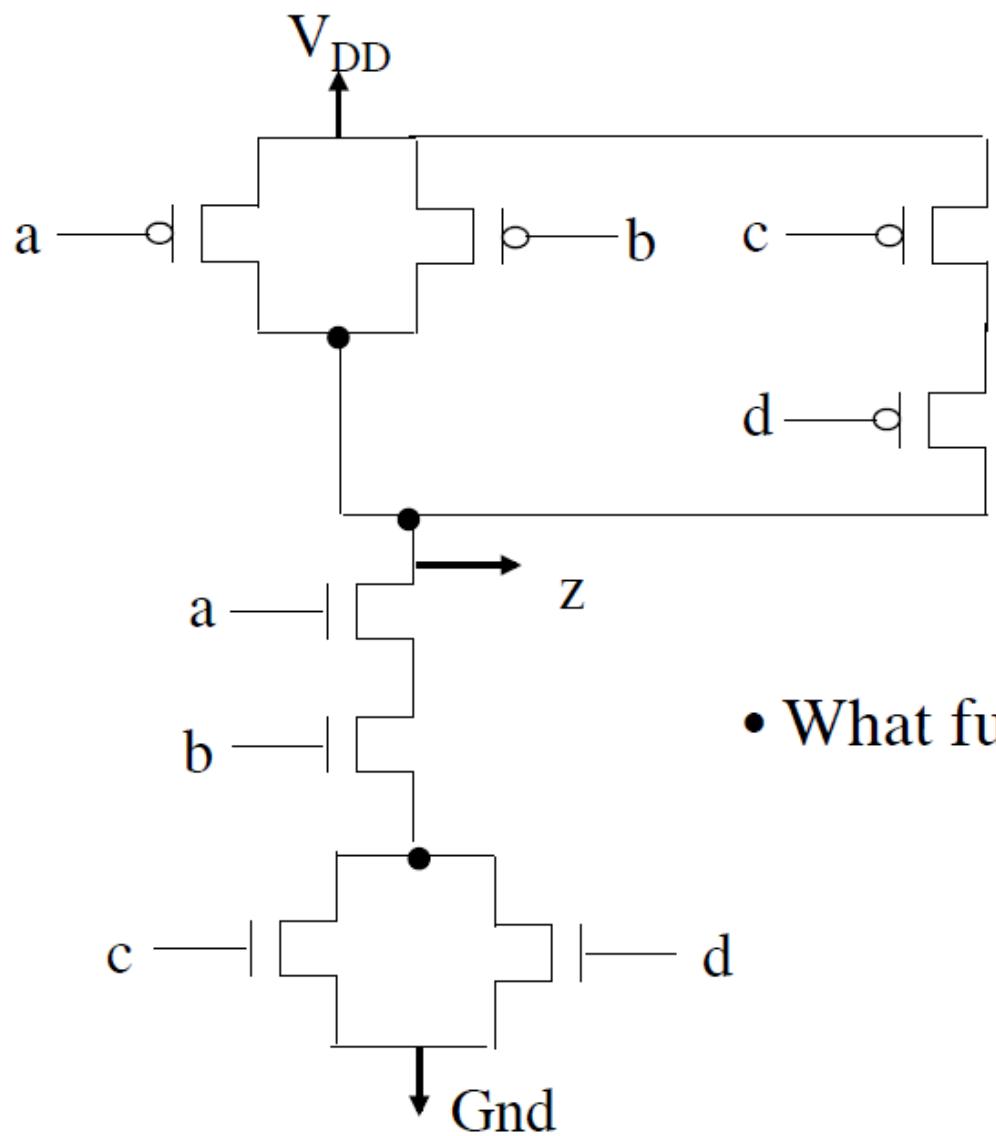
A	B	C	A+B.C	A+B	A+C	(A+B).(A+C)
0	0	0	0	0	0	0
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	1	1	1
1	0	0	1	1	1	1
1	0	1	1	1	1	1
1	1	0	1	1	1	1
1	1	1	1	1	1	1

AO31



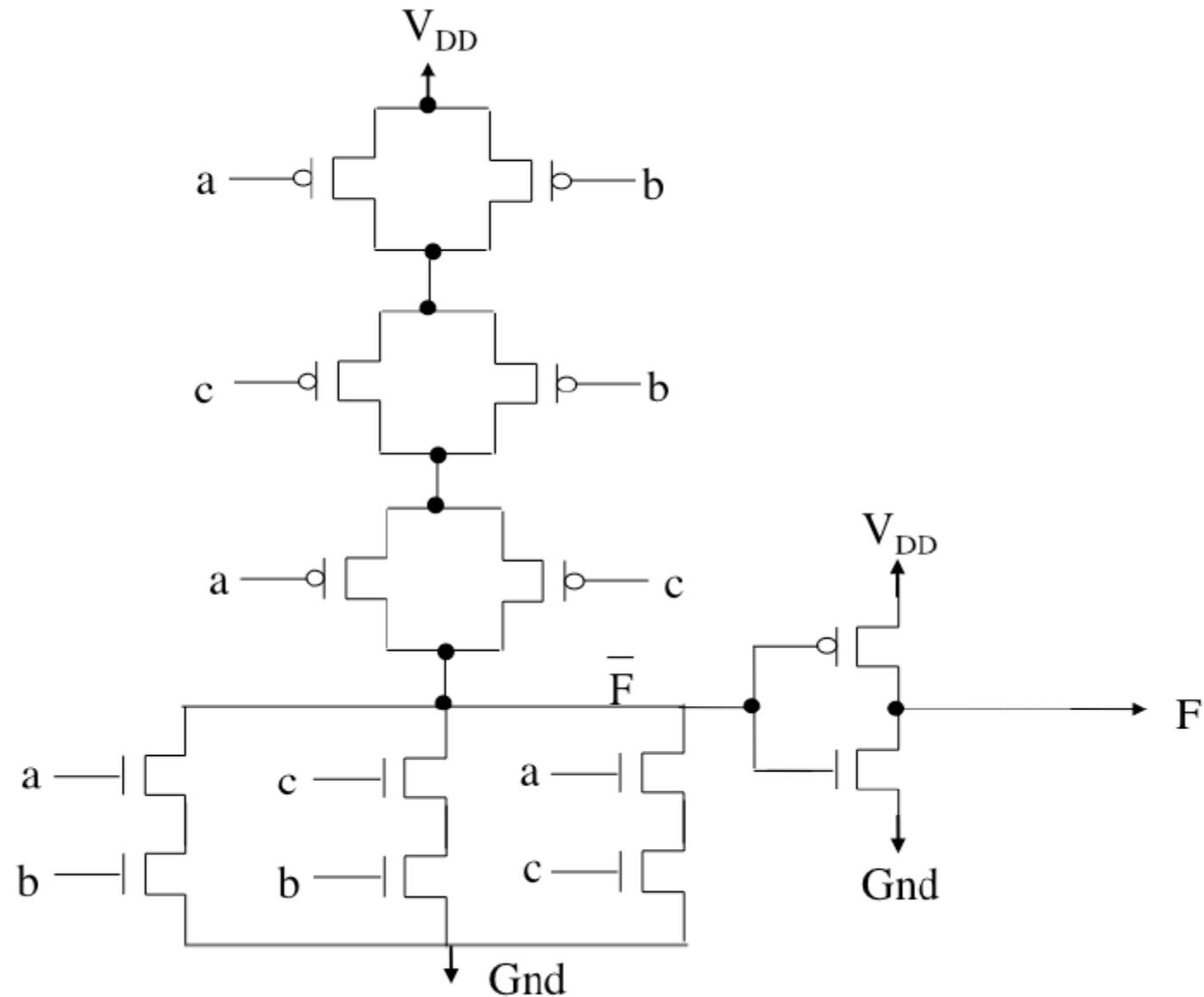
2:1 MUX

How to design? $Y = \overline{(A + B + C)} \bullet D$



- What function is implemented by this circuit?

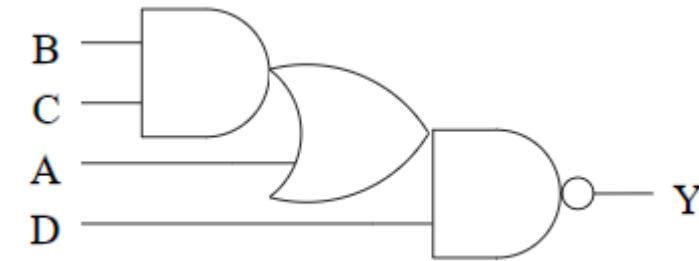
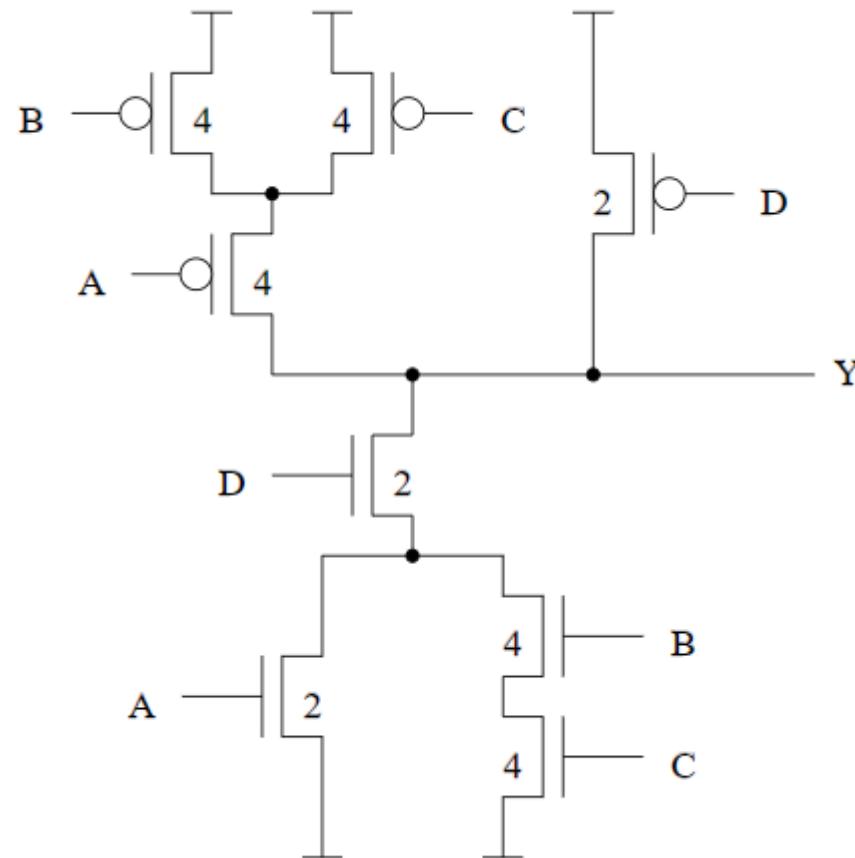
How to implement
 $F = ab + bc + ca$?

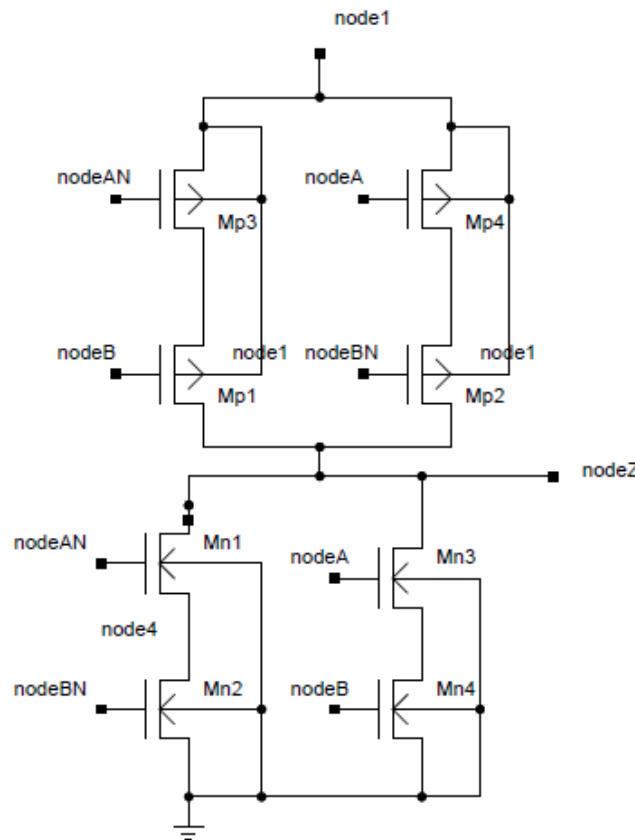
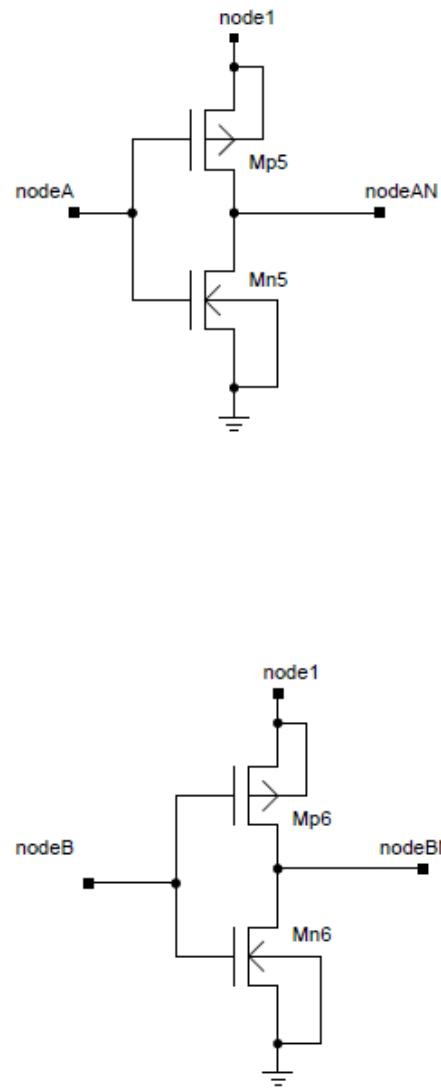


Besides the AOI and OAI gates for complemented two-level normal forms, we can design compound gates for multilevel expressions as well. For example, Boolean expression

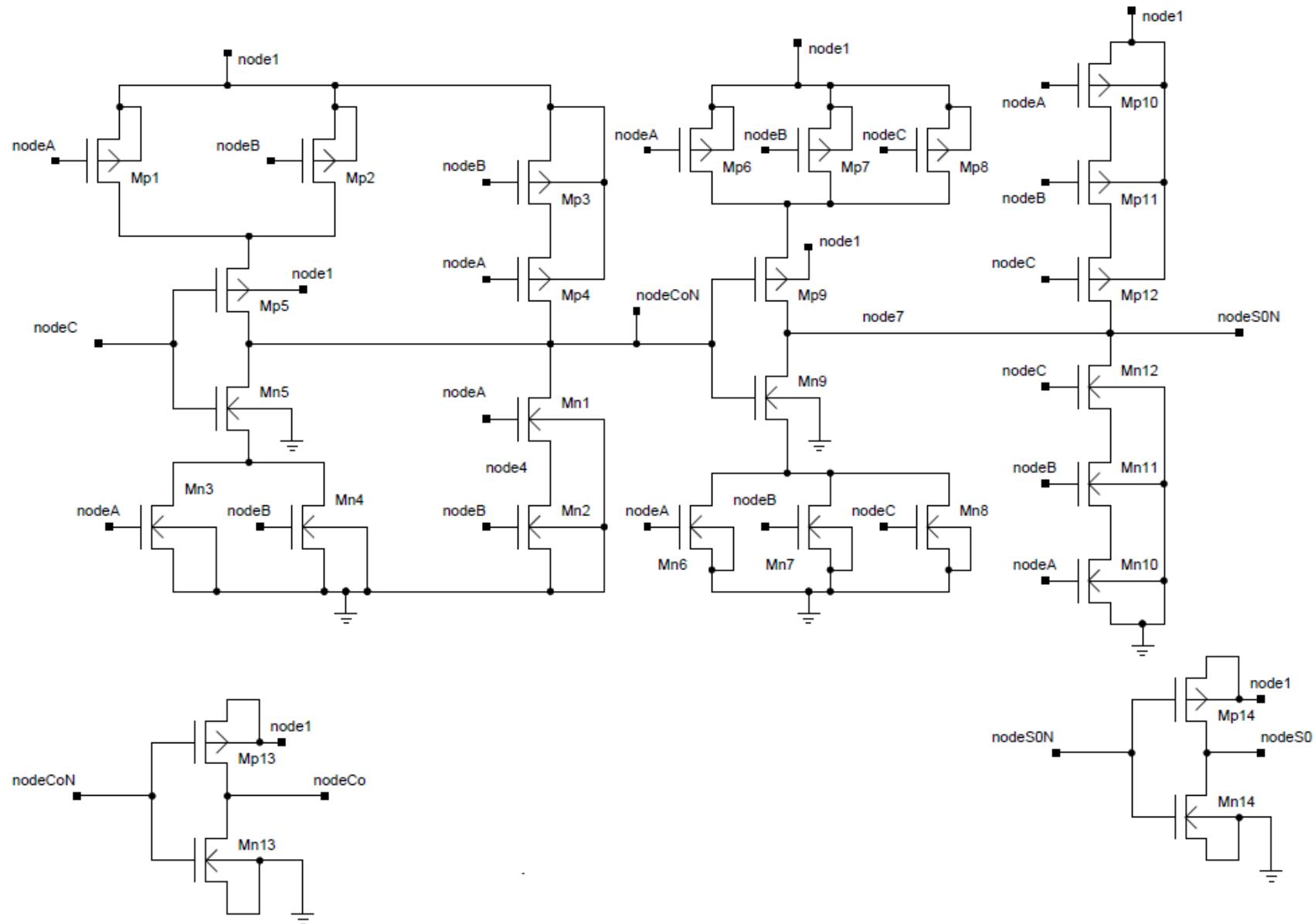
$$Y = \overline{(A + BC) \cdot D}$$

has a pull-down network consisting of a series composition of D and a parallel composition of A and a series composition of B and C .

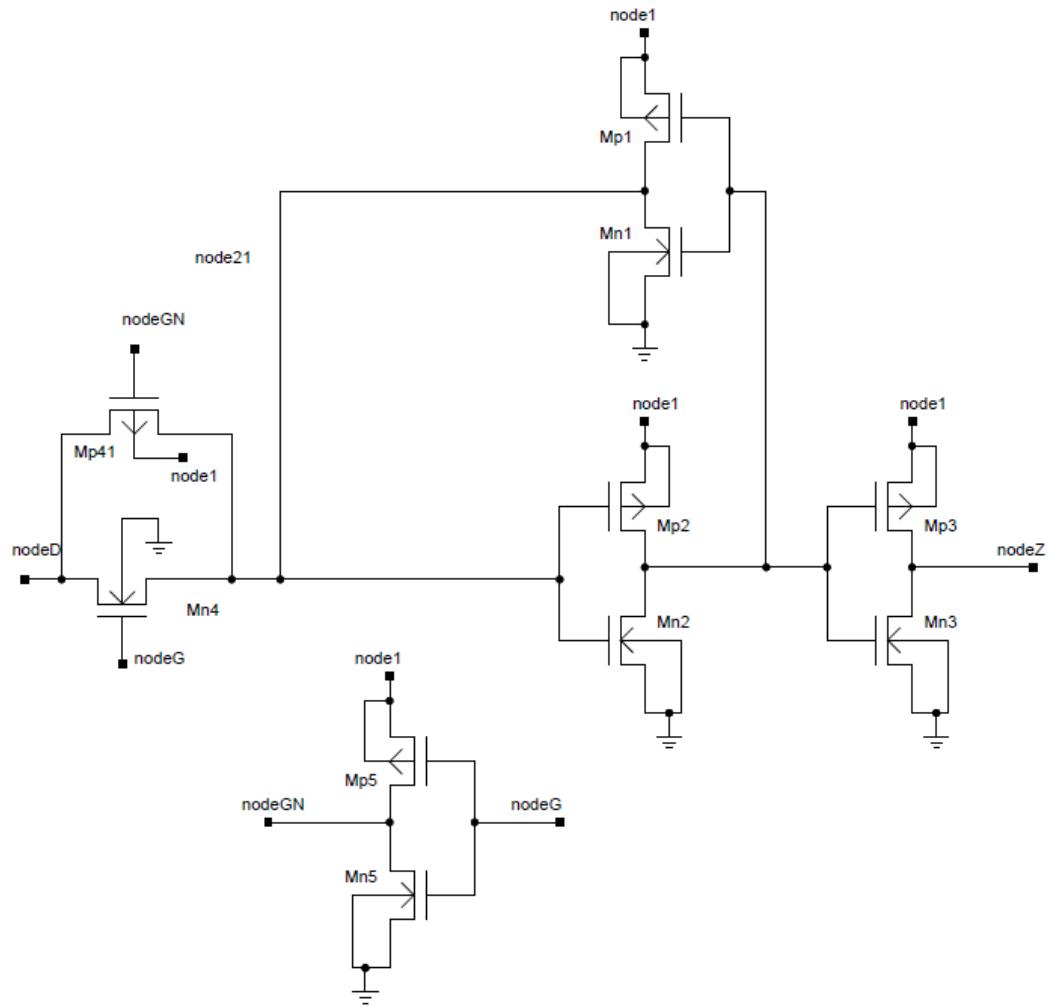




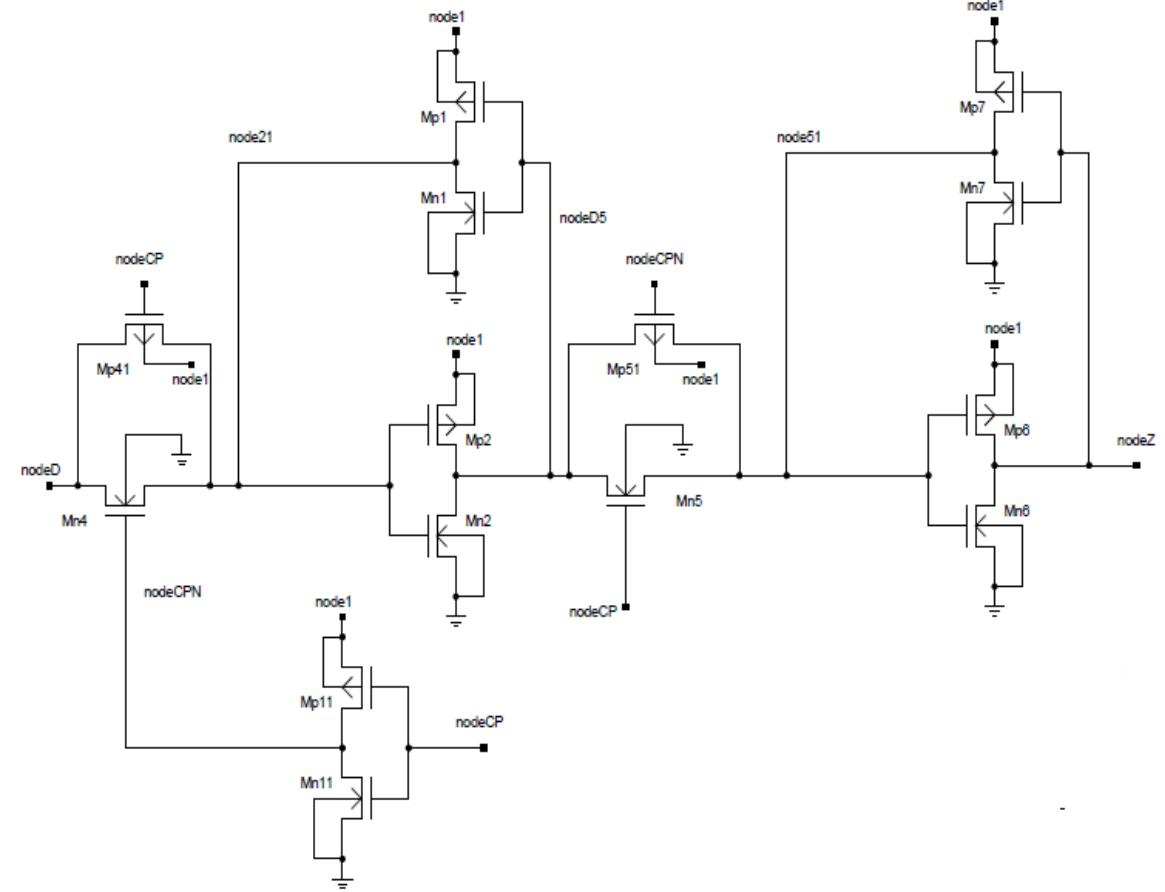
XOR2



Full Adder



LDHQ



DFPQ

