ECE: CMOS References and Regulators **(Date: 29/11/2024)**

End Semester Examination

Instructors: Prof. Abhishek Pullela and Dr. Zia Abbas *Max. Marks:* 125

Instructions:

- Write your assumptions (if required) for each question.

Problem 1 (4 x 4 = 16 Marks)

Fig.1 shows different architectures generating reference voltages. Derive the expressions for V_{REF} (as a function of PTAT and CTAT terms) in all cases and explain how they are invariant to different parameters (P/V/T). Also annotate the relative BJT sizes to be used (1x, 2x, Nx, etc) in each case. Which of these architectures is most suitable to be used in applications where supply voltage is 0.7V? Base current of BJTs can be assumed to be negligible. Assume op-amps to be ideal.

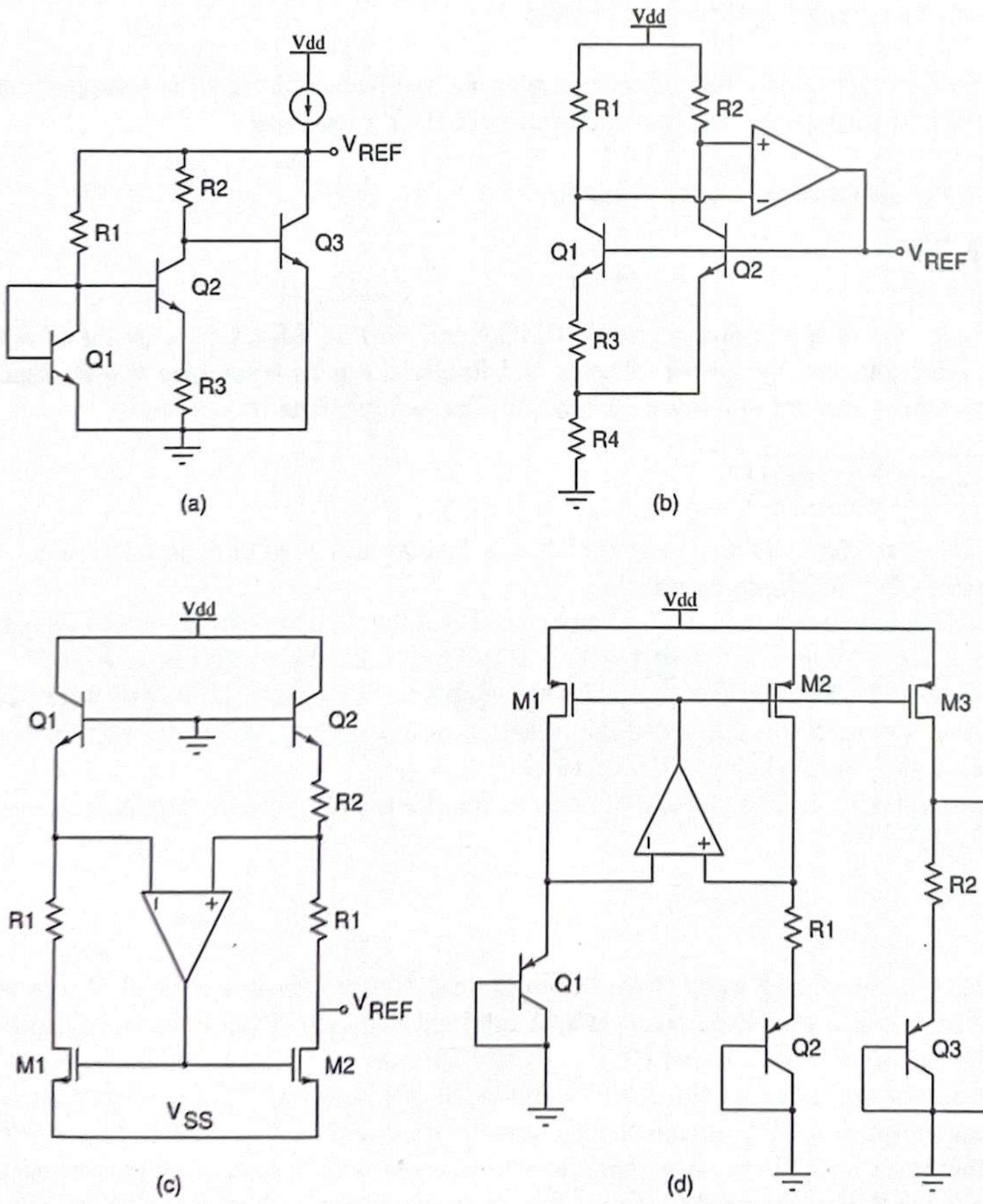

Figure 1

Problem 2 (5 + 20 = 25 Marks)

(a) Draw the circuit diagram of a PMOS LDO consisting of a sub-bandgap reference ,folded cascode op-amp followed by a source follower, and the final pass transistor stage using PMOS.
(b) Assuming the circuit is designed for some specifications and the sizes are fixed, explain the direct and indirect effects on stability, bias margins, speed, area, line regulation, PSRR, load regulation, systematic output variation, and start-up time when :
(i) sub-bandgap reference circuit is replaced by another voltage reference whose current is 100x less than sub-bandgap. Rest all components remain same.
(ii) Pass transistor size is decreased by 10x.
(iii) Current in folded cascode op-amp is decreased by 2x.
(iv) A miller capacitance is added from folded cascode op-amp output to final output.
(v) The beta factor is reduced by 4x.
(vi) A CS amplifier stage is added after folded cascode stage.
Note : All the cases (i), (ii), (iii), (iv), (v), (vi) are independent tests, not sequential.

Problem 3 (6 + 5 + 3 = 14 Marks)

(a) Draw two architectures for current references, one which has NO physical resistors and other having physical resistors. Tabulate the trade-offs by comparing these two circuits.

(a) Draw a PTAT generating architecture which doesn't contain physical resistors and works at a supply voltage of 0.5V. Write the expression for the output and explain the impact of PVT variations.

(b) Using the above PTAT voltage, generate a current reference.

Problem 4 (2 x 5 = 10 Marks)

Draw and explain the bode plots for output impedances of PMOS and NMOS LDOs (consisting of a voltage reference, differential amplifier followed by source follower and finally the pass transistor stage) when (a) output pole is dominant (b) op-amp poles are dominant. Make suitable assumptions if necessary.

Problem 5 (2 + 8 + 3 + 2 = 15 Marks)

A PMOS beta multiplier operating at 10nA current is used to bias a PMOS and NMOS composite pair.
(a) Draw the circuit configurations for the above description.
(b) What kind of temperature dependency the resistor should have if (i) similar Vth devices are used and current should be a reference. (ii) one of the PMOS is replaced by HVT PMOS and current should be a PTAT?
(c) The output voltages of PMOS and NMOS composite pairs are connected to NMOS and PMOS transistors respectively operating as switches (assume the drain voltage is biased accordingly). Write the expressions for switch resistances in both cases and analyze their PVT variations.
(d) Can a one native NMOS transistor be used as a start-up circuit for the PMOS beta multiplier in this case? Explain with suitable reasons.

Problem 6 (10 Marks)

A fully differential signal needs to be amplified using three fully differential amplifier stages as shown in Fig.2. The common mode voltages of inputs INP and INM are 70mV. A differential signal (square wave) of amplitude 70mV and frequency 800MHz is applied at the input (INP - INM). The three stages are biased with $50\mu A$, $70\mu A$, and $40\mu A$ current respectively and have an equal 3dB bandwidth of $(5/\pi)$GHz. Gains of stages are 2, 4 and 2 respectively. The total capacitance at the output of each stage can be assumed to be 5fF. Given NMOS, Native NMOS, and PMOS differential amplifiers with resistive and current source loads, which among them are best suitable to replace each of the three stages? Draw the complete diagram after calculating required parameters. Consider V_{TH} of PMOS and NMOS devices to be 0.6V and 0.5V respectively. V_{TH} of native oxide transistors can be taken to be 0V. Take λ of all devices to be $0.1V^{-1}$ and supply voltage to be 1.8V.

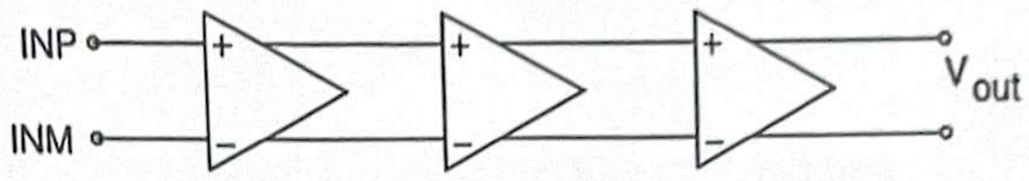

Figure 2

Problem 7 (2 + 2 + 6 = 10 Marks)

Consider the small signal circuit diagram shown in Fig.3. The op-amp and buffer are ideal. Assume L = 3.3μH, C = 10μF, R_{loss} = 50mΩ, $R_1 = R_2$ = 100kΩ.

(a) Draw the bode plot along with pole/zero expressions.

(b) For what values of C_{int} is the circuit stable?

(c) If the required UGB is 1MHz, prove that the system is unstable. To stabilize the system, resistors R_{int} and R_{esr} are added in series with C_{int} and C respectively. What are their suitable values to make the circuit stable?

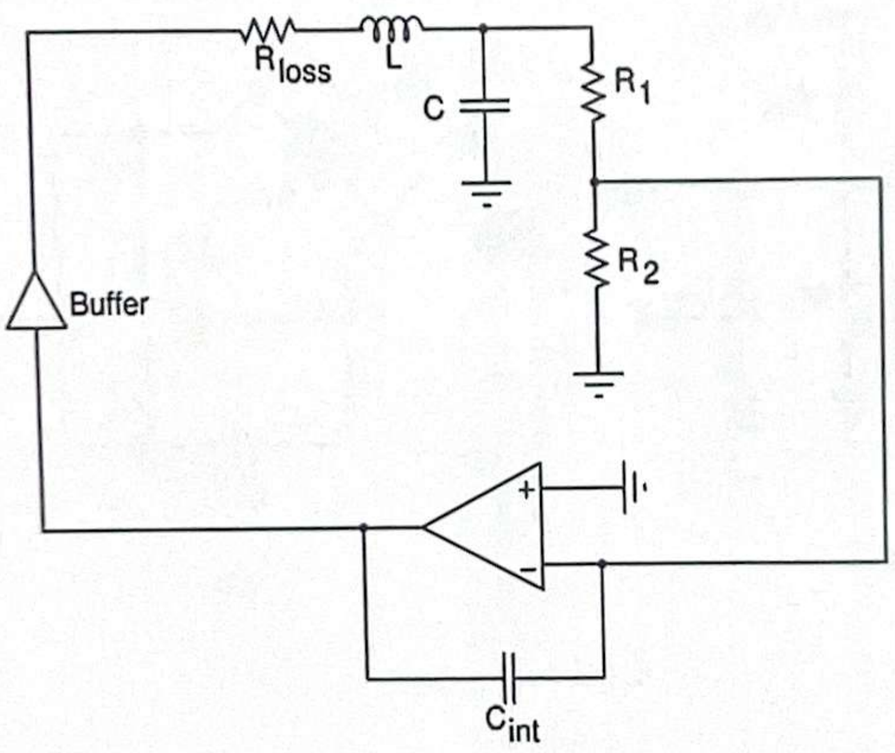

Figure 3

Problem 8 (2 x 2.5 = 5 marks)

Find the small signal gains V_{out}/V_{in} for the circuits shown in Fig.4 at DC. All other bias voltages can be assumed to be DC.

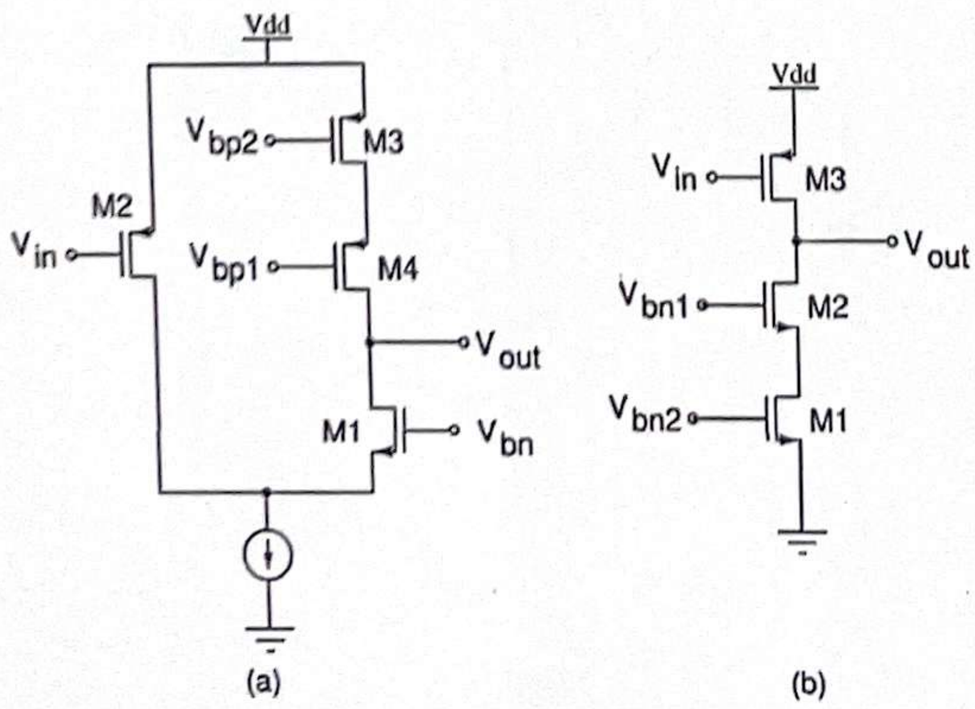

Figure 4

Problem 9 (2 x 2.5 = 5 Marks)

Plot the PSRR w.r.t frequency for (a) PMOS CS amplifier with source degeneration (b) PMOS CD amplifier.

Problem 10 (5 Marks)

An NMOS common-source amplifier with resistive load is driven by a sinusoid $V_{in} = V_0 + V_1 cos\omega t$ where V_0 is the biasing voltage and V_1 is large enough that it can drive the transistor into cutoff and triode regions (in negative and positive cycles of the sinusoid respectively). Sketch the transconductance g_m and output voltage V_{out} as a function of time. Mark the transition points (if any).

Problem 11 (2 x 5 = 10 Marks)

Plot the impedance w.r.t frequency for the circuits (by replacing NMOS with it's small signal model) shown in Fig.5 and mention the regions where the impedance is resistive, capacitive and inductive.

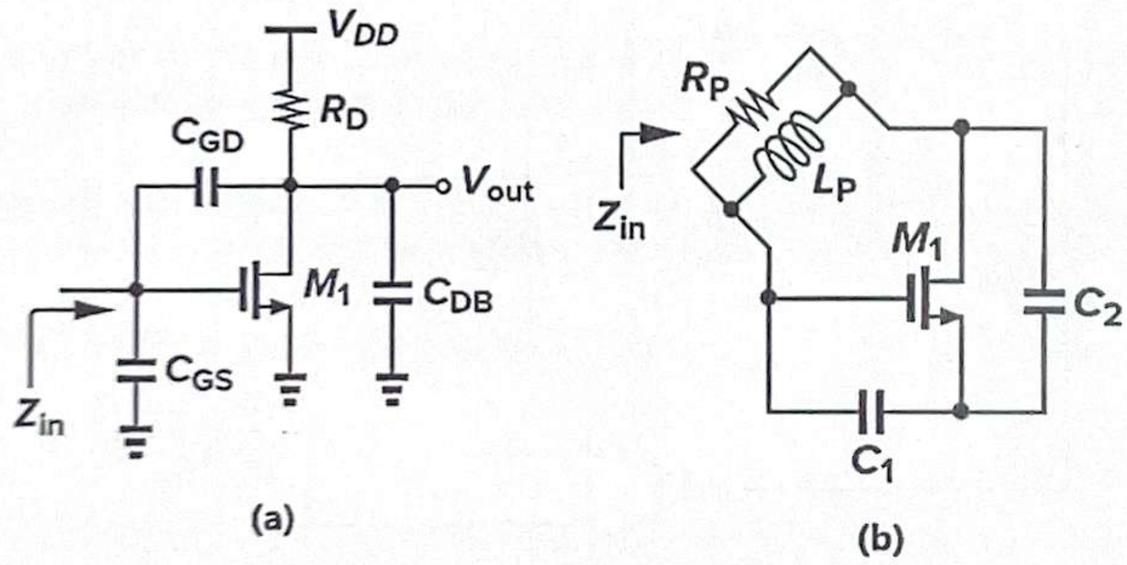

Figure 5