Analog IC Design : End Semester Exam

Spring 2025, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava, Center: CVEST)

Date : 28 April, 2025, Monday, Duration : 3 hr, Max. Marks : 30

Instructions:

1. Clearly write your assumptions (if any).
2. You are allowed to use your own handwritten notes (2 A-4 sheets) and calculators.

1. Consider the circuit shown in Fig. 1, where C_1 and C_2 set the closed-loop gain. Assume that M_2 is biased properly.

   (a) Determine the small-signal step response $v_{out}(t)$ of the circuit. [3 Mark]

   (b) Calculate the positive and negative slew rates. [3 Mark]

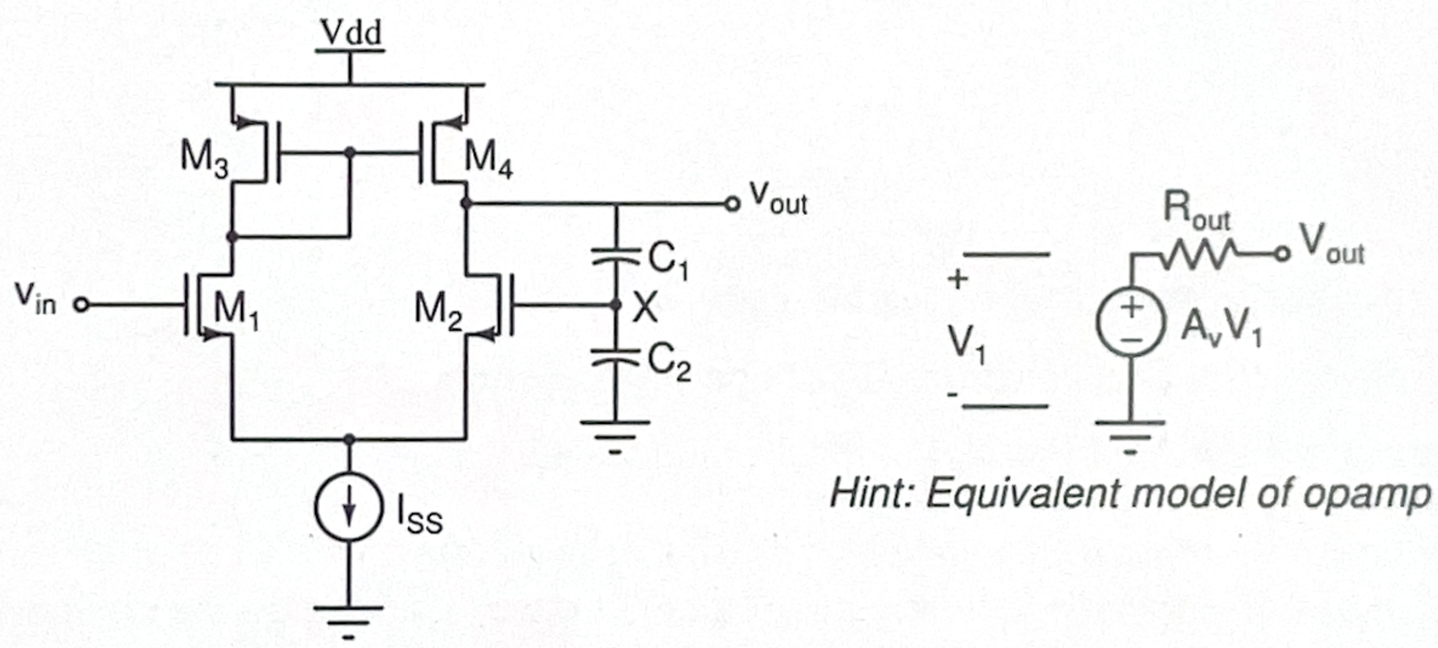

Figure 1

2. Consider a two stage Miller opamp (DACM followed by CS stage), where input transistors of both the stages (M_1, M_2, M_6) are operating in weak inversion. It can be assumed that the $r_0 \approx \frac{1}{\lambda I_D}$ in weak inversion also.

   (a) Show that the dc gain of the opamp is independent of I_D, while the gain bandwidth (GB) is not. [4 Mark]

   (b) Derive the slew rate as a function of GB. [2 Mark]

3. Eq. 2 represents the equivalent noise bandwidth (f_N) of a circuit, where A_{v_0} is the dc gain of the circuit and $A_v(s) = \frac{v_{out}(s)}{v_{in}(s)}$ is the voltage gain transfer function.

$$f_N = \frac{1}{A_{v0}^2} \int_0^{\infty} |A_v(jf)|^2 df \tag{1}$$

Total output noise (v_{nout}) integrated over this bandwidth can be given as

$$v_{nout}^2 = S_{in} A_{v_0}^2 f_N \tag{2}$$

where S_{in} is the input noise voltage spectral density.

   (a) Derive the relation between f_N and -3dB bandwidth (f_1) of an amplifier having single pole transfer function. [3 Mark]

(b) Calculate f_N and v_{nout} at the output of a single-pole amplifier having $A_{v_0} = 100$ and $f_1 = 27kHz$, when the noise source at the input is a resistor of value 22 $k\Omega$. Mention proper units at all steps. [3 Mark]

4. Consider the block diagram shown in Fig. 2. $v_{in}(f)$, $n(f)$, f_ϕ and f_{BW} are the input signal spectrum, noise spectrum, frequency of the square wave (50 % duty cycle) and BW of the amplifier, respectively. It is given that $f_{sig} = 20$ Hz, $f_{BW} = 6$ kHz and $f_c = 1$ kHz, respectively and the dc gain of the amplifier is 5.

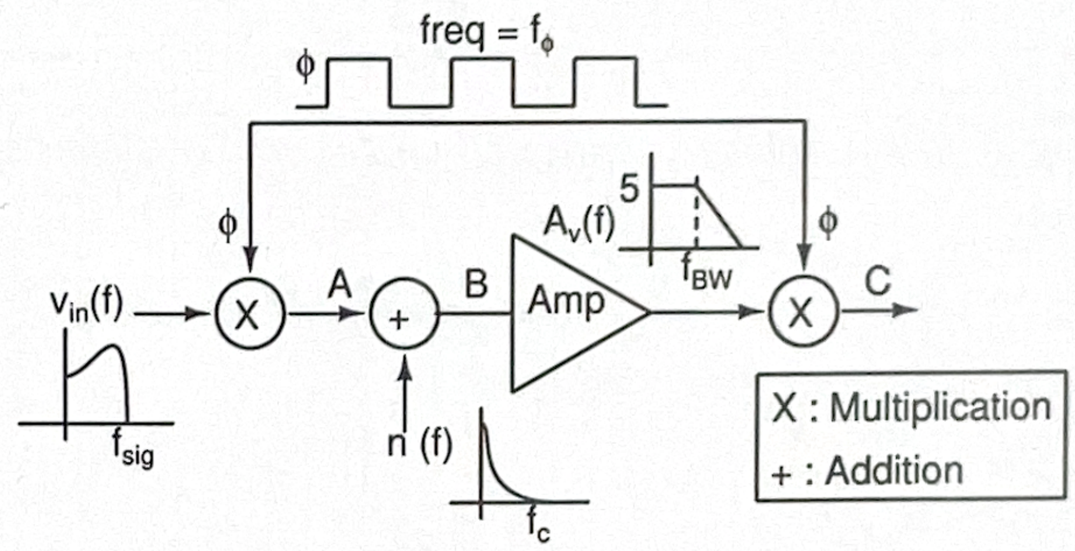

Figure 2

(a) Discuss the utility of the scheme shown in the Fig. 2. [2 Mark]

(b) Suggest a suitable value for f_ϕ with proper reasoning. [1 Mark]

(c) Draw the spectrums at A, B and C for the suggested f_ϕ. [3 Mark]

5. (a) Consider the circuit shown in Fig. 3. Biasing is not shown but all transistors are in saturation. C_L can be considered sufficiently larger than all other parasitics in the circuit. Find the expression for voltage gain, defined as $a_{cmc}(j\omega) = v_{oc}/v_{cmc}$. Also find dominant pole (P_D) and unity gain frequency for $a_{cmc}(j\omega)$. [3 Mark]

(b) How can the phase margin of $a_{cmc}(j\omega)$ be increased for constant tail current (I_{5h}) and constant C_L. Discuss the trade off of your methods? [3 Mark]

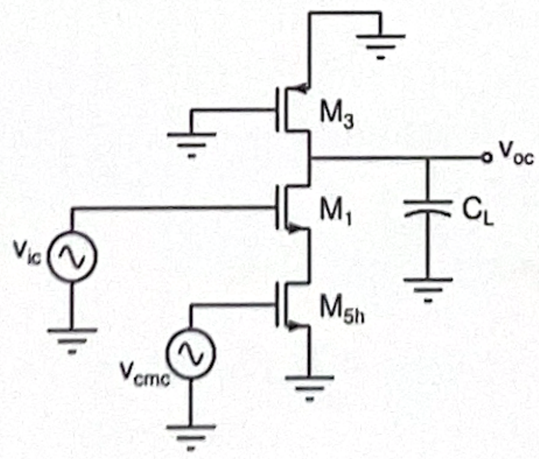

Figure 3

Good luck !!