ECE: CMOS References and Regulators **(Date: 21/09/24)**

Mid Semester Examination

Instructor: Prof. Abhishek Pullela and Dr. Zia Abbas *Max. Marks:* 60

Instructions:

- Write your assumptions (if required) for each question.

Problem 1 (3 + 5 + 2 = 10 marks)

(a) Briefly explain the accumulation, depletion and inversion regions in a PMOS transistor using a suitable diagram.
(b) Write the equations for drain current in a PMOS transistor in different regions of operation (triode, saturation, sub-threshold triode/saturation, cutoff).
(c) Plot the regions of operation of an NMOS transistor on a VDS - VGS graph.

Problem 2 (4 + 2 + 4 = 10 Marks)

Given a constant current source bias,
(a) Design circuits (can be partially block level) based on PNP transistors to generate PTAT and CTAT voltages. Also write the expressions for the voltages and explain how they are of PTAT or CTAT nature.
(b) The constant current source is passed into the drain of a PMOS transistor whose gate and drain are connected and source/bulk are connected to supply voltage. Write the expression for the drain voltage and analyse whether it's PTAT/CTAT, supply variant/supply invariant, process variant/process-invariant. Assume the transistor to be operating in saturation region. Find the worst case PVT corners for the transistor to go out of saturation.
(c) Generate PTAT and CTAT voltages using constant current source and NMOS transistors operating in sub-threshold region. Write the expressions for the voltages and explain how they are of PTAT and CTAT nature.

Problem 3 (2 + 3 + 3 = 8 Marks)

Given an NMOS Widlar current mirror (assume bias current is constant w.r.t PVT and mirroring ratio need not be a whole number) whose mirrored branch current is passed into a PMOS simple current mirror.
(a) Draw the circuit diagram for the above description and explain how it works as a current mirror.
(a) Write the expression for the voltage across resistor in the widlar current mirror. How do you make this voltage of PTAT nature?
(a) Assuming resistor to be a CTAT and all transistors to be operating in sub-threshold region, find the worst case PVT corner for each transistor.

Problem 4 (5 + 8 + 5 = 18 Marks)

(a) Draw the configurations of PMOS simple, widlar, self-cascode, resistor based low voltage cascode, external bias based low voltage cascode and high voltage cascode current mirrors.
(b) Write the expressions for minimum supply voltages required for each of them. Which of them consume the least and the highest headroom?
(c) Write the expressions for output resitances of the current mirrors and compare them.

Problem 5 (4 Marks)

A voltage buffer is a black box which gives an output exactly equal to the input. In a voltage buffer, the current flowing through its input terminal is exactly zero. Such a voltage buffer (as shown in Figure 1(b)) is used in a simple linear network as shown in Figure 1(a).

Consider the following conditions in the circuit diagram of Figure 1(a) :
All the capacitors are initially charged to 1V. V_{in} is a DC voltage of value 1V. Now, Vin is increased suddenly by a small amount 1mV. Analyze the change at the output V_{out}.

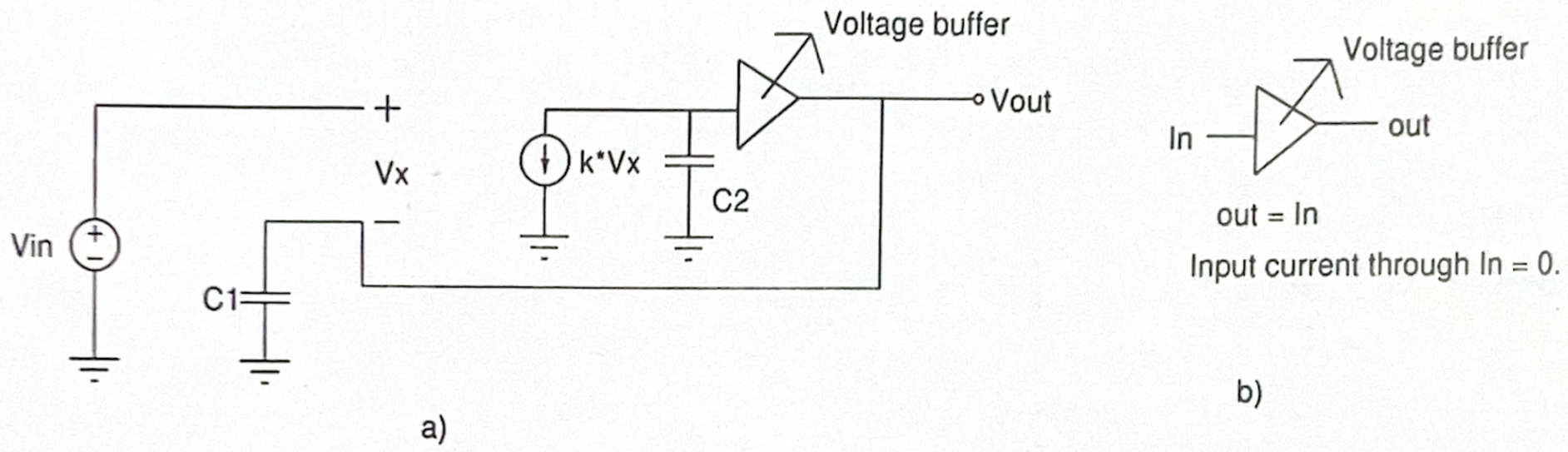

Figure 1

Problem 6 (2.5*4 = 10 Marks)

Find the expressions V_{out}/V_{in} for the circuits shown in Fig.2 when a small signal is applied at V_{in}. Assume that transistors are biased in saturation region.

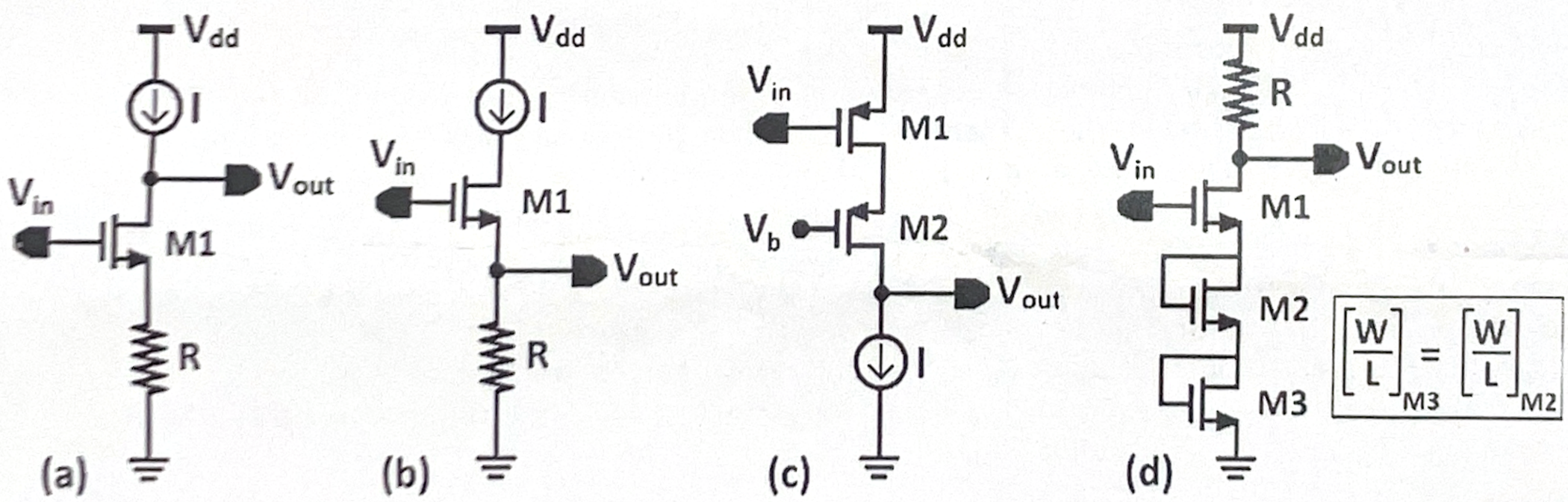

Figure 2