Analog IC Design : Quiz-1

Spring 2025, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava, CVEST)

Date : 7-Feb, 2025, Duration : 1 hr 15 min, Max Marks : 20

Instructions: 1) Clearly write your assumptions (if any), 2) Only 1 own hand written A4 sheet allowed, 3) **Do not ignore** channel length modulation or body effect unless stated

1. Consider the circuit shown in Fig. 1. Assume that M_1 and M_2 transistors are in saturation and have transconductance of g_{m1} and g_{m2}, respectively. V_B is the DC bias voltage.

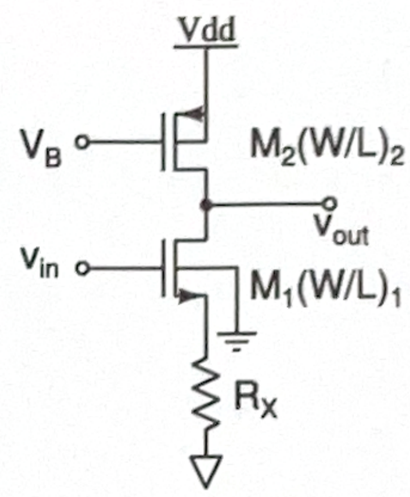

Figure 1

(a) Draw the low frequency small signal equivalent and derive effective transconductance (G_m) and output impedance (R_o) at the v_{out} of the circuit. What is the DC voltage gain ($A_{v1} = \frac{v_{out}}{v_{in}}$) expression for the circuit. [3]

(b) Plot G_m with respect to V_{IN}, where V_{IN} changes from 0 to VDD. What will be the approximate G_m value for smaller overdrive voltage and higher overdrive voltage of M_1, discuss briefly. [2]

(c) If the circuit is modified by replacing M_2 by an ideal current source, then find the DC gain (A_{v2}) expression for the circuit. Briefly discuss what advantage or disadvantage the original circuit will have as compared to the modified one. [2]

2. Current expressions for weak inversion (WI), strong inversion (SI) and velocity saturation regions in the BSIM6 models are given below *(Ref: Hodges, JSSC, 1968, Cunha, JSSC, 1998, Sansen, ICECS, 2013, ISSCC 2015)*

$$I_{DS} = I_{SP}.exp\left(\frac{V_{GS} - V_T}{nU_T}\right) \ (Weak\ Inversion) \tag{1}$$

$$I_{DS} = K'\frac{W}{L}(V_{GS} - V_T)^2 \ (Strong\ Inversion) \tag{2}$$

$$I_{DS} = WC_{OX}v_{sat}(V_{GS} - V_T) \ (Velocity\ Saturation) \tag{3}$$

where, $I_{SP} = K'\frac{W}{L}(V_{GS} - V_T)^2$ is the specific current at the boundary of WI and SI region, which is defined at $V_{GS} = V_{SP} = V_T + 2nU_T$. Other parameters are as follows: $K' = \frac{\mu C_{OX}}{2n}$, $n = (1 + \frac{C_D}{C_{OX}})$, C_D is the capacitance between channel and bulk, C_{OX} is the oxide capacitance, $U_T = \frac{kT}{q}$, k is the Boltzmann constant, and $v_{sat} = 10^7\ cm/s$. Some parameters are also defined as follows: transition frequency $f_T = \frac{g_m}{2\pi C_{GS}}$ and specific conductance $G_{SP} = \frac{I_{SP}}{nU_T}$.

Also given that Inversion Coefficient ($IC = \frac{I_{DS(region)}}{I_{SP}}$), for example, in WI $IC = \frac{I_{DS(WI)}}{I_{SP}} = exp\left(\frac{V_{GS}-V_T}{nU_T}\right)$, in SI $IC = \frac{I_{DS(SI)}}{I_{SP}} = \left(\frac{V_{GS}-V_T}{2nU_T}\right)^2$. It is given that for WI $IC < 1$, for SI $1 < IC < \frac{1}{\lambda_c{}^2}$, for velocity saturation $IC > \frac{1}{\lambda_c{}^2}$, where Lambda-C $\lambda_c = \frac{L_{sat}}{L} = \frac{2\mu U_T}{v_{sat}L}$. For 65 nm technology $n = 1.3$, $\lambda_c = \frac{1}{\sqrt{10}}$, $\mu = 400\ cm^2/s$, $U_T = 26$ mV at room temperature.

(a) Derive transconductance (g_m) as a function of $f(G_{SP}, IC, \lambda_c)$ only for all the three regions. [3]

(b) Plot g_m vs IC clearly marking the graph proportionality with respect to IC in the three regions (for example $g_m \propto IC^2$ etc). [1.5]

(c) Derive $\frac{g_m}{I_D}$ as a function of IC. Plot $\frac{g_m}{I_D}$ vs IC clearly marking the graph proportionality with respect to IC in the three regions. Which is the highest g_m efficiency region. [3]

(d) Plot f_T vs IC clearly marking the graph proportionality with respect to IC in the three regions. [1.5]

(e) Plot $f_T \times \frac{g_m}{I_D}$ vs IC clearly marking the graph proportionality with respect to IC in the three regions. [1.5]

(f) Which region would you like to operate in for minimum power, maximum speed and optimal power-speed. Discuss briefly using the plots obtained above. [1.5]

(g) Will the optimal power-speed region shrink or expand with technology scaling. Explain from the plots. [1]

Good luck !!