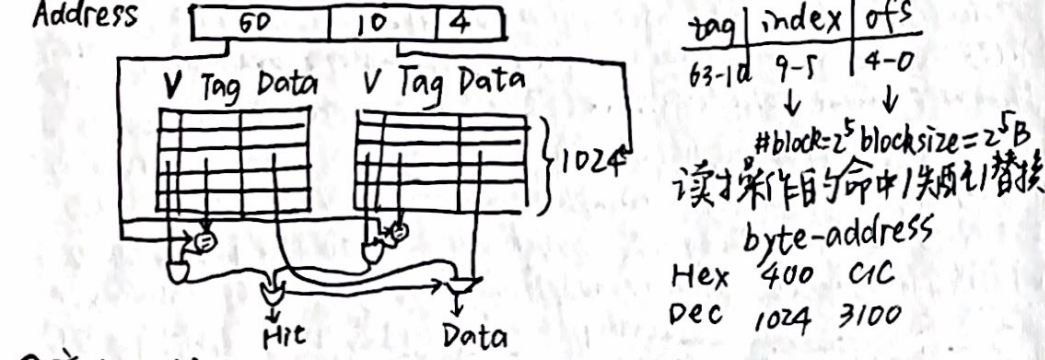


cache data size = 32KB, block size = 2word, word size = 64bit  
 byte-addressed (如果是word-addressed, ofs=2) 共有10byte  
 ① block size = 16B → block ofs = 4bit (地址中的-1代表一个byte)  
 ② cache data size = #blocks × block size, #blocks =  $\frac{32KB}{16B} = 2^{11}$   
 ③ 对于direct-mapped, #sets = #blocks =  $2^{11}$  → index = 11bit  
 tag = 64 - 4 - 11 = 49bit  
 ④ 对于2-way组关联, #sets = #blocks =  $2^{10}$  → index = 10bit  
 关联度是前深  
 tag = 64 - 4 - 10 = 50bit 如果是full-way, 不需要index

① cache total size = (valid + tag + block size) × #blocks  
 直接映射 =  $(1 + 49 + 16 \times 8) \times 2^{11} = 44.5KB$  (得2<sup>13</sup>得KB)  
 2-way =  $(1 + 50 + 16 \times 8) \times 2^{10} = 366592bit = 44.75KB$



① 方法一, 写成二进制地址  
 addr(16) addr(2) tag index ofs h/m content  
 400 010000000000 1 0 0 m Mem[400]-Mem[41F]  
 300 110000001100 3 0 28 m Mem[300]-Mem[31F]  
 ② 方法二, 使用十进制  
 addr(16) ofs index tag content  
 1024 1024%32=0 1024/32=32 1 32×32=1024  
 3100 3100%32=28 3100/32=96 3 96×32=3072  
 Write Hit - write back: 只改cache, 需dirty bit, 1个字的buffer  
 write through: 同时改cache和mem, buffer最小只要2word  
 Write Miss - write allocate: 先读入cache, 再写  
 write around (no write allocate): 不读入cache, 直接改mem

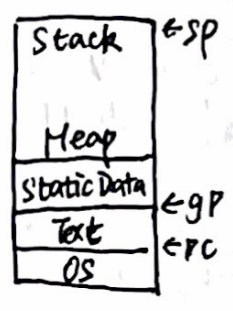
根据需求: memory用DRAM, cache用SRAM。DRAM分成①classic异步②SDRAM(synchronous)同步③DDR SDRAM 2倍速率④DDR2 4倍速率  
 temporal locality, 时间局部性, 其本身在之后会访问; spatial ~, 空间局部性, 增大block size可以提高。Hierarchy: L1 cache(片上) → L2 cache → Main Memory → Disk。常用的替换策略: Random, FIFO, LRU(如2-way, 使用Ref bit) Memory Design 1个周期送读信号, 15个周期读内存, 1个周期送回data, block size = 4word, 1word = 4byte ① 1-word-wide memory, bandwidth = bytes/clock cycle. time to transfer 1 block (miss penalty) = 1 + 4 × (15 + 1) = 65 CLKs, bandwidth =  $\frac{4 \times 4}{65} = \frac{1}{4}$  ② 4-word wide, miss penalty = 1 + 15 + 1 = 16, bandwidth =  $\frac{16}{17}$  ③ 4-way interleaved 并行从4个memory bank读4个word, miss penalty = 1 + 15 + 4 × 1 = 20  
 miss rate = 100次10失配n次, misses/inst = 100  
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 0 1 2 3  
 4 5 6 7  
 8 9 10 11  
 12 13 14 15  
 16 17 18 19  
 20 21 22 23  
 24 25 26 27  
 28 29 30 31  
 32 33 34 35  
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 60 61 62 63  
 64 65 66 67  
 68 69 70 71  
 72 73 74 75  
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```
fib(int i) i-x10, fib(i)-x10
if(i==0) return 0;
else if(i==1) return 1;
else return fib(i-1)+fib(i-2);

b: beq x10, x0, done
addi x5, x0, 1
beq x10, x5, done
addi x2, x2, -8
sw x1, 0(x2)
lw x10, 4(x2)
addi x10, x10, -1
jal x1, fib
lw x5, 4(x2) // x5=i
```

```
sw x10, 4(x2) // push fib(i-1) on stack
addi x10, x5, -2
jal x1, fib
lw x5, 4(x2) // x5=fib(i-1)
add x10, x10, x5
lw x1, 0(x2)
addi x2, x2, 8
done:
jalr x0, &0(x1)
```



caller save: x1 (ra), argument, 重要寄存器; callee: s 寄存器压栈

Inst	ALUop	RW	ALUSrc2	MR	MzR	MW	Imm	taken	jal	lui	jalr
ALUWR	f3/7	1	0(rs2)	0	0	0	X	0	0	0	0
ALUWZ	f3	1	1(imm)	0	0	0	Iz	0	0	0	0
load	+	1	1	1	1	0	Iz	0	0	0	0
jalr	+	1	1	0	X	0	Iz	1	0	0	1
store	+	0	1	0	X	1	Sz	0	0	0	0
branch	cmp	0	0	0	X	0	Sz	Xcmp	0	0	0
jal	X	1	X	0	X	0	Uz	1	1	0	0
lui	X	1	X	0	X	0	Uz	0	0	1	0

latency = time between inst issued and complete; throughput = 每秒完成的指令条数。结构竞争解决方式①分离IMem和DMem,防止IP和MEM撞车②对于RegFile, 页地址写, 随后读(double bump)③流水线不流水, 或增加流水级数(not common case) 数据竞争成因: 数据依赖关系, RAW, WAR, WAW (乱序流水线上可能会有竞争)

Way 1. Stall (硬件或软件插入nop)

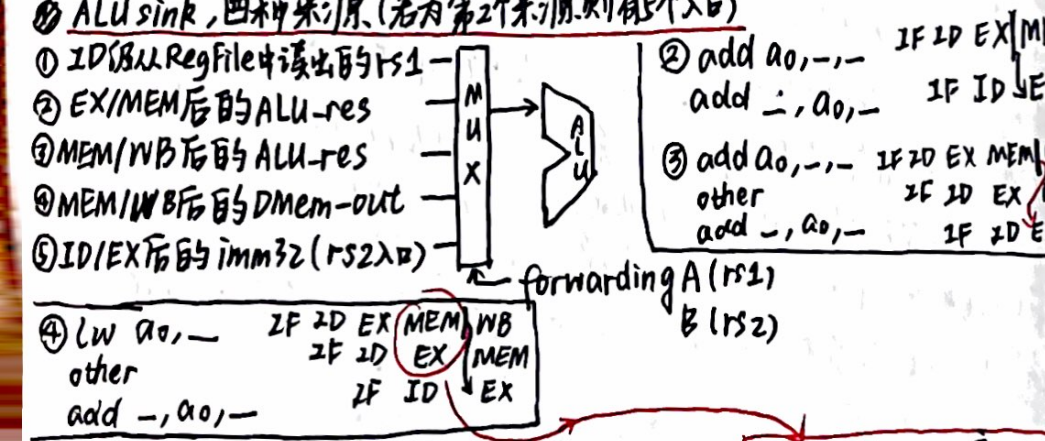
① add a0, --, -- IF ID EX MEM WB  
nop add --, a0, -- IF ID 0 0 } 停2拍  
nop IF ID 0  
IF ID

② add a0, --, -- IF ID EX MEM WB  
other IF ID EX MEM  
nop add --, a0, -- IF ID 0 停1拍  
IF ID  
IF

EX/M ID IF EX/M EX/M ID  
Stall = regWrite && (opcode == RISIB && rd != 0 && rd == rs1) ||  
(opcode == RISIB && rd != 0 && rd == rs2)

③ beq a0, a1, label IF ID EX MEM WB  
IF ID 0 0 } 停3拍  
Stall = EX && branch.cmp.res IF 0 0  
+jal+jalr IF 0  
EX EX IF

Way 2. forwarding source (产生数据) -> sink (使用数据, ALU和DMem)

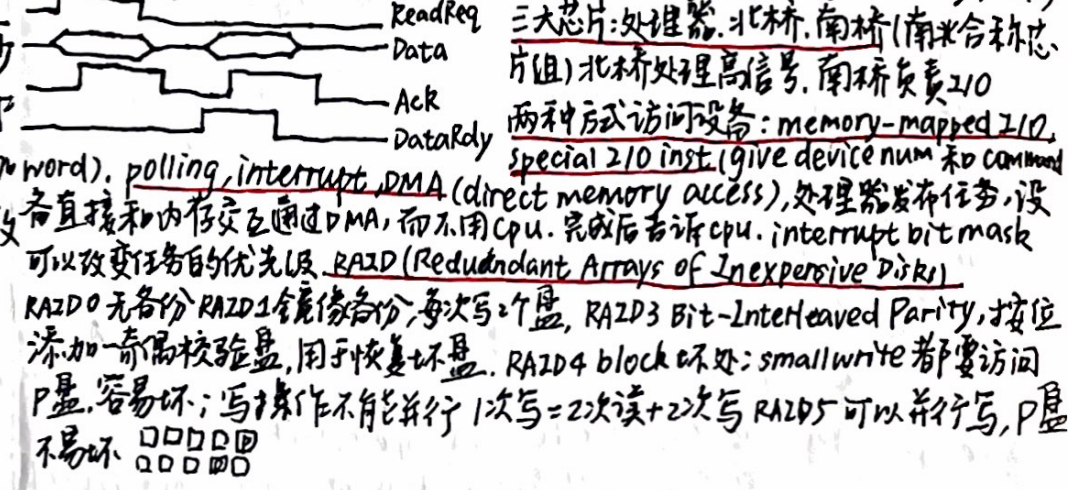


特殊情况① double hazard  
add x1, x1, x2 IF ID EX MEM WB  
add x1, x1, x3 IF ID EX MEM  
add x1, x1, x4 IF ID EX  
DMem sink,  
① EX/MEM后的ALU-res (正常)  
② MEM/WB后的ALU-res  
③ MEM/WB后的DMem-out  
② add x1, --, -- ③ lw x1, --  
sw x1, -- sw x1, --

控制竞争① predict-not taken CPI = 1 + (Jmp% + branch% \* taken%) \* 3 stall  
② 提前至ID及计算pc-branch, stall=1, 问题: add a0, --, --; beq a0, --, --  
要stall 1; ld x1, --, beq x1, -- 要stall 2  
IF ID EX MEM WB clock cycle time(single) = 1250 ld total latency = 1250/1350  
250 350 450 550 650 750 850 950 clock cycle time(pipeline) = 350  
Speedup for pipeline = CPI unipipeline / CPI pipeline \* clock cycle unipipeline / clock cycle pipelined  
CPI pipelined = 1 + stall cycles / inst

mtvec base[31:2] mode[1:0] 00: PC-base mcause 中断原因 0异常[30:0]原因  
csrrw rd, csr, rs1 csrrwi rd, csr, zimm5, csrrs rd, csr, rs1 csrrc rd, csr, rs1  
① 准备进入中断: mstatus[3] \* mip[1] & mie[1]  
② 准备: mepc < PC, PC < mtvec, mstatus[7] < mstatus[3] 改mcause  
③ 返回: mret: PC < mepc (或+4, 为异常), mstatus[3] < mstatus[5]

I/O 特性: behavior (read once, input, output (write only, not read), storage (rew, partner, data rate, dependability (可靠性), the quality of delivered service (accomplishment \* interruption), 可靠性 reliability MTTF (failure), MTTR (repair), MTBF (between failure) = MTTF + MTTR availability = MTTF / MTBF  
增加MTTF - fault avoid / tolerance (增加冗余度) / forecast, bus有control line和data line, 有input/output两种操作. 三种线: processor-memory (short high speed, custom design), backplane (high speed, standardized, PCI), I/O (lengthy, SCSI) 两种方式: synchronous (使用时钟和握手协议, 要求所有设备同步, bus短), asynchronous 用handshaking (ReadReq, DataRdy, Ack)



三大芯片: 处理器, 北桥, 南桥 (南桥合称芯片组) 北桥处理高信号, 南桥负责I/O  
两种方式访问设备: memory-mapped I/O, special I/O inst (give device num 和 command word). polling, interrupt, DMA (direct memory access), 处理器发布任务, 设备直接和内存交互通过DMA, 而不通过CPU. 完成后告诉CPU. interrupt bit mask  
可以改变任务的优先级 RAID (Redundant Arrays of Inexpensive Disks)  
RAID 0 无备份 RAID 1 全冗余备份, 每次写个盘, RAID 3 Bit-Interleaved Parity, 按位添加一奇偶校验盘, 用于恢复坏盘. RAID 4 block 坏处: small write 都要访问P盘. 容易坏; 写操作不能并行 1次写=2次读+2次写 RAID 5 可以并行写, P盘不易坏

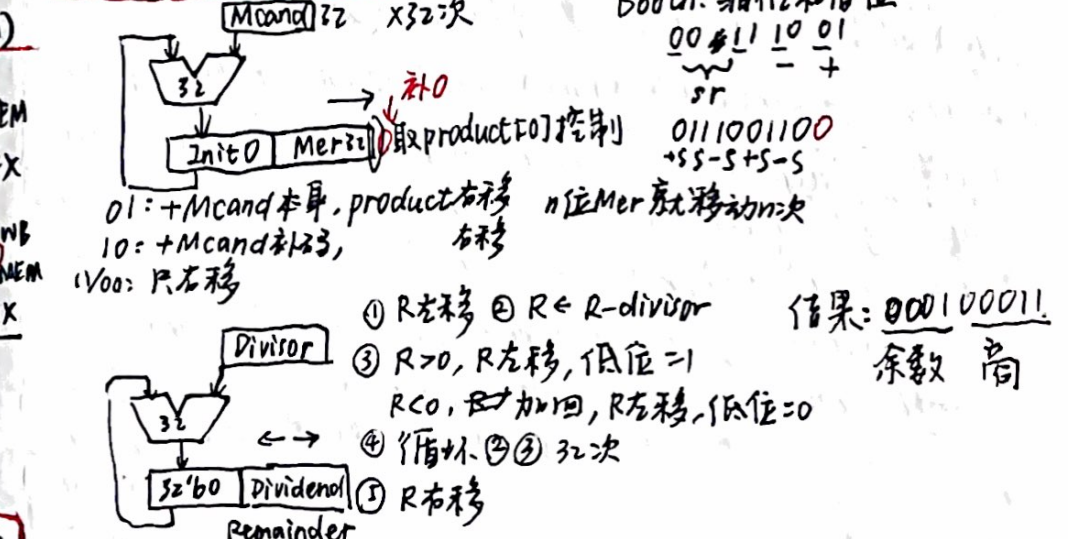
N位 unsigned [0, 2^n-1] signed [-2^(n-1), 2^(n-1)-1] sign-magnitude 反码及补码  
移码 = 补码最高位取反 [X] bias = X + 2^(n-1) float 18 23 exp[1, 24] [-12, 127]  
+1011 0101 1101 255 其余0 -> +00 double 111 52 exp[-1022, 1023]  
-1011 1010 0010 全0 -> 0, 否则非规格化 overflow: exp > 255

浮点加法① 获取双符号位的尾数及阶码 (补码表示的[-126, 127])  
② 阶码小, 阶码大阶对齐 (尾数右移) 1.101 -> 001101  
-1.101 -> 110011

③ 规格化  
01.XX -> 00.1XX 右归, frac右移, exp++ #11.00001  
10.XX -> 11.0XX -> 00.11110  
00.0XX -> 00.1X 左归, frac左移, exp--, 借位 -> -1.1110 frac  
11.1XX -> 11.0X

④ 舍入 ⑤ 溢出 exp > 127 与溢; exp < -126 下溢

逻辑移位ext, 算术sxt 浮点乘法, fracA + fracB, exp1 + exp2 - 127



Virtual Addr  
8 (一级页表) 11 (二级页表) 12 (page of S)  
PTE=6B PTE=4B  
最大页表空间 2048 2^8 \* 2^11 \* 4B + 2^8 \* 6B

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