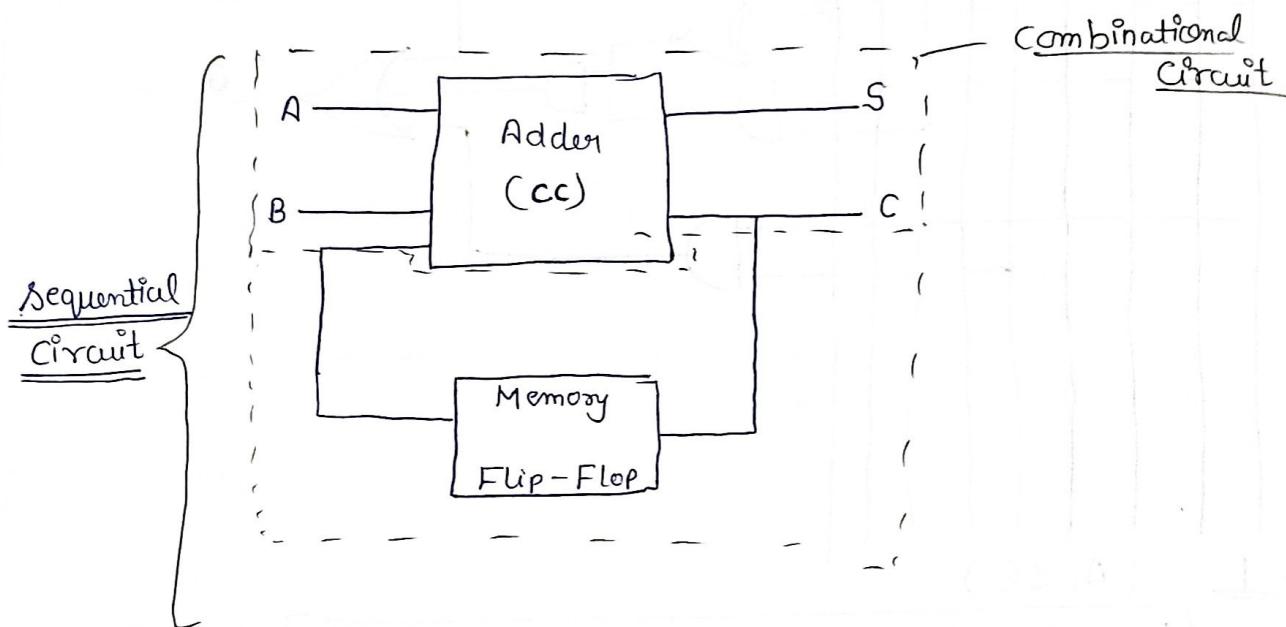


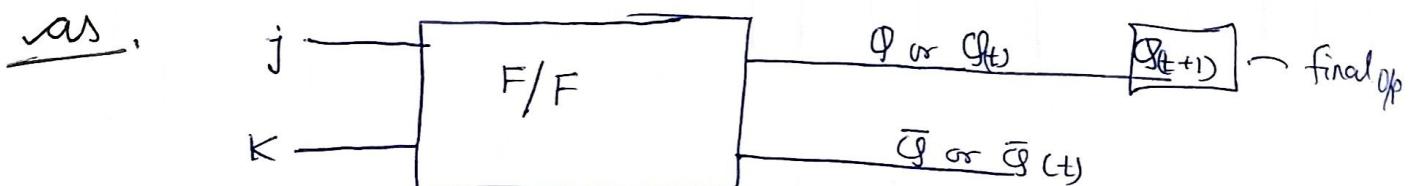
UNIT-3

Sequential Circuits

→ Sequential circuit is a logic circuit, where the output depends on present value of the input as well as the sequence past input/output, as.

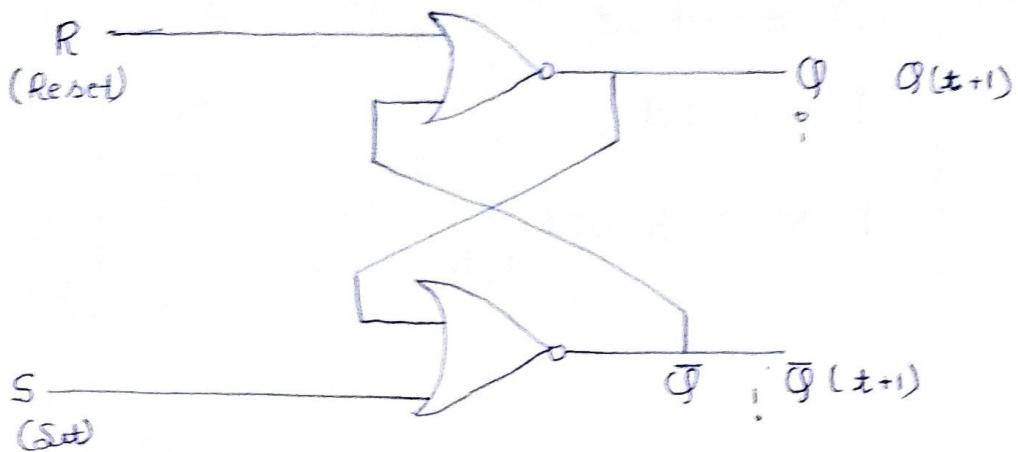


- * Flip-Flop : → Flip flop is a basic memory element.
→ It can store 1-bit of data/information.
- Flip Flop have two stable states, hence it is known as bistable multivibrator.
- Flip flop have two outputs which are complementary to each other i.e. one output for normal values and other for complement.
- Flip-Flop maintain a state until directed by input to change the state.



» Types of flip flop :-

- (i) S-R or R-S flip flop
- (ii) J-K flip-flop
- (iii) D- flip flop
- (iv) T- flip-flop
- (v) Conversion from one flip flop to another

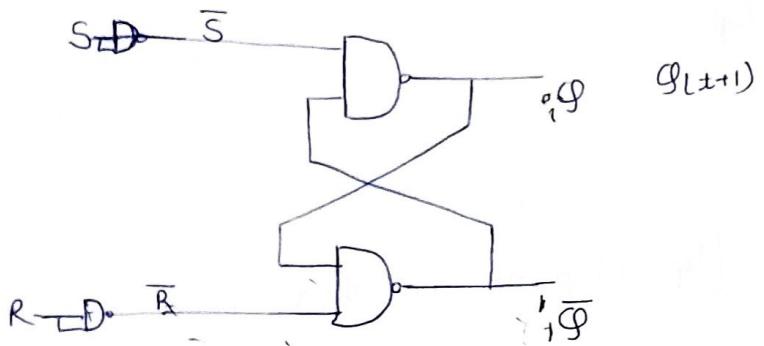
S-R / R-S Latch :-◎ S-R using NOR Gate (R-S)

R	S	$Q(t+1)$	
0	0	0	← Previous State
0	1	1	← Set
1	0	0	← Reset
1	1	0	← Invalid State

for T.T
NOR

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

→ by using NAND gate

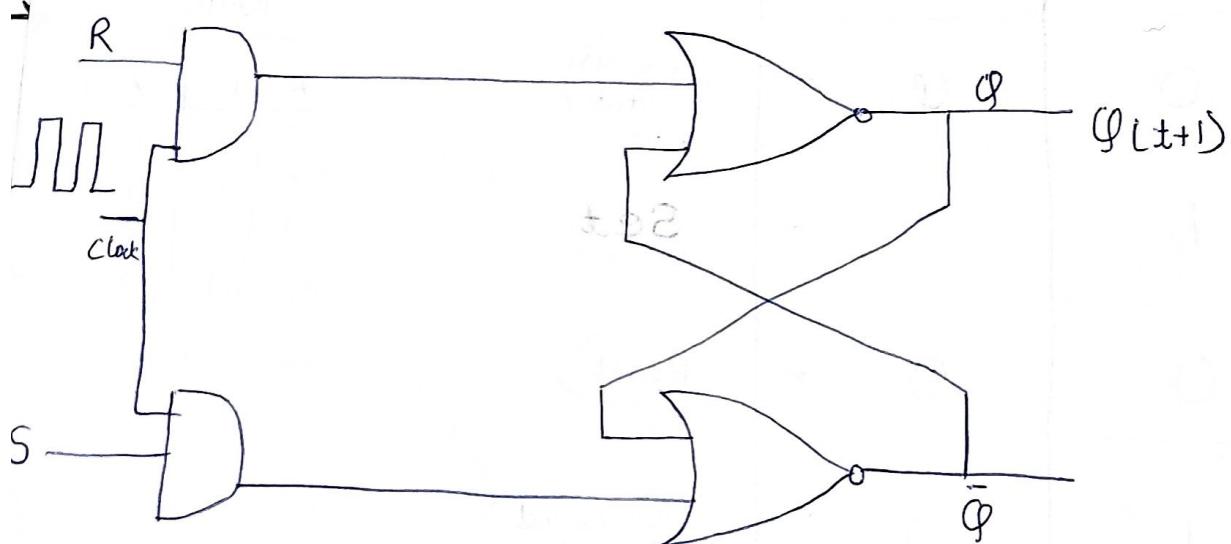


TT for NAND		
A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

ϕ	S	R	$Q(t+1)$
0	0	0	0 }
1	0	0	1 }
X	0	1	0 ← Reset
X	1	0	1 ← Set
X	1	1	1 ← Invalid State

* # S-R flip flop :-

<a> Using NOR



Truth table

<u>CLK</u>	<u>R</u>	<u>S</u>	<u>Q(t+1)</u>
0	x	x	1
1	0	0	Q or Q(t) ← Previous state
1	0	1	1 ← set
1	1	0	0 ← Reset
1	1	1	Invalid (x)

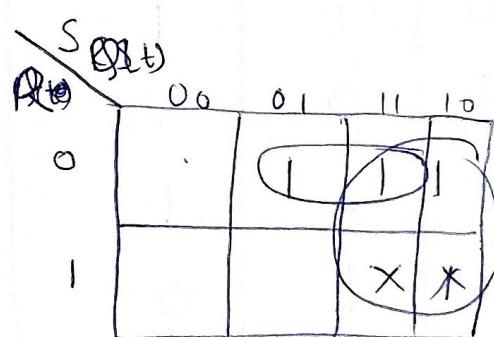
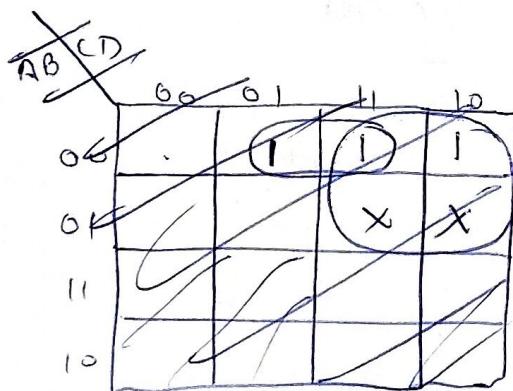
Characteristic table

<u>R</u>	<u>S</u>	<u>Q(t)</u>	<u>Q(t+1)</u>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	x
1	1	1	x

Characteristics table ko
Truth table ke input +
 $Q(t)$ ko as a input leke
 $Q(t+1)$ ki value nikalege.

* Excitation table me input
port par $Q(t)$ aur $Q(t+1)$ raha
and inputs zhi bits ko characteristic
table ke output se compare
Krega to jo same comparison
ka hogा $Q = 0 \ 0 \ 1 \ 1$ (R or S ka)
To R S
0 0 }
0 1 }
} in output
R S
0 x

$$Q(t+1) = \sum m(1, 2, 3) + \sum d(6, 7)$$

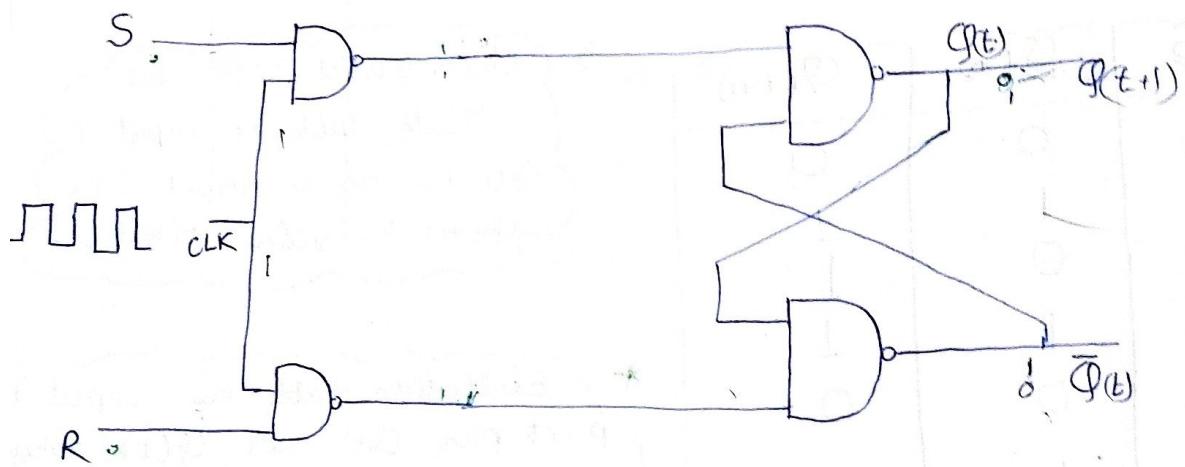


$$Q(t+1) = \bar{R}Q(t) + S$$

» Excitation table

<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>R</u>	<u>S</u>
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

» S-R-Flip Flop using NAND Gate



→ Characteristic table :-

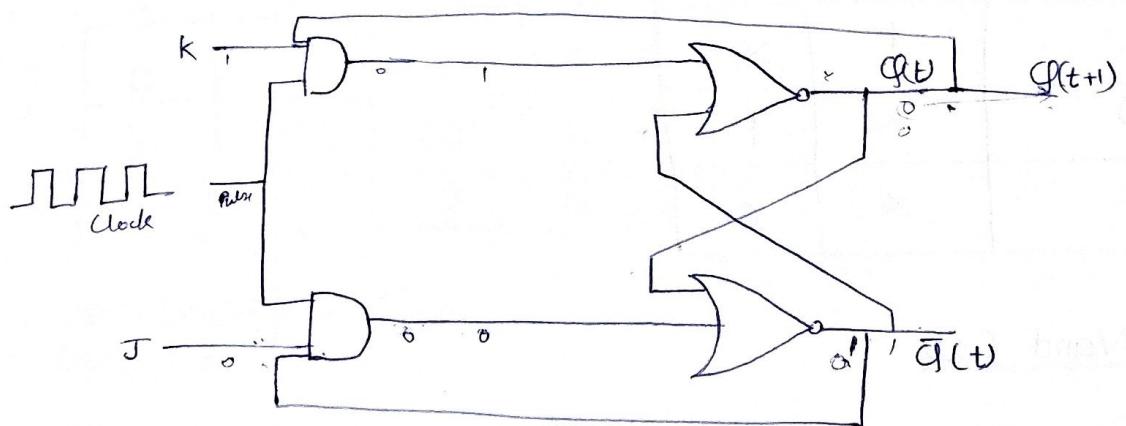
<u>R</u>	<u>S</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	X
1	1	1	X

Annotations on the table:

- Row 2: A bracket groups the first two columns under the heading "Previous State".
- Row 4: A bracket groups the last two columns under the heading "Set".
- Row 6: A bracket groups the last two columns under the heading "Reset".
- Row 8: A bracket groups the last two columns under the heading "Invalid".

② JK-Flip-Flop :-

① Using NOR Latch



→ Characteristics table

<u>CLK</u>	<u>J</u>	<u>K</u>	<u>Q(t)</u>	<u>Q(t+1)</u>	
0	X	X	X	Hold	
1	0	0	0	0	
1	0	0	1	1	Previous state
1	0	1	0	0	
1	0	1	1	0	Reset state
1	1	0	0	1	
1	1	0	1	1	Set
1	1	1	0	1	
1	1	1	1	0	Toggle state

$$Q(t+1) = \sum m(1, 4, 5, 6)$$

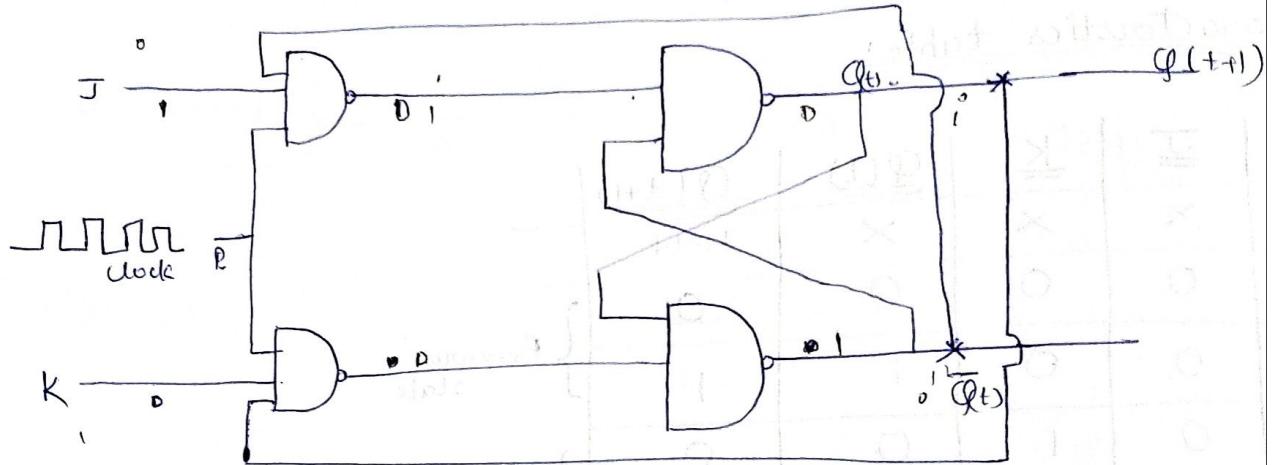
	<u>K (t)</u>	<u>J (t)</u>	<u>Q(t)</u>	<u>Q(t+1)</u>
	00	0	0	0
	01	0	1	1
	11	0	1	0
	10	1	0	1

$$Q(t+1) \Rightarrow \bar{K} Q(t) + \cancel{J} \cancel{K} \bar{Q}(t) + \cancel{J} \bar{K} Q(t)$$

Excitation table

<u>Q_t</u>	<u>Q_{t+1}</u>	<u>J</u>	<u>K</u>
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(b) Using Nand Gate



Characteristics table

<u>CLK</u>	<u>J</u>	<u>K</u>	<u>Q_t</u>	<u>Q_{t+1}</u>
0	X	X	X	Hold
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Excitation table

<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>J</u>	<u>K</u>
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

⇒ Characteristic Eqn

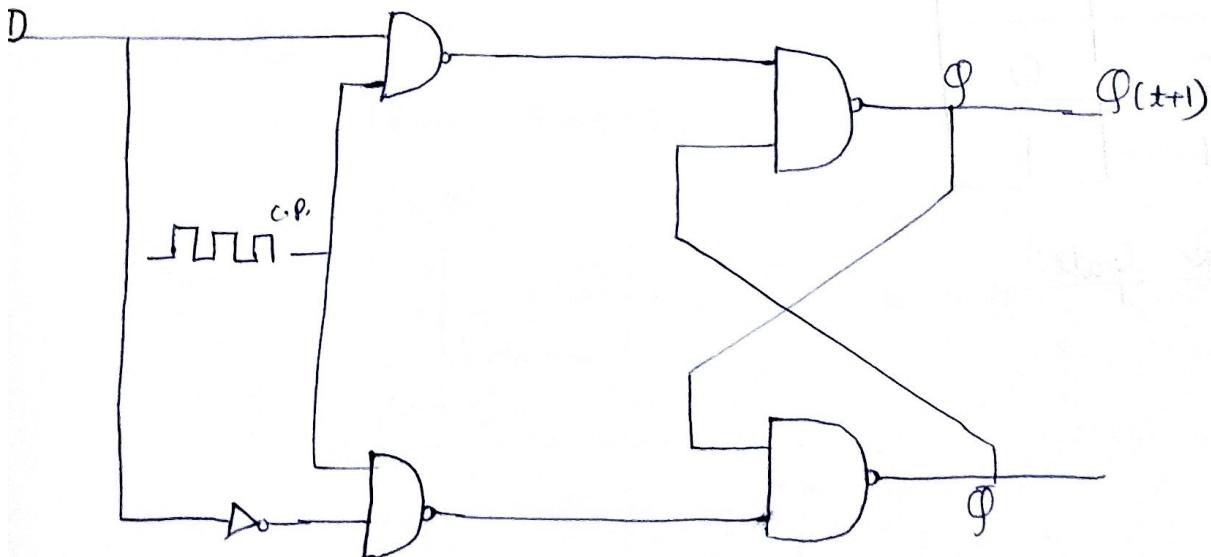
$$Q(t+1) = \Sigma m(1, 4, 5, 6)$$

		<u>K QU</u>		<u>J</u>
		00	01	
<u>Q</u>	0	1	1	0
	1	1	1	1

$$\boxed{Q(t+1) = \bar{K} Q(t) + J \bar{Q}(t) / \lambda}$$

iii) D-Flip-Flop :-

→ Using Nand Gate

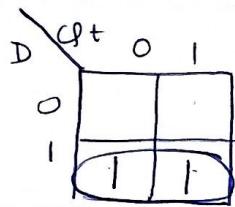


Characteristics table

<u>CLK</u>	<u>D</u>	<u>(Q(t))</u>	<u>(Q(t+1))</u>
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Characteristic eqn

$$Q(t+1) = \sum m(2, 3)$$

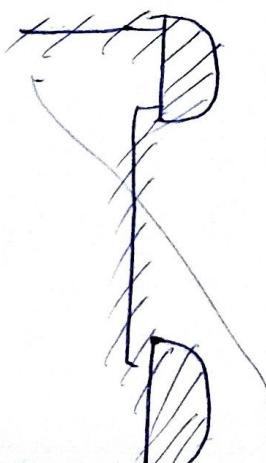


$$Q(t+1) \Rightarrow D$$

Excitation table

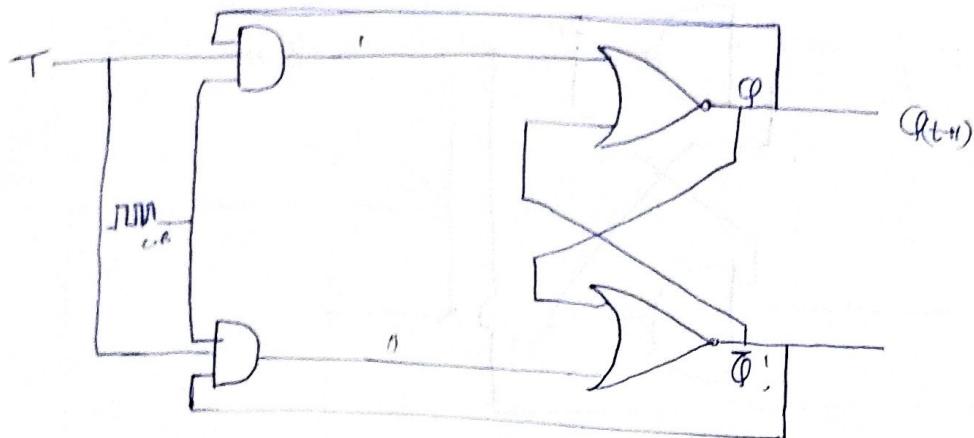
<u>Q(t)</u>	<u>Q(t+1)</u>	<u>D</u>
0	0	0
0	1	1
1	0	0
1	1	1

→ using NOR gate



T-Flip-Flop

→ by using NOR gate



Characteristic table

3/p

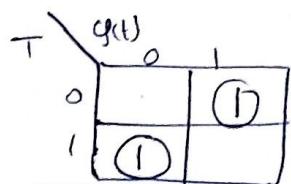
<u>CLK</u>	<u>T</u>	<u>Q(t)</u>	<u>Q(t+1)</u> (ϕ/p)
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

P.S.

Toggle State

Characteristic Eqn

$$Q(t+1) = \Sigma m(1,2)$$



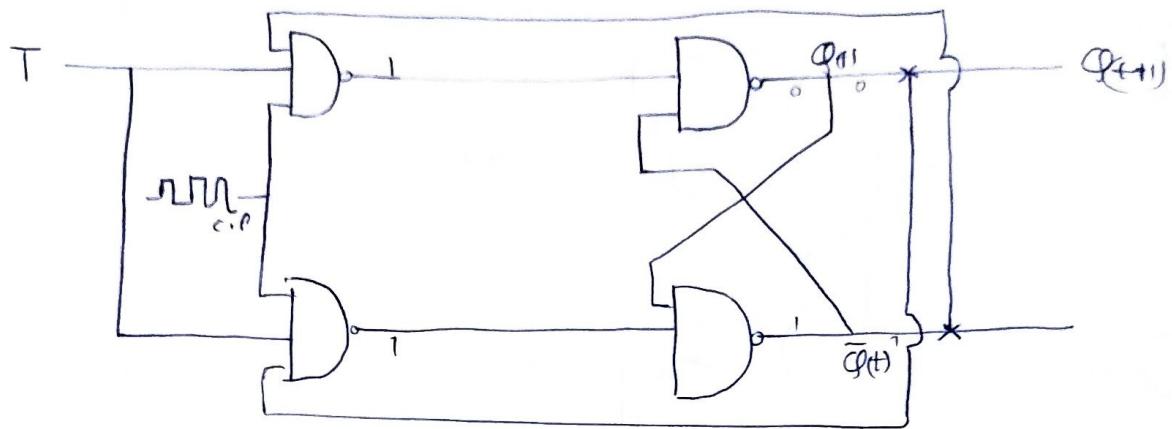
$$Q(t+1) = T + Q(t)\bar{T}$$

$$Q(t+1) \Rightarrow Q(t) \oplus T$$

Excitation table

<u>Q(t)</u>	<u>Q(t+1)</u>	<u>T</u>
0	0	0
0	1	1
1	0	1
1	1	0

→ by using Nand



Characteristic table

<u>CLK</u>	<u>I</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic Eqn

$$Q(t+1) = \Sigma m(1, 2)$$

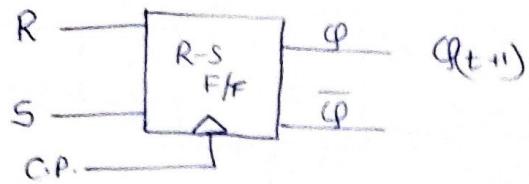
$$Q(t+1) = \bar{T} Q(t) + \bar{Q}(t) T$$

$$Q(t+1) = T \oplus Q(t)$$

excitation table same as - characteristic eqn,

#① S-R- flip-flop

summary



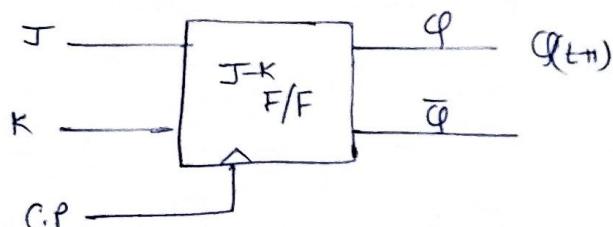
Characteristic table

R	S	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
0	0	0	0 } P.S.
0	0	1	1 }
0	1	0	1 } Set
0	1	1	1 }
1	0	0	0 } Reset
1	0	1	0 }
1	1	0	X } Invalid state
1	1	1	X }

Excitation table

<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>R</u>	<u>S</u>
0	0	X	0
0	1	0	1
1	0	1	0
1	1	0	X

) J-K F/F



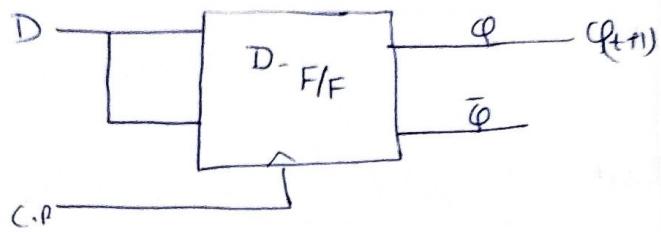
Characteristic table

<u>J</u>	<u>K</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
0	0	0	0 } P.S.
0	0	1	1 }
0	1	0	0 } Reset
0	1	1	0 }
1	0	0	1 } Set
1	0	1	1 }
1	1	1	0 } Toggle state
1	1	0	1 }

Excitation table

<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>J</u>	<u>K</u>
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

③ D- Flip-Flop



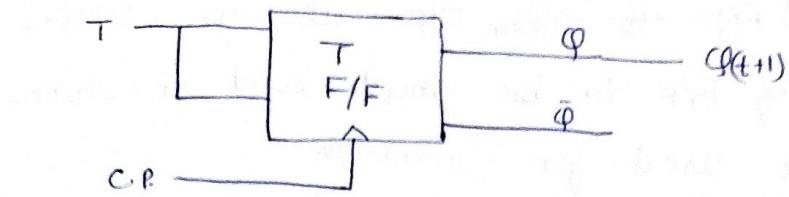
Characteristic Eqn/ table

<u>D</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
0	0	0
0	1	0
1	0	1
1	1	1

Excitation table

<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>D</u>
0	0	0
0	1	1
1	0	0
1	1	1

(4) T-Flip-Flop



Characteristic table

<u>T</u>	<u>Q(t)</u>	<u>Q(t+1)</u>
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table

<u>Q(t)</u>	<u>Q(t+1)</u>	<u>T</u>
0	0	0
0	1	1
1	0	1
1	1	0

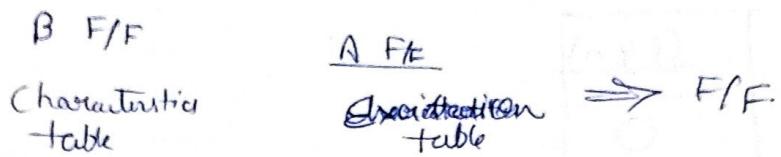
* * * * * Combine Excitation table :-

<u>Q(t)</u>	<u>Q(t+1)</u>	<u>R's</u>	<u>J K</u>	<u>D</u>	<u>T</u>
0	0	x 0	0 x	0	0
0	1	0 1	1 x	1	1
1	0	1 0	x 1	0	1
1	1	0 x	x 0	1	0

Rules for conversion of one F/F to other F/F

* for conversion of I F/F to other F/F always write characteristics table of F/F to be made and excitation table of F/F to be used for conversion.

Eg. A F/F to B F/F.



- (1) Conversion of D F/F to T F/F.
- (2) Conversion of T F/F to D F/F.
- (3) Conversion of D F/F to JKF/F.
- (4) " " JK F/F to D F/F.
- (5) " " S-R F/F to J-K F/F.
- (6) " " J-K F/F to S-R F/F.
- (7) " " S-R F/F to D F/F.
- (8) " " JK F/F to ~~S-R~~ F/F.

Poss:-

③ Characteristics Table J-K F/F

<u>J</u>	<u>K</u>	<u>$Q(t)$</u>	<u>$Q(t+1)$</u>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

D

P.S. 0

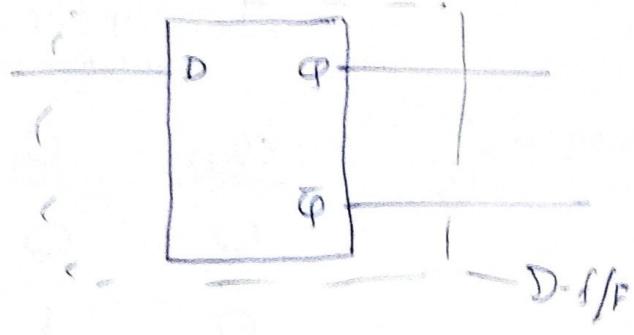
Reset 0

Set 1

Toggle State 0

D - F/F
↓
Excitation table

<u>$Q(t)$</u>	<u>$Q(t+1)$</u>	<u>D</u>
0	0	0
0	1	1
1	0	0
1	1	1



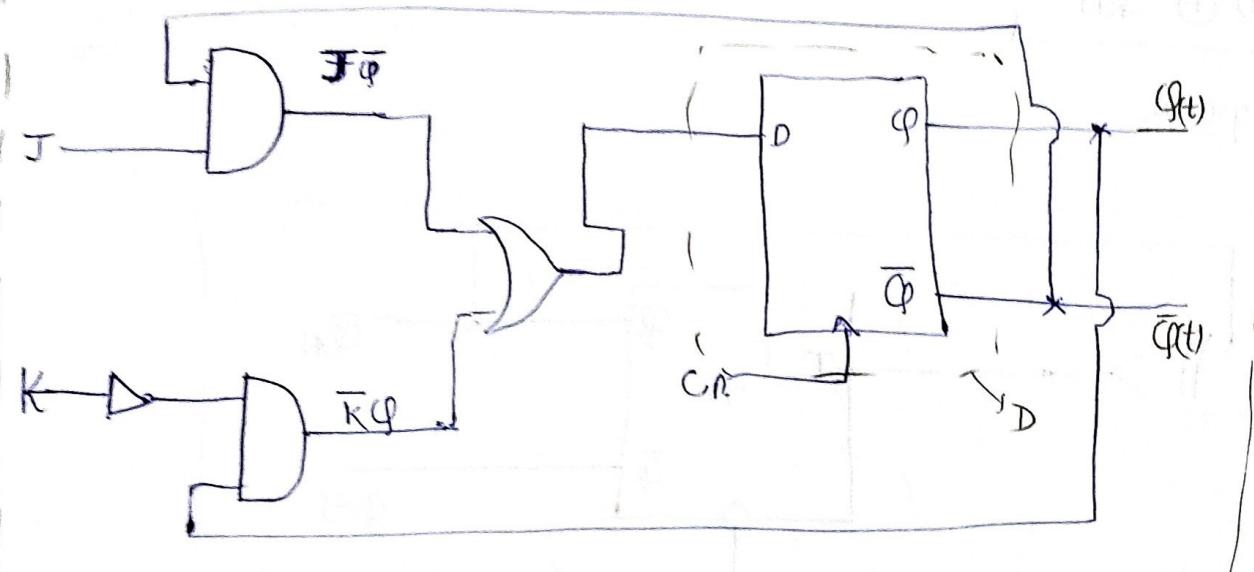
* K-Map for D

$$D = \sum m(1, 4, 5, 6)$$

K(PIH)

J	Q0	Q1	Q2	Q3
0	1	0	1	1
1	0	1	1	1

$$D = J \bar{Q}(t) + \bar{K} Q(t)$$



J-K f/F

①

D F/F
Characteristics table

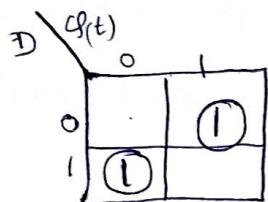
<u>D</u>	<u>$Q(t)$</u>	<u>$\bar{Q}(t+1)$</u>	<u>T</u>
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

T - flip flop
Excitation table

<u>$Q(t)$</u>	<u>$\bar{Q}(t+1)$</u>	<u>T</u>
0	0	0
0	1	1
1	0	1
1	1	0

K-Map for T

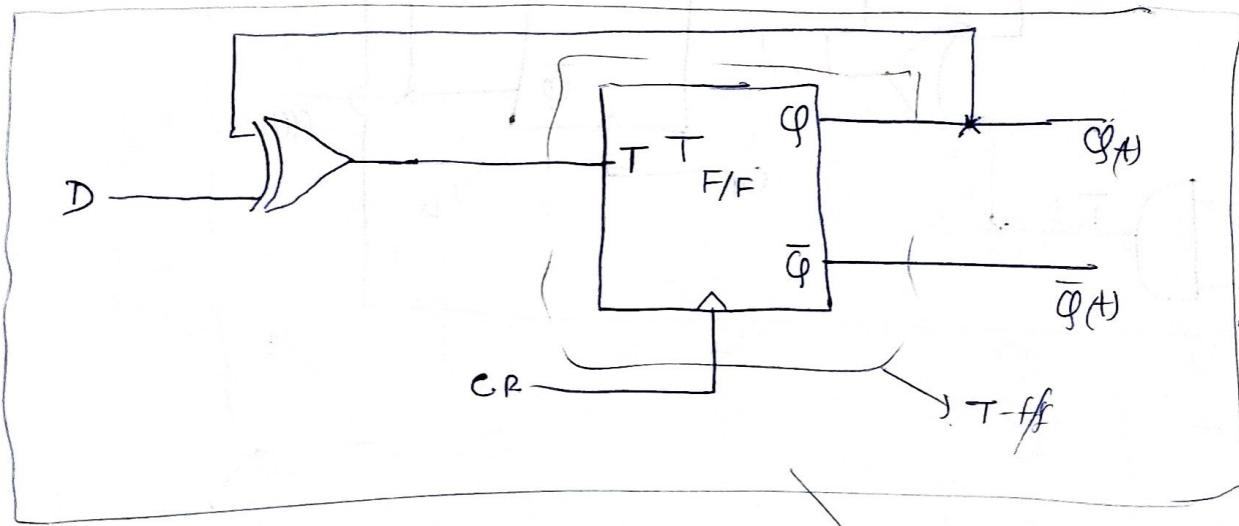
$$T = \sum m(1, 2)$$



$$T = D \bar{Q}(t) + \bar{D} Q(t)$$

$$T = D \oplus Q(t)$$

Circuit diagram



D - F/F

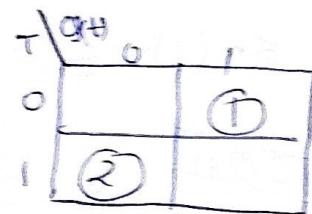


Q.

D F-F characteristic table

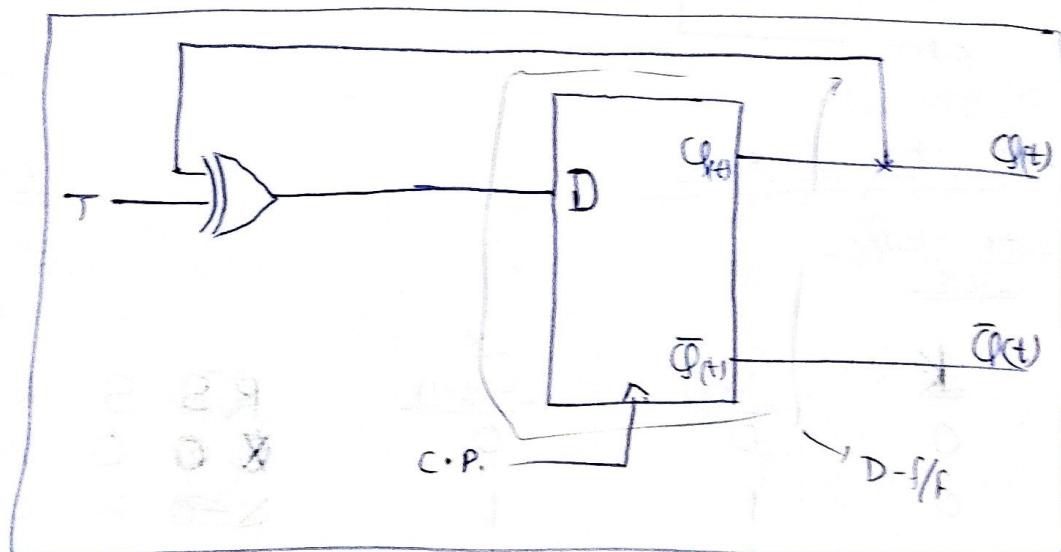
I	$Q(t)$	$\bar{Q}(t)$	D	→ excitation table
0	0	0	0	00
0	1	1	1	11
1	0	1	1	10
1	1	0	0	01

$$D = \sum_m (1, 2)$$



$$D \Rightarrow T \oplus Q(t)$$

Circuit diagram



Q

Q

T_f/F

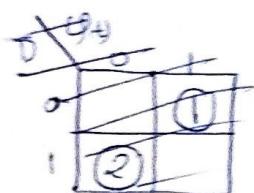
4.

Characteristic table of D F/F

D	Q_t	Q_{t+1}	JK
0	0	0	0x
0	1	0	x1
1	0	1	z*
1	1	1	x 0

k-map for JK

$$JK = \sum m(1) + \sum d(1,3)$$

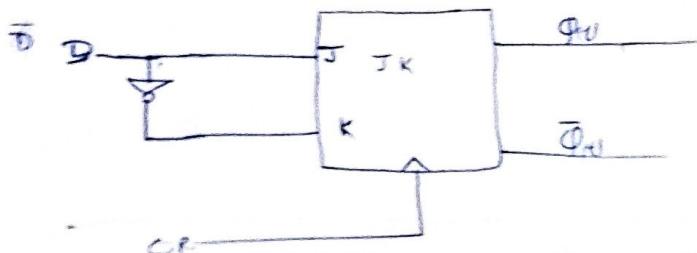


$$J = \sum m(2) + \sum d(1,3)$$

$$K = \sum m(1) + \sum d(0,2)$$

$$JK = \bar{D}Q(t) + D\bar{Q}(t) \quad \text{by k-map}$$

J = D
K = D



5.

S-R to J K

Characteristic table
JK

S.R
excitation table

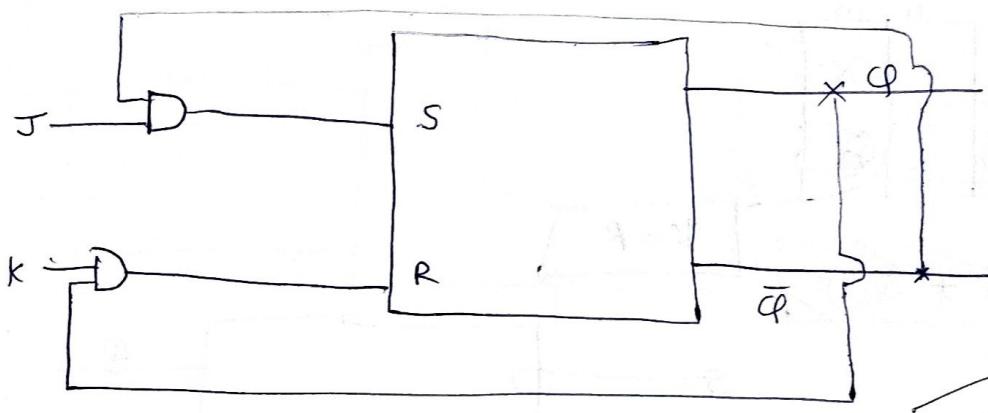
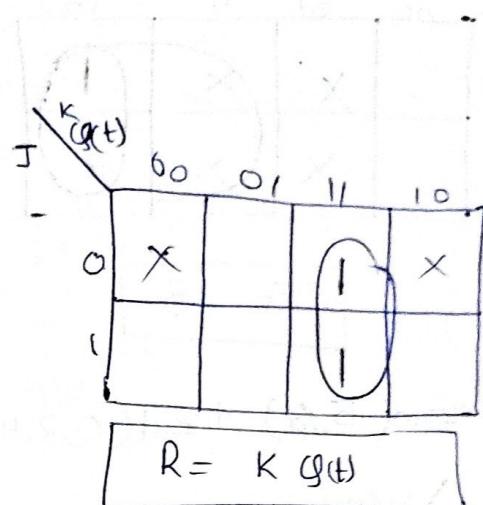
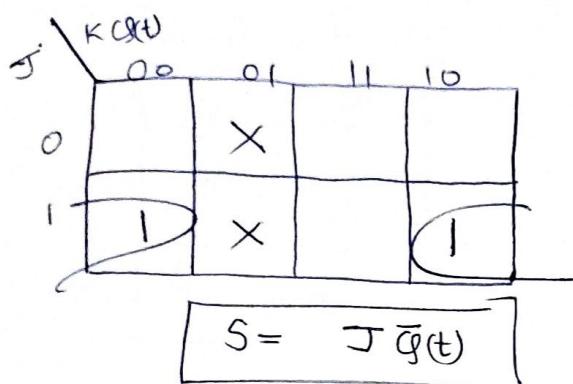
R	S	Q_t	Q_{t+1}	Q_{t+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0



S	R
0	X
X	0
0	X
0	1
1	0
X	0
1	0
0	1

$$S = \sum m(4,6) + \sum d(1,5)$$

$$R = \sum m(3,7) + \sum d(0,2)$$



⑥

Characteristics table

S.R

<u>J</u>	<u>K</u>	<u>$Q(t)$</u>	<u>$Q(t+)$</u>	<u>$Q(t++)$</u>	<u>J</u>	<u>K</u>
0	0	0	0	0	0	X
0	0	1	X	1	X	0
0	1	0	1	1	1	X
0	1	1	0	1	X	0
1	0	0	X	0	0	X
1	0	1	0	0	X	1
1	1	0	X	X	X	X
1	1	1	X	X	X	X

excitation table

$$J = \sum_m(2) + \sum_d(1, 3, 5, 6, 7)$$

~~R~~ ~~S(kt)~~

	00	01	11	10
0	X	X		1
1	X	X		X

$$J = S$$

$$K = \sum_m(5) + \sum_d(0, 2, 4, 6)$$

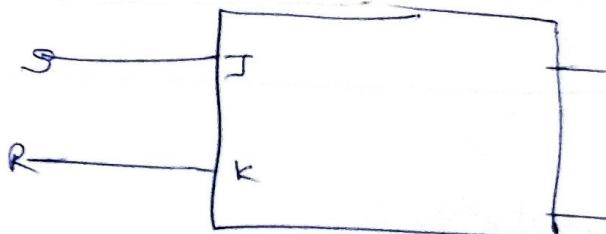
~~R~~ ~~S(kt)~~

	00	01	11	10
0	X			X
1	X	1	X	0

~~$K = R \bar{S} + Q(t)$~~

$$K = R$$

③ S - R to D

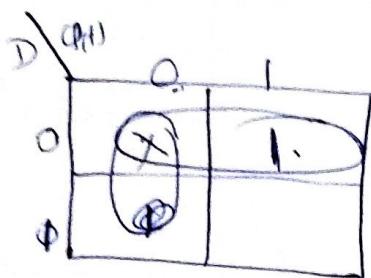


Characteristic table

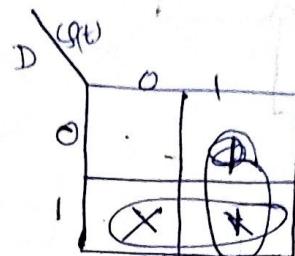
<u>D</u>	<u>C(+)</u>	<u>C(A+)</u>	<u>R</u>	<u>S</u>
0	0	0	X	0
0	1	0	1	0
1	0	1	0	1
1	1	1	0	X

$$R = \sum m(2) + \sum d(0)$$

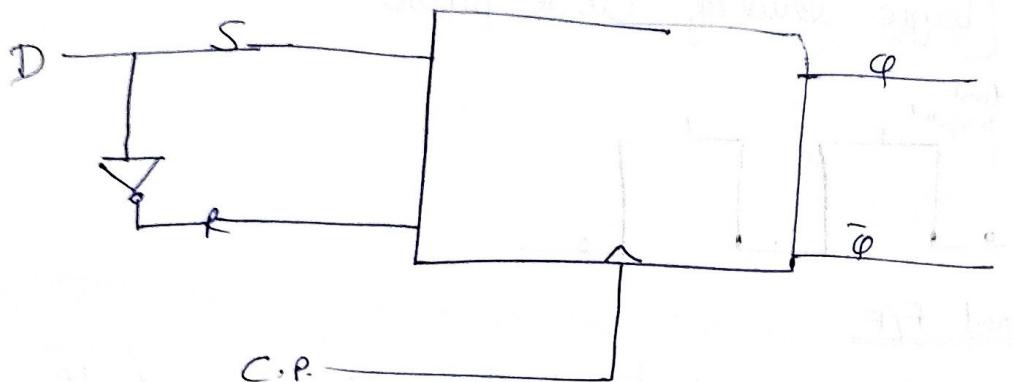
$$S = \sum m(1) + \sum d(3)$$



$$R = \overline{D} \oplus$$



$$R = \overline{D}$$



$\rightarrow \underline{J \text{ } K \rightarrow T}$

$$\begin{array}{c|cc|c} \equiv & \underline{Q(t)} & \underline{\dot{Q}(t+1)} \\ \hline 0 & 0 & 0 \\ \end{array}$$

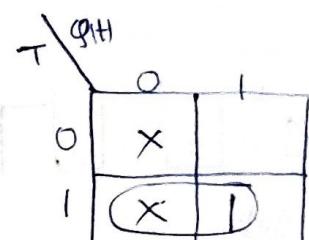
$$\begin{array}{c|cc|c} \equiv & \underline{J} & \underline{K} \\ \hline 0 & X \\ \end{array}$$

$$\begin{array}{c|cc|c} 0 & 1 & 1 \\ \hline 1 & 0 & 1 \\ \end{array}$$

$$\begin{array}{c|cc|c} & X & 0 \\ \hline 1 & 1 & X \\ \end{array}$$

$$\begin{array}{c|cc|c} 1 & 1 & 0 \\ \hline \end{array}$$

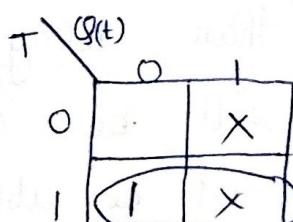
$$\begin{array}{c|cc|c} & X & 1 \\ \hline \end{array}$$



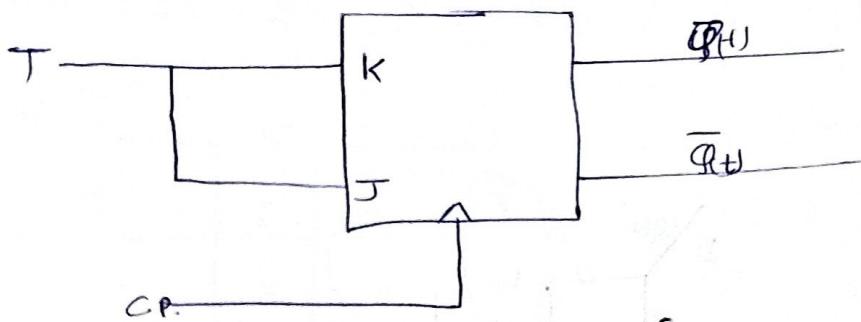
$$K = T$$

$$J = \sum m(2) + \sum d(1,3)$$

$$K = \sum m(3) + \sum d(0,2)$$



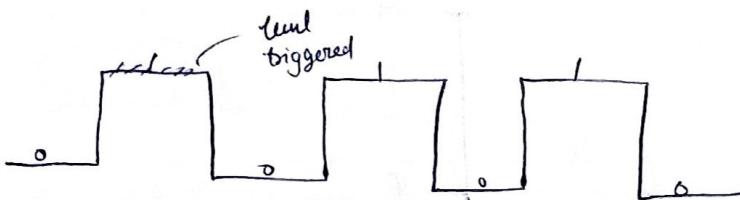
$$J = T$$



Types of clock pulse

(1) Level triggered F/F

→ In level triggered F/F output of F/F changes according to value of logic level of clock pulse



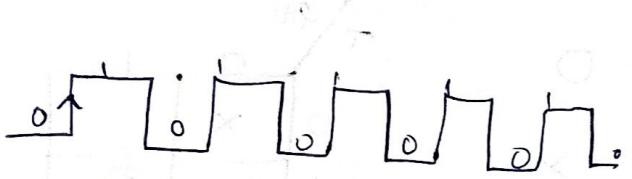
(2) Edge triggered F/F

→ In edge triggered F/F output of F/F changes at the edge of Clock pulse.

▷ two types -

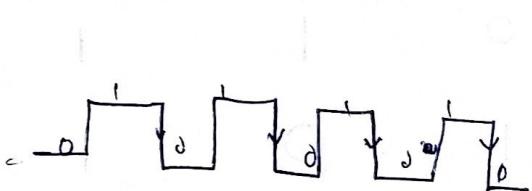
(i) positive edge triggered F/F

$\boxed{\text{Low} \rightarrow \text{High (F/F ON)}}$



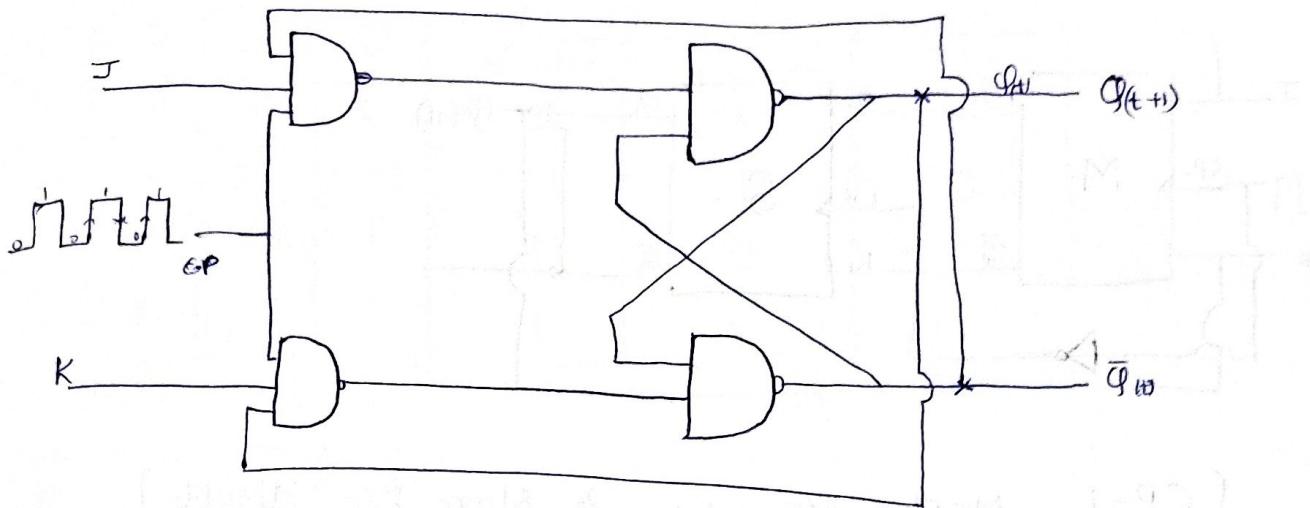
(ii) Negative edge triggered F/F

$\boxed{\text{High} \rightarrow \text{Low (F/F ON)}}$

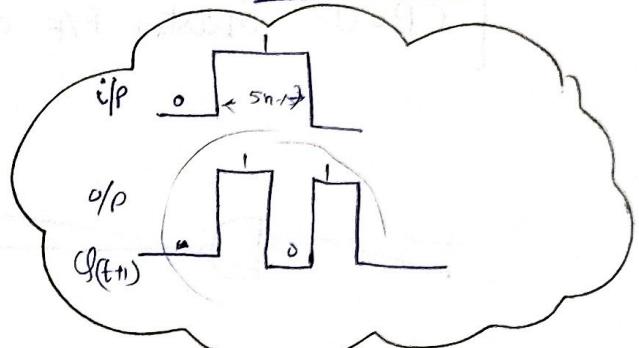


Race around Condition :-

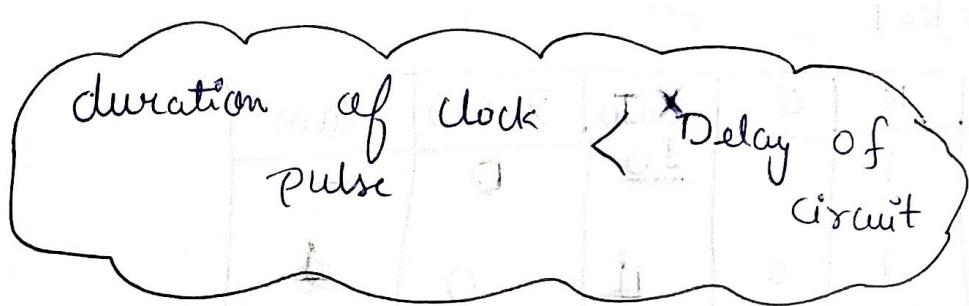
"if duration of clock pulse is larger than delay of Flip Flop then output of Flip Flop will be changing in such a manner that we will not be able to predict the o/p of F/F after clock pulse has been applied such a condition is called race around condition".



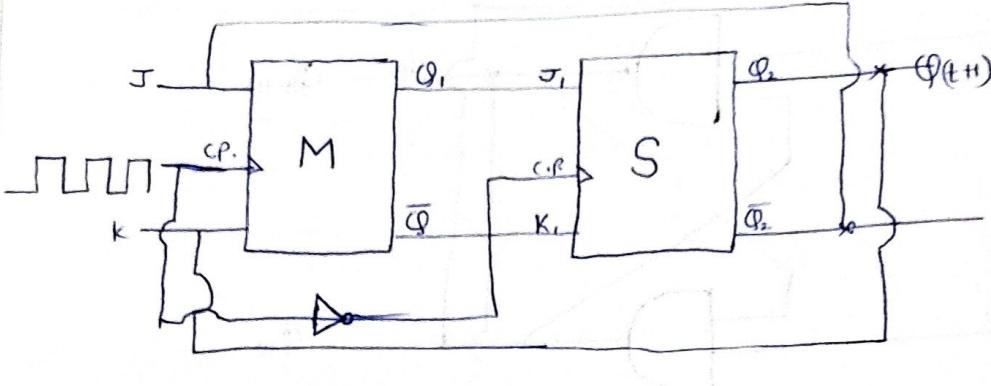
race around condition



- To avoid Race around Condition duration of clock pulse must be less than total propagation delay of the circuit in other words delay of ckt should be more than duration of clock pulse
- For a faster device it is also necessary that delay should be as less as possible practically it is very difficult to design a clock pulse of a very less duration so because of this reason we will move for edge triggered F/F.

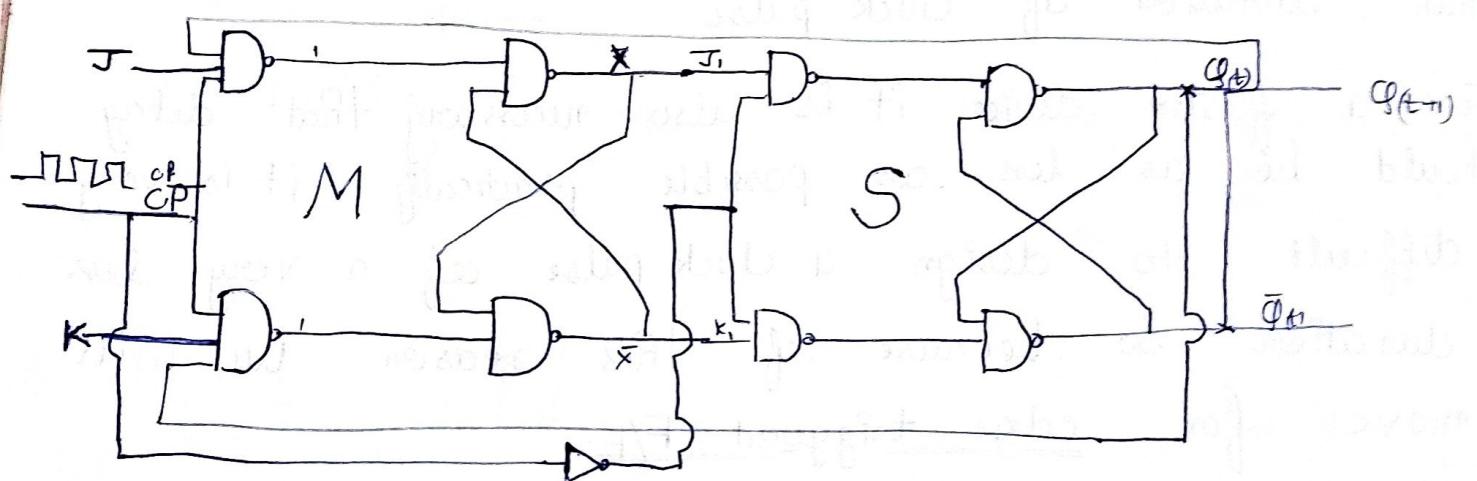
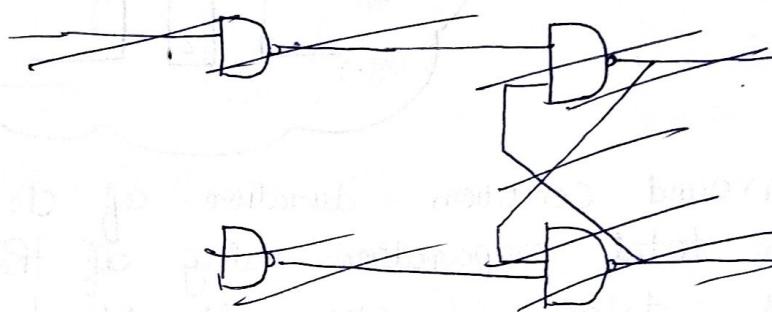


» Master Slave F/F



$\left\{ \begin{array}{l} CP=1 \text{ Master F/F active \& Slave F/F disable} \\ CP=0 \text{ Master F/F disable \& Slave F/F active} \end{array} \right\}$

~~Master Slave F/F~~



Case (I)

$$J = K = 1$$

C.P	J	K	Q	$\bar{Q}(t)$	$\bar{X}(K)$	$Q(t+1)$
1	1	1	0	1	0	-
0	1	1	0	1	0	1
1	1	1	1	0	1	-
0	1	1	1	0	1	0

Case (2)

$J = K = 0$

C.P.	<u>J</u>	<u>K</u>	<u>Q</u>	<u>X (J_t)</u>	<u>X (K_t)</u>	<u>Q(t+1)</u>
1	0	0	0	0	1	-
0	0	0	0	0	1	0
1	0	0	1	1	0	-
0	0	0	1	1	0	1

Case (III)

$J = 0, K = 1$

C.P.	<u>J(X)</u>	<u>K(X)</u>	<u>Q(t+1)</u>
1	0	1	-
0	0	1	0

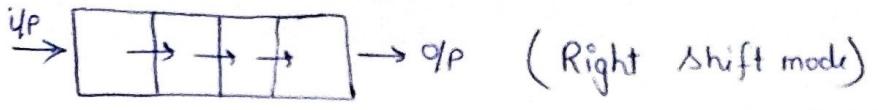
Case (IV)

C.P.	<u>X (J_t)</u>	<u>X̄ (K_t)</u>	<u>Q(t+1)</u>
1	1	0	-
0	1	0	1

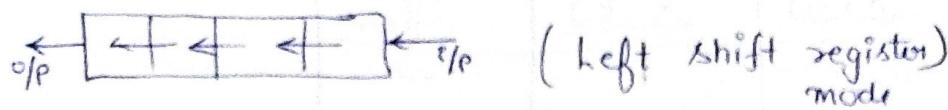
Register :- Register is a logic circuit made with the help of group of flip-flops which can store data of many bits.

→ Since 1 FF can store data of 1-bit. So a register is capable of storing data of n-bits will consist of n-flip flops.

* Shift register :- "A register capable of shifting its binary information in \pm or both direction is called shift register".



left shift mode
data shift from right side to left side
MSB
LSB



- The logical configuration of shift register: consists of a chain of F/F in cascade of in the o/p of one F/F Connected to the input of other (next) F/F
- all F/F receive , common clock pulse which activate the shift from one stage to the next stage.

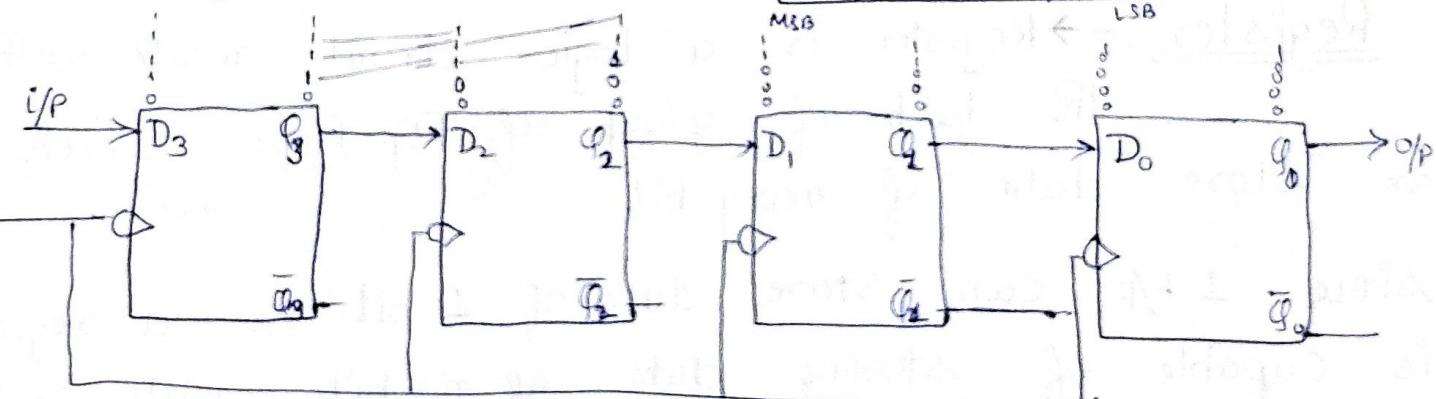
Serial in parallel out (SIPo)

Various types of register

- (1) Serial in Serial out (SISO)
- (2) Serial in Parallel out (SIPO)
- (3) Parallel in serial out (PISO)
- (4) Parallel in Parallel out (PIPO)

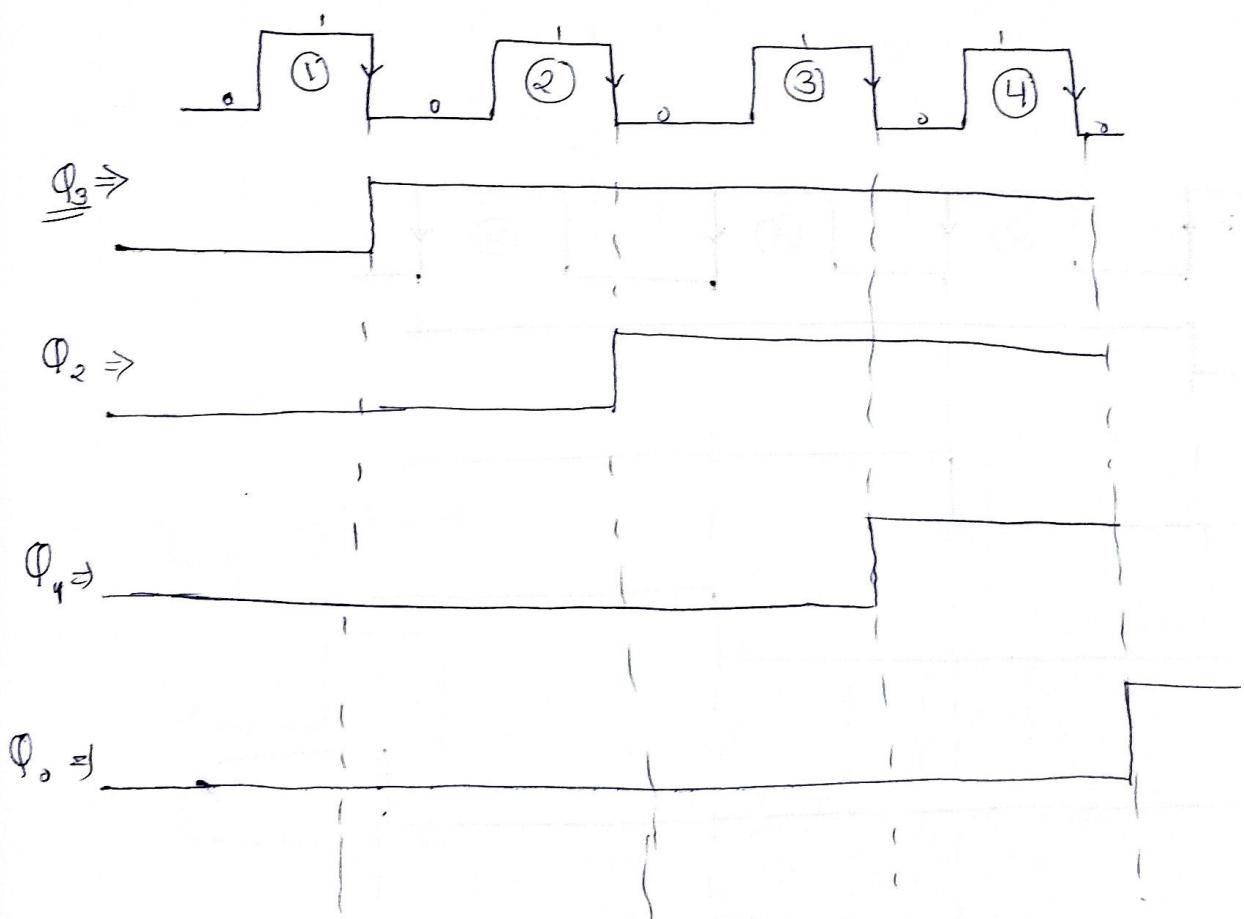
(1) Serial in Serial out :-

(a) Right shift mode

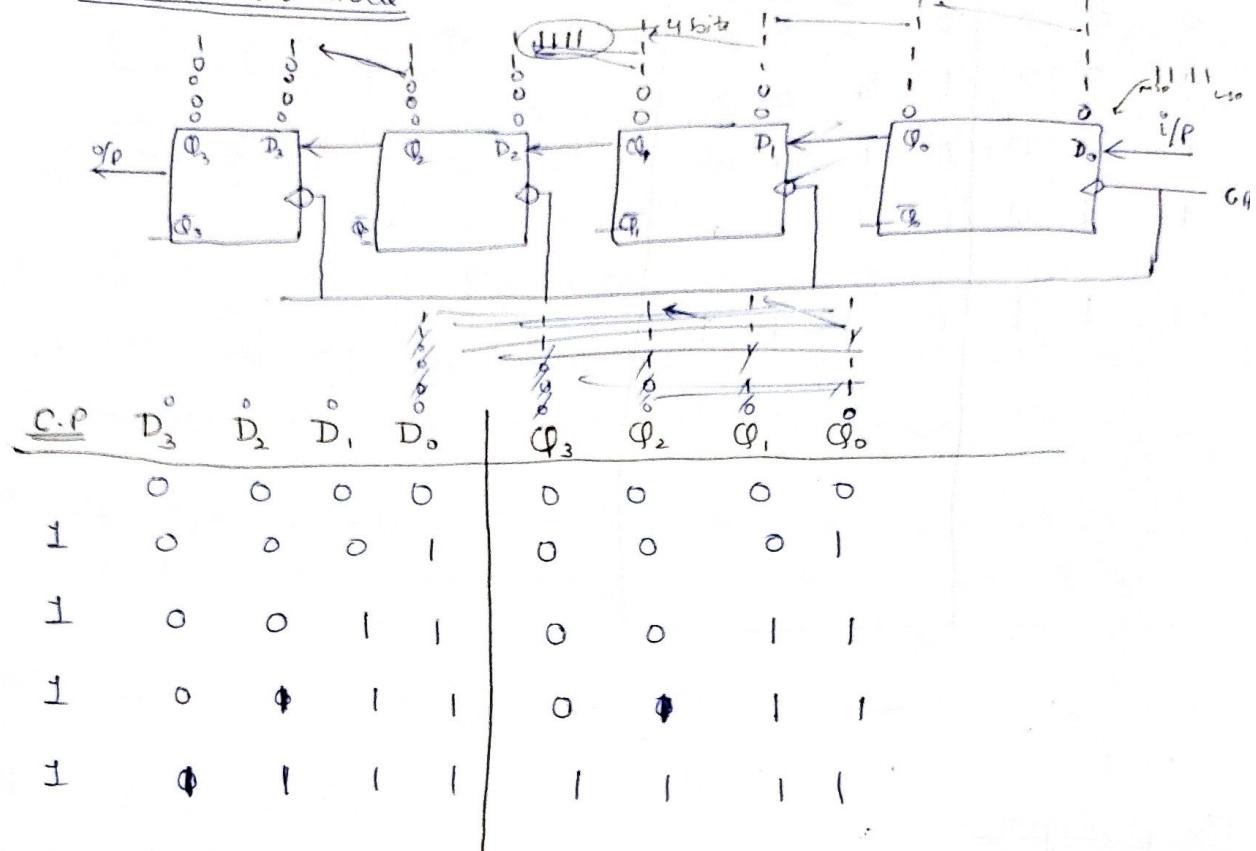


	<u>C.P</u>	<u>D₂</u>	<u>D₁</u>	<u>D₀</u>	<u>Q₃</u>	<u>Q₂</u>	<u>Q₁</u>	<u>Q₀</u>
1	1	0	0	0	1	0	0	0
2	1	1	0	0	1	1	0	0
3	1	1	1	0	1	1	1	0
4	1	1	1	1	1	1	1	1

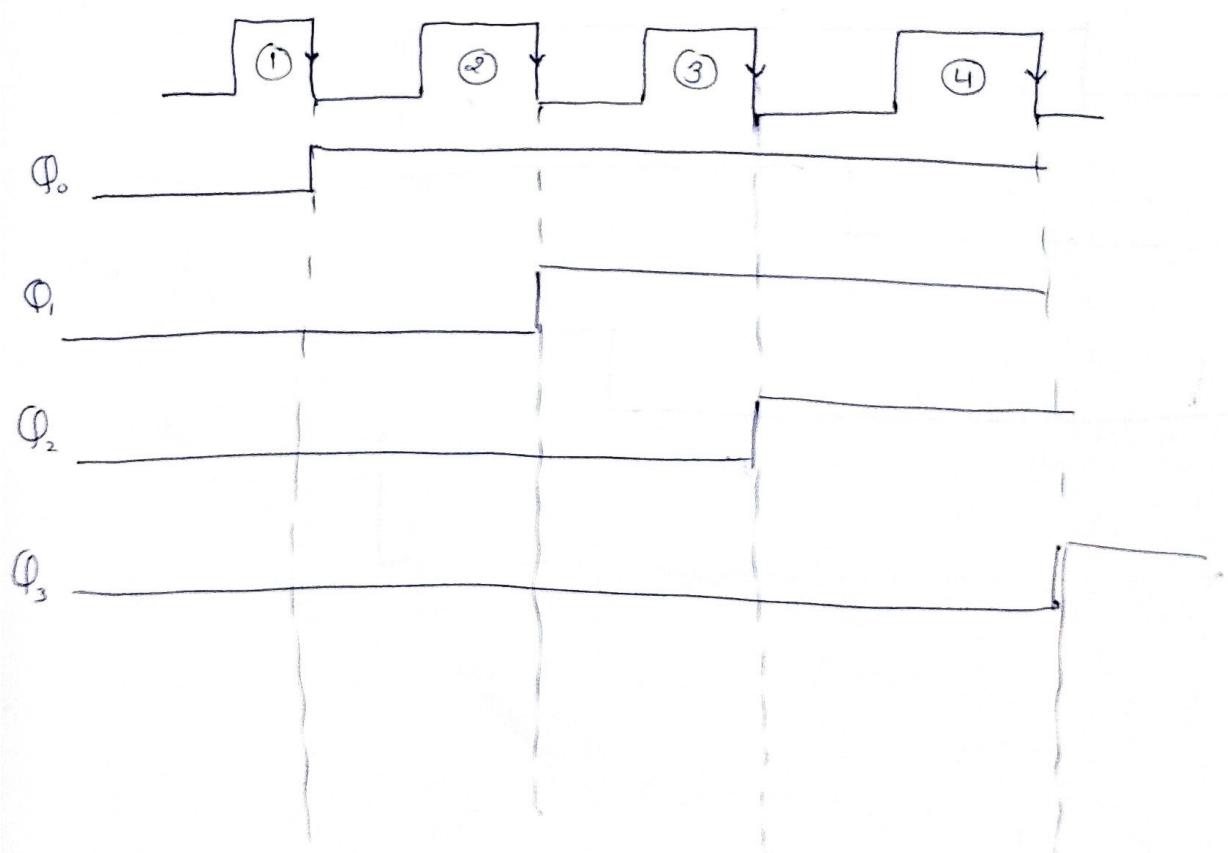
» Timing diagram

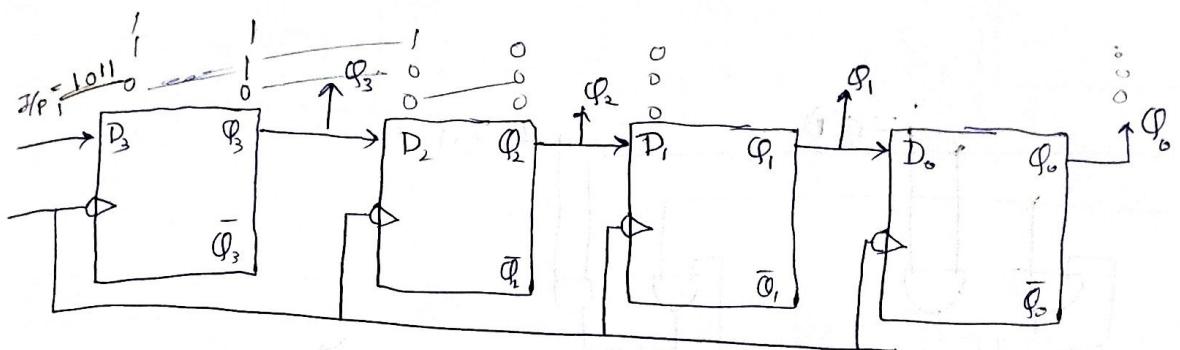
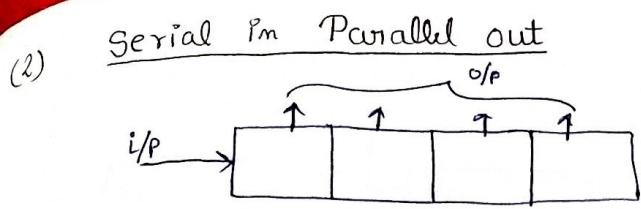


(b) left shift mode



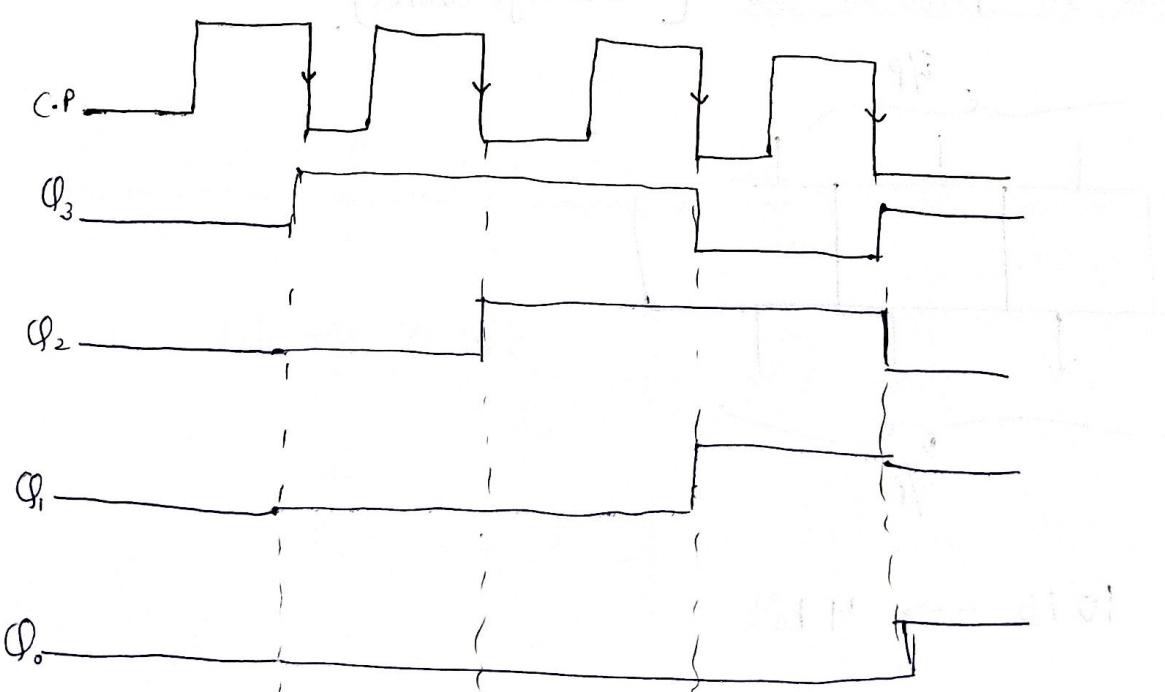
Timing diagram



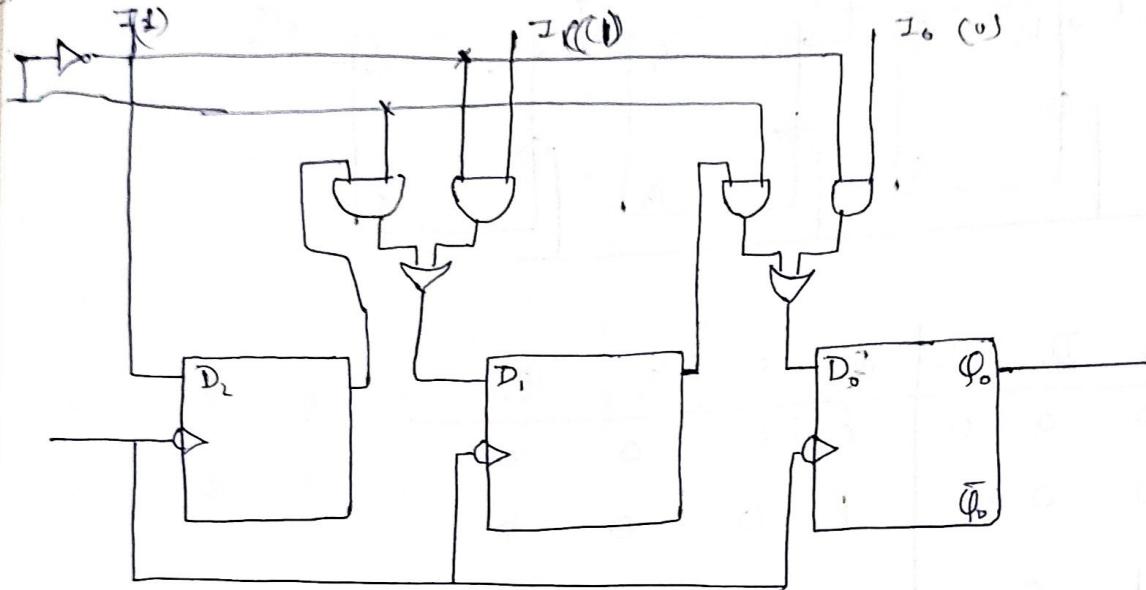
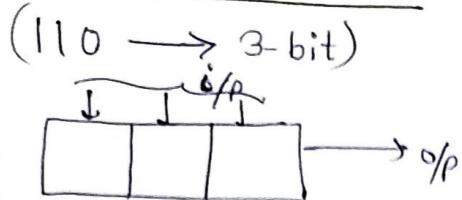


C.P.	<u>D₃</u>	<u>D₂</u>	<u>D₁</u>	<u>D₀</u>	<u>Q₃</u>	<u>Q₂</u>	<u>-Q₁</u>	<u>Q₀</u>
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
1	1	1	0	0	1	1	0	0
1	0	1	1	0	0	1	1	0
1	1	0	1	1	1	0	1	1

Timing diagram



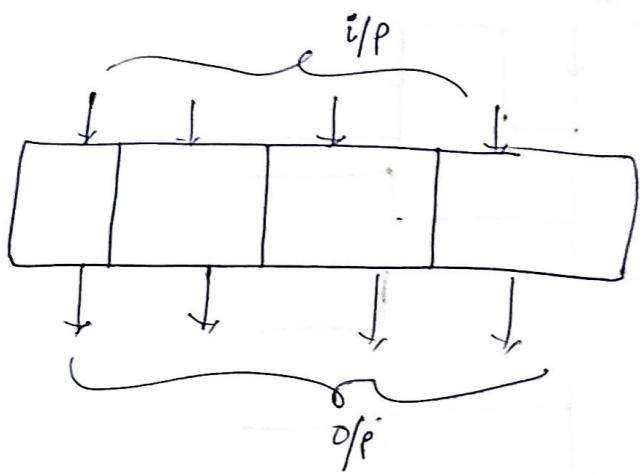
(3) Parallel in Serial out



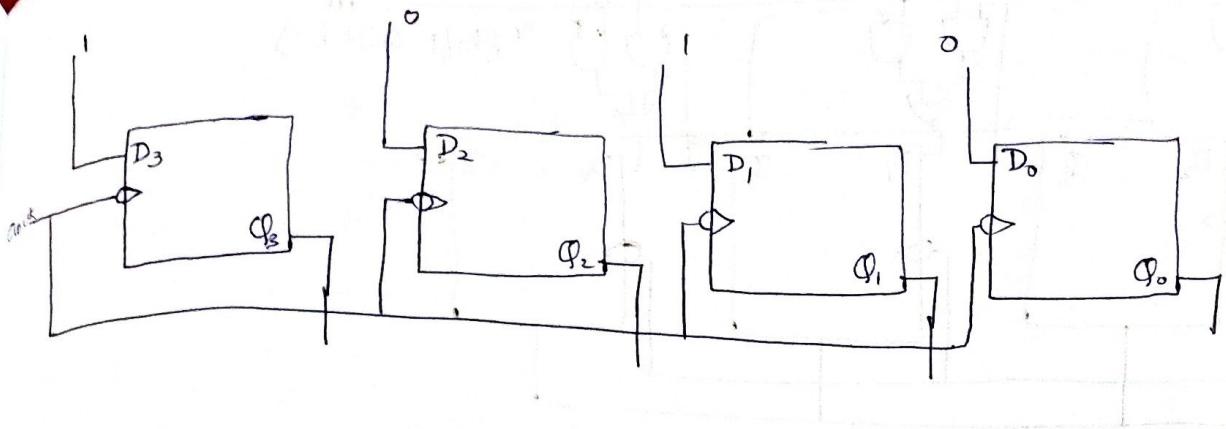
Control = 1 = $T_{2,3}$
= 0 \leftarrow T_1

C.P.	D ₂	D ₁	D ₀	Q ₂	Q ₁	Q ₀
0	0	0	0	0	0	0
1	1	1	1	1	1	1
1	1	1	0	1	1	0

(4) Parallel in Parallel out [Storage device].



1010 → 4 bit



<u>C.P.</u>	<u>D₃</u>	<u>D₂</u>	<u>D₁</u>	<u>D₀</u>	<u>Q₃</u>	<u>Q₂</u>	<u>Q₁</u>	<u>Q₀</u>
	0	0	0	0	0	0	0	0
↖	1	0	1	0	1	0	1	0

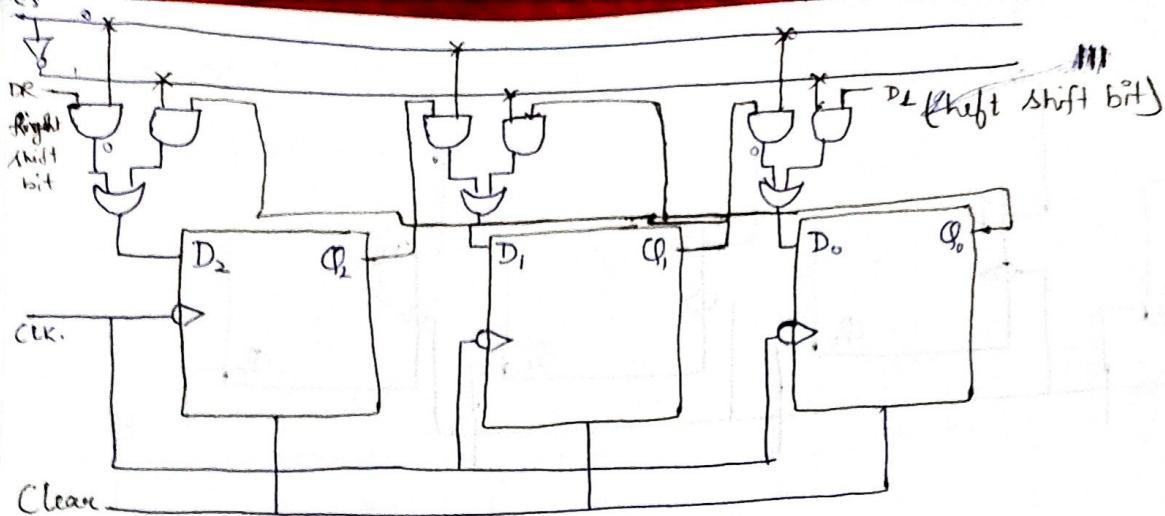
GP n-bit

SISO =	n	n
SIPO =	n	n
PISO =	1	n
PJPO =	1	n

Bidirectional shift register :-

→

111 → 3-bit



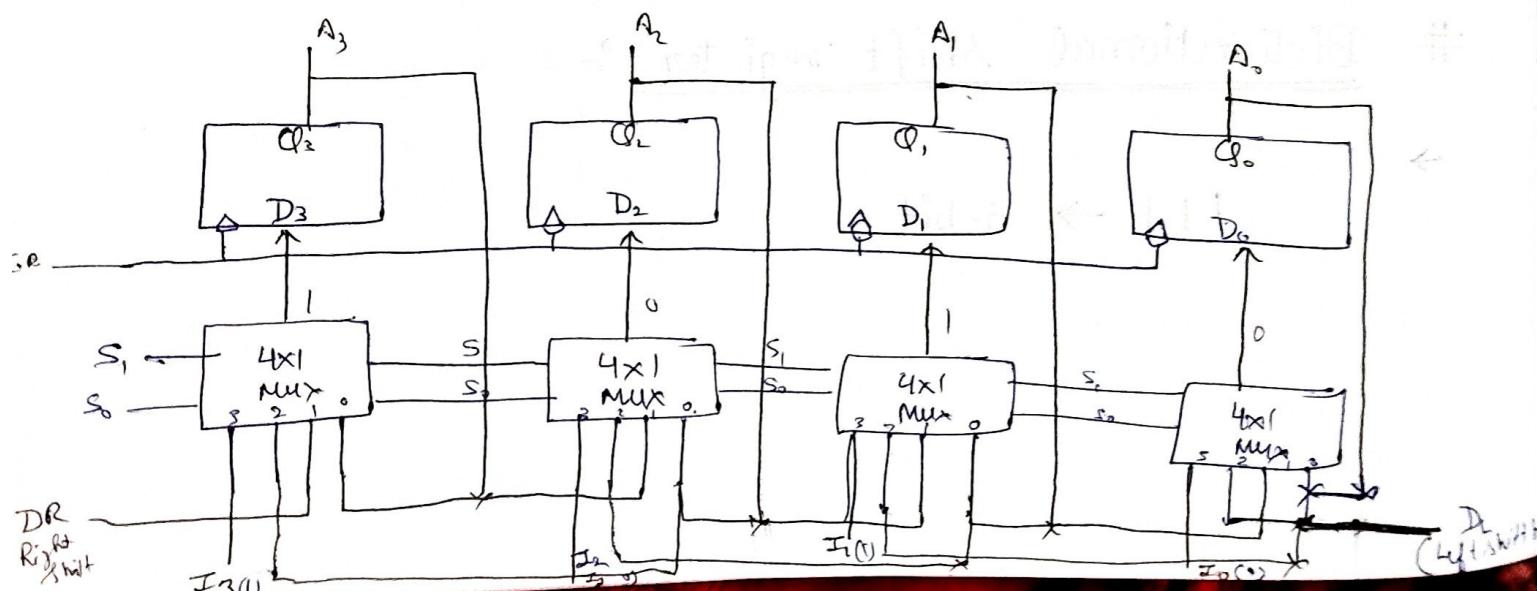
Control	CP	D ₂	D ₁	D ₀	Q ₂	Q ₁	Q ₀
0	1	0	0	1	0	0	1
0	2	0	1	1	0	1	1
0	3	1	1	1	1	1	1
Clear		0	0	0	0	0	0
1	4	1	0	0	1	0	0
1	5	1	1	0	1	1	0
1	6	1	1	1	1	1	1

left shift
(CS=0)

Right shift
(CS=1)

~~jmps.~~
Universal Shift register :-
 $1010 \rightarrow 4 \text{ bit}$

every FF output connect to
D



* Left side input \rightarrow Right shift
 Right side input \rightarrow Left shift

- | | |
|----------------------|-----------------------------|
| <u>S₁</u> | <u>S₀</u> |
| 0 | 0 \rightarrow No change |
| 1 | 0 \rightarrow Right shift |
| 1 | 1 \rightarrow Left shift |
| 0 | 1 \rightarrow Load mode |

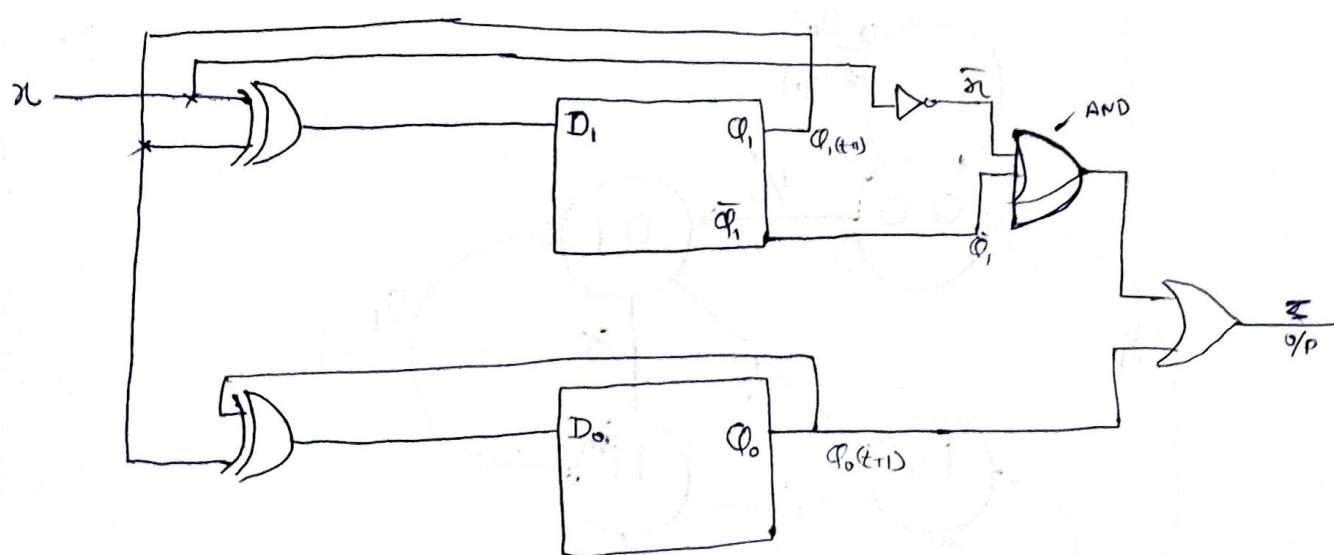
C.P.	D ₃	D ₂	D ₁	D ₀	A ₃	A ₂	A ₁	A ₀
	0	0	0	0	0	0	0	0
Σt	1	0	1	0	1	0	1	0
Σt	0	1	0	1	0	1	0	1
Σt	1	0	1	0	1	0	1	0
Σt	1	0	1	0	1	0	1	0

→ R.S.

Analysis of Sequential circuit

→ In analysis of sequential ckt. or state equation is given and we do analysis about various states and O/p of circuit.

Ques:- find State diagram of Ckt?



Stat Eqn

$$D_1 = Q_1(t+1) = x \oplus Q_1 = x\bar{Q}_1 + \bar{x}Q_1$$

$$D_0 = Q_0(t+1) = Q_0 \oplus Q_1 = Q_0\bar{Q}_1 + \bar{Q}_0Q_1$$

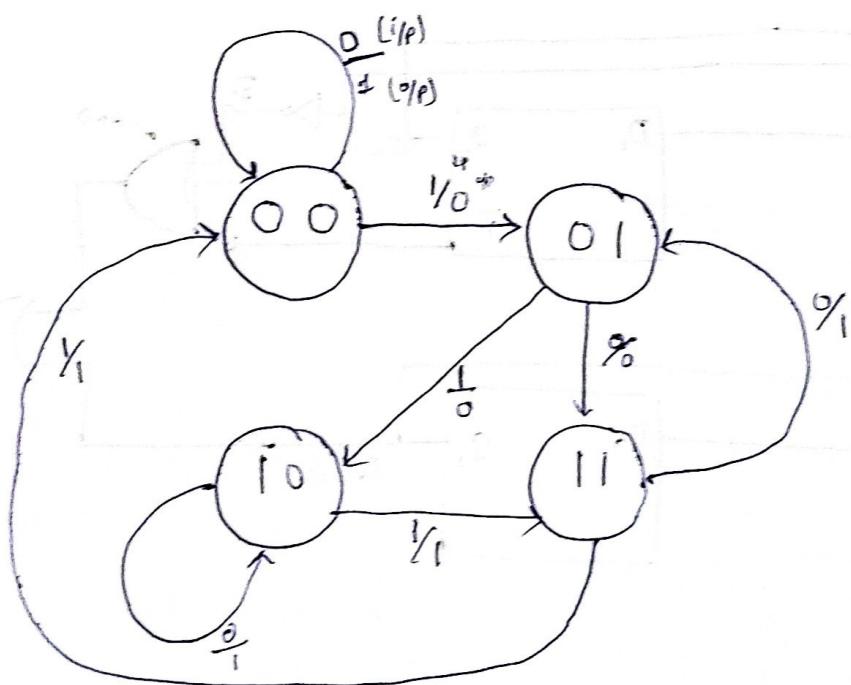
$$Z = Q_0 + \bar{x}\bar{Q}_1$$

$x=0 \rightarrow$ same & \neq
different

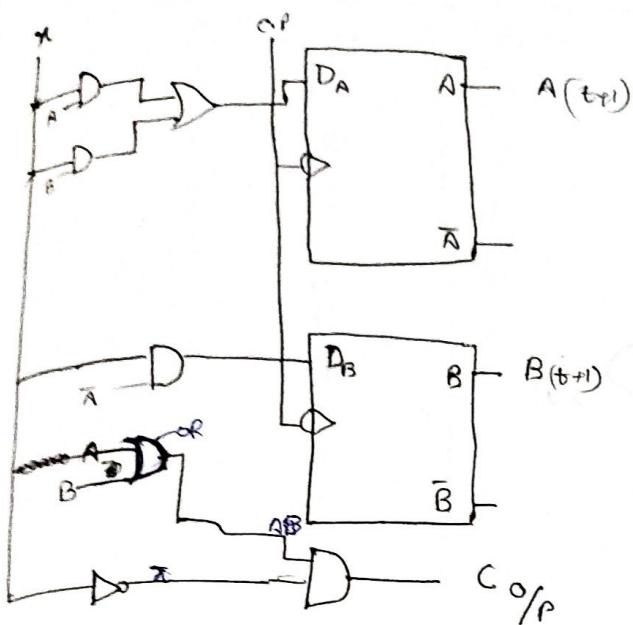
State table

<u>Prev. state</u>		<u>input</u>	<u>Next state</u>		<u>output</u>
Q_0	Q_1	x	$Q_0(t+1)$	$Q_1(t+1)$	Z
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	1	0
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	1	0	0	1

⇒ State diagram



Ques: find state Eqn, state table & state diagram to given circuit?



State Eqn

$$D_A = \bar{A}t + Bx$$

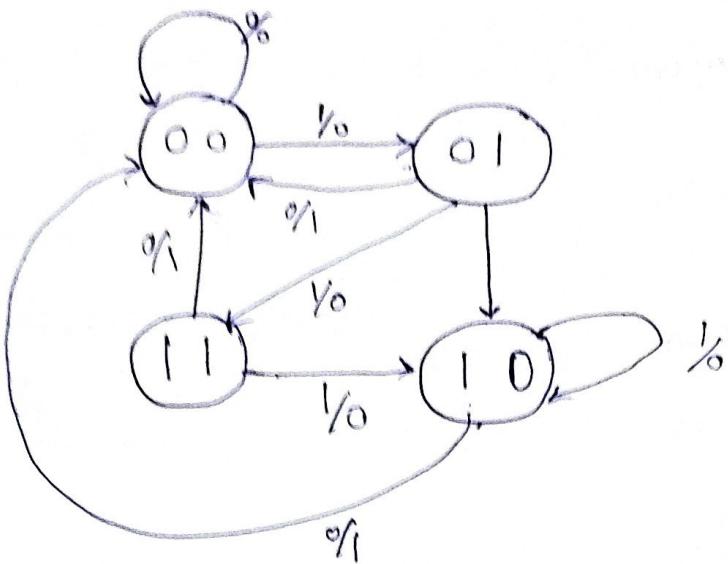
$$D_B = \bar{x}A$$

$$C = (\bar{A} + B)\bar{x}$$

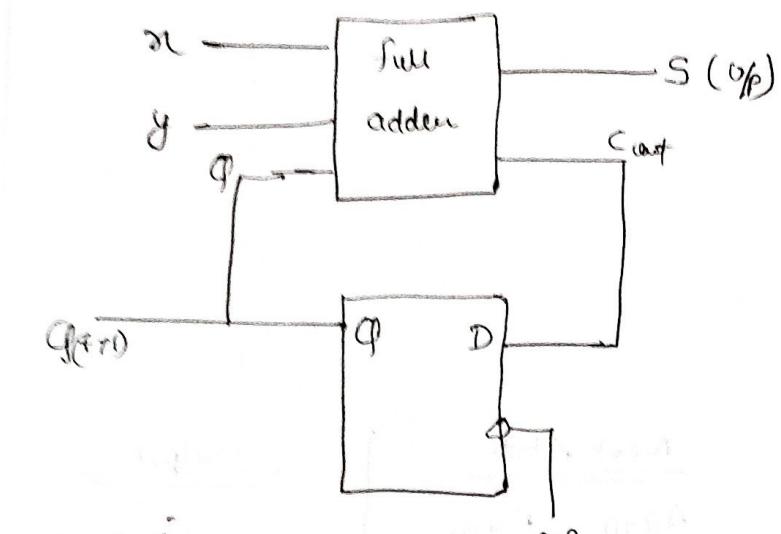
State table

<u>Prev. stat</u>		<u>input</u>		<u>Next stat</u>		<u>output</u>	
A	B	x		A(t+1)	B(t+1)	C	
0	0	0	.	0	0	0	0
0	0	1	.	0	1	0	0
0	1	0	.	0	0	1	1
0	1	1	.	1	1	0	0
1	0	0	.	0	0	1	1
1	0	1	.	1	0	0	0
1	1	0	.	0	0	1	1
1	1	1	.	1	0	0	0

State diagram



Ques: find State diagram —



State Eqn

$$S = n \oplus y \oplus c_f$$

$$C = ny + Yc_f + c_fn$$

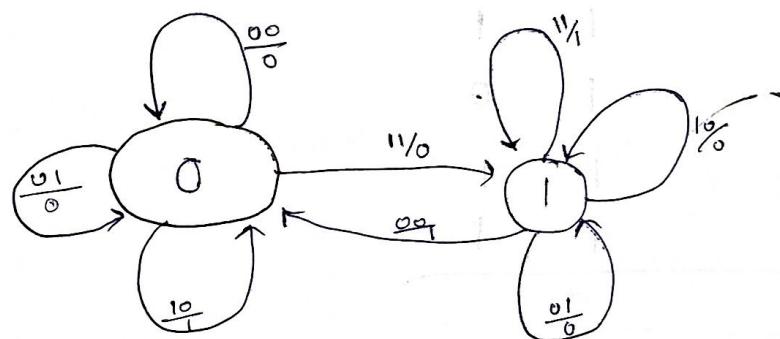
$$Q_{t+1} = D = C = ny + Yc_f + c_fn$$

State table

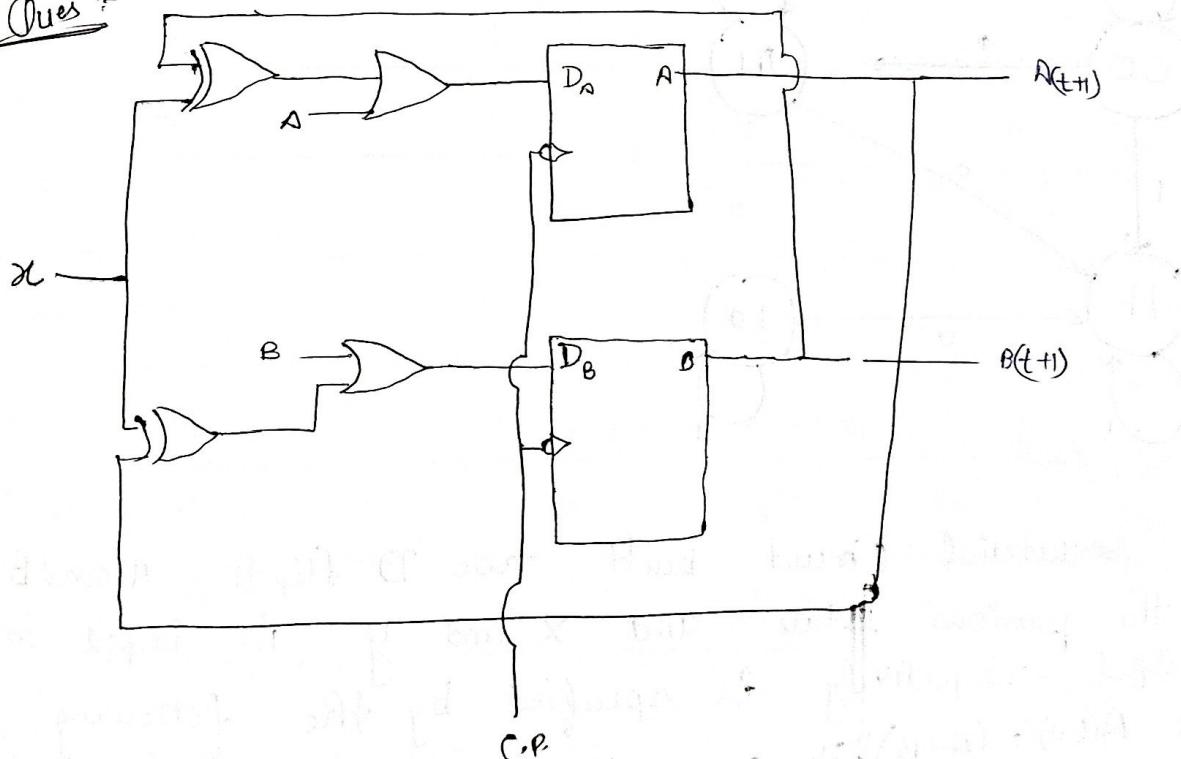


<u>P.S</u>	<u>x</u>	<u>y</u>	<u>Next State</u>	<u>S</u>	
0	0	0	0	0	$(0, 0, 0) + 0 = (0, 0)$
0	0	1	0	1	$(0, 0, 1) + 0 = (0, 1)$
0	1	0	0	1	$(0, 1, 0) + 0 = (0, 1)$
0	1	1	1	0	$(0, 1, 1) + 0 = (1, 0)$
1	0	0	0	1	$(1, 0, 0) + 0 = (1, 0)$
1	0	1	1	0	$(1, 0, 1) + 0 = (1, 0)$
1	1	0	1	0	$(1, 1, 0) + 0 = (1, 0)$
1	1	1	1	1	$(1, 1, 1) + 1 = (0, 0)$

State diagram



Ques :-



State Eqn

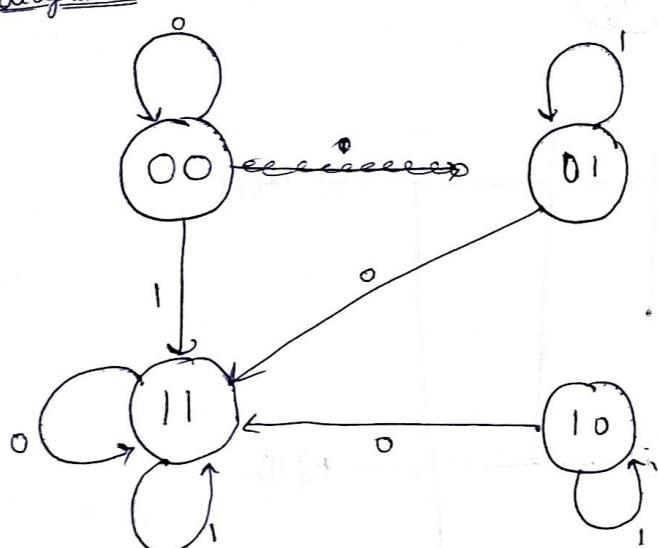
$$D_A = A(t+1) = A + (\bar{x} \oplus B)$$

$$D_B = B(t+1) = B + (\bar{x} \oplus A)$$

State table

Prev. state		Input x	Next state	
			A(t+1)	B(t+1)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	1	1

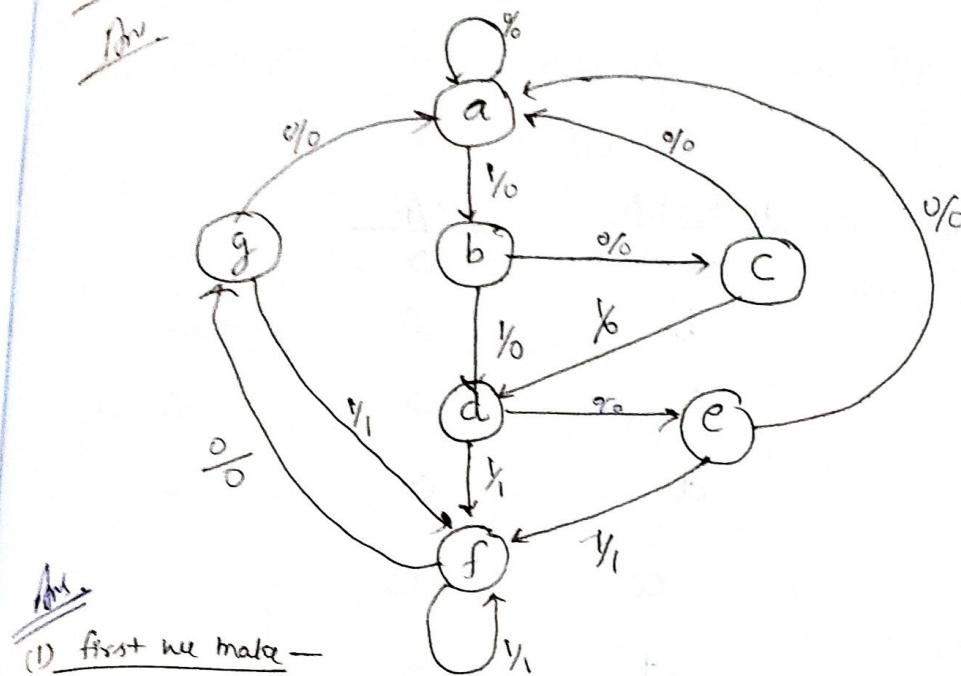
State diagram



other type

Ques: A sequential circuit built two D flip flop A and B is the previous state and x and y is input to output respectively is specified by the following next state $A(t+1) = (A+B) \cdot x$ and $B(t+1) = \bar{A} \cdot x$? Draw its logic diagram and state diagram.

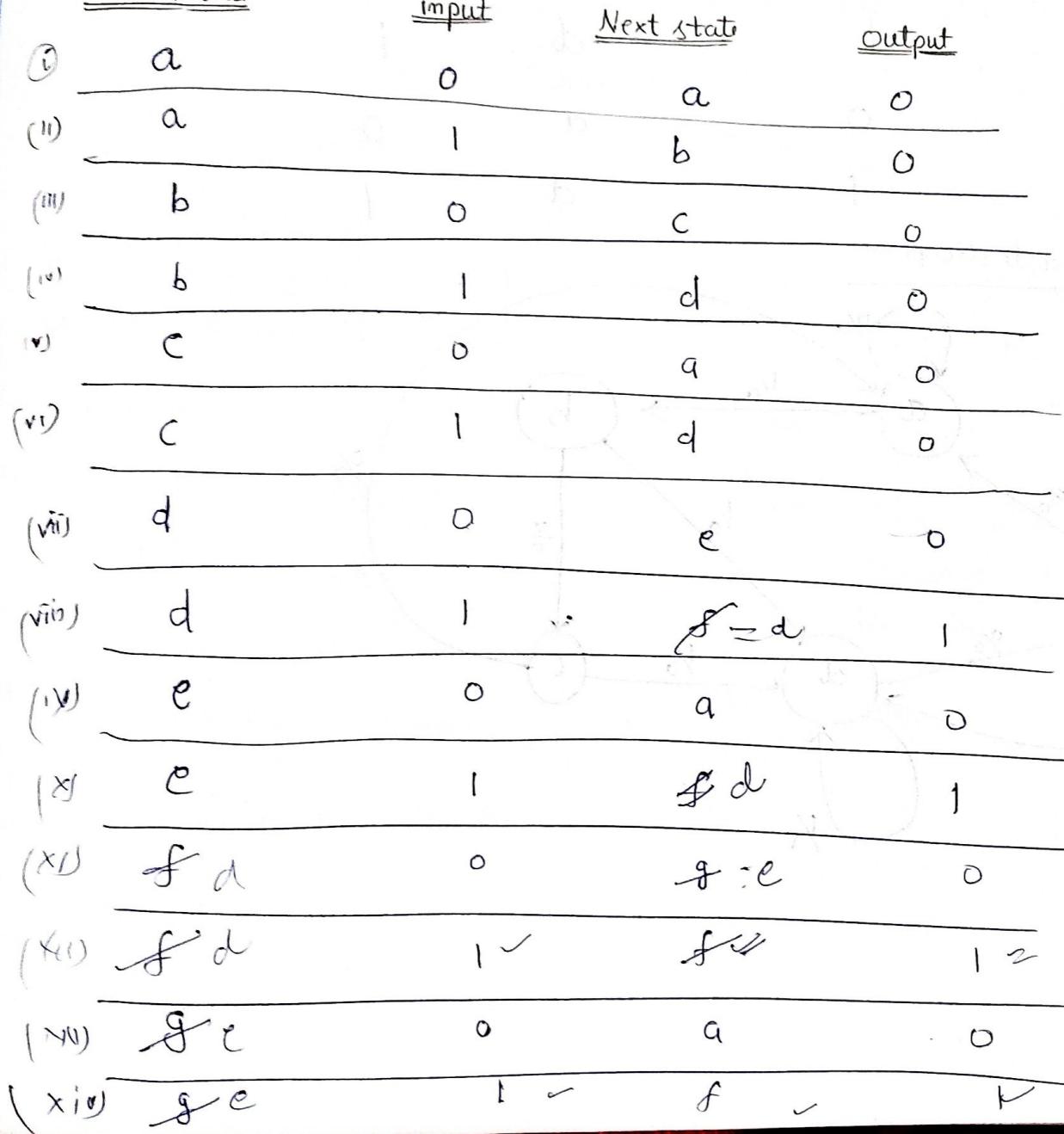
Ques: find state deduction diagram for the state diagram?



(1) first we make -

Stable)

Prov. State



match found

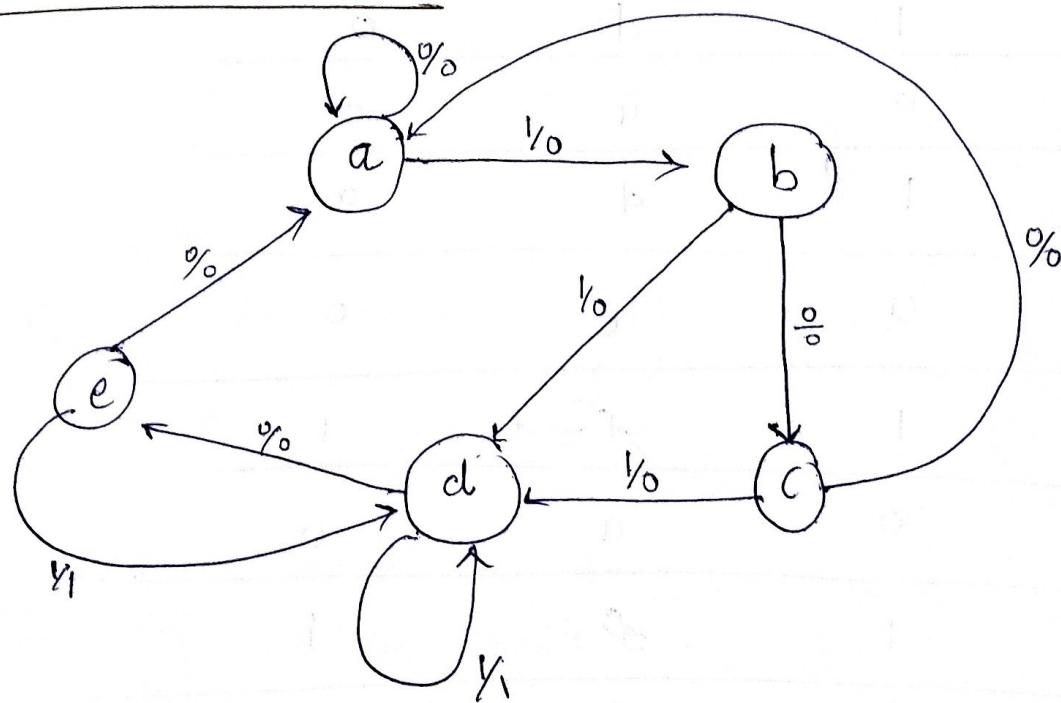
$d = f$

$e = g$

Reduced table

<u>Prev. state</u>	<u>Y/P</u>	<u>next stat</u>	<u>O/P</u>
a	0	a	0
a	1	b	0
b	0	c	0
b	1	d	0
c	0	a	0
c	1	d	0
d	0	e	0
d	1	d	1
e	0	a	0
e	1	d	1

Reduced stat diagram



COUNTER :-

- Counters are basically used to count the number of clock pulse applied.
- Counters can also be used as frequency divider, waveform generators, timers, distance measurements for frequency measurements.
- In Counter bit n -Flip-flop maximum states are 2^n states.

$$N \leq 2^n$$

No. of states used in a counter is also known as "modulous count".

» Based on clock pulse counter are classified into

Counter

Synchronous

(same clock pulse are applied to all Flip-Flop)

↳ faster

↳ Any count sequence is possible

$$\text{Ex. } M \rightarrow 4 = 2^2 = 2^2$$

$$M \rightarrow 6 = \textcircled{3}$$

↳ Eg: → Ring Counter,

→ Johnson Counter

Asynchronous

→ different clock pulse are applied to all Flip-Flop.

↳ Slower

↳ Only fixed counter Sequence (up or down) is possible.

$$M \rightarrow 4, 8, 16 \quad (2^n)$$

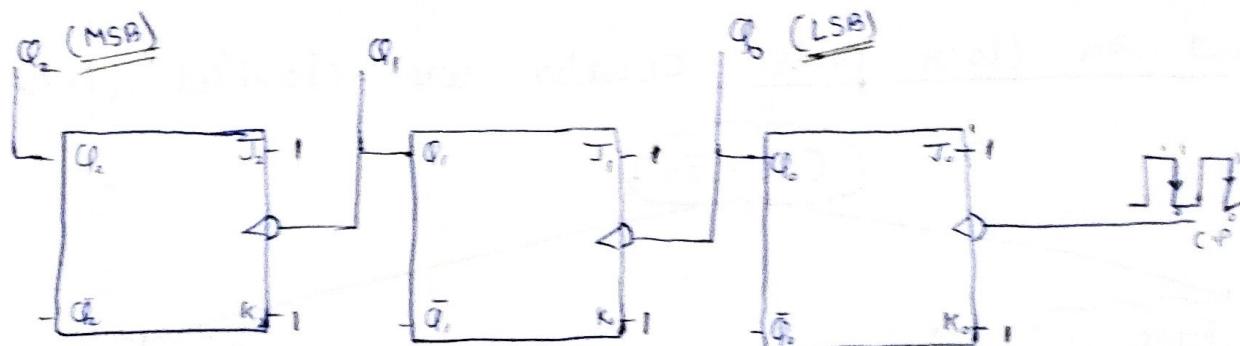
↳ Eg: → Ripple Counter.

* Ripple Counter :-

- It is an asynchronous counter.
- In this different Flip-Flop are applied with different clock frequency.
- In this, Flip-Flop are operated in "toggle mode" ($J=K=F_F$)
- In this, External clock is applied to only first Flip-Flop and the clock to the next F/F is connected from the output of previous Flip-Flop.
- In ripple counter Flip-Flop applied input clock will also act as the LSB.

3-bit-UP Ripple Counter :-

3 F/F $2^3 = 0 - 7$



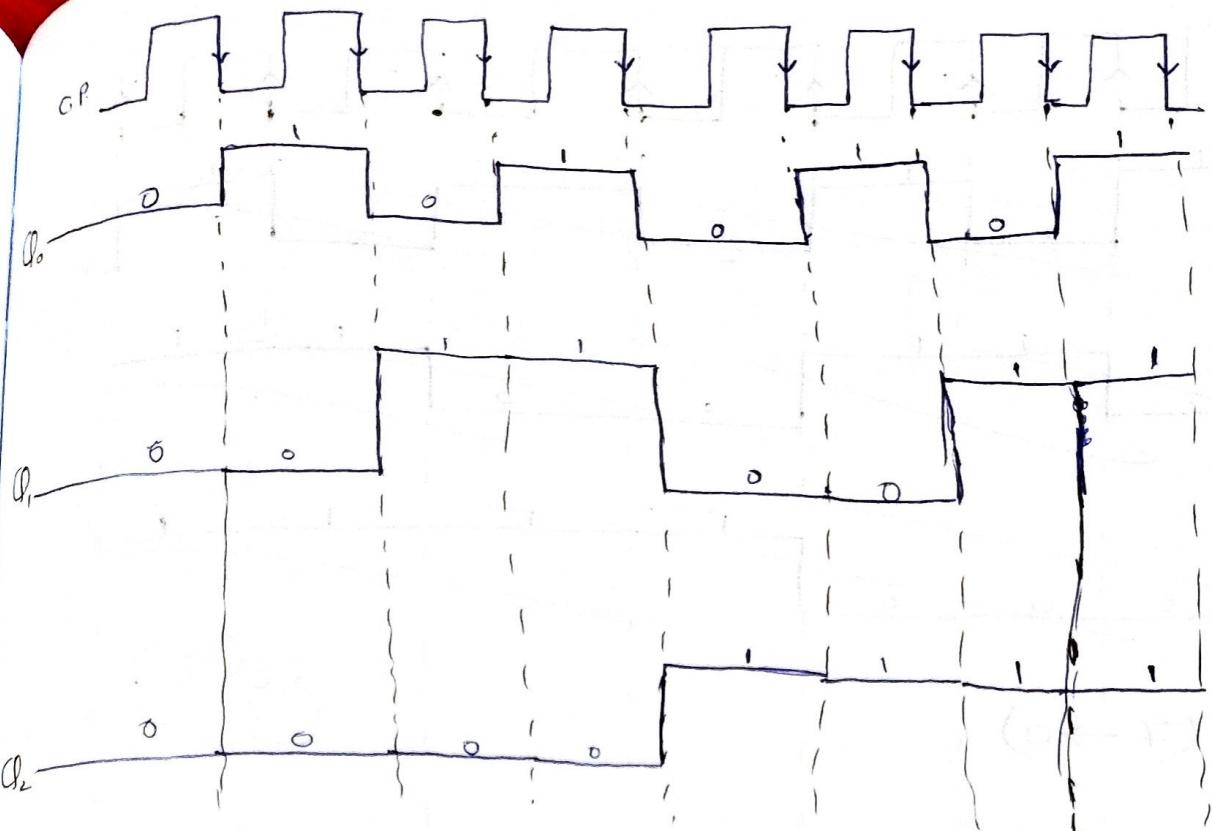
Toggle mode →

<u>J</u>	<u>K</u>	<u>Q(t)</u>	<u>Q(t+1)</u>
1	1	0	1
1	1	1	0

<u>Truth table</u>			
<u>Q₂</u>	<u>Q₁</u>	<u>Q₀</u>	
0 → 0	0	0	
1 → 0	0	1	
2 → 0	1	0	
3 → 0	1	1	
4 → 1	0	0	
5 → 1	0	1	
6 → 1	1	0	
7 → 1	1	1	

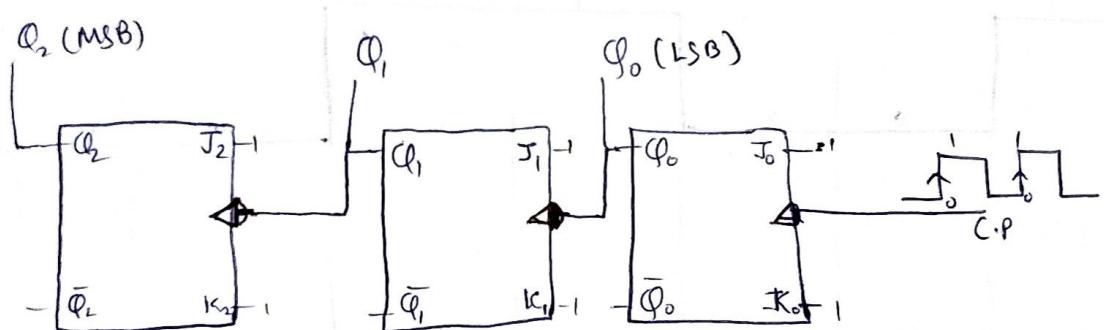
> Timing diagram :-

On next page



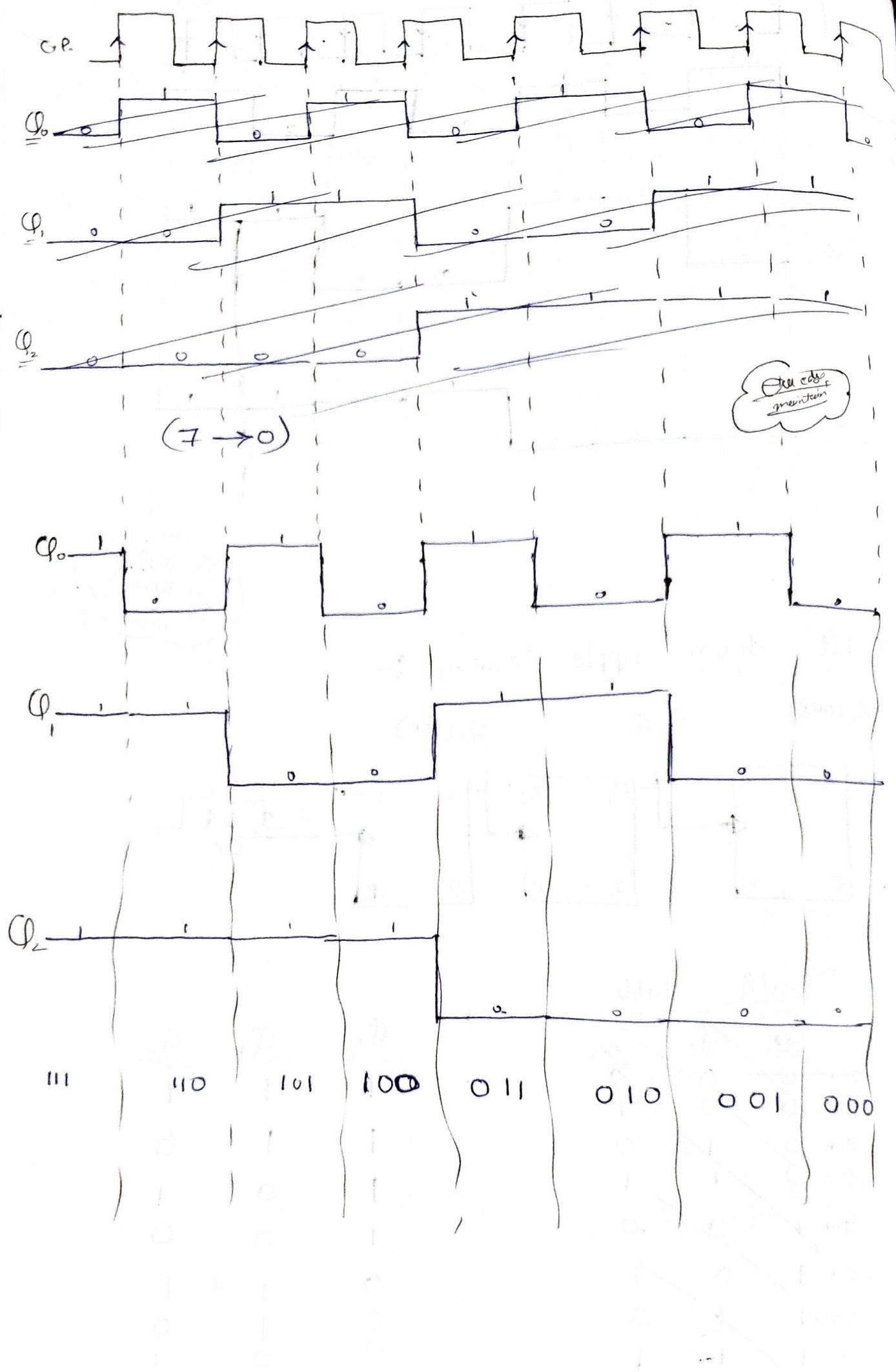
Give (0-1) TR
 Some Rcharge &
 1 → 0 TR charge
 hogus

3-bit down ripple counter :-

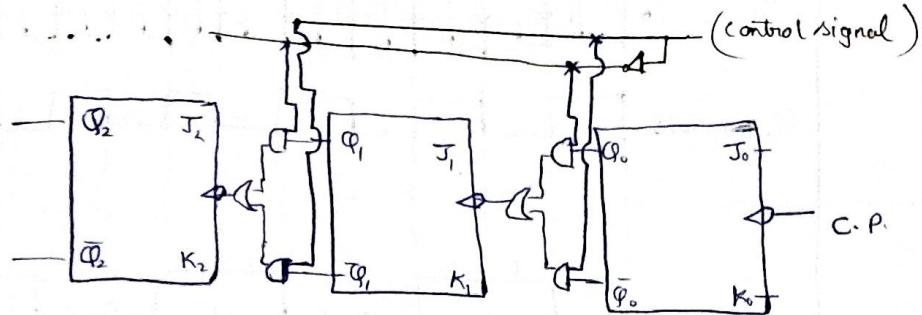


Truth table

	<u>Q_2</u>	<u>Q_1</u>	<u>Q_0</u>		<u>Q_2</u>	<u>Q_1</u>	<u>Q_0</u>
0 →	0	0	0		0	1	0
1 →	0	0	1		1	1	0
2 →	0	1	0		1	0	1
3 →	0	1	1		0	0	0
4 →	1	0	0		1	0	0
5 →	1	0	1		0	1	1
6 →	1	1	0		0	0	1
7 →	1	1	1		0	0	0



3-bit up-down Ripple counter



$\xrightarrow{Q_0, Q_1}$
 $C=0$ (up counter)

$\xrightarrow{\bar{Q}_0, \bar{Q}_1}$
 $C=1$ (down counter)

One cycle
 toggle state
 $0 \rightarrow 1$
 $1 \rightarrow 0$

ONE

$C = 0$			$C = 1$		
\bar{Q}_2	\bar{Q}_1	\bar{Q}_0	\bar{Q}_2	\bar{Q}_1	\bar{Q}_0
0	0	0	1	1	1
1	0	1	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	0	0
5	1	0	1	0	1
6	1	1	0	1	0
7	1	1	1	0	0

- Ques :-
- ① Design a Mod 6 ripple counter.
 - ② Design a mod-12 ripple up counter.
 - ③ Design a decade ripple counter (BCD counter).

Ans. ②.

Mod-12 (0-11)

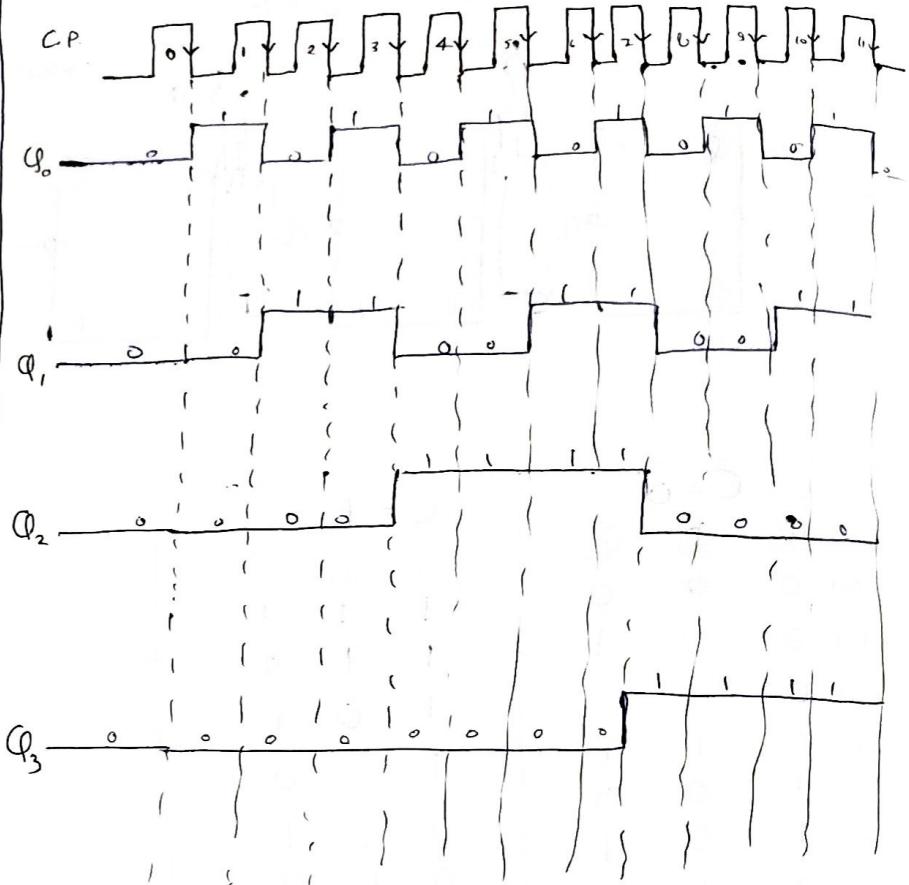
$(12 \rightarrow 1100 \rightarrow 4 \text{ bit})$



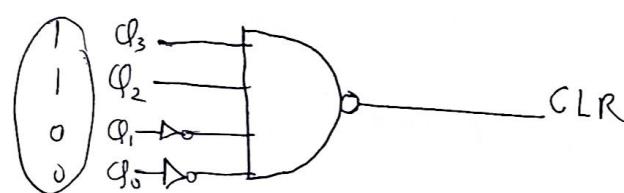
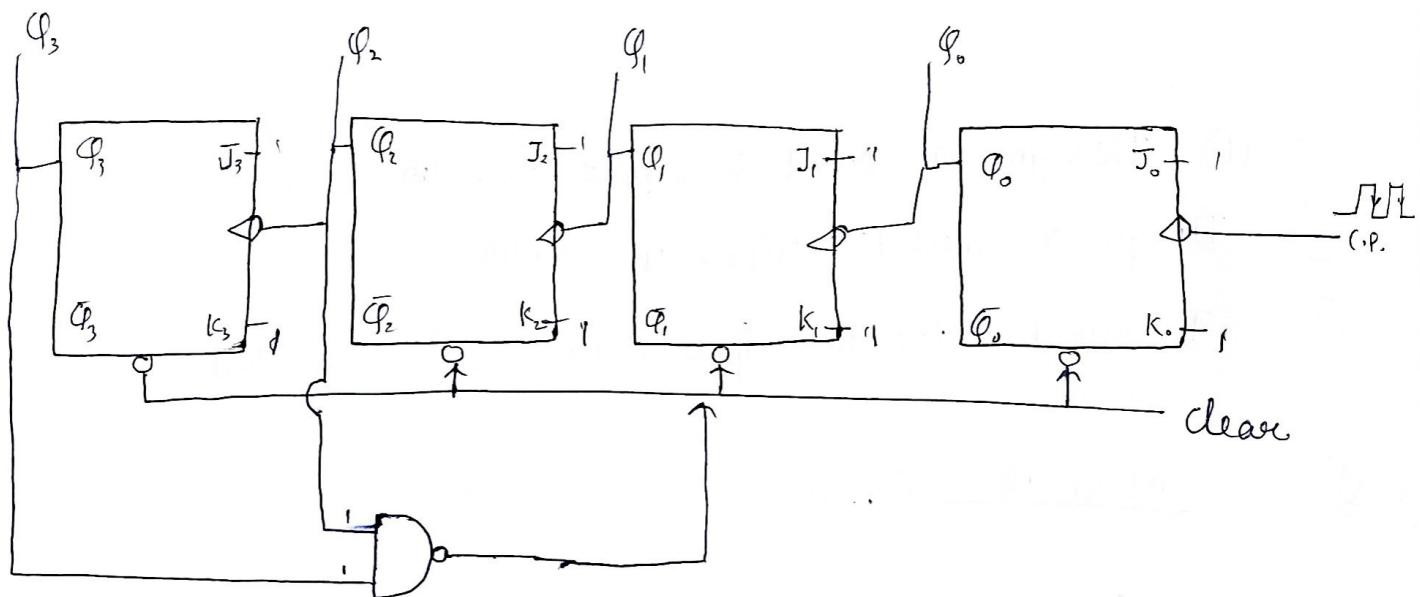
4 Flip-Flop used

<u>Q_3</u>	<u>Q_2</u>	<u>Q_1</u>	<u>Q_0</u>
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1 1 0 0			

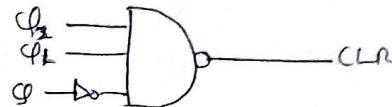
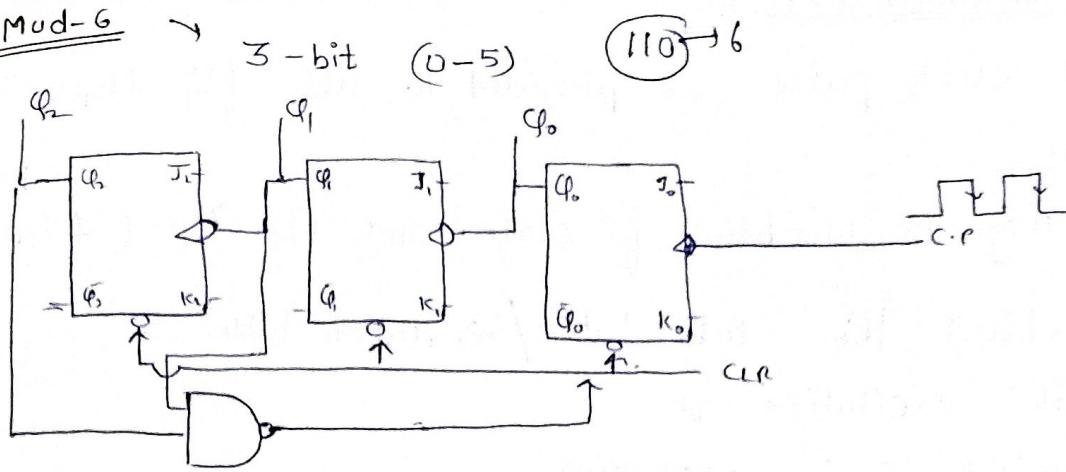
Timing diagram



unstable state



Ans. (ii) Mud-G



<u>Q₂</u>	<u>Q₁</u>	<u>Q₀</u>
----------------------	----------------------	----------------------

0 0 0

0 0 1

0 1 0

0 1 1

1 0 0

1 0 1

1	1	0
---	---	---

unstable state

Ans.
(iii)

BCD (Decade)↓
10

(0 → 9)

4 bit

<u>Q₃</u>	<u>Q₂</u>	<u>Q₁</u>	<u>Q₀</u>
----------------------	----------------------	----------------------	----------------------

0 0 0 0

0 0 0 1

0 0 1 0

0 0 1 1

0 1 0 1

0 1 1 0

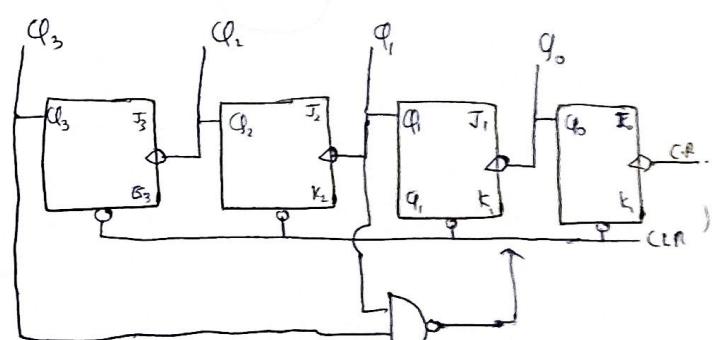
0 1 1 1

1 0 0 0

1 0 0 1

1	0	1	0
---	---	---	---

unstable state



Synchronous Counter

→ Same clock pulse are provided to all flip-flops.

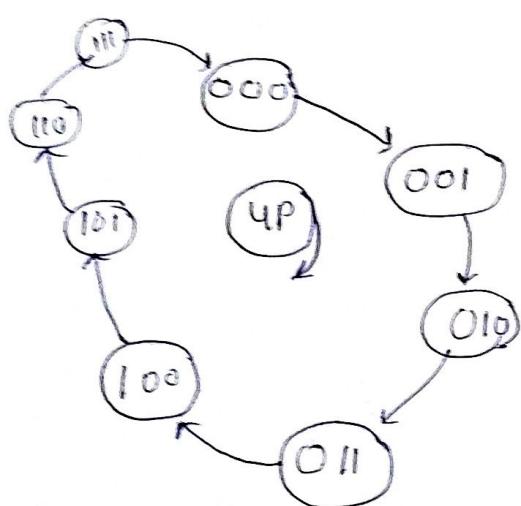
Procedure →

- (i) Identify the number of states and flip-flop. ($1 F/F = \frac{\text{two bits}}{\text{one bit}}$)
- (ii) Construct the state table / excitation table.
- (iii) Write excitation eqn
- (iv) Minimized logic expression
- (v) Implement logic circuit.

3-bit up Synchronous Counter

↳ 3 F/F

↳ $2^3 = 8$ (0 - 7)



Increasing → UP

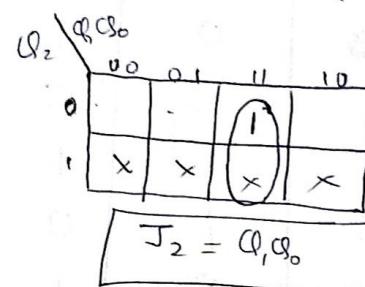
» Excitation table

F Excitation table :-

(Previous State)			(Next State)			J_2, K_2	J_1, K_1	J_0, K_0
Q_2	Q_1	Q_0	$Q_2(t+1)$	$Q_1(t+1)$	$Q_0(t+1)$			
0	0	0	0	0	1	0x	0x	1x
0	0	1	0	1	0	0x	1x	x1
0	1	0	0	1	1	0x	x0	1x
0	1	1	1	0	0	1x	x1	x1
1	0	0	1	0	1	x0	0x	1x
1	0	1	1	1	0	x0	1x	x1
1	1	0	1	1	1	x0	x0	1x
1	1	1	0	0	0	x1	x1	x1

K-Map for J_2

$$J_2 = \Sigma_m(3) + \Sigma_d(4, 5, 6, 7)$$



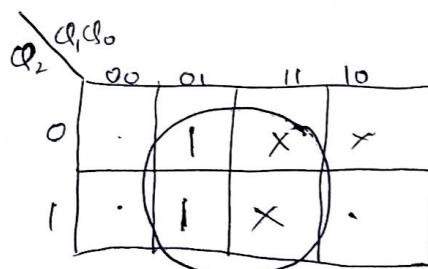
$$J_2 = Q_1 Q_0$$

Excitation table

Q	Q_{t+1}	J	K
0	0	0x	
0	1	1x	
1	0	x1	
1	1	x0	

for J_1

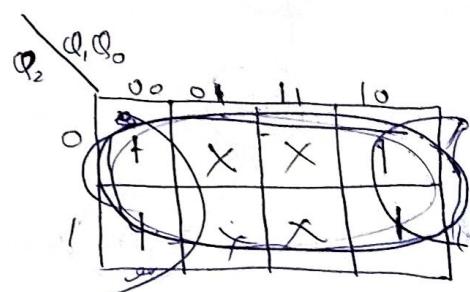
$$J_1 = \Sigma_m(1, 5) + \Sigma_d(2, 3, 6, 7)$$



$$J_1 = Q_0 = K_1$$

for J_0

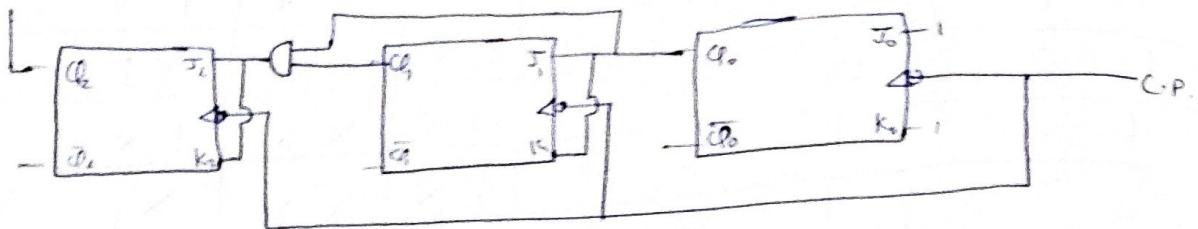
$$J_0 = \Sigma_m(0, 2, 4, 6) + \Sigma_d(1, 3, 5, 7)$$



$$J_0 = Q_0 = K_0$$

$$J_0 = 1 = K_0$$

Logic circuit design



3 bit down Synchronous Counter

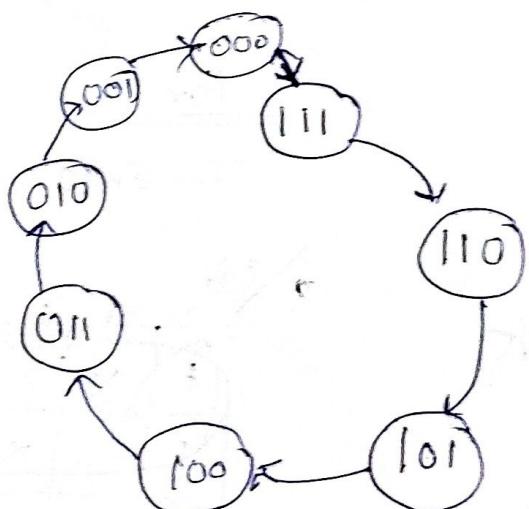
$$\frac{(D - E/F)}{F} \longrightarrow$$

↳ 3 F/F

$$(7 \rightarrow 6 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1)$$

Exitation table

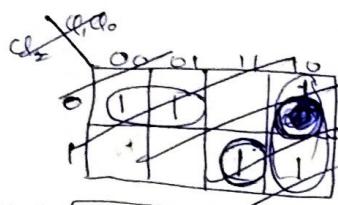
<u>P. S.</u>	<u>N. S.</u>	<u>D₂</u>	<u>D₁</u>	<u>D₀</u>
1110	110	1	1	0
110	101	10	0	1
101	100	1	0	0
100	011	0	1	1
011	010	0	1	0
010	001	0	0	1
001	000	0	0	0
000	111	1	1	1



>> K-Map

for D_2

$$D_2 = \sum m(0, 1, 2, 7)$$



$$D_2 = \overline{Q}_2 \overline{Q}_1 + \overline{Q}_2 Q_0 + Q_2 Q_1 Q_0$$

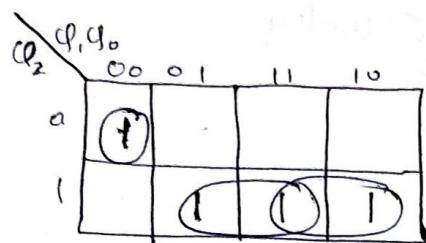
Nothing

for D_1

$$D_1 = \sum m(0, 3, 4, 7)$$

for D_2

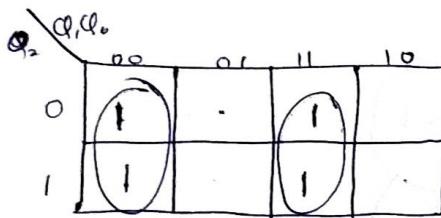
$$D_2 = \sum m(7, 6, 5, 0)$$



$$D_2 = \overline{Q}_2 \overline{Q}_1 \overline{Q}_0 + Q_2 Q_0 + Q_0 Q_1$$

for D_1

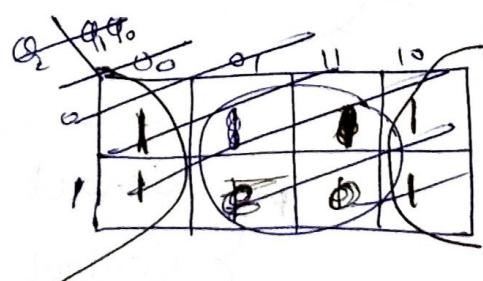
$$D_1 = \sum m(7, 4, 3, 0)$$



$$D_1 = \overline{Q}_1 \overline{Q}_0 + Q_1 Q_0$$

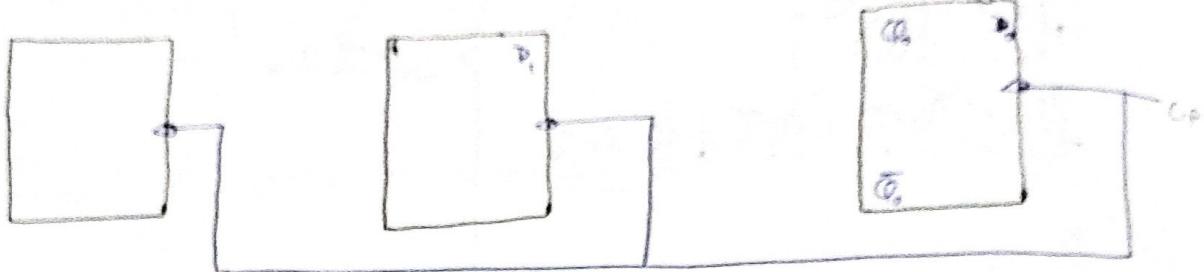
for D_0

$$D_0 = \sum m(6, 4, 2, 0)$$



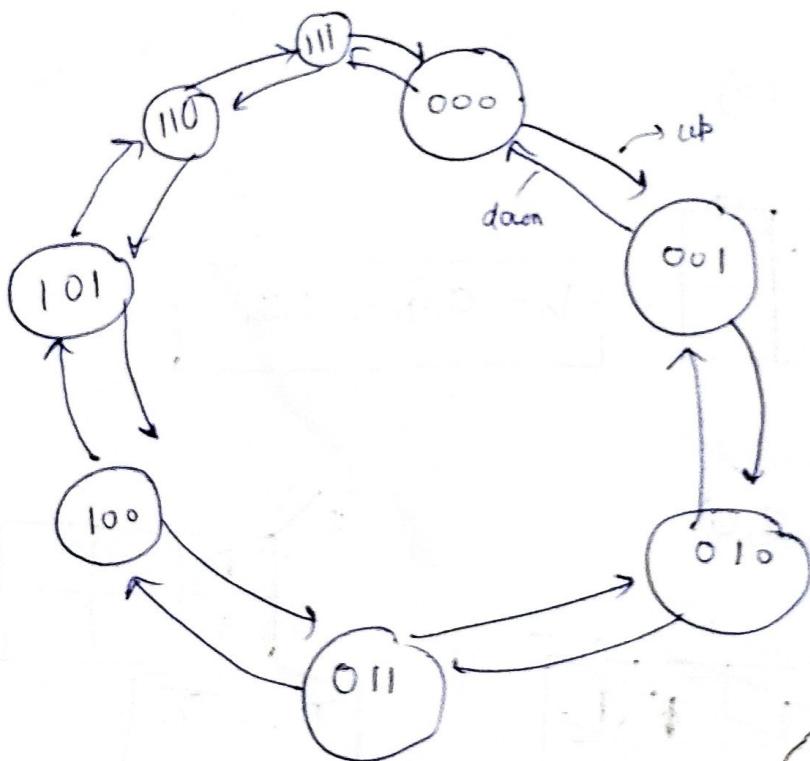
$$D_0 = \overline{Q}_0$$

Logic circuit



» 3-bit synchronous up/down counter

$$2^3 = 8 \quad (0 \leftrightarrow 7)$$



* Control Signal = 0 = u_d
Control Signal = 1 = d_u

» Excitation table

Prev. State c C ₂ C ₁ C ₀	Next State	F/F Input		
		T ₂	T ₁	T ₀
0 0 0 0	0 0 1	0	0	1
0 0 0 1	0 1 0	0	1	1
0 0 1 0	0 1 1	0	0	1
0 0 1 1	1 0 0	1	1	1
0 1 0 0	1 0 1	0	0	1
0 1 0 1	1 1 0	0	1	1
0 1 1 0	1 1 1	0	0	1
0 1 1 1	0 0 0	1	1	1
1 0 0 0	1 1 1	1	1	1
1 0 0 1	1 1 1	0	0	1
1 0 1 0	0 0 1	0	1	1
1 0 1 1	0 1 0	0	0	1
1 1 0 0	0 1 1	1	1	1
1 1 0 1	1 0 0	0	0	1
1 1 1 0	1 0 1	0	1	1
1 1 1 1	1 1 0	0	0	1

K-Map

$$T_2 = \Sigma m(3, 7, 8, 12)$$

$$T_1 = \Sigma m(1, 3, 5, 7, 8, 10, 12, 14)$$

$$T_0 = \Sigma m(0-15)$$

for T_2

CQ_1	CQ_0	00	01	11	10
00
01
11	(1)
10	(1)

$$T_2 = \bar{C} Q_1 Q_0 + C \bar{Q}_1 \bar{Q}_0$$

for T_1

CQ_1	CQ_0	00	01	11	10
00
01
11	(1)	(1)	(1)	.	.
10	(1)	.	.	(1)	.

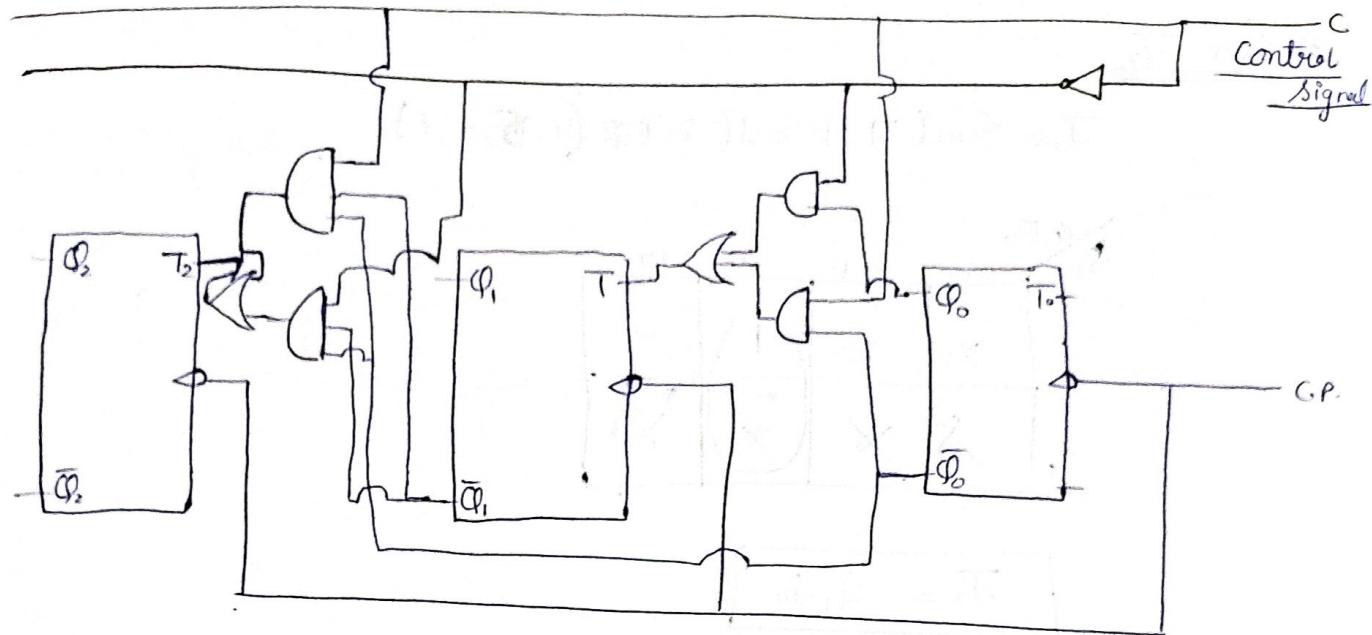
$$T_1 = \cancel{CQ_1 Q_0} + C Q_1 \bar{Q}_0 + \bar{C} \bar{Q}_0$$

$$\bar{C} Q_0 + C \bar{Q}_0 \Rightarrow C \oplus Q_0$$

T_0

$$= 1$$

circuit diagram :-



Question :-

Design mod-5 by using up counter

		Excitation of J-K	
Q _J	Q _K	J	K
0	0	0	X
0	1	X	X
1	0	X	1
1	1	X	0

by using $J-K$ $F/F -$

$$\frac{2^3 = 8}{(0 \rightarrow) (5 - 7 \rightarrow x)}$$

<u>Prev. State</u>	<u>Next State</u>	<u>J₂ K₂</u>	<u>J₁ K₁</u>	<u>J₀ k₀</u>
$Q_2 \ Q_1 \ Q_0$	$Q_2(Q_1) \ Q_2(Q_1) \ Q_0(Q_1)$			
0 0 0	0 0 1	0 X	0 X	1 X
0 0 1	0 1 0	0 X	1 X	X #
0 1 0	0 1 1	0 X	X D	1 X
0 1 1	1 0 0	1 X	X #	X #
1 0 0	0 0 0	X 1 #	0 X	0 X
1 0 1	X X X	X X	X X	X X
1 1 0	X X X	X X	X X	X X
1 1 1	X X X	X X	X X	X X

① for J_2

$$J_2 = \sum_m(3) + \sum_d(\cancel{4, 5, 6, 7})$$

Φ_1, Φ_0

	00	01	11	10
0	X	X	1	X
1	X	X	X	X

$$J_2 = \Phi_1, \Phi_0$$

② for J_1

$$J_1 = \sum_m(1) + \sum_d(2, 3, 5, 6, 7)$$

Φ_1, Φ_0

	00	01	11	10
0	-	1	X	X
1	X	X	X	X

$$J_1 = \Phi_1$$

③ for J_0

$$J_0 = \sum_m(0, 2, \emptyset) + \sum_d(1, 3, 5, 6, 7)$$

Φ_1, Φ_0

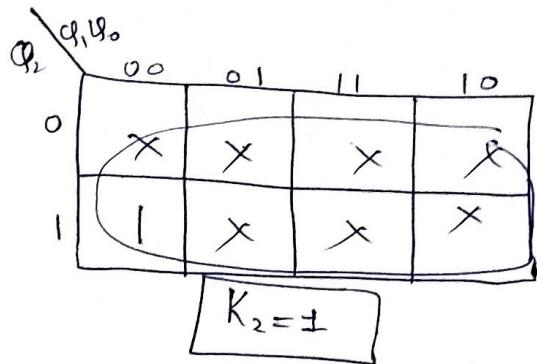
	00	01	11	10
0	1	X	X	1
1	1	X	X	X

$$J_0 = \bar{\Phi}_1$$

$$\begin{matrix} H &= \Phi_2 \\ V &= \cancel{\Phi_2} \end{matrix}$$

for K_2

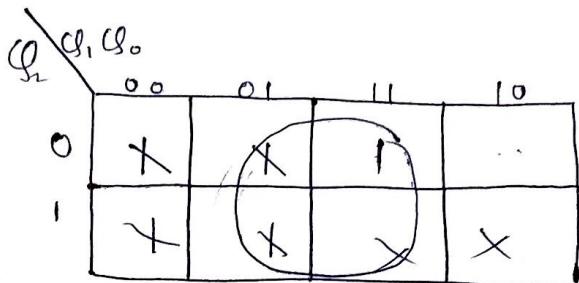
$$K_2 = \Sigma_m(4) + \Sigma_d(0, 1, 2, 3, 5, 6, 7)$$



$$K_2 = 1$$

for K_1

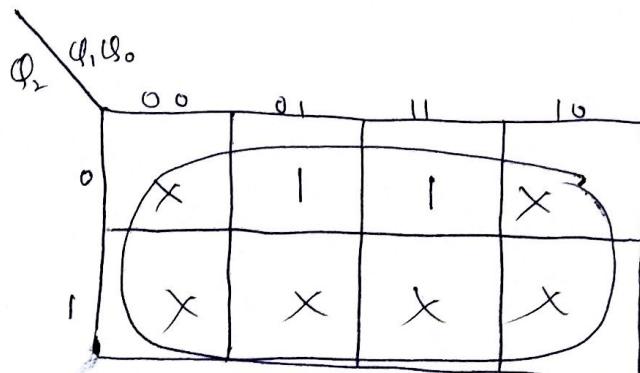
$$K_1 = \Sigma_m(3) + \Sigma_d(0, 1, 4, 5, 6, 7)$$



$$K_1 = Q_0$$

for K_0

$$K_0 = \Sigma_m(1, 3) + \Sigma_d(0, 2, 4, 5, 6, 7)$$



$$K_0 = 1$$