TEXAS INSTRUMENTS
TPS62A01-Q1, TPS62A01A-Q1
ZHCSR54A – FEBRUARY 2023 – REVISED NOVEMBER 2023

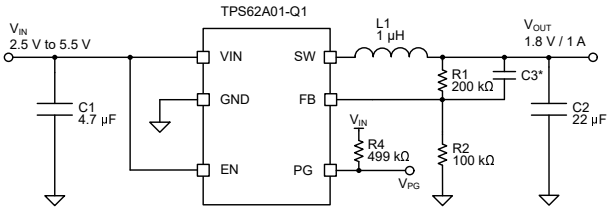
TPS62A01x-Q1 采用 SOT563 封装的 2.5V 至 5.5V、1A 汽车类降压转换器

1 特性

- 输入电压范围为 2.5V 至 5.5V
- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 +125°C T_A
- 可调输出电压范围：0.6V 至 V_{IN}
- 100mΩ 和 67mΩ 低 R_{DSON} 开关
- 小于 25μA 的静态电流
- 1.5% 反馈精度（-40°C 至 150°C）
- 100% 模式运行
- 2.4MHz 开关频率
- 支持节电模式或 PWM 选项
- 电源正常状态输出引脚
- 短路保护 (HICCUP)
- 内部软启动
- 有源输出放电
- 热关断保护
- 采用 1.60mm × 1.60mm SOT563 封装

2 应用

- 前置摄像头
- 环视系统 ECU
- 汽车仪表组显示器



典型应用

3 说明

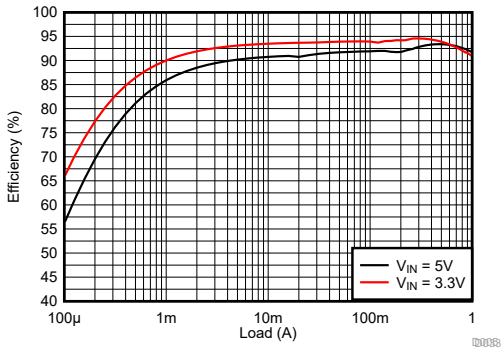
TPS62A01x-Q1 系列器件是同步直流/直流降压转换器，经过优化可实现高效率和紧凑型设计尺寸。这些器件集成了可提供高达 1A 输出电流的开关。在中等负载至重负载情况下，这些器件将以 2.4MHz 开关频率在脉宽调制 (PWM) 模式下运行。在轻载情况下，这些器件自动进入节能模式 (PSM)，从而在整个负载电流范围内保持高效率。关断时，电流消耗量也最低。该器件系列的 TPS62A01A-Q1 型号在整个负载电流范围内以强制 PWM 模式运行。

TPS62A01x-Q1 器件通过一个外部电阻分压器提供可调节输出电压。内部软启动电路可限制启动期间的浪涌电流。内置的其他特性包括过流保护、热关断保护和电源正常指示。这些器件采用 SOT-563 封装。

器件信息

器件型号(2)	运行模式	封装(1)	封装尺寸(3)
TPS62A01-Q1	PSM、PWM	DRL（SOT-563，6）	1.60mm × 1.60mm
TPS62A01A-Q1	FPWM		

(1) 有关详细信息，请参阅 节 11。
(2) 请参阅 *器件比较表*。
(3) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



效率与输出电流间的关系曲线（电压为 1.8V_{OUT} 时）

Table of Contents

4 Device Comparison Table

Device Number	Output Current	Operation Mode
TPS62A01-Q1	1 A	PSM, PWM
TPS62A01A-Q1	1 A	FPWM

5 Pin Configuration and Functions

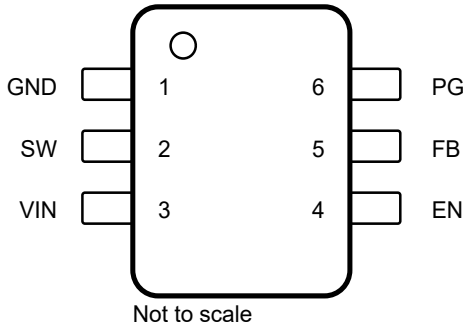


图 5-1. 6-Pin DRL SOT-563 Package (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	4	I	Device enable logic input. Logic high enables the device. Logic low disables the device and turns the device into shutdown. Do not leave the pin floating.
FB	5	I	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.
GND	1	G	Ground pin
PG	6	O	Power-good open-drain output pin. The pullup resistor cannot be connected to any voltage higher than 5.5 V. If unused, leave the pin open or connect to GND.
SW	2	O	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
VIN	3	I	Power supply voltage pin

(1) I = Input, O = Output, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, PG	–0.3	6	V
	SW, DC	–0.3	V_{IN} + 0.3	V
	SW, transient < 10 ns	–3.0	10	V
	FB	–0.3	3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range		2.5		5.5	V
V_{OUT}	Output voltage range		0.6		V_{IN}	V
I_{OUT}	Output current range	TPS62A01			1	A
L	Effective inductance			1.0		µH
I_{PG}	Power-Good input current capability		0		1	mA
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS62A01(A)-Q1		UNIT
		JEDEC	EVM	
		6 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.2	122.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.3	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.9	n/a(2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.4	42.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.
(2) Not applicable to an EVM.

6.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{IN} = 2.5 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = High, V_{FB} = 610 mV		23		µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = Low		0.01	4	µA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	2.3	2.4	2.5	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	2.2	2.3	2.4	V
ENABLE						
$V_{EN(R)}$	High-level input voltage (EN)	EN rising, enable switching	1.2			V
$V_{EN(F)}$	Low-level input voltage (EN)	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} = 5 V			250	nA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	PWM mode	591	600	609	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.6 V			100	nA
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FPWM operation	V_{IN} = 5 V; VOUT = 1.8 V		2400		kHz
STARTUP						
	Internal fixed soft-start time	From EN = High to V_{FB} = 0.56 V			1	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 5 V		100		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 5 V		67		mΩ
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit		1.5	1.8		A
$I_{LS(OC)}$	Low-side valley current limit			1.8		A
POWER GOOD						
V_{PGTH}	Power Good threshold	PG low, FB falling		93.5		%
V_{PGTH}	Power Good threshold	PG high, FB rising		96		%
	PG delay falling			35		µs
	PG delay rising			10		µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5 V			100	nA
	PG pin output low-level voltage	I_{PG} = 1 mA			400	mV
OUTPUT DISCHARGE						
	Output discharge current on SW pin	V_{IN} = 3 V, V_{OUT} = 2.0 V		76		mA
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		170		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

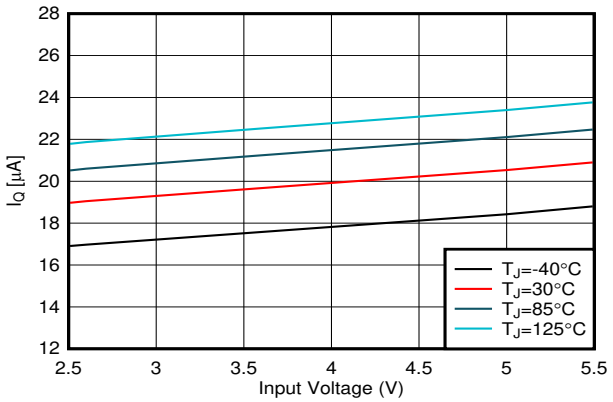


图 6-1. Quiescent Current vs Input Voltage (TPS62A01-Q1)

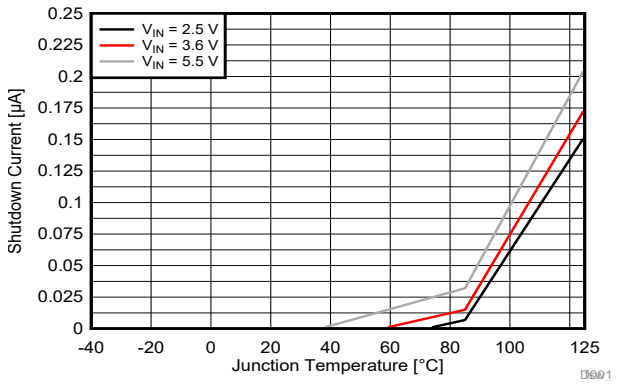


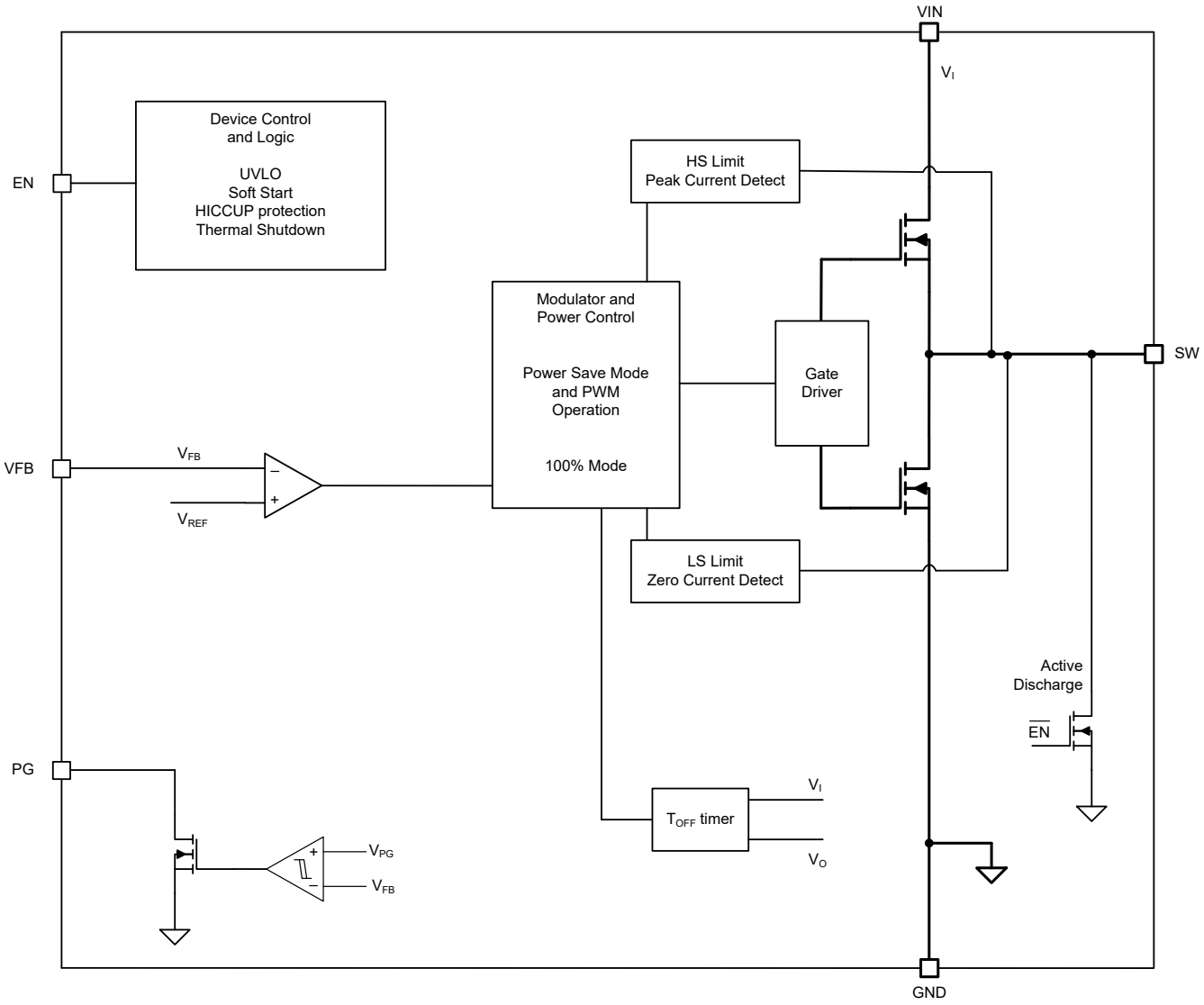
图 6-2. Shutdown Current vs Junction Temperature

7 Detailed Description

7.1 Overview

The TPS62A01x-Q1 is a high-efficiency synchronous step-down converter. The device operates with an adaptive off time with a peak current control scheme. The device operates typically at 2.4-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET, making the switching frequency relatively constant regardless of the variation of the input voltage, output voltage, and load current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Save Mode

The device automatically enters power save mode to improve efficiency at light load when the inductor current becomes discontinuous. In power save mode, the converter reduces the switching frequency and minimizes current consumption. In power save mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or adding a feedforward capacitor.

7.3.2 100% Duty Cycle Low Dropout Operation

The device offers low input-to-output voltage difference by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (1)$$

where

- $R_{DS(ON)}$ = High-side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

7.3.3 Soft Start

After enabling the device, internal soft-start circuitry ramps up the output voltage, which reaches the nominal output voltage during start-up time, avoiding excessive inrush current and creating a smooth voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The TPS62A01x-Q1 is able to start into a prebiased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to the nominal value.

7.3.4 Switch Current Limit and Short-Circuit Protection (HICCUP)

The switch current limit prevents the device from high inductor current and drawing excessive current from the battery or input rail. Due to internal propagation delay, the AC peak current can exceed the static current limit during that time. Excessive current can occur with a shorted or saturated inductor, an overload or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current with an adaptive off time.

When this switch current limit is triggered 32 times, the device stops switching to protect the output. The device then automatically starts a new start-up after a typical delay time of 100 µs has passed. This action is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears. HICCUP protection is also enabled during the start-up.

7.3.5 Undervoltage Lockout

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) is implemented, which shuts down the device at voltages lower than V_{UVLO}.

7.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.

7.4 Device Functional Modes

7.4.1 Enable and Disable

The device is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

7.4.2 Power Good

The TPS62A01x-Q1 has a built-in power-good (PG) feature to indicate whether the output voltage has reached the target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. VIN must remain present for the PG pin to stay low. If not used, the power good can be tie to GND or left open. The PG indicator has a de-glitch to avoid the signal indicating glitches or transient responses from the loop.

表 7-1. Power-Good indicator Functional Table

Logic Signals				PG Status
V_I	EN Pin	Thermal Shutdown	V_O	
V_I > UVLO	HIGH	NO	V_O on target	High Impedance
			V_O < target	LOW
			YES	LOW
		YES	x	LOW
	UVLO < V_I < 1.8 V	x	x	LOW
V_I < 1.8 V	x	x	x	Undefined

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

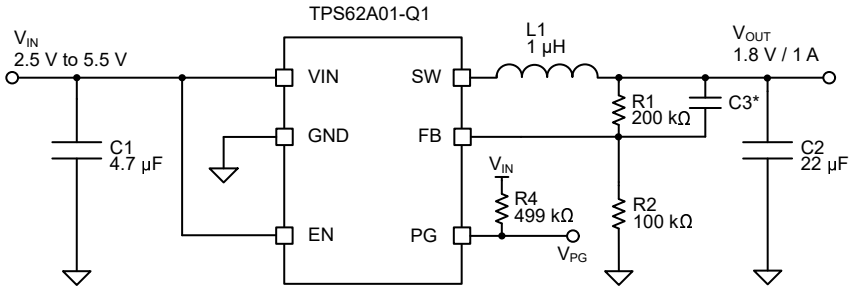


图 8-1. TPS62A01x-Q1 Typical Application Circuit

*C3 is optional

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters

表 8-1. Design Parameters

Design Parameter	Example Value
Input voltage	2.5 V to 5.5 V
Output voltage	1.8 V
Maximum output current	1.0 A

表 8-2 lists the components used for the example.

表 8-2. List of Components

Reference	Description	Manufacturer(1)
C1	4.7 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A475KA73L	Murata
C2	22 µF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BZ71A226KE15L	Murata
L1	1 µH, Power Inductor, XGL3520-102MEC	Coilcraft
R1, R2	Chip resistor, 1%, size 0603	Std.
C3	Optional, 27 pF or 33 pF if needed(2)	Std.

(1) See the *Third-Party Products Disclaimer*.
(2) TI recommends 33 pF for ≤1.8-V output voltage and 27 pF for 3.3-V output voltage.

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to 方程式 2.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (2)$$

R2 must not be higher than 100 kΩ to provide acceptable noise sensitivity.

8.2.2.2 Output Filter Design

The inductor and output capacitor together provide a low-pass filter. To simplify this process, 表 8-3 outlines possible inductor and capacitor value combinations. Please note that stability may vary based on board layout and parasitic elements and it is essential to evaluate and confirm the appropriate values for each specific application. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

In case a lower output ripple is desired, higher output capacitance may help reduce the ripple.

表 8-3. Matrix of Output Capacitor and Inductor Combinations for TPS62A01x-Q1

V_{OUT} [V]	L [µH](1)	C_{OUT} [µF](2)		
		10	22	2 × 22
0.6 ⩽ V_{OUT} < 1.2	1		+	++(3)
1.2 ⩽ V_{OUT} < 1.8	1	+(4)	++(3)	+
1.8 ⩽ V_{OUT}	1	+(4)	++(3)	+

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) This LC combination is the standard value and recommended for most applications.
(4) The minimum C_{OUT} of 10 µF does not support an additional feedforward capacitor.

8.2.2.3 Input and Output Capacitor Selection

The architecture of the TPS62A01x-Q1 allows use of tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are thus recommended. To keep the resistance up to high frequencies and to achieve narrow capacitance variation with temperature, TI recommends to use X7R dielectric.

The input capacitor is the low impedance energy source for the converter that helps provide stable operation. TI recommends a low-ESR multilayer ceramic capacitor for best filtering. For most applications, a 4.7-µF input capacitor is sufficient; a larger value reduces input voltage ripple.

A feedforward capacitor reduces the output ripple in PSM and improves the load transient response. A 33-pF capacitor is good for the 1.8-V output typical application. For the 3.3-V output typical application a 27-pF capacitor is recommended.

8.2.3 Application Curves

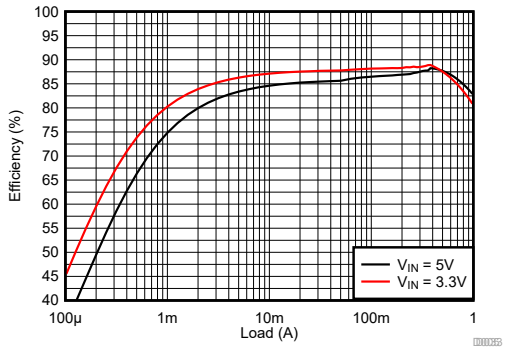


图 8-2. 0.6-V Output Efficiency (TPS62A01-Q1)

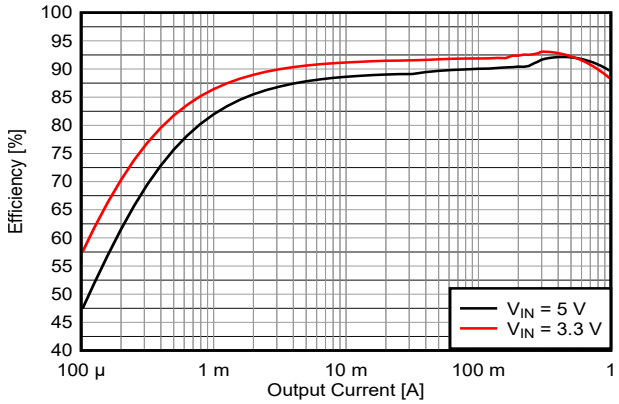


图 8-3. 1.2-V Output Efficiency (TPS62A01-Q1)

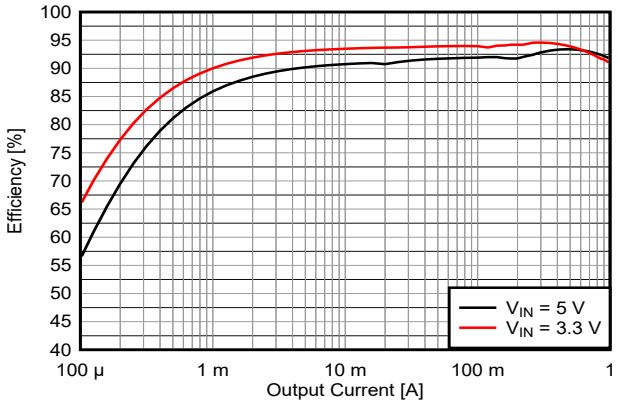


图 8-4. 1.8-V Output Efficiency (TPS62A01-Q1)

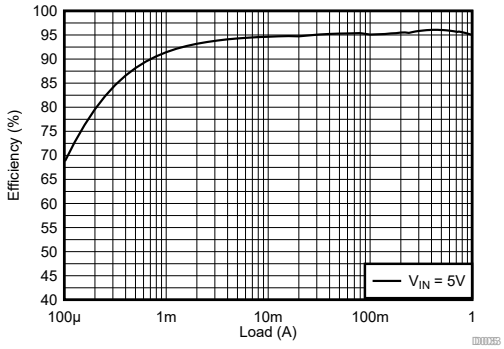


图 8-5. 3.3-V Output Efficiency (TPS62A01-Q1)

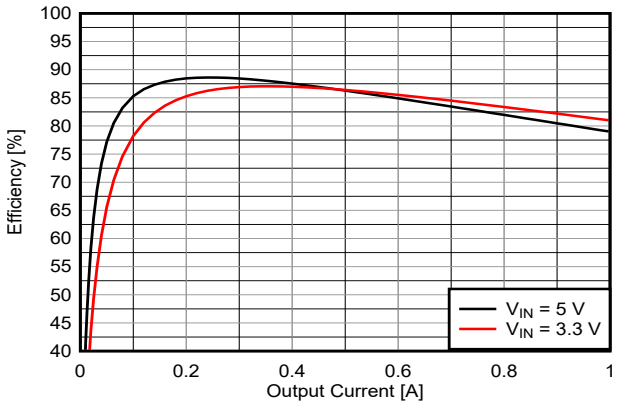


图 8-6. 0.6-V Output Efficiency (TPS62A01A-Q1)

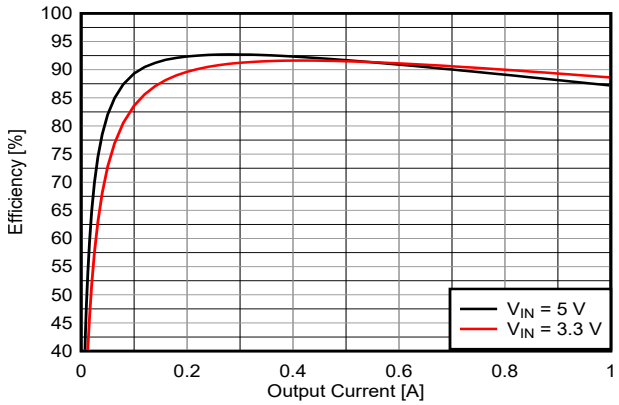


图 8-7. 1.2-V Output Efficiency (TPS62A01A-Q1)

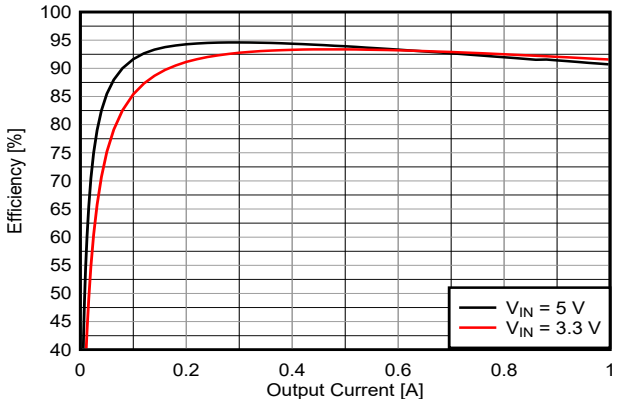


图 8-8. 1.8-V Output Efficiency (TPS62A01A-Q1)

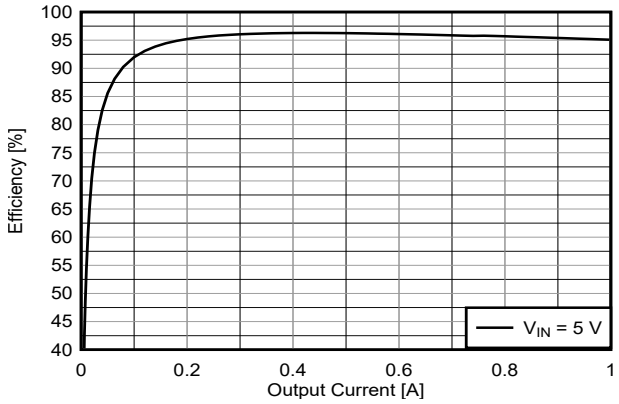
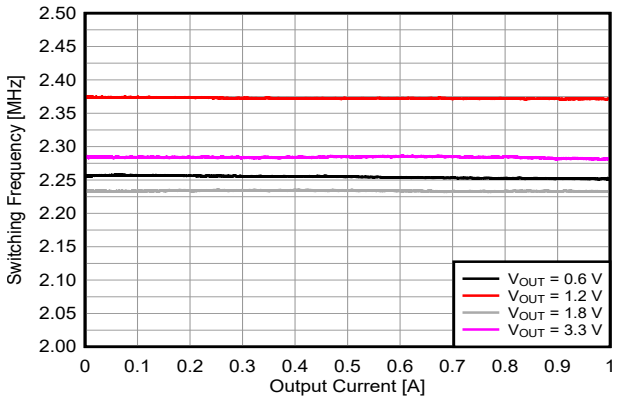
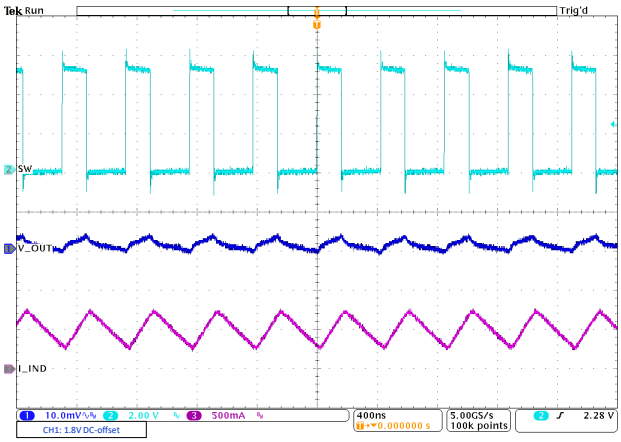


图 8-9. 3.3-V Output Efficiency (TPS62A01A-Q1)



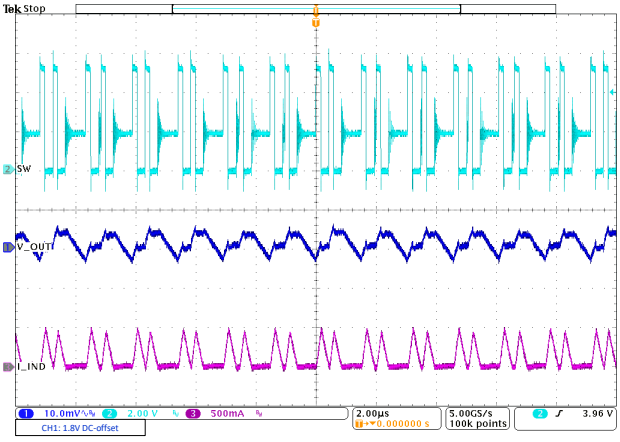
VIN = 5 V Forced-PWM

图 8-10. Switching Frequency vs. Output Current



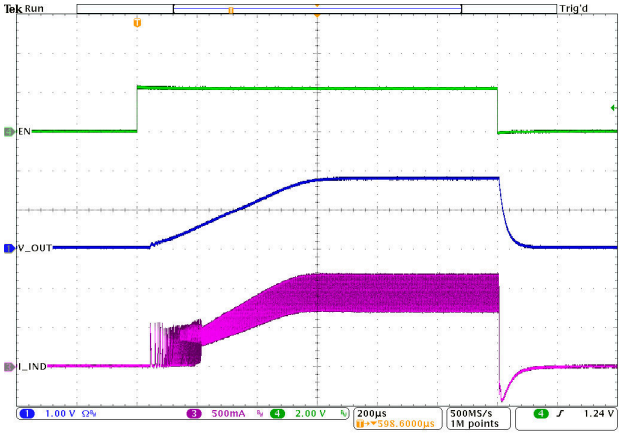
IOUT = 500 mA

图 8-11. PWM Operation



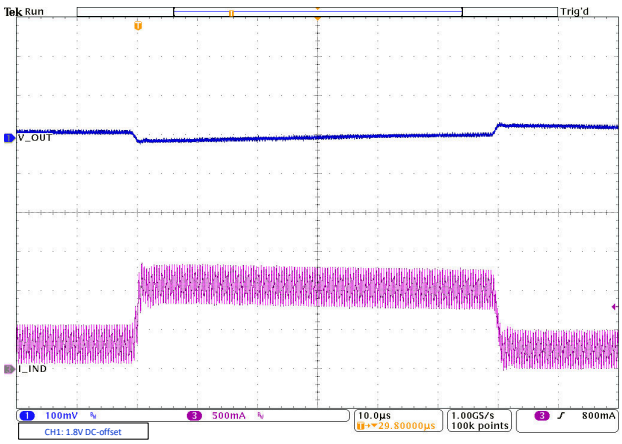
IOUT = 100 mA

图 8-12. Power Save Mode Operation



IOUT = 1 A

图 8-13. Start-Up with Load



Load step: 0.3 A to 1 A

图 8-14. Load Transient

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.5 V to 5.5 V. Make sure that the input power supply has a sufficient current rating for the application.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the TPS62A01x-Q1 device.

- The input, output capacitors and the inductor must be placed as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- The low side of the input and output capacitors must be connected properly to the GND pin to avoid a ground potential shift.
- The sense traces connected to FB is a signal trace. Special care must be taken to avoid noise being induced. Keep these traces away from SW nodes.
- A common ground must be used. GND layers can be used for shielding.

See 图 8-15 for the recommended PCB layout.

8.4.2 Layout Example

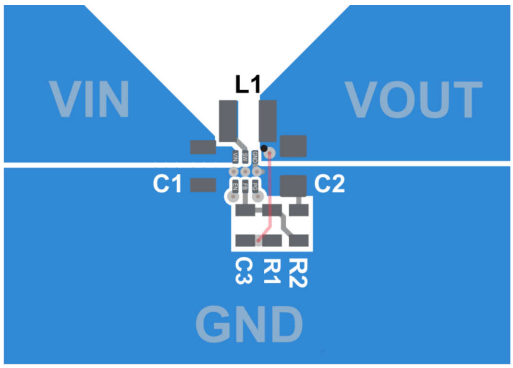


图 8-15. TPS62A01x-Q1 PCB Layout Recommendation

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.1.1 第三方产品免责声明

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9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (February 2023) to Revision A (November 2023)	Page
• 首次公开发布的完整产品说明书	1
• 将文档状态从“预告信息”更改为“量产数据”	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62A01QDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	1OG	Samples
XPS62A01AQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS62A01-Q1, TPS62A01A-Q1 :

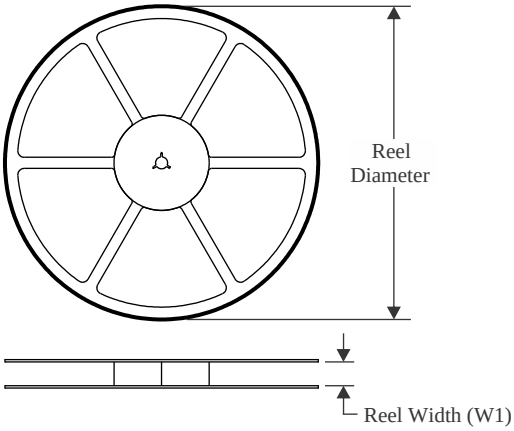
- Catalog : TPS62A01, TPS62A01A

NOTE: Qualified Version Definitions:

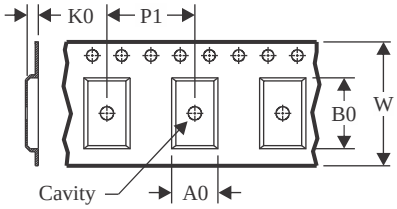
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

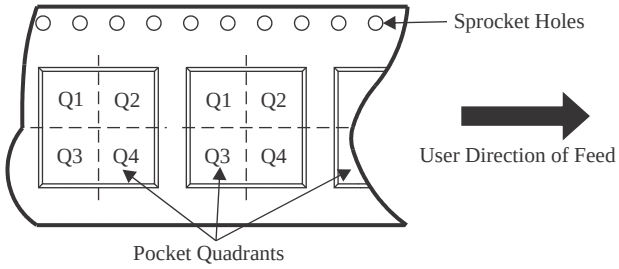


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

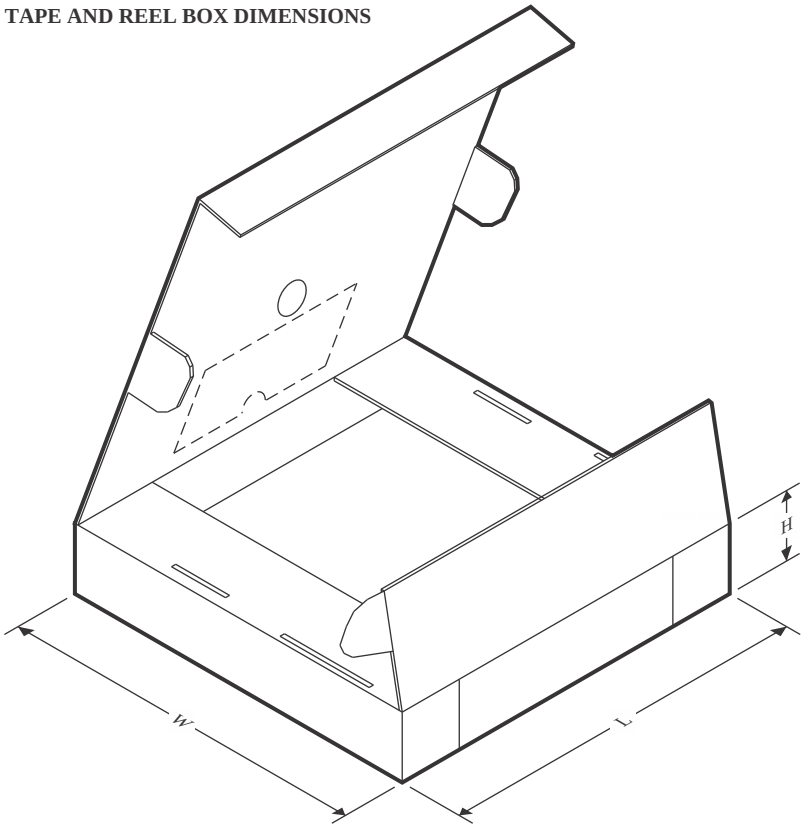
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62A01QDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

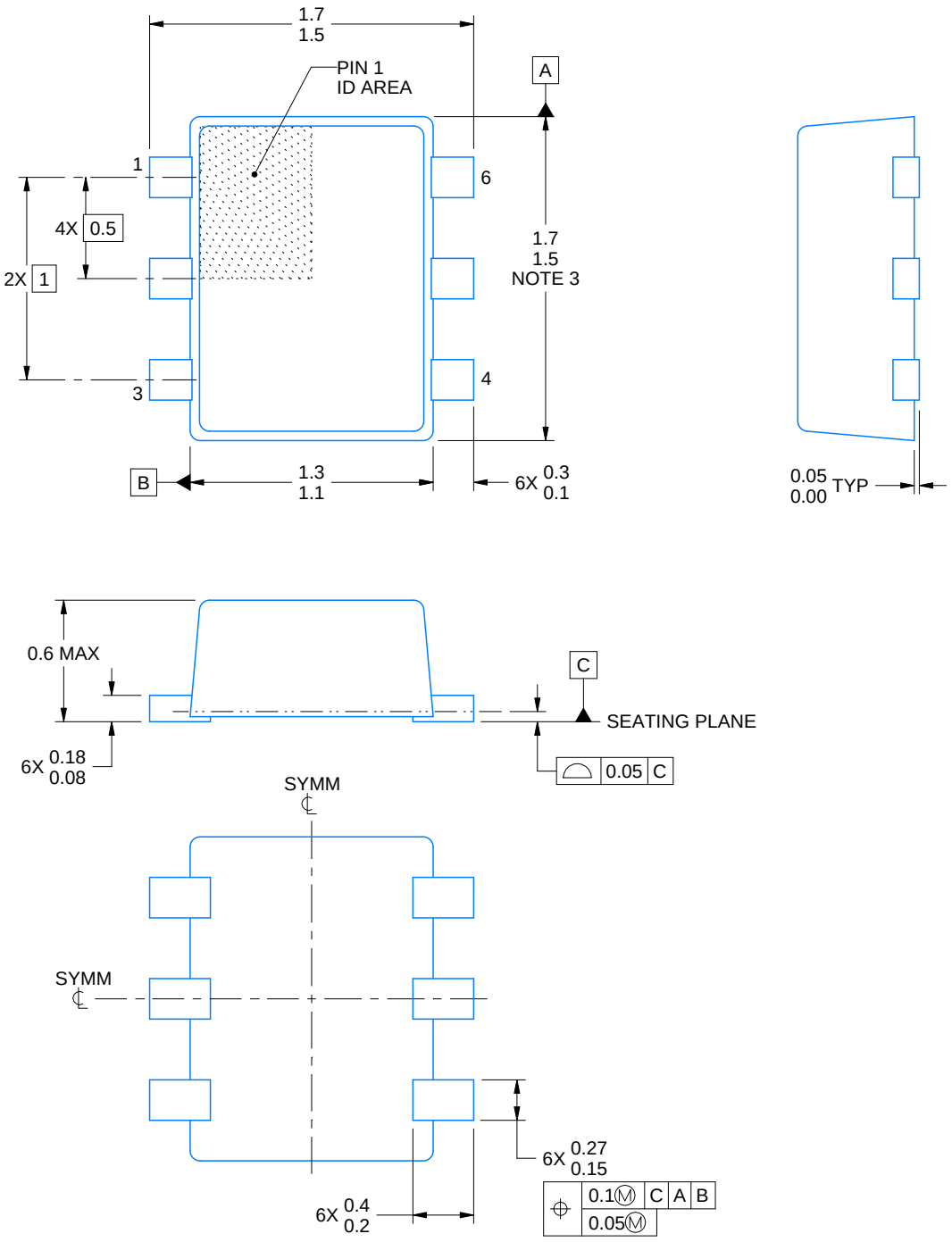
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62A01QDRLRQ1	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

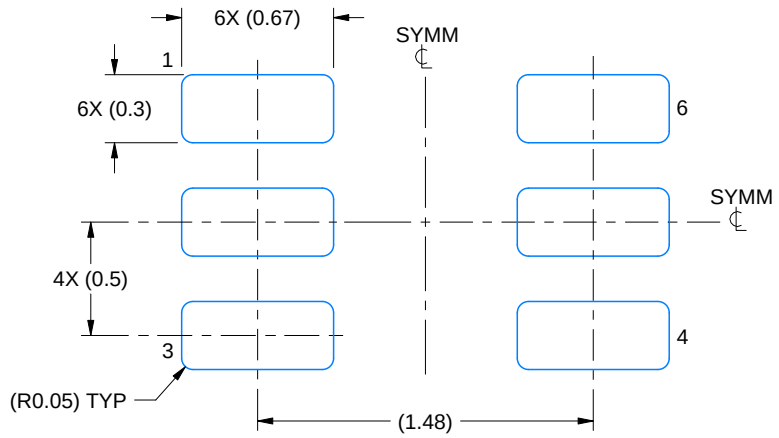
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

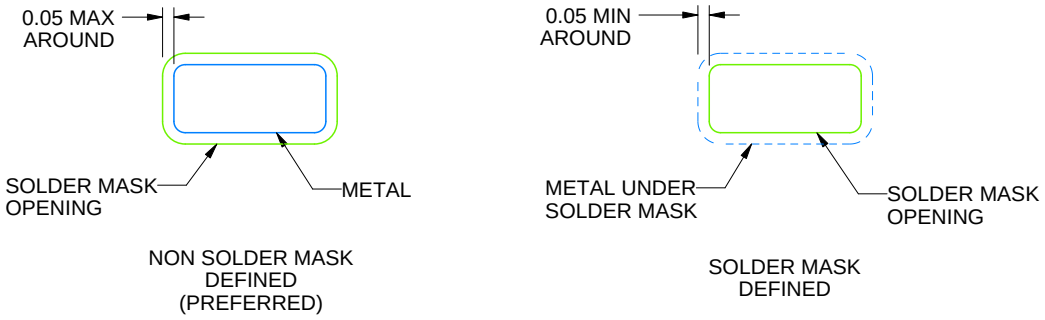


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

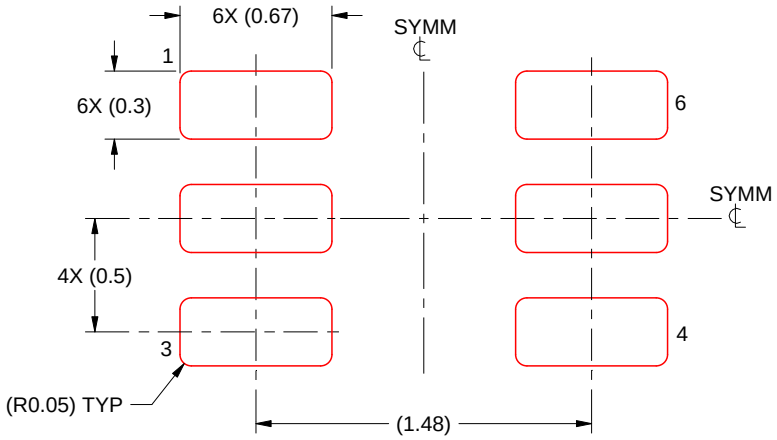
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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