以下基于NUCLEO-F401RE

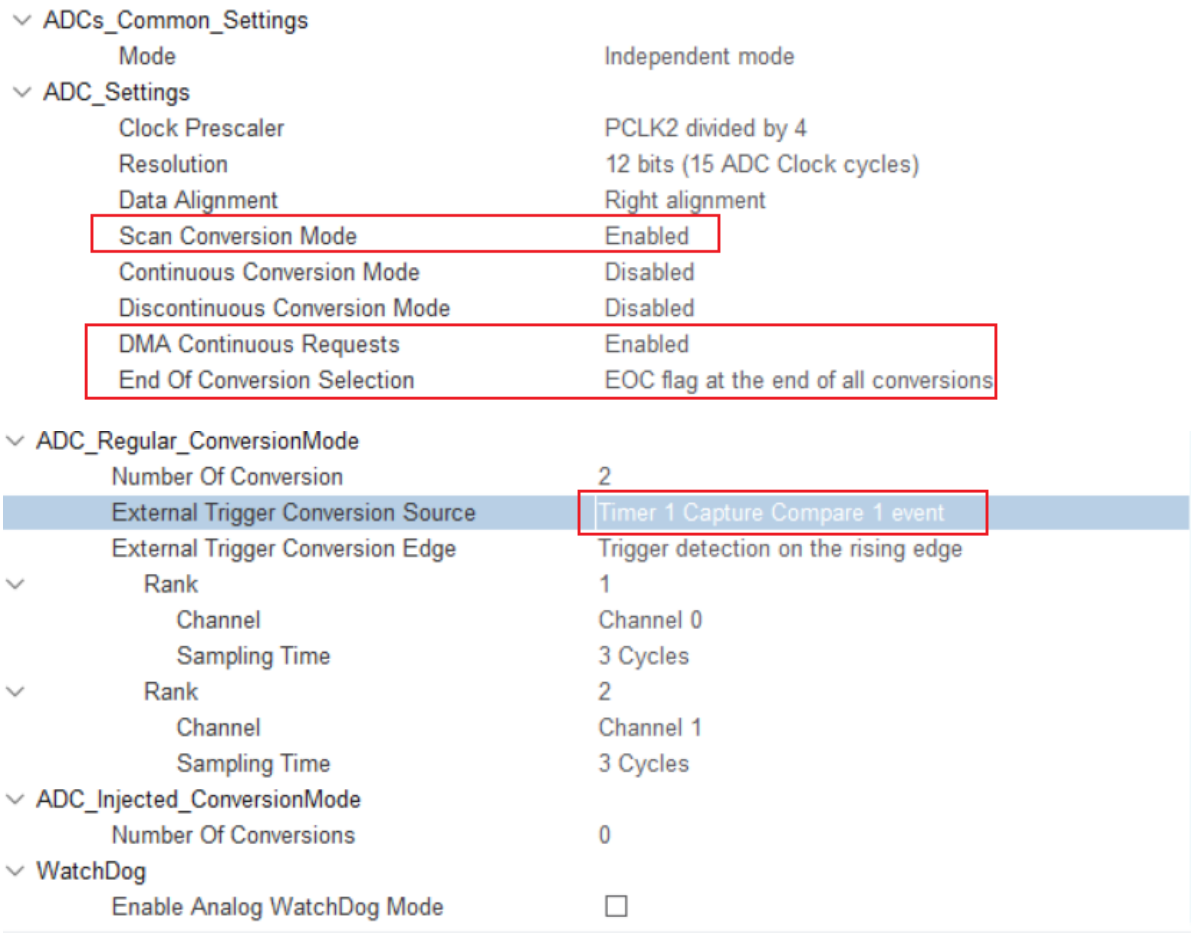
ADC选择Timer触发源

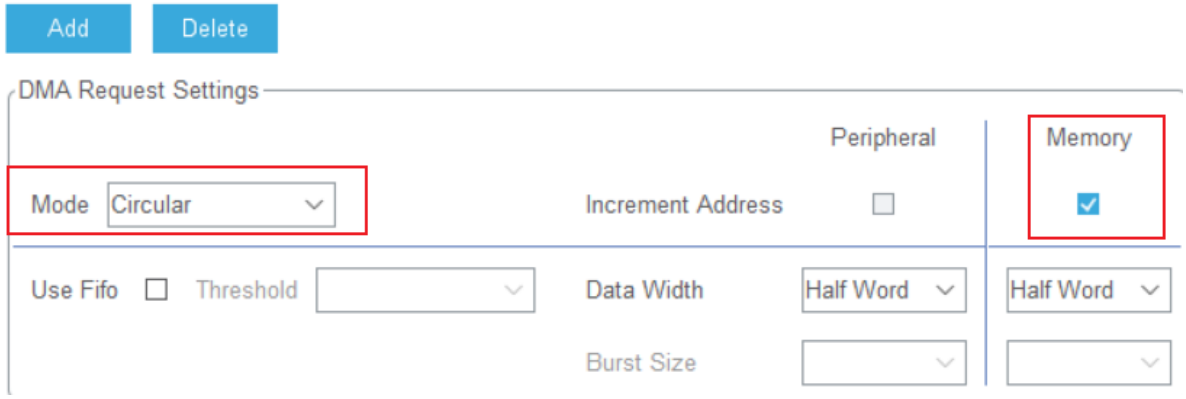
Timer的TGRI、TGRO用来协同与其他Timer或ADC工作。选择TGRO来源，可以是Reset, Enable, Update, Compare等。

Output Compare触发ADC

1.ADC

- 设置连续扫描
- 开启DMA通道
- 设置触发源





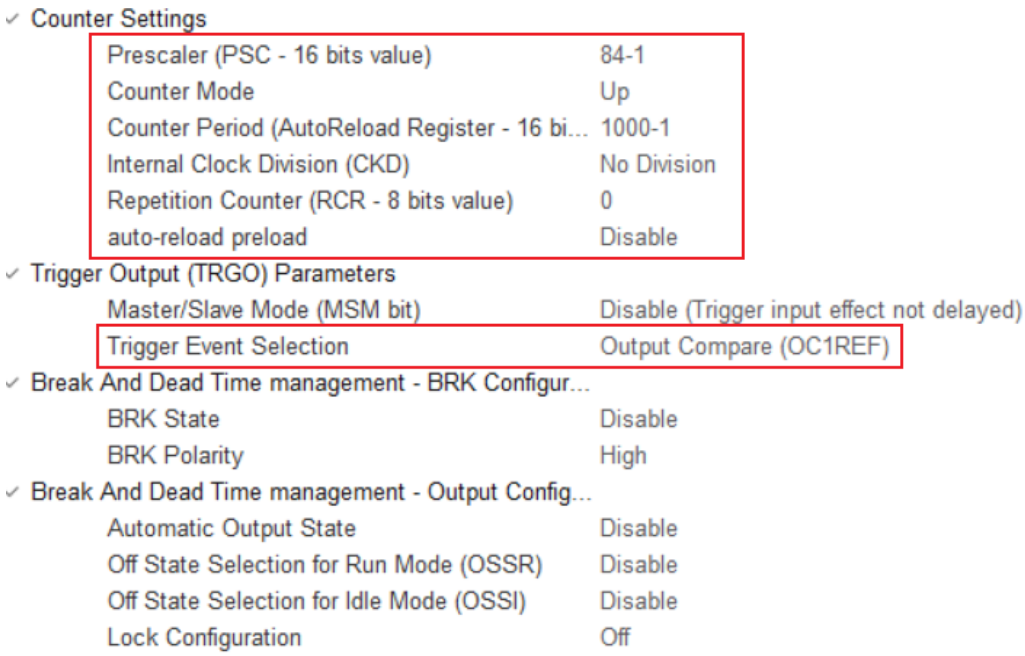
2.Timer1

- 选择时钟源、开启通道
- 设置分频、Period
- 设置Trigger Event

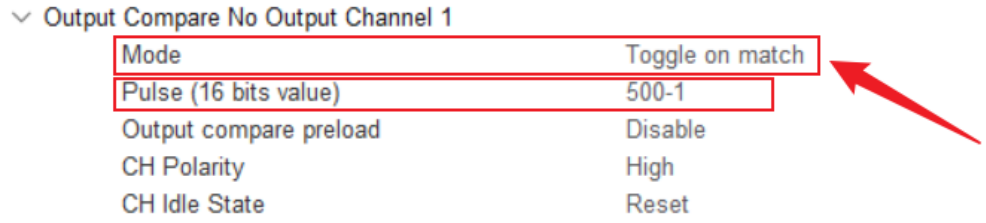
分频、Period根据所在总线时钟设置。

Trigger Event选择OC1REF。MSM bit是用于控制TRGI和TRGO，实现当前Tmer与slave timer同步，不需要配置。

*TRGO Trigger Event*选择信号与*ADC*中选择触发源一致。关注*TRGO Trigger Event*选择信号的控制寄存器。



Mode不能选择FROZEN。FROZEN会“冻结” OC1REF信号。详见 4.Timer1重要寄存器说明



3.程序

```c
/*都可以改为中断式*/
uint16_t ADCdata[2] = {0,0};
HAL_ADC_Start_DMA(&hadc1, (uint32_t*)ADCdata, 2);
HAL_TIM_Base_Start(&htim1);
HAL_TIM_OC_Start(&htim1,TIM_CHANNEL_1);
```

4.Timer1重要寄存器说明

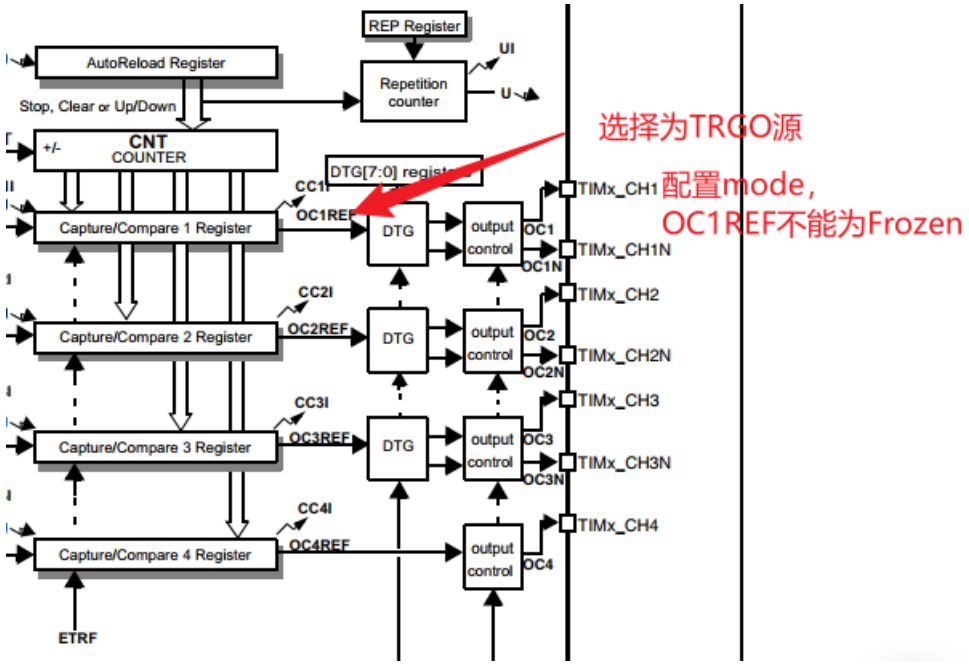
Trigger Event选择OC1REF TIMx_CR2 MMS bit

Bits 6:4 **MMS[2:0]**: Master mode selection

These bits allow to select the information to be sent in master mode to slave timers for synchronization (TRGO). The combination is as follows:
000: **Reset** - the UG bit from the TIMx_EGR register is used as trigger output (TRGO). If the reset is generated by the trigger input (slave mode controller configured in reset mode) then the signal on TRGO is delayed compared to the actual reset.
001: **Enable** - the Counter Enable signal CNT_EN is used as trigger output (TRGO). It is useful to start several timers at the same time or to control a window in which a slave timer is enable. The Counter Enable signal is generated by a logic OR between CEN control bit and the trigger input when configured in gated mode. When the Counter Enable signal is controlled by the trigger input, there is a delay on TRGO, except if the master/slave mode is selected (see the MSM bit description in TIMx_SMCR register).
010: **Update** - The update event is selected as trigger output (TRGO). For instance a master timer can then be used as a prescaler for a slave timer.
011: **Compare Pulse** - The trigger output send a positive pulse when the CC1IF flag is to be set (even if it was already high), as soon as a capture or a compare match occurred. (TRGO).
100: **Compare** - OC1REF signal is used as trigger output (TRGO)
101: **Compare** - OC2REF signal is used as trigger output (TRGO)
110: **Compare** - OC3REF signal is used as trigger output (TRGO)
111: **Compare** - OC4REF signal is used as trigger output (TRGO)

Note: The clock of the slave timer and ADC must be enabled prior to receiving events from the master timer, and must not be changed on-the-fly while triggers are received from the master timer.

输出通道**分级控制**，output compare **MODE控制OC1REF信号**，而不是直接作用于 引脚电平output。OC1REF通过output control驱动 引脚电平output。



output compare MODE控制 TIMx_CCMR1 OC1M bit

Bits 6:4 **OC1M**: Output Compare 1 mode

These bits define the behavior of the output reference signal OC1REF from which OC1 and OC1N are derived. OC1REF is active high whereas OC1 and OC1N active level depends on CC1P and CC1NP bits.

000: Frozen - The comparison between the output compare register TIMx_CCR1 and the counter TIMx_CNT has no effect on the outputs.(this mode is used to generate a timing base). Frozen时，OC1REF锁定不受match影响

001: Set channel 1 to active level on match. OC1REF signal is forced high when the counter TIMx_CNT matches the capture/compare register 1 (TIMx_CCR1).

010: Set channel 1 to inactive level on match. OC1REF signal is forced low when the counter TIMx_CNT matches the capture/compare register 1 (TIMx_CCR1).

011: Toggle - OC1REF toggles when TIMx_CNT=TIMx_CCR1.

100: Force inactive level - OC1REF is forced low.

101: Force active level - OC1REF is forced high.

110: PWM mode 1 - In upcounting, channel 1 is active as long as TIMx_CNT<TIMx_CCR1 else inactive. In downcounting, channel 1 is inactive (OC1REF='0') as long as TIMx_CNT>TIMx_CCR1 else active (OC1REF='1').

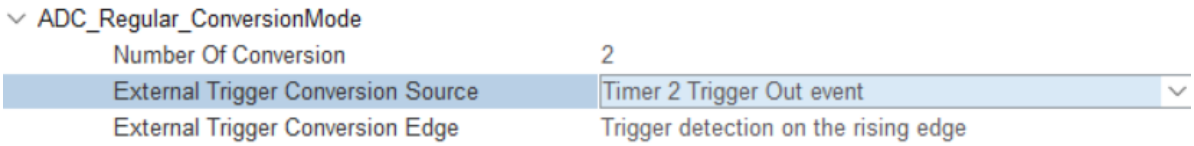
111: PWM mode 2 - In upcounting, channel 1 is inactive as long as TIMx_CNT<TIMx_CCR1 else active. In downcounting, channel 1 is active as long as TIMx_CNT>TIMx_CCR1 else inactive.

Update触发ADC

只说明与*Output Compare*触发*ADC*区别的部分

1.ADC

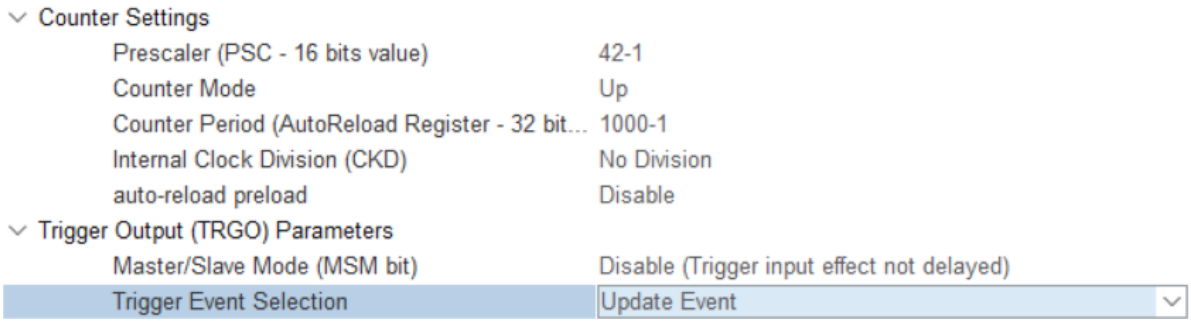
Timer2 Trigger Out



2.Timer2

Trigger Event选择Update Event。

*TRGO Trigger Event*选择信号与*ADC*中选择触发源一致。关注*TRGO Trigger Event*选择信号的控制寄存器。



3.程序

```
uint16_t ADCdata[2] = {0,0};
HAL_ADC_Start_DMA(&hadc1, (uint32_t*)ADCdata, 2);
HAL_TIM_Base_Start(&htim2);
```

调试