Cache Organization & Associativity

In this lab you will get introduced to sim-cache simulator. You will use this simulator to do cache simulation with various configurations.

Quick fact about sim-outorder simulator

It is a memory system simulator. This simulator can emulate a system with multiple levels of instruction and data caches, each of which can be configured for different sizes and organizations. This simulator is ideal for fast cache simulation if the effect of cache performance on execution time is not needed.

All the simulators including sim-cache are available in the home/simplesim-3.0 directory.

Go to home/simplesim-3.0 directory and type the following to seek help about sim-cache.

> home/simplesim-3.0$./sim-cache –h

Help can also be invoked just by typing simulator name without any arguments.

Make sure that the simulator is configured as PISA Simulator, perform the following exercises on test-math program
available in home/simplesim-3.0/tests-pisa/bin/ directory.

1) Use a single run of sim-cache to simulate the performance of the cache under the following conditions:

- least-recently-used (LRU) replacement policy
- 32 to 512 sets
- 1-way to 8-way associativity
- 16-byte cache lines (block size)

Do this two times, once each for a data-only cache and an instruction-only cache. Please copy the configuration files from here   lab1_cache_1a.cfg   lab1_cache_2a.cfg   and modify them to conduct the following experiments. Fill in the tables 1 and 2 below

Miss Ratio (I-Cache)	1-way	2-way	4-way	8-way
32 sets				
64 sets				
128 sets				
256 sets				
512 sets				

Miss Ratio (D-Cache)	1-way	2-way	4-way	8-way
32 sets				
64 sets				
128 sets				
256 sets				
512 sets				

Now use MATLAB or EXCEL to plot the results of the simulations. For each of the simulations (data, instruction), plot the miss ratio versus associativity for each number of sets. Using markers, show the points on the curves which correspond to total cache sizes of 1 Kbytes, 2 Kbytes, 4 Kbytes and 8 K bytes (total cache size = sets * block size * associativity). For each simulation, you should produce something that resembles the plot below. In the plot results are shown from the instruction cache simulation.

Associativity vs Miss Ratio for various IL1 cache configurations
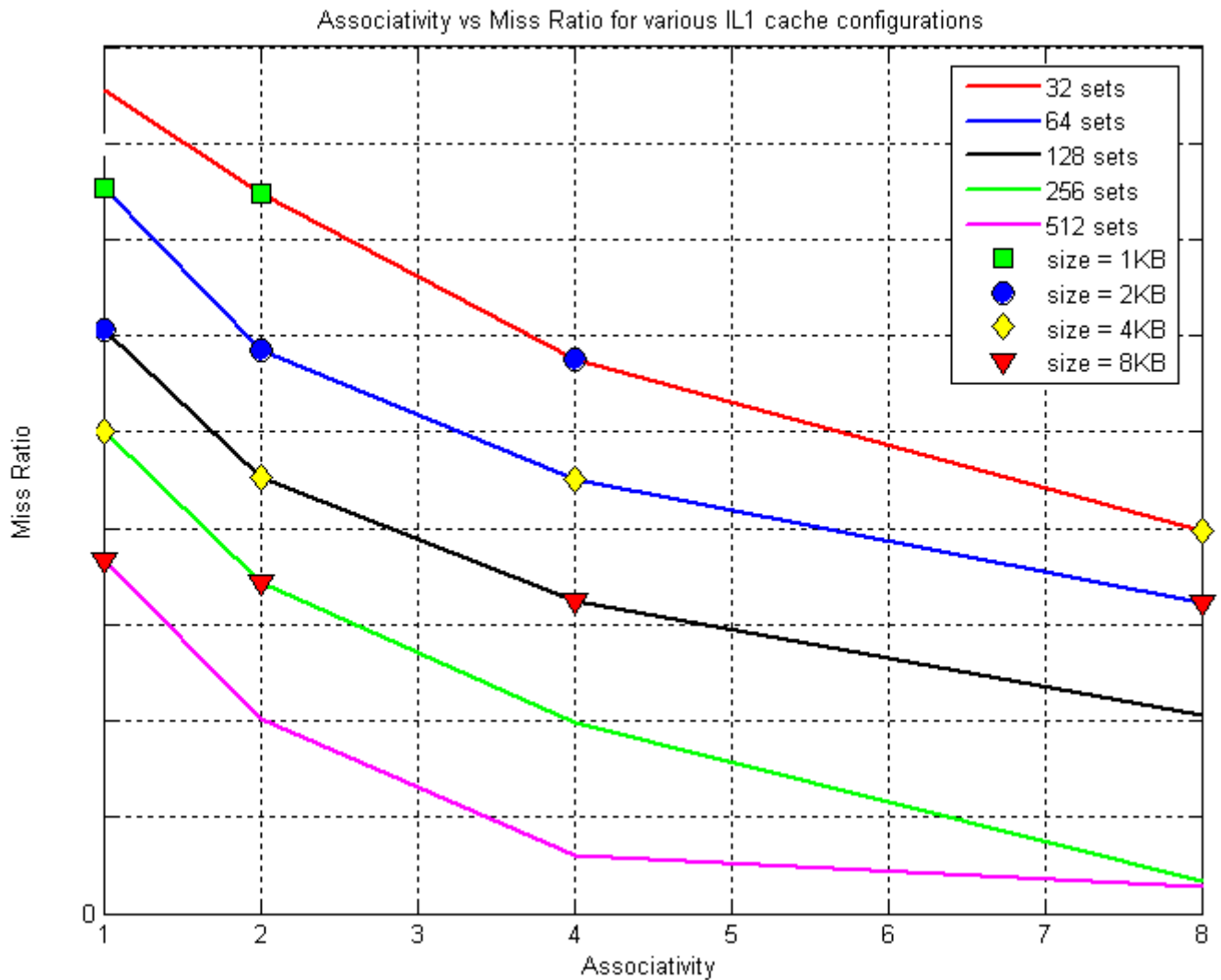
Now answer the following questions based on the above results.

Q 1) For a given number of sets, what effect does increasing associativity have on the miss ratio?

Q 2) For a given associativity, what is the effect of increasing the number of sets?

Q 3) For a given cache size, how does the miss ratio change when going from an associativity of one to two to four? Explain.

Q 4) If you were to design a Instruction cache, limited to a total cache size of 4 Kbytes, which cache organization would you choose, based solely on performance?

Q 5) If you were to design a data cache, limited to a total cache size of 4 Kbytes, which cache organization would you choose, based solely on performance?

Bonus Part

Repeat part 1) for only Instruction cache except that change the replacement scheme from LRU to Random. Plot the results as shown in the above figure. You don't need to answer the questions in part 1).