

Project 2 - Part 1

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1. Introduction

Cache organization and associativity.

2. Implementation

Prepare

Environment

- Docker image krmlr/debian-ssh on Debian 10 (host).
- File `~/simplsim-3v0e.tgz` is downloaded from <http://www.simplscalar.com/>.
- File `~/lab_cache_1a.cfg` is downloaded from http://www.ecs.umass.edu/ece/koren/architecture/Simplscalar/lab1_cache_1a.cfg.
- File `~/lab_cache_2a.cfg` is downloaded from http://www.ecs.umass.edu/ece/koren/architecture/Simplscalar/lab1_cache_2a.cfg

Script

```
# install
apt-get install tar build-essential

# unzip
tar zxvf simplsim-3v0e.tgz

# move
mv lab_cache_1a.cfg simplsim-3.0/
mv lab_cache_2a.cfg simplsim-3.0/
```

Compile

```
cd ~/simplesim-3.0
make clean
make config-pisa
make
make sim-tests
cd ~
```

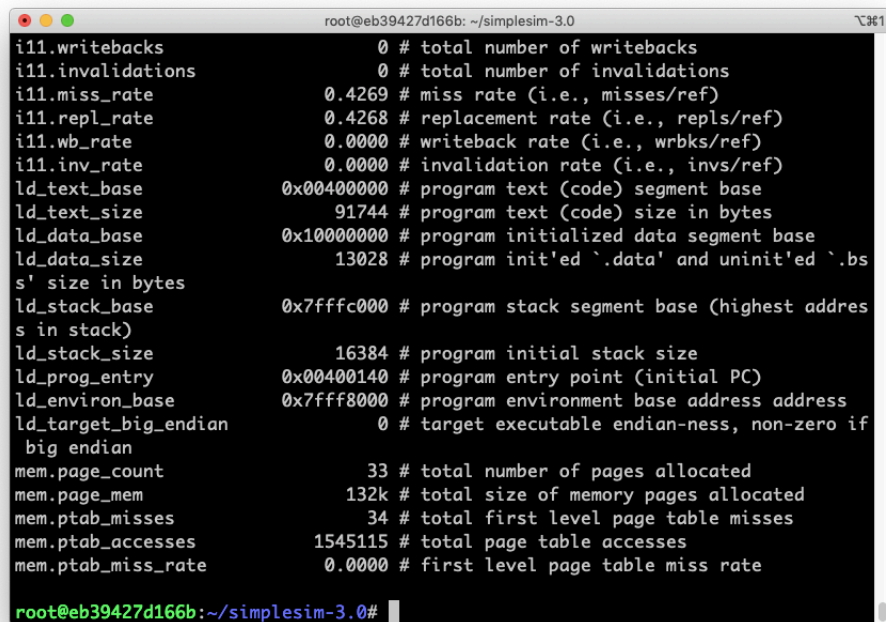
Run

```
cd ./simplesim-3.0/

# change file `lab1_cache_1a.cfg` and run several time
./sim-cache -config lab1_cache_1a.cfg tests-pisa/bin.little/test-math

# change file `lab1_cache_2a.cfg` and run several time
./sim-cache -config lab1_cache_2a.cfg tests-pisa/bin.little/test-math
```

3. Result

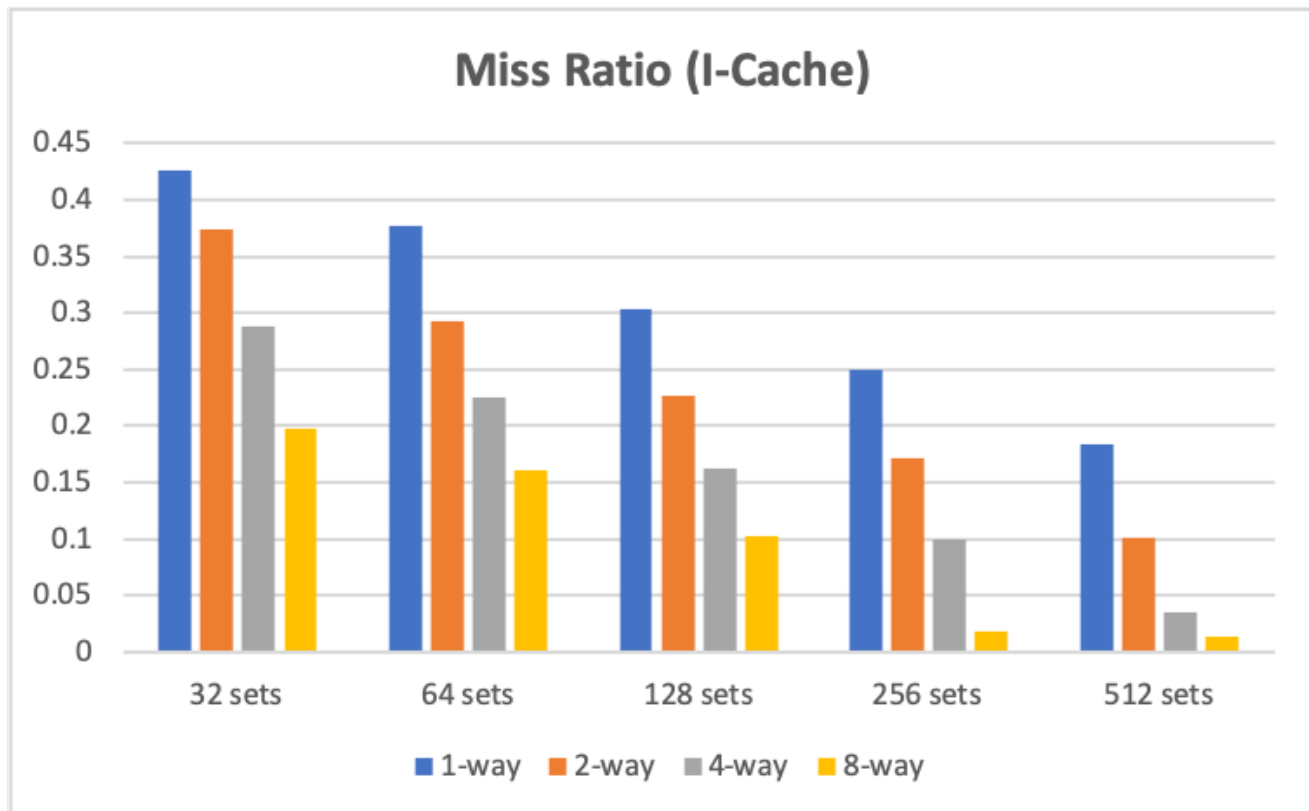


```
root@eb39427d166b: ~/simplesim-3.0
i11.writebacks          0 # total number of writebacks
i11.invalidations        0 # total number of invalidations
i11.miss_rate            0.4269 # miss rate (i.e., misses/ref)
i11.repl_rate            0.4268 # replacement rate (i.e., repls/ref)
i11.wb_rate              0.0000 # writeback rate (i.e., wrbks/ref)
i11.inv_rate             0.0000 # invalidation rate (i.e., invs/ref)
ld_text_base            0x00400000 # program text (code) segment base
ld_text_size            91744 # program text (code) size in bytes
ld_data_base            0x10000000 # program initialized data segment base
ld_data_size            13028 # program init'ed `.data' and uninit'ed `.bs
s' size in bytes
ld_stack_base           0x7fffc000 # program stack segment base (highest address
s in stack)
ld_stack_size           16384 # program initial stack size
ld_prog_entry           0x00400140 # program entry point (initial PC)
ld_environ_base         0x7fff8000 # program environment base address address
ld_target_big_endian    0 # target executable endianness, non-zero if
big endian
mem.page_count           33 # total number of pages allocated
mem.page_mem            132k # total size of memory pages allocated
mem.ptab_misses         34 # total first level page table misses
mem.ptab_accesses       1545115 # total page table accesses
mem.ptab_miss_rate      0.0000 # first level page table miss rate

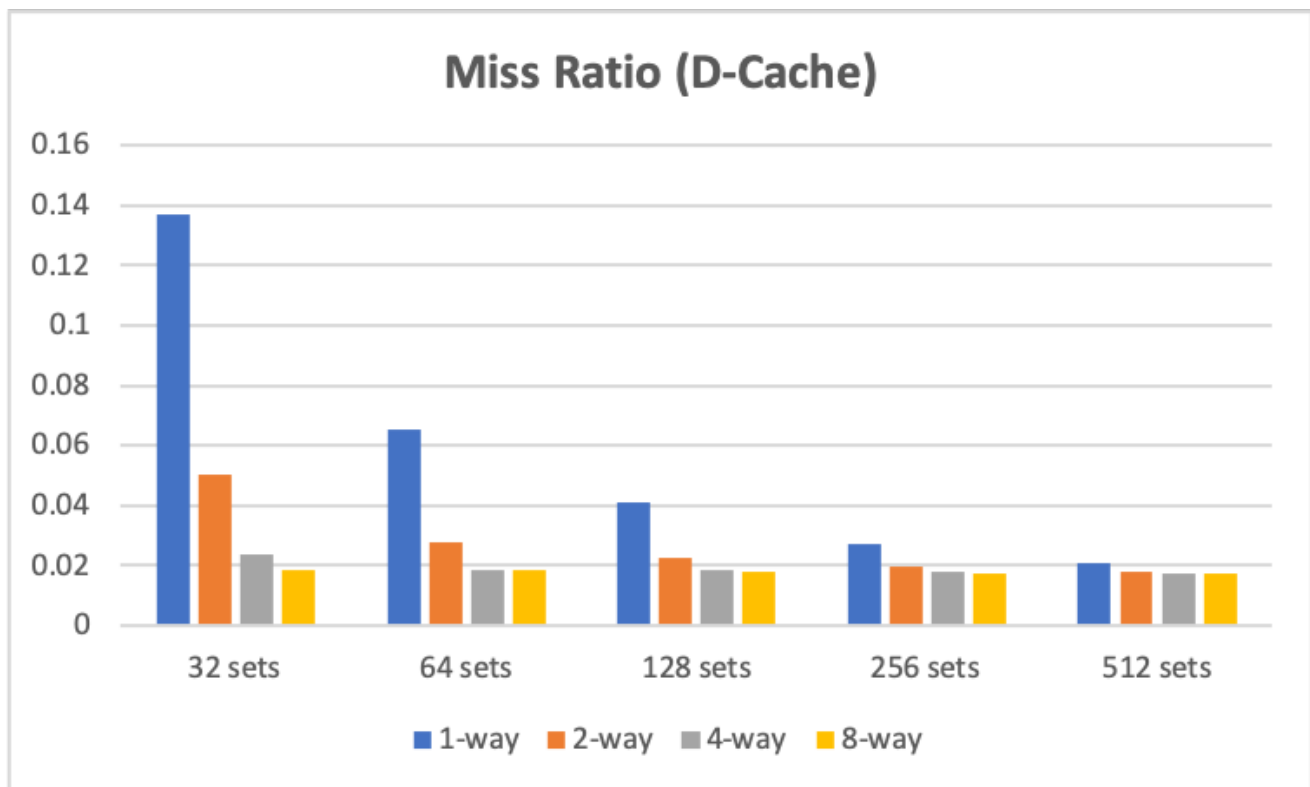
root@eb39427d166b:~/simplesim-3.0#
```

4. Conclusion

| Miss Ratio (I-Cache) | 1-way | 2-way | 4-way | 8-way |
|----------------------|--------|--------|--------|--------|
| 32 sets | 0.4269 | 0.3735 | 0.2880 | 0.1983 |
| 64 sets | 0.3765 | 0.2921 | 0.2256 | 0.1614 |
| 128 sets | 0.3031 | 0.2268 | 0.1619 | 0.1028 |
| 256 sets | 0.2504 | 0.1720 | 0.0994 | 0.0176 |
| 512 sets | 0.1834 | 0.1010 | 0.0348 | 0.0142 |



| Miss Ratio (D-Cache) | 1-way | 2-way | 4-way | 8-way |
|----------------------|--------|--------|--------|--------|
| 32 sets | 0.1372 | 0.0503 | 0.0236 | 0.0185 |
| 64 sets | 0.0654 | 0.0280 | 0.0187 | 0.0184 |
| 128 sets | 0.0408 | 0.0223 | 0.0184 | 0.0177 |
| 256 sets | 0.0273 | 0.0195 | 0.0177 | 0.0176 |
| 512 sets | 0.0209 | 0.0179 | 0.0176 | 0.0176 |



5. Discussion

1. For a given number of sets, what effect does increasing associativity have on the miss ratio?

The miss ratio will decrease during increasing associativity for fixed number of sets.

2. For a given associativity, what is the effect of increasing the number of sets?

The miss ratio will decrease during increasing the number of sets for fixed associativity.

3. For a given cache size, how does the miss ratio change when going from an associativity of one to two to four? Explain.

The miss ratio will decrease during increasing associativity for fixed cache size.

4. If you were to design a Instruction cache, limited to a total cache size of 4 Kbytes, which cache organization would you choose, based solely on performance?

I would like to choose the organization of "16 bytes - 32 sets - 8 ways".

5. If you were to design a data cache, limited to a total cache size of 4 Kbytes, which cache organization would you choose, based solely on performance?

I would like to choose the organization of "16 bytes - 32 sets - 8 ways".