# **Project 3**

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## 1. Introduction

Pipelining and Superscalar.

## 2. Implementation

## **Prepare**

#### **Environment**

- Docker image <u>krlmlr/debian-ssh</u> on Debian 10 (host).
- File ~/simplesim-3v0e.tgz is downloaded from <a href="http://www.simplescalar.com/">http://www.simplescalar.com/</a>.

#### **Script**

```
# install
apt-get install tar build-essential

# unzip
tar zxvf simplesim-3v0e.tgz
```

## Compile

```
cd ~/simplesim-3.0
make clean
make config-pisa
make
make sim-tests
cd ~
```

## **Config**

#### Script

```
mkdir labs
cp ~/simplesim-3.0/config/default.cfg ~/labs/config_a.cfg
cp ~/simplesim-3.0/tests-pisa/bin.little/test-math ~/labs/
cd labs/
vim config_a.cfg
vim config_b.cfg
vim config_c.cfg
vim config_c.cfg
vim config_d.cfg
vim config_e.cfg
vim config_e.cfg
vim config_e.cfg
vim config_g.cfg
alias soo='~/simplesim-3.0/sim-outorder'
alias pv='~/simplesim-3.0/pipeview.pl'
cd ~
```

#### File

```
# config_a

-decode:width 4
-fetch:ifqsize 4
-lsq:size 8
-ruu:size 8
-issue:width 1
-res:memport 1
-issue:inorder true
-res:ialu 1
-res:imult 1
-res:fpalu 1
-res:fpmult 1
```

```
# config_b

-decode:width 4
-fetch:ifqsize 4
-lsq:size 8
-ruu:size 8
-issue:width 1
-res:memport 1
-issue:inorder false
-res:ialu 1
-res:fpalu 1
-res:fpmult 1
```

```
# config_c

-decode:width 4
-fetch:ifqsize 4
-lsq:size 8
-ruu:size 8
-issue:width 1
-res:memport 1
-issue:inorder true
-res:ialu 4
-res:imult 4
-res:fpalu 4
-res:fpmult 4
```

```
# config_d

-decode:width 4
-fetch:ifqsize 4
-lsq:size 8
-ruu:size 8
-issue:width 1
-res:memport 1
-issue:inorder false
-res:ialu 4
-res:imult 4
-res:fpalu 4
-res:fpmult 4
```

```
# config_e

-decode:width 4
-fetch:ifqsize 4
-lsq:size 8
-ruu:size 8
-issue:width 4
-res:memport 4
-issue:inorder false
-res:ialu 1
-res:imult 1
-res:fpalu 1
-res:fpmult 1
```

```
# config_f

-decode:width 4
-fetch:ifqsize 4
-lsq:size 8
-ruu:size 8
-issue:width 4
-res:memport 4
-issue:inorder false
-res:ialu 4
-res:imult 4
-res:fpalu 4
-res:fpmult 4
```

```
# config_g

-decode:width 4
-fetch:ifqsize 4
-lsq:size 8
-ruu:size 16
-issue:width 4
-res:memport 4
-issue:inorder false
-res:ialu 4
-res:imult 4
-res:fpalu 4
-res:fpmult 4
```

#### Run

```
cd ~/labs
soo -config config_a.cfg -ptrace config_a.trc 0:1024 -redir:sim sim_config_a.out
./test-math
soo -config config_b.cfg -ptrace config_b.trc 0:1024 -redir:sim sim_config_b.out
./test-math
soo -config config_c.cfg -ptrace config_c.trc 0:1024 -redir:sim sim_config_c.out
./test-math
soo -config config_d.cfg -ptrace config_d.trc 0:1024 -redir:sim sim_config_d.out
./test-math
soo -config config_e.cfg -ptrace config_e.trc 0:1024 -redir:sim sim_config_e.out
./test-math
soo -config config_f.cfg -ptrace config_f.trc 0:1024 -redir:sim sim_config_f.out
./test-math
soo -config config_f.cfg -ptrace config_f.trc 0:1024 -redir:sim sim_config_f.out
./test-math
```

## 3. Result

```
root@eb39427d166b: ~/labs
                                                                                    ₹#1
root@eb39427d166b:~/labs# soo -config config_a.cfg -ptrace config_a.trc 0:1024
redir:sim sim_configa.out ./test-math
pow(12.0, 2.0) == 144.000000
pow(10.0, 3.0) == 1000.000000
pow(10.0, -3.0) == 0.001000
str: 123.456
x: 123.000000
str: 123.456
x: 123.456000
str: 123.456
x: 123.456000
123.456 123.456000 123 1000
sinh(2.0) = 3.62686
sinh(3.0) = 10.01787
h=3.60555
atan2(3,2) = 0.98279
pow(3.60555, 4.0) = 169
169 / \exp(0.98279 * 5) = 1.24102
3.93117 + 5*log(3.60555) = 10.34355
cos(10.34355) = -0.6068, sin(10.34355) = -0.79486
      0.5x
x0.5
    0.5x
-1e-17 != -1e-17 Worked!
root@eb39427d166b:~/labs#
```

## 4. Conclusion

This part seems too long to read.

If you would like to skip it, just go to **the last-3rd page** to see the part of "5. Discussion".

#### config\_a

```
sim: ** simulation statistics **
                           213598 # total number of instructions committed
sim_num_insn
                            56890 # total number of loads and stores committed
sim num refs
                             34096 # total number of loads committed
sim num loads
                 22794.0000 # total number of stores committed
sim num stores
                             38571 # total number of branches committed
sim num branches
                                 1 # total simulation time in seconds
sim elapsed time
sim inst rate
                     213598.0000 # simulation speed (in insts/sec)
sim total insn
                           219022 # total number of instructions executed
sim total refs
                            58314 # total number of loads and stores executed
sim total loads
                             35232 # total number of loads executed
                       23082.0000 # total number of stores executed
sim total stores
                             39719 # total number of branches executed
sim total branches
                            368591 # total simulation time in cycles
sim cycle
sim IPC
                            0.5795 # instructions per cycle
                            1.7256 # cycles per instruction
sim CPI
                            0.5942 # total instructions (mis-spec + committed)
sim_exec_BW
per cycle
                           5.5378 # instruction per branch
sim IPB
                           1009897 # cumulative IFQ occupancy
IFQ count
                            224756 # cumulative IFQ full count
IFQ fcount
                            2.7399 # avg IFQ occupancy (insn's)
ifq occupancy
                            0.5942 # avg IFQ dispatch rate (insn/cycle)
ifq rate
                            4.6109 # avg IFQ occupant latency (cycle's)
ifq_latency
ifq_full
                            0.6098 # fraction of time (cycle's) IFQ was full
RUU count
                            916280 # cumulative RUU occupancy
RUU fcount
                              1436 # cumulative RUU full count
                            2.4859 # avg RUU occupancy (insn's)
ruu_occupancy
                            0.5942 # avg RUU dispatch rate (insn/cycle)
ruu rate
                            4.1835 # avg RUU occupant latency (cycle's)
ruu latency
                            0.0039 # fraction of time (cycle's) RUU was full
ruu full
                            246205 # cumulative LSQ occupancy
LSQ_count
LSQ fcount
                                 0 # cumulative LSQ full count
1sq occupancy
                            0.6680 # avg LSQ occupancy (insn's)
                            0.5942 # avg LSQ dispatch rate (insn/cycle)
lsq_rate
lsq latency
                            1.1241 # avg LSQ occupant latency (cycle's)
lsq full
                            0.0000 # fraction of time (cycle's) LSQ was full
```

```
sim_slip
                           1423560 # total number of slip cycles
avg sim slip
                            6.6647 # the average slip between issue and
retirement
bpred_bimod.lookups
                            41442 # total number of bpred lookups
bpred bimod.updates
                            38571 # total number of updates
bpred bimod.addr hits
                           34621 # total number of address-predicted hits
bpred bimod.dir hits
                            35114 # total number of direction-predicted hits
(includes addr-hits)
bpred_bimod.misses
                             3457 # total number of misses
                     3520 # total number of address-predicted hits for
bpred bimod.jr hits
JR's
                     3542 # total number of JR's seen
bpred_bimod.jr_seen
                                      28 # total number of address-predicted
bpred bimod.jr non ras hits.PP
hits for non-RAS JR's
bpred_bimod.jr_non_ras_seen.PP
                                       41 # total number of non-RAS JR's seen
bpred_bimod.bpred_addr_rate 0.8976 # branch address-prediction rate (i.e.,
addr-hits/updates)
bpred bimod.bpred dir rate 0.9104 # branch direction-prediction rate (i.e.,
all-hits/updates)
bpred bimod.bpred jr rate 0.9938 # JR address-prediction rate (i.e., JR addr-
hits/JRs seen)
bpred bimod.bpred jr non ras rate.PP 0.6829 # non-RAS JR addr-pred rate (ie,
non-RAS JR hits/JRs seen)
bpred bimod.retstack pushes 3662 # total number of address pushed onto
ret-addr stack
bpred_bimod.retstack_pops 4352 # total number of address popped off of
ret-addr stack
                             3501 # total number of RAS predictions used
bpred bimod.used ras.PP
                               3492 # total number of RAS hits
bpred_bimod.ras_hits.PP
bpred_bimod.ras_rate.PP 0.9974 # RAS prediction rate (i.e., RAS hits/used RAS)
                            243652 # total number of accesses
ill.accesses
                            227647 # total number of hits
ill.hits
                             16005 # total number of misses
ill.misses
ill.replacements
                            15494 # total number of replacements
                                 0 # total number of writebacks
ill.writebacks
                                 0 # total number of invalidations
ill.invalidations
ill.miss rate
                           0.0657 # miss rate (i.e., misses/ref)
                           0.0636 # replacement rate (i.e., repls/ref)
il1.repl_rate
il1.wb rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
ill.inv rate
                          0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses
                            56890 # total number of accesses
                             56342 # total number of hits
dl1.hits
dl1.misses
                              548 # total number of misses
                               64 # total number of replacements
dl1.replacements
dl1.writebacks
                               59 # total number of writebacks
dll.invalidations
                                 0 # total number of invalidations
```

```
dl1.miss rate
                            0.0096 # miss rate (i.e., misses/ref)
dl1.repl rate
                            0.0011 # replacement rate (i.e., repls/ref)
                            0.0010 # writeback rate (i.e., wrbks/ref)
dl1.wb rate
dl1.inv_rate
                           0.0000 # invalidation rate (i.e., invs/ref)
ul2.accesses
                            16612 # total number of accesses
                            15392 # total number of hits
ul2.hits
ul2.misses
                             1220 # total number of misses
                                 0 # total number of replacements
ul2.replacements
ul2.writebacks
                                 0 # total number of writebacks
                                 0 # total number of invalidations
ul2.invalidations
                            0.0734 # miss rate (i.e., misses/ref)
ul2.miss rate
ul2.repl_rate
                            0.0000 # replacement rate (i.e., repls/ref)
                           0.0000 # writeback rate (i.e., wrbks/ref)
ul2.wb rate
                            0.0000 # invalidation rate (i.e., invs/ref)
ul2.inv rate
                           243652 # total number of accesses
itlb.accesses
itlb.hits
                            243629 # total number of hits
itlb.misses
                                23 # total number of misses
                                 0 # total number of replacements
itlb.replacements
                                 0 # total number of writebacks
itlb.writebacks
itlb.invalidations
                                 0 # total number of invalidations
                           0.0001 # miss rate (i.e., misses/ref)
itlb.miss rate
itlb.repl rate
                           0.0000 # replacement rate (i.e., repls/ref)
                           0.0000 # writeback rate (i.e., wrbks/ref)
itlb.wb rate
itlb.inv rate
                           0.0000 # invalidation rate (i.e., invs/ref)
dtlb.accesses
                            56890 # total number of accesses
dtlb.hits
                             56880 # total number of hits
                                10 # total number of misses
dtlb.misses
                                 0 # total number of replacements
dtlb.replacements
                                 0 # total number of writebacks
dtlb.writebacks
dtlb.invalidations
                                 0 # total number of invalidations
dtlb.miss rate
                           0.0002 # miss rate (i.e., misses/ref)
dtlb.repl rate
                           0.0000 # replacement rate (i.e., repls/ref)
dtlb.wb rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
dtlb.inv rate
                            0.0000 # invalidation rate (i.e., invs/ref)
sim invalid addrs
                                 0 # total non-speculative bogus addresses seen
(debug var)
                       0x00400000 # program text (code) segment base
ld text base
ld_text_size
                             91744 # program text (code) size in bytes
ld data base
                       0x10000000 # program initialized data segment base
ld data size
                             13028 # program init'ed `.data' and uninit'ed
`.bss' size in bytes
ld_stack_base
                   0x7fffc000 # program stack segment base (highest address
in stack)
                             16384 # program initial stack size
ld stack size
ld_prog_entry
                       0x00400140 # program entry point (initial PC)
ld_environ_base
                        0x7fff8000 # program environment base address address
```

```
ld_target_big_endian 0 # target executable endian-ness, non-zero if big endian

mem.page_count 33 # total number of pages allocated

mem.page_mem 132k # total size of memory pages allocated

mem.ptab_misses 37 # total first level page table misses

mem.ptab_accesses 1964554 # total page table accesses

mem.ptab_miss_rate 0.0000 # first level page table miss rate
```

#### config\_b

```
sim: ** simulation statistics **
sim num insn
                            213598 # total number of instructions committed
                             56890 # total number of loads and stores committed
sim_num_refs
                             34096 # total number of loads committed
sim num loads
                 22794.0000 # total number of stores committed
sim num stores
sim num branches
                             38571 # total number of branches committed
                                 1 # total simulation time in seconds
sim elapsed time
                     213598.0000 # simulation speed (in insts/sec)
sim inst rate
sim total insn
                            227937 # total number of instructions executed
                             60728 # total number of loads and stores executed
sim total refs
                             36672 # total number of loads executed
sim total loads
                   24056.0000 # total number of stores executed
sim total stores
sim total branches
                             41589 # total number of branches executed
                            350523 # total simulation time in cycles
sim cycle
                            0.6094 # instructions per cycle
sim IPC
                            1.6410 # cycles per instruction
sim CPI
                            0.6503 # total instructions (mis-spec + committed)
sim exec BW
per cycle
sim IPB
                            5.5378 # instruction per branch
                            893582 # cumulative IFQ occupancy
IFQ count
                            209899 # cumulative IFQ full count
IFQ fcount
ifq_occupancy
                            2.5493 # avg IFQ occupancy (insn's)
ifq rate
                            0.6503 # avg IFQ dispatch rate (insn/cycle)
ifq latency
                            3.9203 # avg IFQ occupant latency (cycle's)
ifq full
                            0.5988 # fraction of time (cycle's) IFQ was full
RUU count
                           2070304 # cumulative RUU occupancy
RUU fcount
                            216064 # cumulative RUU full count
                            5.9063 # avg RUU occupancy (insn's)
ruu occupancy
                            0.6503 # avg RUU dispatch rate (insn/cycle)
ruu rate
ruu_latency
                            9.0828 # avg RUU occupant latency (cycle's)
                            0.6164 # fraction of time (cycle's) RUU was full
ruu full
LSQ count
                            567451 # cumulative LSQ occupancy
LSQ fcount
                             1706 # cumulative LSO full count
                           1.6189 # avg LSQ occupancy (insn's)
1sq occupancy
lsq rate
                            0.6503 # avg LSQ dispatch rate (insn/cycle)
```

```
lsq_latency
                            2.4895 # avg LSQ occupant latency (cycle's)
lsq full
                            0.0049 # fraction of time (cycle's) LSQ was full
                           2847369 # total number of slip cycles
sim slip
avg_sim_slip
                           13.3305 # the average slip between issue and
retirement
                           43806 # total number of bpred lookups
bpred bimod.lookups
bpred bimod.updates
                            38571 # total number of updates
bpred_bimod.addr_hits
                            34411 # total number of address-predicted hits
bpred_bimod.dir_hits
                            35114 # total number of direction-predicted hits
(includes addr-hits)
                            3457 # total number of misses
bpred bimod.misses
bpred_bimod.jr_hits 3311 # total number of address-predicted hits for
JR's
                             3542 # total number of JR's seen
bpred bimod.jr seen
bpred bimod.jr non ras hits.PP
                                        28 # total number of address-predicted
hits for non-RAS JR's
bpred bimod.jr non ras seen.PP
                                       41 # total number of non-RAS JR's seen
bpred bimod.bpred addr rate 0.8921 # branch address-prediction rate (i.e.,
addr-hits/updates)
bpred bimod.bpred dir rate 0.9104 # branch direction-prediction rate (i.e.,
all-hits/updates)
bpred bimod.bpred jr rate 0.9348 # JR address-prediction rate (i.e., JR addr-
hits/JRs seen)
bpred bimod.bpred jr non ras rate.PP 0.6829 # non-RAS JR addr-pred rate (ie,
non-RAS JR hits/JRs seen)
bpred_bimod.retstack_pushes 3905 # total number of address pushed onto
ret-addr stack
bpred bimod.retstack pops 4511 # total number of address popped off of
ret-addr stack
bpred bimod.used ras.PP
                              3501 # total number of RAS predictions used
bpred bimod.ras hits.PP
                               3283 # total number of RAS hits
bpred bimod.ras rate.PP 0.9377 # RAS prediction rate (i.e., RAS hits/used RAS)
                            253460 # total number of accesses
ill.accesses
ill.hits
                            237329 # total number of hits
                             16131 # total number of misses
ill.misses
                            15620 # total number of replacements
ill.replacements
                                 0 # total number of writebacks
ill.writebacks
ill.invalidations
                                 0 # total number of invalidations
ill.miss rate
                           0.0636 # miss rate (i.e., misses/ref)
ill.repl rate
                            0.0616 # replacement rate (i.e., repls/ref)
il1.wb rate
                            0.0000 # writeback rate (i.e., wrbks/ref)
ill.inv_rate
                           0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses
                            56907 # total number of accesses
dl1.hits
                             56357 # total number of hits
dl1.misses
                               550 # total number of misses
dl1.replacements
                                65 # total number of replacements
```

```
dl1.writebacks
                                60 # total number of writebacks
                                 0 # total number of invalidations
dll.invalidations
                            0.0097 # miss rate (i.e., misses/ref)
dl1.miss rate
dl1.repl_rate
                           0.0011 # replacement rate (i.e., repls/ref)
dl1.wb rate
                           0.0011 # writeback rate (i.e., wrbks/ref)
                          0.0000 # invalidation rate (i.e., invs/ref)
dl1.inv rate
ul2.accesses
                            16741 # total number of accesses
ul2.hits
                            15521 # total number of hits
ul2.misses
                             1220 # total number of misses
                                 0 # total number of replacements
ul2.replacements
                                 0 # total number of writebacks
ul2.writebacks
                                 0 # total number of invalidations
ul2.invalidations
ul2.miss rate
                           0.0729 # miss rate (i.e., misses/ref)
                           0.0000 # replacement rate (i.e., repls/ref)
ul2.repl rate
ul2.wb rate
                          0.0000 # writeback rate (i.e., wrbks/ref)
                           0.0000 # invalidation rate (i.e., invs/ref)
ul2.inv_rate
itlb.accesses
                           253460 # total number of accesses
                           253437 # total number of hits
itlb.hits
                                23 # total number of misses
itlb.misses
                                0 # total number of replacements
itlb.replacements
                                 0 # total number of writebacks
itlb.writebacks
itlb.invalidations
                                 0 # total number of invalidations
itlb.miss rate
                          0.0001 # miss rate (i.e., misses/ref)
itlb.repl rate
                           0.0000 # replacement rate (i.e., repls/ref)
itlb.wb rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
itlb.inv rate
                          0.0000 # invalidation rate (i.e., invs/ref)
                            56907 # total number of accesses
dtlb.accesses
                            56897 # total number of hits
dtlb.hits
                               10 # total number of misses
dtlb.misses
dtlb.replacements
                                 0 # total number of replacements
                                 0 # total number of writebacks
dtlb.writebacks
dtlb.invalidations
                                 0 # total number of invalidations
dtlb.miss rate
                           0.0002 # miss rate (i.e., misses/ref)
dtlb.repl rate
                           0.0000 # replacement rate (i.e., repls/ref)
                            0.0000 # writeback rate (i.e., wrbks/ref)
dtlb.wb rate
                           0.0000 # invalidation rate (i.e., invs/ref)
dtlb.inv rate
sim invalid addrs
                                 0 # total non-speculative bogus addresses seen
(debug var)
ld text base
                      0x00400000 # program text (code) segment base
ld text size
                             91744 # program text (code) size in bytes
ld data base
                      0x10000000 # program initialized data segment base
ld_data_size
                             13028 # program init'ed `.data' and uninit'ed
`.bss' size in bytes
ld stack base 0x7fffc000 # program stack segment base (highest address
in stack)
ld_stack_size
                             16384 # program initial stack size
```

```
ld_prog_entry
                        0x00400140 # program entry point (initial PC)
ld environ base
                        0x7fff8000 # program environment base address address
                                 0 # target executable endian-ness, non-zero if
ld target big endian
big endian
mem.page count
                                33 # total number of pages allocated
                              132k # total size of memory pages allocated
mem.page mem
                                37 # total first level page table misses
mem.ptab misses
                          2006598 # total page table accesses
mem.ptab_accesses
mem.ptab_miss_rate
                           0.0000 # first level page table miss rate
```

#### config c

```
sim: ** simulation statistics **
                            213598 # total number of instructions committed
sim num insn
                              56890 # total number of loads and stores committed
sim num refs
sim num loads
                              34096 # total number of loads committed
sim num stores
                       22794.0000 # total number of stores committed
sim num branches
                              38571 # total number of branches committed
sim elapsed time
                                  1 # total simulation time in seconds
                    213598.0000 # simulation speed (in insts/sec)
sim inst rate
                             219022 # total number of instructions executed
sim total insn
                              58314 # total number of loads and stores executed
sim total refs
                              35232 # total number of loads executed
sim total loads
                        23082.0000 # total number of stores executed
sim total stores
                              39719 # total number of branches executed
sim_total_branches
sim cycle
                             368591 # total simulation time in cycles
                             0.5795 # instructions per cycle
sim IPC
                            1.7256 # cycles per instruction
sim CPI
                            0.5942 # total instructions (mis-spec + committed)
sim exec BW
per cycle
                            5.5378 # instruction per branch
sim IPB
                            1009897 # cumulative IFQ occupancy
IFQ_count
IFQ fcount
                             224756 # cumulative IFQ full count
ifq occupancy
                            2.7399 # avg IFQ occupancy (insn's)
ifq rate
                            0.5942 # avg IFQ dispatch rate (insn/cycle)
ifq_latency
                            4.6109 # avg IFQ occupant latency (cycle's)
ifq full
                            0.6098 # fraction of time (cycle's) IFQ was full
                            916280 # cumulative RUU occupancy
RUU count
                               1436 # cumulative RUU full count
RUU fcount
                             2.4859 # avg RUU occupancy (insn's)
ruu_occupancy
                             0.5942 # avg RUU dispatch rate (insn/cycle)
ruu rate
                             4.1835 # avg RUU occupant latency (cycle's)
ruu latency
                            0.0039 # fraction of time (cycle's) RUU was full
ruu_full
LSQ count
                             246205 # cumulative LSQ occupancy
LSQ fcount
                                  0 # cumulative LSQ full count
```

```
1sq occupancy
                            0.6680 # avg LSQ occupancy (insn's)
1sq rate
                            0.5942 # avg LSQ dispatch rate (insn/cycle)
                           1.1241 # avg LSQ occupant latency (cycle's)
1sq latency
lsq_full
                          0.0000 # fraction of time (cycle's) LSQ was full
sim_slip
                         1423560 # total number of slip cycles
                          6.6647 # the average slip between issue and
avg sim slip
retirement
                          41442 # total number of bpred lookups
bpred_bimod.lookups
bpred_bimod.updates
                            38571 # total number of updates
bpred bimod.addr hits
                           34621 # total number of address-predicted hits
                            35114 # total number of direction-predicted hits
bpred bimod.dir hits
(includes addr-hits)
                            3457 # total number of misses
bpred bimod.misses
bpred_bimod.jr_hits 3520 # total number of address-predicted hits for
JR's
                       3542 # total number of JR's seen
bpred_bimod.jr_seen
bpred bimod.jr non ras hits.PP
                                     28 # total number of address-predicted
hits for non-RAS JR's
bpred_bimod.jr_non_ras_seen.PP
                                       41 # total number of non-RAS JR's seen
bpred bimod.bpred addr rate 0.8976 # branch address-prediction rate (i.e.,
addr-hits/updates)
bpred bimod.bpred dir rate 0.9104 # branch direction-prediction rate (i.e.,
all-hits/updates)
bpred bimod.bpred jr rate 0.9938 # JR address-prediction rate (i.e., JR addr-
hits/JRs seen)
bpred_bimod.bpred_jr_non_ras_rate.PP      0.6829 # non-RAS JR addr-pred rate (ie,
non-RAS JR hits/JRs seen)
bpred bimod.retstack pushes 3662 # total number of address pushed onto
ret-addr stack
bpred_bimod.retstack_pops 4352 # total number of address popped off of
ret-addr stack
bpred bimod.used ras.PP
                             3501 # total number of RAS predictions used
                               3492 # total number of RAS hits
bpred bimod.ras hits.PP
bpred_bimod.ras_rate.PP 0.9974 # RAS prediction rate (i.e., RAS hits/used RAS)
                            243652 # total number of accesses
ill.accesses
                            227647 # total number of hits
ill.hits
                            16005 # total number of misses
ill.misses
ill.replacements
                            15494 # total number of replacements
ill.writebacks
                                 0 # total number of writebacks
                                0 # total number of invalidations
ill.invalidations
ill.miss rate
                           0.0657 # miss rate (i.e., misses/ref)
il1.repl_rate
                           0.0636 # replacement rate (i.e., repls/ref)
ill.wb rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
                           0.0000 # invalidation rate (i.e., invs/ref)
ill.inv rate
dl1.accesses
                            56890 # total number of accesses
dl1.hits
                             56342 # total number of hits
```

```
dl1.misses
                               548 # total number of misses
dl1.replacements
                                64 # total number of replacements
                                59 # total number of writebacks
dl1.writebacks
                                 0 # total number of invalidations
dll.invalidations
dl1.miss_rate
                           0.0096 # miss rate (i.e., misses/ref)
                           0.0011 # replacement rate (i.e., repls/ref)
dl1.repl rate
                           0.0010 # writeback rate (i.e., wrbks/ref)
dl1.wb rate
                           0.0000 # invalidation rate (i.e., invs/ref)
dl1.inv rate
ul2.accesses
                             16612 # total number of accesses
                             15392 # total number of hits
ul2.hits
                             1220 # total number of misses
ul2.misses
ul2.replacements
                                 0 # total number of replacements
ul2.writebacks
                                 0 # total number of writebacks
ul2.invalidations
                                 0 # total number of invalidations
ul2.miss rate
                           0.0734 # miss rate (i.e., misses/ref)
                           0.0000 # replacement rate (i.e., repls/ref)
ul2.repl_rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
ul2.wb rate
                            0.0000 # invalidation rate (i.e., invs/ref)
ul2.inv rate
                            243652 # total number of accesses
itlb.accesses
itlb.hits
                            243629 # total number of hits
itlb.misses
                                23 # total number of misses
itlb.replacements
                                 0 # total number of replacements
itlb.writebacks
                                 0 # total number of writebacks
itlb.invalidations
                                 0 # total number of invalidations
itlb.miss rate
                           0.0001 # miss rate (i.e., misses/ref)
itlb.repl rate
                            0.0000 # replacement rate (i.e., repls/ref)
                            0.0000 # writeback rate (i.e., wrbks/ref)
itlb.wb rate
itlb.inv rate
                           0.0000 # invalidation rate (i.e., invs/ref)
                            56890 # total number of accesses
dtlb.accesses
dtlb.hits
                             56880 # total number of hits
dtlb.misses
                               10 # total number of misses
                                 0 # total number of replacements
dtlb.replacements
                                 0 # total number of writebacks
dtlb.writebacks
dtlb.invalidations
                                 0 # total number of invalidations
dtlb.miss rate
                            0.0002 # miss rate (i.e., misses/ref)
                            0.0000 # replacement rate (i.e., repls/ref)
dtlb.repl rate
dtlb.wb rate
                            0.0000 # writeback rate (i.e., wrbks/ref)
dtlb.inv_rate
                           0.0000 # invalidation rate (i.e., invs/ref)
sim invalid addrs
                                 0 # total non-speculative bogus addresses seen
(debug var)
ld text base
                       0x00400000 # program text (code) segment base
ld_text_size
                             91744 # program text (code) size in bytes
ld data base
                       0x10000000 # program initialized data segment base
                             13028 # program init'ed `.data' and uninit'ed
ld data size
`.bss' size in bytes
```

```
ld stack base
                        0x7fffc000 # program stack segment base (highest address
in stack)
ld stack size
                             16384 # program initial stack size
ld_prog_entry
                       0x00400140 # program entry point (initial PC)
ld_environ_base
                       0x7fff8000 # program environment base address address
                                 0 # target executable endian-ness, non-zero if
ld target big endian
big endian
                               33 # total number of pages allocated
mem.page_count
mem.page_mem
                             132k # total size of memory pages allocated
                                37 # total first level page table misses
mem.ptab misses
mem.ptab accesses
                         1964554 # total page table accesses
mem.ptab_miss_rate
                           0.0000 # first level page table miss rate
```

## config\_d

```
sim: ** simulation statistics **
sim_num_insn
                            213598 # total number of instructions committed
sim num refs
                            56890 # total number of loads and stores committed
sim num loads
                             34096 # total number of loads committed
                       22794.0000 # total number of stores committed
sim_num_stores
                             38571 # total number of branches committed
sim num branches
                                 1 # total simulation time in seconds
sim elapsed time
sim inst rate
                       213598.0000 # simulation speed (in insts/sec)
                            227937 # total number of instructions executed
sim total insn
                             60728 # total number of loads and stores executed
sim_total_refs
                             36672 # total number of loads executed
sim total loads
                       24056.0000 # total number of stores executed
sim total stores
                             41589 # total number of branches executed
sim total branches
sim cycle
                            350523 # total simulation time in cycles
sim IPC
                            0.6094 # instructions per cycle
                            1.6410 # cycles per instruction
sim CPI
sim_exec_BW
                            0.6503 # total instructions (mis-spec + committed)
per cycle
sim IPB
                            5.5378 # instruction per branch
                            893582 # cumulative IFQ occupancy
IFQ_count
IFQ_fcount
                           209899 # cumulative IFQ full count
                           2.5493 # avg IFQ occupancy (insn's)
ifq occupancy
                           0.6503 # avg IFQ dispatch rate (insn/cycle)
ifq rate
                            3.9203 # avg IFQ occupant latency (cycle's)
ifq_latency
ifq_full
                            0.5988 # fraction of time (cycle's) IFQ was full
                           2070287 # cumulative RUU occupancy
RUU count
                            216065 # cumulative RUU full count
RUU fcount
                            5.9063 # avg RUU occupancy (insn's)
ruu_occupancy
                            0.6503 # avg RUU dispatch rate (insn/cycle)
ruu rate
ruu latency
                            9.0827 # avg RUU occupant latency (cycle's)
```

```
ruu_full
                            0.6164 # fraction of time (cycle's) RUU was full
LSQ count
                            567447 # cumulative LSQ occupancy
LSQ fcount
                             1706 # cumulative LSQ full count
lsq_occupancy
                           1.6189 # avg LSQ occupancy (insn's)
lsq_rate
                           0.6503 # avg LSQ dispatch rate (insn/cycle)
                           2.4895 # avg LSQ occupant latency (cycle's)
lsq latency
lsq full
                           0.0049 # fraction of time (cycle's) LSQ was full
                           2847348 # total number of slip cycles
sim_slip
avg_sim_slip
                          13.3304 # the average slip between issue and
retirement
                            43806 # total number of bpred lookups
bpred bimod.lookups
bpred_bimod.updates
                            38571 # total number of updates
bpred bimod.addr hits
                            34411 # total number of address-predicted hits
bpred bimod.dir hits
                            35114 # total number of direction-predicted hits
(includes addr-hits)
bpred_bimod.misses
                             3457 # total number of misses
                     3311 # total number of address-predicted hits for
bpred bimod.jr hits
JR's
bpred bimod.jr seen
                     3542 # total number of JR's seen
                                      28 # total number of address-predicted
bpred bimod.jr non ras hits.PP
hits for non-RAS JR's
bpred_bimod.jr_non_ras_seen.PP
                                       41 # total number of non-RAS JR's seen
bpred bimod.bpred addr rate 0.8921 # branch address-prediction rate (i.e.,
addr-hits/updates)
bpred_bimod.bpred_dir_rate 0.9104 # branch direction-prediction rate (i.e.,
all-hits/updates)
bpred bimod.bpred jr rate 0.9348 # JR address-prediction rate (i.e., JR addr-
hits/JRs seen)
bpred_bimod.bpred_jr_non_ras_rate.PP      0.6829 # non-RAS JR addr-pred rate (ie,
non-RAS JR hits/JRs seen)
bpred bimod.retstack pushes 3905 # total number of address pushed onto
ret-addr stack
bpred bimod.retstack pops 4511 # total number of address popped off of
ret-addr stack
bpred bimod.used ras.PP
                              3501 # total number of RAS predictions used
                               3283 # total number of RAS hits
bpred bimod.ras hits.PP
bpred bimod.ras rate.PP 0.9377 # RAS prediction rate (i.e., RAS hits/used RAS)
ill.accesses
                            253460 # total number of accesses
                            237329 # total number of hits
ill.hits
                            16131 # total number of misses
ill.misses
ill.replacements
                            15620 # total number of replacements
ill.writebacks
                                 0 # total number of writebacks
il1.invalidations
                                 0 # total number of invalidations
                           0.0636 # miss rate (i.e., misses/ref)
ill.miss rate
                            0.0616 # replacement rate (i.e., repls/ref)
ill.repl rate
                            0.0000 # writeback rate (i.e., wrbks/ref)
il1.wb_rate
```

```
ill.inv_rate
                            0.0000 # invalidation rate (i.e., invs/ref)
dl1.accesses
                             56907 # total number of accesses
dl1.hits
                             56357 # total number of hits
dl1.misses
                              550 # total number of misses
dl1.replacements
                               65 # total number of replacements
dl1.writebacks
                                60 # total number of writebacks
dl1.invalidations
                                 0 # total number of invalidations
dl1.miss rate
                           0.0097 # miss rate (i.e., misses/ref)
dl1.repl rate
                           0.0011 # replacement rate (i.e., repls/ref)
dl1.wb rate
                            0.0011 # writeback rate (i.e., wrbks/ref)
                           0.0000 # invalidation rate (i.e., invs/ref)
dll.inv rate
ul2.accesses
                            16741 # total number of accesses
                            15521 # total number of hits
ul2.hits
                             1220 # total number of misses
ul2.misses
                                 0 # total number of replacements
ul2.replacements
ul2.writebacks
                                 0 # total number of writebacks
ul2.invalidations
                                 0 # total number of invalidations
ul2.miss rate
                           0.0729 # miss rate (i.e., misses/ref)
                           0.0000 # replacement rate (i.e., repls/ref)
ul2.repl rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
ul2.wb rate
                           0.0000 # invalidation rate (i.e., invs/ref)
ul2.inv rate
itlb.accesses
                           253460 # total number of accesses
itlb.hits
                            253437 # total number of hits
itlb.misses
                                23 # total number of misses
itlb.replacements
                                 0 # total number of replacements
itlb.writebacks
                                 0 # total number of writebacks
itlb.invalidations
                                 0 # total number of invalidations
                           0.0001 # miss rate (i.e., misses/ref)
itlb.miss rate
itlb.repl rate
                           0.0000 # replacement rate (i.e., repls/ref)
itlb.wb rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
itlb.inv rate
                          0.0000 # invalidation rate (i.e., invs/ref)
dtlb.accesses
                            56907 # total number of accesses
dtlb.hits
                             56897 # total number of hits
dtlb.misses
                                10 # total number of misses
                                 0 # total number of replacements
dtlb.replacements
                                 0 # total number of writebacks
dtlb.writebacks
                                 0 # total number of invalidations
dtlb.invalidations
dtlb.miss_rate
                           0.0002 # miss rate (i.e., misses/ref)
dtlb.repl rate
                           0.0000 # replacement rate (i.e., repls/ref)
dtlb.wb rate
                          0.0000 # writeback rate (i.e., wrbks/ref)
dtlb.inv rate
                           0.0000 # invalidation rate (i.e., invs/ref)
sim_invalid_addrs
                                 0 # total non-speculative bogus addresses seen
(debug var)
                       0x00400000 # program text (code) segment base
ld text base
ld text size
                             91744 # program text (code) size in bytes
ld_data_base
                       0x10000000 # program initialized data segment base
```

```
ld_data_size
                              13028 # program init'ed `.data' and uninit'ed
`.bss' size in bytes
ld stack base
                        0x7fffc000 # program stack segment base (highest address
in stack)
ld stack size
                              16384 # program initial stack size
                        0x00400140 # program entry point (initial PC)
ld prog entry
ld environ base
                        0x7fff8000 # program environment base address address
                                 0 # target executable endian-ness, non-zero if
ld_target_big_endian
big endian
                                33 # total number of pages allocated
mem.page count
                              132k # total size of memory pages allocated
mem.page mem
                                37 # total first level page table misses
mem.ptab_misses
                          2006598 # total page table accesses
mem.ptab_accesses
                           0.0000 # first level page table miss rate
mem.ptab miss rate
```

#### config\_e

```
sim: ** simulation statistics **
sim num insn
                            213598 # total number of instructions committed
                             56890 # total number of loads and stores committed
sim num refs
                             34096 # total number of loads committed
sim_num_loads
                  22794.0000 # total number of stores committed
sim num stores
                              38571 # total number of branches committed
sim num branches
                                 1 # total simulation time in seconds
sim elapsed time
                       213598.0000 # simulation speed (in insts/sec)
sim_inst_rate
                            227292 # total number of instructions executed
sim total insn
                             60580 # total number of loads and stores executed
sim total refs
                             36590 # total number of loads executed
sim_total_loads
                       23990.0000 # total number of stores executed
sim total stores
sim total branches
                             41566 # total number of branches executed
                            307391 # total simulation time in cycles
sim cycle
sim IPC
                            0.6949 # instructions per cycle
sim CPI
                            1.4391 # cycles per instruction
sim exec BW
                            0.7394 # total instructions (mis-spec + committed)
per cycle
sim IPB
                           5.5378 # instruction per branch
                            709474 # cumulative IFQ occupancy
IFQ count
                            165191 # cumulative IFQ full count
IFQ fcount
ifq_occupancy
                            2.3081 # avg IFQ occupancy (insn's)
                            0.7394 # avg IFQ dispatch rate (insn/cycle)
ifq_rate
ifq latency
                            3.1214 # avg IFQ occupant latency (cycle's)
ifq full
                           0.5374 # fraction of time (cycle's) IFQ was full
                          1628971 # cumulative RUU occupancy
RUU_count
RUU fcount
                            164288 # cumulative RUU full count
                            5.2993 # avg RUU occupancy (insn's)
ruu occupancy
```

```
ruu_rate
                            0.7394 # avg RUU dispatch rate (insn/cycle)
ruu latency
                            7.1669 # avg RUU occupant latency (cycle's)
ruu full
                            0.5345 # fraction of time (cycle's) RUU was full
LSQ_count
                           417278 # cumulative LSQ occupancy
LSQ_fcount
                               959 # cumulative LSO full count
                           1.3575 # avg LSQ occupancy (insn's)
1sq occupancy
                           0.7394 # avg LSQ dispatch rate (insn/cycle)
1sq rate
                           1.8359 # avg LSQ occupant latency (cycle's)
lsq_latency
lsq_full
                            0.0031 # fraction of time (cycle's) LSQ was full
                           2272410 # total number of slip cycles
sim slip
                           10.6387 # the average slip between issue and
avg sim slip
retirement
                            43739 # total number of bpred lookups
bpred bimod.lookups
bpred bimod.updates
                            38571 # total number of updates
bpred bimod.addr hits
                            34415 # total number of address-predicted hits
                            35114 # total number of direction-predicted hits
bpred_bimod.dir_hits
(includes addr-hits)
bpred bimod.misses
                             3457 # total number of misses
bpred bimod.jr hits
                     3315 # total number of address-predicted hits for
JR's
                            3542 # total number of JR's seen
bpred bimod.jr seen
bpred bimod.jr non ras hits.PP
                                        28 # total number of address-predicted
hits for non-RAS JR's
bpred bimod.jr non ras seen.PP
                                        41 # total number of non-RAS JR's seen
bpred_bimod.bpred_addr_rate 0.8923 # branch address-prediction rate (i.e.,
addr-hits/updates)
bpred_bimod.bpred_dir_rate 0.9104 # branch direction-prediction rate (i.e.,
all-hits/updates)
bpred_bimod.bpred_jr_rate     0.9359 # JR address-prediction rate (i.e., JR addr-
hits/JRs seen)
bpred bimod.bpred jr non ras rate.PP 0.6829 # non-RAS JR addr-pred rate (ie,
non-RAS JR hits/JRs seen)
bpred bimod.retstack pushes 3914 # total number of address pushed onto
ret-addr stack
bpred_bimod.retstack_pops 4509 # total number of address popped off of
ret-addr stack
bpred bimod.used ras.PP
                             3501 # total number of RAS predictions used
bpred_bimod.ras_hits.PP
                               3287 # total number of RAS hits
bpred bimod.ras rate.PP 0.9389 # RAS prediction rate (i.e., RAS hits/used RAS)
ill.accesses
                            252224 # total number of accesses
ill.hits
                            236110 # total number of hits
il1.misses
                             16114 # total number of misses
ill.replacements
                            15603 # total number of replacements
ill.writebacks
                                 0 # total number of writebacks
ill.invalidations
                                 0 # total number of invalidations
il1.miss_rate
                            0.0639 # miss rate (i.e., misses/ref)
```

```
ill.repl rate
                            0.0619 # replacement rate (i.e., repls/ref)
                            0.0000 # writeback rate (i.e., wrbks/ref)
ill.wb rate
                            0.0000 # invalidation rate (i.e., invs/ref)
ill.inv rate
                            56954 # total number of accesses
dl1.accesses
dl1.hits
                             56404 # total number of hits
                              550 # total number of misses
dl1.misses
                               65 # total number of replacements
dl1.replacements
dl1.writebacks
                                60 # total number of writebacks
dl1.invalidations
                                 0 # total number of invalidations
dl1.miss rate
                           0.0097 # miss rate (i.e., misses/ref)
dl1.repl rate
                            0.0011 # replacement rate (i.e., repls/ref)
dl1.wb_rate
                           0.0011 # writeback rate (i.e., wrbks/ref)
                          0.0000 # invalidation rate (i.e., invs/ref)
dl1.inv rate
                            16724 # total number of accesses
ul2.accesses
                            15504 # total number of hits
ul2.hits
ul2.misses
                             1220 # total number of misses
                                 0 # total number of replacements
ul2.replacements
                                 0 # total number of writebacks
ul2.writebacks
                                 0 # total number of invalidations
ul2.invalidations
ul2.miss rate
                          0.0729 # miss rate (i.e., misses/ref)
                          0.0000 # replacement rate (i.e., repls/ref)
ul2.repl rate
ul2.wb rate
                          0.0000 # writeback rate (i.e., wrbks/ref)
ul2.inv rate
                           0.0000 # invalidation rate (i.e., invs/ref)
itlb.accesses
                           252224 # total number of accesses
itlb.hits
                            252201 # total number of hits
itlb.misses
                                23 # total number of misses
itlb.replacements
                                 0 # total number of replacements
                                 0 # total number of writebacks
itlb.writebacks
                                 0 # total number of invalidations
itlb.invalidations
itlb.miss_rate
                          0.0001 # miss rate (i.e., misses/ref)
itlb.repl rate
                          0.0000 # replacement rate (i.e., repls/ref)
                          0.0000 # writeback rate (i.e., wrbks/ref)
itlb.wb rate
itlb.inv rate
                          0.0000 # invalidation rate (i.e., invs/ref)
dtlb.accesses
                             56961 # total number of accesses
                             56951 # total number of hits
dtlb.hits
                               10 # total number of misses
dtlb.misses
                                 0 # total number of replacements
dtlb.replacements
dtlb.writebacks
                                 0 # total number of writebacks
                                 0 # total number of invalidations
dtlb.invalidations
                          0.0002 # miss rate (i.e., misses/ref)
dtlb.miss rate
dtlb.repl rate
                          0.0000 # replacement rate (i.e., repls/ref)
dtlb.wb_rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
dtlb.inv rate
                           0.0000 # invalidation rate (i.e., invs/ref)
                                 0 # total non-speculative bogus addresses seen
sim invalid addrs
(debug var)
               0x00400000 # program text (code) segment base
ld_text_base
```

```
ld_text_size
                              91744 # program text (code) size in bytes
ld data base
                        0x10000000 # program initialized data segment base
                              13028 # program init'ed `.data' and uninit'ed
ld data size
`.bss' size in bytes
ld stack base
                       0x7fffc000 # program stack segment base (highest address
in stack)
                             16384 # program initial stack size
ld stack size
                       0x00400140 # program entry point (initial PC)
ld_prog_entry
ld_environ_base
                        0x7fff8000 # program environment base address address
                                 0 # target executable endian-ness, non-zero if
ld target big endian
big endian
                                33 # total number of pages allocated
mem.page_count
                              132k # total size of memory pages allocated
mem.page_mem
                                37 # total first level page table misses
mem.ptab misses
                          2001494 # total page table accesses
mem.ptab accesses
                           0.0000 # first level page table miss rate
mem.ptab_miss_rate
```

## config\_f

```
sim: ** simulation statistics **
                           213598 # total number of instructions committed
sim_num_insn
                             56890 # total number of loads and stores committed
sim num refs
                              34096 # total number of loads committed
sim num loads
                       22794.0000 # total number of stores committed
sim num stores
                              38571 # total number of branches committed
sim_num_branches
                                 1 # total simulation time in seconds
sim elapsed time
                     213598.0000 # simulation speed (in insts/sec)
sim inst rate
                            223139 # total number of instructions executed
sim total insn
                             59348 # total number of loads and stores executed
sim total refs
                             35910 # total number of loads executed
sim total loads
                        23438.0000 # total number of stores executed
sim total stores
                              40262 # total number of branches executed
sim_total_branches
sim cycle
                            245787 # total simulation time in cycles
                            0.8690 # instructions per cycle
sim IPC
sim CPI
                            1.1507 # cycles per instruction
sim_exec_BW
                            0.9079 # total instructions (mis-spec + committed)
per cycle
                            5.5378 # instruction per branch
sim IPB
IFQ count
                            454131 # cumulative IFQ occupancy
                            101663 # cumulative IFQ full count
IFQ_fcount
                            1.8477 # avg IFQ occupancy (insn's)
ifq occupancy
                            0.9079 # avg IFQ dispatch rate (insn/cycle)
ifq rate
ifq_latency
                            2.0352 # avg IFQ occupant latency (cycle's)
ifq full
                            0.4136 # fraction of time (cycle's) IFQ was full
RUU count
                           1045536 # cumulative RUU occupancy
```

```
RUU fcount
                             97501 # cumulative RUU full count
ruu occupancy
                            4.2538 # avg RUU occupancy (insn's)
                            0.9079 # avg RUU dispatch rate (insn/cycle)
ruu rate
ruu_latency
                            4.6856 # avg RUU occupant latency (cycle's)
ruu_full
                            0.3967 # fraction of time (cycle's) RUU was full
                           243088 # cumulative LSQ occupancy
LSQ count
                               316 # cumulative LSQ full count
LSQ fcount
                          0.9890 # avg LSQ occupancy (insn's)
lsq_occupancy
lsq_rate
                           0.9079 # avg LSQ dispatch rate (insn/cycle)
                            1.0894 # avg LSQ occupant latency (cycle's)
lsq latency
                           0.0013 # fraction of time (cycle's) LSQ was full
lsq full
                          1536832 # total number of slip cycles
sim_slip
                           7.1950 # the average slip between issue and
avg_sim_slip
retirement
bpred bimod.lookups
                           42563 # total number of bpred lookups
bpred_bimod.updates
                            38571 # total number of updates
                           34621 # total number of address-predicted hits
bpred_bimod.addr_hits
                            35114 # total number of direction-predicted hits
bpred bimod.dir hits
(includes addr-hits)
                            3457 # total number of misses
bpred bimod.misses
bpred_bimod.jr_hits 3520 # total number of address-predicted hits for
JR's
                      3542 # total number of JR's seen
bpred bimod.jr seen
bpred bimod.jr non ras hits.PP
                                      28 # total number of address-predicted
hits for non-RAS JR's
bpred_bimod.jr_non_ras_seen.PP
                                       41 # total number of non-RAS JR's seen
bpred_bimod.bpred_addr_rate     0.8976 # branch address-prediction rate (i.e.,
addr-hits/updates)
bpred_bimod.bpred_dir_rate     0.9104 # branch direction-prediction rate (i.e.,
all-hits/updates)
bpred bimod.bpred jr rate 0.9938 # JR address-prediction rate (i.e., JR addr-
hits/JRs seen)
bpred bimod.bpred jr non ras rate.PP 0.6829 # non-RAS JR addr-pred rate (ie,
non-RAS JR hits/JRs seen)
bpred_bimod.retstack_pushes 3717 # total number of address pushed onto
ret-addr stack
bpred bimod.retstack pops 4435 # total number of address popped off of
ret-addr stack
bpred bimod.used ras.PP
                             3501 # total number of RAS predictions used
bpred bimod.ras hits.PP
                               3492 # total number of RAS hits
bpred_bimod.ras_rate.PP 0.9974 # RAS prediction rate (i.e., RAS hits/used RAS)
ill.accesses
                            247629 # total number of accesses
ill.hits
                            231610 # total number of hits
                            16019 # total number of misses
ill.misses
                            15508 # total number of replacements
ill.replacements
ill.writebacks
                                 0 # total number of writebacks
```

```
ill.invalidations
                                 0 # total number of invalidations
ill.miss rate
                            0.0647 # miss rate (i.e., misses/ref)
ill.repl rate
                            0.0626 # replacement rate (i.e., repls/ref)
il1.wb_rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
ill.inv rate
                           0.0000 # invalidation rate (i.e., invs/ref)
                            56763 # total number of accesses
dl1.accesses
dl1.hits
                             56211 # total number of hits
dl1.misses
                               552 # total number of misses
dl1.replacements
                                66 # total number of replacements
dl1.writebacks
                                61 # total number of writebacks
                                 0 # total number of invalidations
dll.invalidations
dl1.miss_rate
                           0.0097 # miss rate (i.e., misses/ref)
                           0.0012 # replacement rate (i.e., repls/ref)
dl1.repl rate
                           0.0011 # writeback rate (i.e., wrbks/ref)
dl1.wb rate
dll.inv rate
                           0.0000 # invalidation rate (i.e., invs/ref)
ul2.accesses
                            16632 # total number of accesses
ul2.hits
                             15412 # total number of hits
                              1220 # total number of misses
ul2.misses
                                 0 # total number of replacements
ul2.replacements
ul2.writebacks
                                 0 # total number of writebacks
ul2.invalidations
                                 0 # total number of invalidations
ul2.miss rate
                           0.0734 # miss rate (i.e., misses/ref)
ul2.repl rate
                           0.0000 # replacement rate (i.e., repls/ref)
ul2.wb rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
ul2.inv rate
                            0.0000 # invalidation rate (i.e., invs/ref)
itlb.accesses
                            247629 # total number of accesses
                            247606 # total number of hits
itlb.hits
                                23 # total number of misses
itlb.misses
                                0 # total number of replacements
itlb.replacements
itlb.writebacks
                                 0 # total number of writebacks
itlb.invalidations
                                 0 # total number of invalidations
itlb.miss rate
                           0.0001 # miss rate (i.e., misses/ref)
itlb.repl rate
                            0.0000 # replacement rate (i.e., repls/ref)
itlb.wb rate
                            0.0000 # writeback rate (i.e., wrbks/ref)
itlb.inv rate
                            0.0000 # invalidation rate (i.e., invs/ref)
                            57243 # total number of accesses
dtlb.accesses
                             57233 # total number of hits
dtlb.hits
dtlb.misses
                               10 # total number of misses
dtlb.replacements
                                 0 # total number of replacements
dtlb.writebacks
                                 0 # total number of writebacks
dtlb.invalidations
                                 0 # total number of invalidations
dtlb.miss_rate
                           0.0002 # miss rate (i.e., misses/ref)
dtlb.repl rate
                            0.0000 # replacement rate (i.e., repls/ref)
                            0.0000 # writeback rate (i.e., wrbks/ref)
dtlb.wb rate
                           0.0000 # invalidation rate (i.e., invs/ref)
dtlb.inv rate
```

```
sim_invalid_addrs
                                 0 # total non-speculative bogus addresses seen
(debug var)
                        0x00400000 # program text (code) segment base
ld text base
ld_text_size
                             91744 # program text (code) size in bytes
ld_data_base
                        0x10000000 # program initialized data segment base
                             13028 # program init'ed `.data' and uninit'ed
ld data size
`.bss' size in bytes
                       0x7fffc000 # program stack segment base (highest address
ld_stack_base
in stack)
                             16384 # program initial stack size
ld stack size
ld prog entry
                        0x00400140 # program entry point (initial PC)
ld_environ_base
                        0x7fff8000 # program environment base address address
                                 0 # target executable endian-ness, non-zero if
ld target big endian
big endian
                                33 # total number of pages allocated
mem.page count
                              132k # total size of memory pages allocated
mem.page_mem
mem.ptab misses
                                37 # total first level page table misses
mem.ptab accesses
                          1981776 # total page table accesses
mem.ptab miss rate
                            0.0000 # first level page table miss rate
```

## config\_g

```
sim: ** simulation statistics **
                            213598 # total number of instructions committed
sim num insn
                             56890 # total number of loads and stores committed
sim_num_refs
                             34096 # total number of loads committed
sim num loads
                       22794.0000 # total number of stores committed
sim_num_stores
                             38571 # total number of branches committed
sim_num_branches
sim elapsed time
                                 1 # total simulation time in seconds
                       213598.0000 # simulation speed (in insts/sec)
sim inst rate
                            232968 # total number of instructions executed
sim total insn
                             61946 # total number of loads and stores executed
sim_total_refs
sim total loads
                             37532 # total number of loads executed
sim total stores
                        24414.0000 # total number of stores executed
                             42756 # total number of branches executed
sim total branches
sim_cycle
                            223665 # total simulation time in cycles
sim IPC
                            0.9550 # instructions per cycle
                            1.0471 # cycles per instruction
sim CPI
                            1.0416 # total instructions (mis-spec + committed)
sim_exec_BW
per cycle
                           5.5378 # instruction per branch
sim IPB
                            349171 # cumulative IFQ occupancy
IFQ count
                            73294 # cumulative IFQ full count
IFQ fcount
ifq occupancy
                           1.5611 # avg IFQ occupancy (insn's)
ifq rate
                            1.0416 # avg IFQ dispatch rate (insn/cycle)
```

```
ifq_latency
                            1.4988 # avg IFQ occupant latency (cycle's)
ifq full
                            0.3277 # fraction of time (cycle's) IFQ was full
                           1427733 # cumulative RUU occupancy
RUU count
RUU_fcount
                            45299 # cumulative RUU full count
ruu_occupancy
                           6.3834 # avg RUU occupancy (insn's)
                           1.0416 # avg RUU dispatch rate (insn/cycle)
ruu rate
                           6.1285 # avg RUU occupant latency (cycle's)
ruu latency
ruu full
                           0.2025 # fraction of time (cycle's) RUU was full
LSQ_count
                           304051 # cumulative LSQ occupancy
                              4116 # cumulative LSQ full count
LSQ fcount
                           1.3594 # avg LSQ occupancy (insn's)
1sq occupancy
                           1.0416 # avg LSQ dispatch rate (insn/cycle)
lsq_rate
                           1.3051 # avg LSQ occupant latency (cycle's)
lsq latency
                           0.0184 # fraction of time (cycle's) LSQ was full
lsq full
                          1940667 # total number of slip cycles
sim slip
                           9.0856 # the average slip between issue and
avg_sim_slip
retirement
                            44131 # total number of bpred lookups
bpred bimod.lookups
                            38571 # total number of updates
bpred bimod.updates
bpred bimod.addr hits
                            34542 # total number of address-predicted hits
                           35130 # total number of direction-predicted hits
bpred bimod.dir hits
(includes addr-hits)
bpred bimod.misses
                            3441 # total number of misses
bpred bimod.jr hits
                            3425 # total number of address-predicted hits for
JR's
bpred_bimod.jr_seen
                     3542 # total number of JR's seen
bpred bimod.jr non ras hits.PP
                                       28 # total number of address-predicted
hits for non-RAS JR's
bpred_bimod.jr_non_ras_seen.PP
                                       41 # total number of non-RAS JR's seen
bpred_bimod.bpred_addr_rate 0.8955 # branch address-prediction rate (i.e.,
addr-hits/updates)
bpred_bimod.bpred_dir_rate 0.9108 # branch direction-prediction rate (i.e.,
all-hits/updates)
bpred_bimod.bpred_jr_rate     0.9670 # JR address-prediction rate (i.e., JR addr-
hits/JRs seen)
bpred bimod.bpred jr non ras rate.PP 0.6829 # non-RAS JR addr-pred rate (ie,
non-RAS JR hits/JRs seen)
                                3906 # total number of address pushed onto
bpred_bimod.retstack_pushes
ret-addr stack
bpred bimod.retstack pops 4531 # total number of address popped off of
ret-addr stack
bpred_bimod.used_ras.PP 3501 # total number of RAS predictions used
bpred bimod.ras hits.PP
                               3397 # total number of RAS hits
bpred bimod.ras rate.PP 0.9703 # RAS prediction rate (i.e., RAS hits/used RAS)
ill.accesses
                           255935 # total number of accesses
ill.hits
                            239826 # total number of hits
```

```
il1.misses
                             16109 # total number of misses
ill.replacements
                             15598 # total number of replacements
                                 0 # total number of writebacks
ill.writebacks
ill.invalidations
                                 0 # total number of invalidations
ill.miss rate
                           0.0629 # miss rate (i.e., misses/ref)
                           0.0609 # replacement rate (i.e., repls/ref)
ill.repl rate
                           0.0000 # writeback rate (i.e., wrbks/ref)
ill.wb rate
                           0.0000 # invalidation rate (i.e., invs/ref)
ill.inv_rate
dll.accesses
                             56926 # total number of accesses
                             56375 # total number of hits
dl1.hits
                              551 # total number of misses
dl1.misses
                               66 # total number of replacements
dl1.replacements
dl1.writebacks
                               61 # total number of writebacks
dll.invalidations
                                 0 # total number of invalidations
dl1.miss rate
                           0.0097 # miss rate (i.e., misses/ref)
                           0.0012 # replacement rate (i.e., repls/ref)
dl1.repl_rate
dl1.wb rate
                           0.0011 # writeback rate (i.e., wrbks/ref)
                           0.0000 # invalidation rate (i.e., invs/ref)
dl1.inv rate
                            16721 # total number of accesses
ul2.accesses
ul2.hits
                            15500 # total number of hits
                             1221 # total number of misses
ul2.misses
ul2.replacements
                                 0 # total number of replacements
ul2.writebacks
                                 0 # total number of writebacks
ul2.invalidations
                                 0 # total number of invalidations
ul2.miss rate
                           0.0730 # miss rate (i.e., misses/ref)
ul2.repl rate
                            0.0000 # replacement rate (i.e., repls/ref)
                            0.0000 # writeback rate (i.e., wrbks/ref)
ul2.wb rate
ul2.inv rate
                            0.0000 # invalidation rate (i.e., invs/ref)
                            255935 # total number of accesses
itlb.accesses
itlb.hits
                            255912 # total number of hits
itlb.misses
                                23 # total number of misses
                                 0 # total number of replacements
itlb.replacements
                                 0 # total number of writebacks
itlb.writebacks
itlb.invalidations
                                 0 # total number of invalidations
itlb.miss rate
                            0.0001 # miss rate (i.e., misses/ref)
                            0.0000 # replacement rate (i.e., repls/ref)
itlb.repl rate
itlb.wb rate
                            0.0000 # writeback rate (i.e., wrbks/ref)
                           0.0000 # invalidation rate (i.e., invs/ref)
itlb.inv_rate
dtlb.accesses
                            57605 # total number of accesses
                             57595 # total number of hits
dtlb.hits
dtlb.misses
                                10 # total number of misses
dtlb.replacements
                                 0 # total number of replacements
dtlb.writebacks
                                 0 # total number of writebacks
dtlb.invalidations
                                 0 # total number of invalidations
dtlb.miss rate
                            0.0002 # miss rate (i.e., misses/ref)
                            0.0000 # replacement rate (i.e., repls/ref)
dtlb.repl_rate
```

```
0.0000 # writeback rate (i.e., wrbks/ref)
dtlb.wb_rate
                            0.0000 # invalidation rate (i.e., invs/ref)
dtlb.inv rate
sim invalid addrs
                                 0 # total non-speculative bogus addresses seen
(debug var)
ld_text_base
                       0x00400000 # program text (code) segment base
ld text size
                             91744 # program text (code) size in bytes
ld data base
                       0x10000000 # program initialized data segment base
ld_data_size
                             13028 # program init'ed `.data' and uninit'ed
`.bss' size in bytes
ld stack base
                       0x7fffc000 # program stack segment base (highest address
in stack)
ld_stack_size
                             16384 # program initial stack size
ld_prog_entry
                       0x00400140 # program entry point (initial PC)
ld environ base
                        0x7fff8000 # program environment base address address
                                 0 # target executable endian-ness, non-zero if
ld_target_big_endian
big endian
                                33 # total number of pages allocated
mem.page_count
                              132k # total size of memory pages allocated
mem.page mem
                                37 # total first level page table misses
mem.ptab misses
mem.ptab_accesses
                          2017814 # total page table accesses
                           0.0000 # first level page table miss rate
mem.ptab_miss_rate
```

## 5. Discussion

## config\_a

- 1. Describe the configuration.
- Decode: width = 1
- Fetch queue size = 1
- Load store queue size = 8
- Register update unit (ruu) size = 8
- Issue width = 1
- Memory ports = 1
- Inorder = true
- Resources all types = 1
  - 2. What is the IPC of the test-math program using this configuration?

The IPC is 0.5795.

3. Is the forwarding implemented?

I am not sure.

## config\_b

- 1. Describe the configuration.
- Decode: width = 1
- Fetch queue size = 1
- Load store queue size = 8
- Register update unit (ruu) size = 8
- Issue width = 1
- Memory ports = 1
- Inorder = false
- Resources all types = 1
  - 2. What is the IPC of the test-math program using this configuration?

The IPC is 0.6094.

3. Compared to part (1) or configuration A, what can you say about this configuration?

It seems that changing inorder from "true" to "false" increases the IPC.

4. The commit stage CT reorders the execution of instructions, explain why is it necessary?

I am not sure.

## config\_c

1. What is the IPC of the test-math program using this configuration?

The IPC is 0.5795.

2. Compare this configuration with the configuration in part 2 of the previous lab.

It seems that there is a positive correlation between the IPC and resources.

## config\_d

1. What is the IPC of the test-math program using this configuration?

The IPC is 0.6094.

2. Compare this configuration and configuration in part 1 of this lab. Does the out of order increase performance?

Yes.

3. As the system contains 4 Functional units in parallel, find the bottleneck of execution. This means changing the number of which parameter of these - memory port, issue width and decode width - will increase the performance most.

See the part of "config\_e" below.

4. Based on part e) what is the new IPC and what is your conclusion?

See the part of "config\_e" below.

## config\_e

1. What is the IPC of the test-math program using this configuration?

The IPC is 0.6949.

2. Compare this configuration with the configuration in part 2 of the previous lab.

It is clear that the IPC is increased.

## config\_f

1. What is the IPC of the test-math program using this configuration?

The IPC is 0.8690.

## config\_g

1. What is the IPC of the test-math program using this configuration?

The IPC is 0.9550.