Project 2 - Part 2

Zhicheng Zhang - G45149856

1. Introduction

Cache organization with unified/separate instruction and data caches.

2. Implementation

Prepare

Environment

- Docker image krlmlr/debian-ssh on Debian 10 (host).
- File `~/simplesim-3v0e.tgz` is downloaded from http://www.simplescalar.com/.

Script

```
# install
apt-get install tar build-essential

# unzip
tar zxvf simplesim-3v0e.tgz
```

Compile

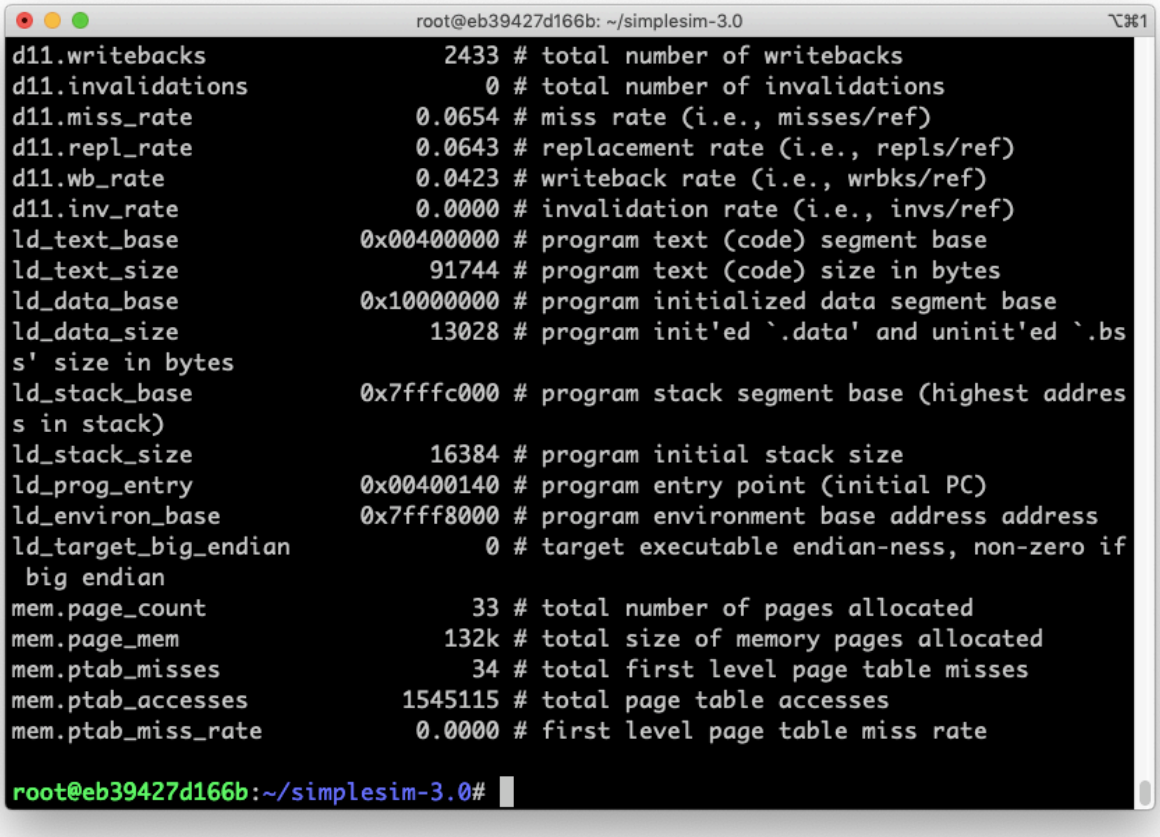
```
cd ~/simplesim-3.0
make clean
make config-pisa
make
make sim-tests
cd ~
```

Run

```
cd ./simplesim-3.0/
```

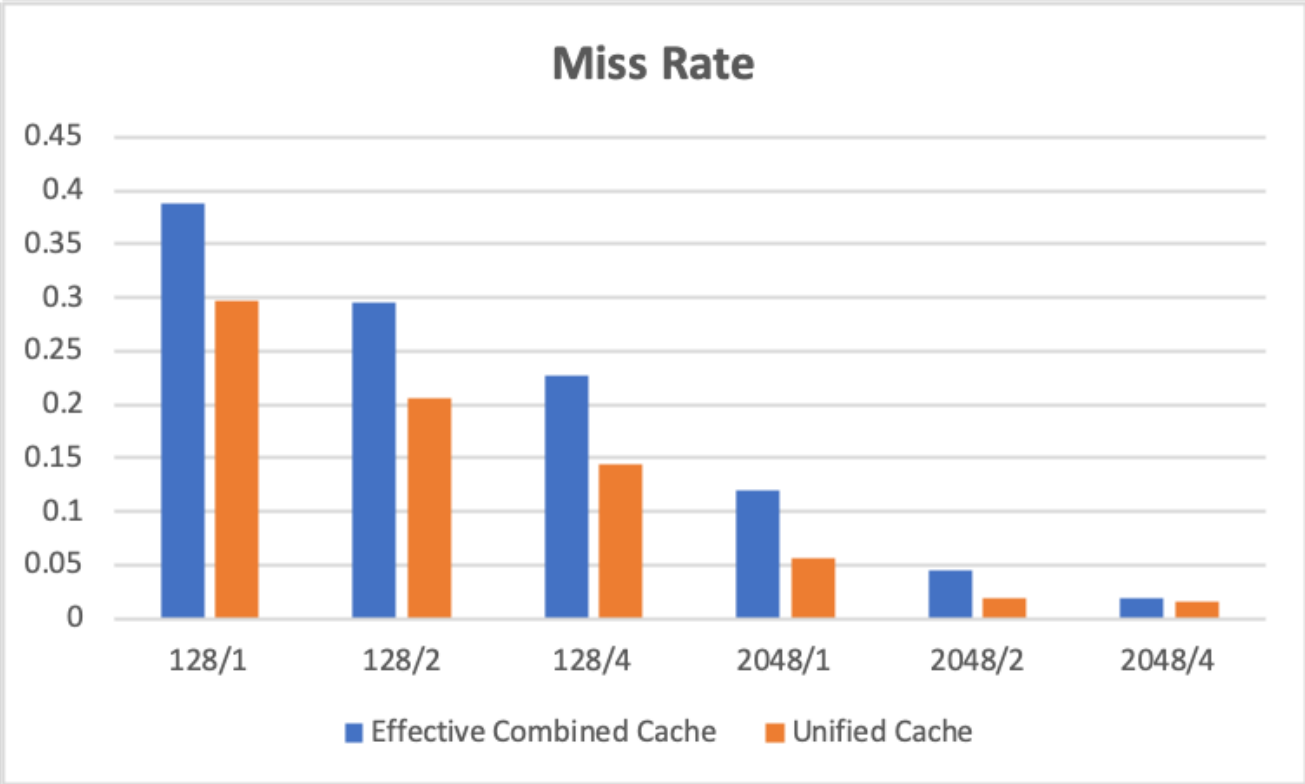
```
# 128/1
./sim-cache -cache:il1 i11:64:16:1:l -cache:dl1 d11:64:16:1:l -cache:il2 none -
cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math
./sim-cache -cache:il1 dl1 -cache:dl1 ul1:128:16:1:l -cache:il2 none -cache:dl2
none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math

# 128/2
./sim-cache -cache:il1 i11:64:16:2:l -cache:dl1 d11:64:16:2:l -cache:il2 none -
cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math
./sim-cache -cache:il1 dl1 -cache:dl1 ul1:128:16:2:l -cache:il2 none -cache:dl2
none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math

# 128/4
./sim-cache -cache:il1 i11:64:16:4:l -cache:dl1 d11:64:16:4:l -cache:il2 none -
cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math
./sim-cache -cache:il1 dl1 -cache:dl1 ul1:128:16:4:l -cache:il2 none -cache:dl2
none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math

# 2048/1
./sim-cache -cache:il1 i11:1024:16:1:l -cache:dl1 d11:1024:16:1:l -cache:il2 none
-cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math
./sim-cache -cache:il1 dl1 -cache:dl1 ul1:2048:16:1:l -cache:il2 none -cache:dl2
none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math

# 2048/2
./sim-cache -cache:il1 i11:1024:16:2:l -cache:dl1 d11:1024:16:2:l -cache:il2 none
-cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math
./sim-cache -cache:il1 dl1 -cache:dl1 ul1:2048:16:2:l -cache:il2 none -cache:dl2
none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math

# 2048/4
./sim-cache -cache:il1 i11:1024:16:4:l -cache:dl1 d11:1024:16:4:l -cache:il2 none
-cache:dl2 none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math
./sim-cache -cache:il1 dl1 -cache:dl1 ul1:2048:16:4:l -cache:il2 none -cache:dl2
none -tlb:itlb none -tlb:dtlb none tests-pisa/bin.little/test-math
```

3. Result


root@eb39427d166b: ~/simplesim-3.0
⌥⌘1
d11.writebacks 2433 # total number of writebacks
d11.invalidations 0 # total number of invalidations
d11.miss_rate 0.0654 # miss rate (i.e., misses/ref)
d11.repl_rate 0.0643 # replacement rate (i.e., repls/ref)
d11.wb_rate 0.0423 # writeback rate (i.e., wrbks/ref)
d11.inv_rate 0.0000 # invalidation rate (i.e., invs/ref)
ld_text_base 0x00400000 # program text (code) segment base
ld_text_size 91744 # program text (code) size in bytes
ld_data_base 0x10000000 # program initialized data segment base
ld_data_size 13028 # program init'ed `.data' and uninit'ed `.bss' size in bytes
ld_stack_base 0x7fffc000 # program stack segment base (highest address in stack)
ld_stack_size 16384 # program initial stack size
ld_prog_entry 0x00400140 # program entry point (initial PC)
ld_environ_base 0x7fff8000 # program environment base address address
ld_target_big_endian 0 # target executable endian-ness, non-zero if big endian
mem.page_count 33 # total number of pages allocated
mem.page_mem 132k # total size of memory pages allocated
mem.ptab_misses 34 # total first level page table misses
mem.ptab_accesses 1545115 # total page table accesses
mem.ptab_miss_rate 0.0000 # first level page table miss rate
root@eb39427d166b:~/simplesim-3.0#

4. Conclusion

Sets/Assoc	I-Cache Miss No (N/2 sets)	D-Cache Miss No (N/2 sets)	Effective Combined Cache Miss Rate	Unified Cache Miss Rate
128/1	64	64	0.3878	0.2971
128/2	64	64	0.2948	0.2060
128/4	64	64	0.2265	0.1438
2048/1	1024	1024	0.1201	0.0554
2048/2	1024	1024	0.0454	0.0184
2048/4	1024	1024	0.0186	0.0149



5. Discussion

It seems that the miss rate of the unified cache is usually smaller than which of the separate cache.