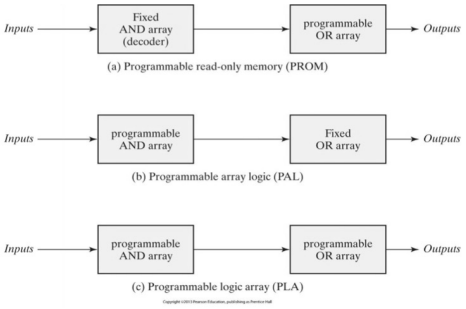
Ch.7 Memory And Programmable Logic - part B

Combinational PLD

AND-OR SOP → AND array, OR array로 나누어진 programmable한 집적회로



1. **PROM** : fixed AND array(decoder) + programmable OR array
2. **PAL** : programmable AND array + fixed OR array
3. **PLA** : programmable AND array + programmable OR array

Programmable Logic Array(PLA)

programmable AND array

\+ programmable OR array

PLA Programming Table

		Inputs			Outputs (T)	(C)
	Product Term	A	B	C	F_1	F_2
AB'	1	1	0	—	1	—
AC	2	1	—	1	1	1
BC	3	—	1	1	—	1
$A'BC'$	4	0	1	0	1	—

F_2는 complement

input → n개

output → m개

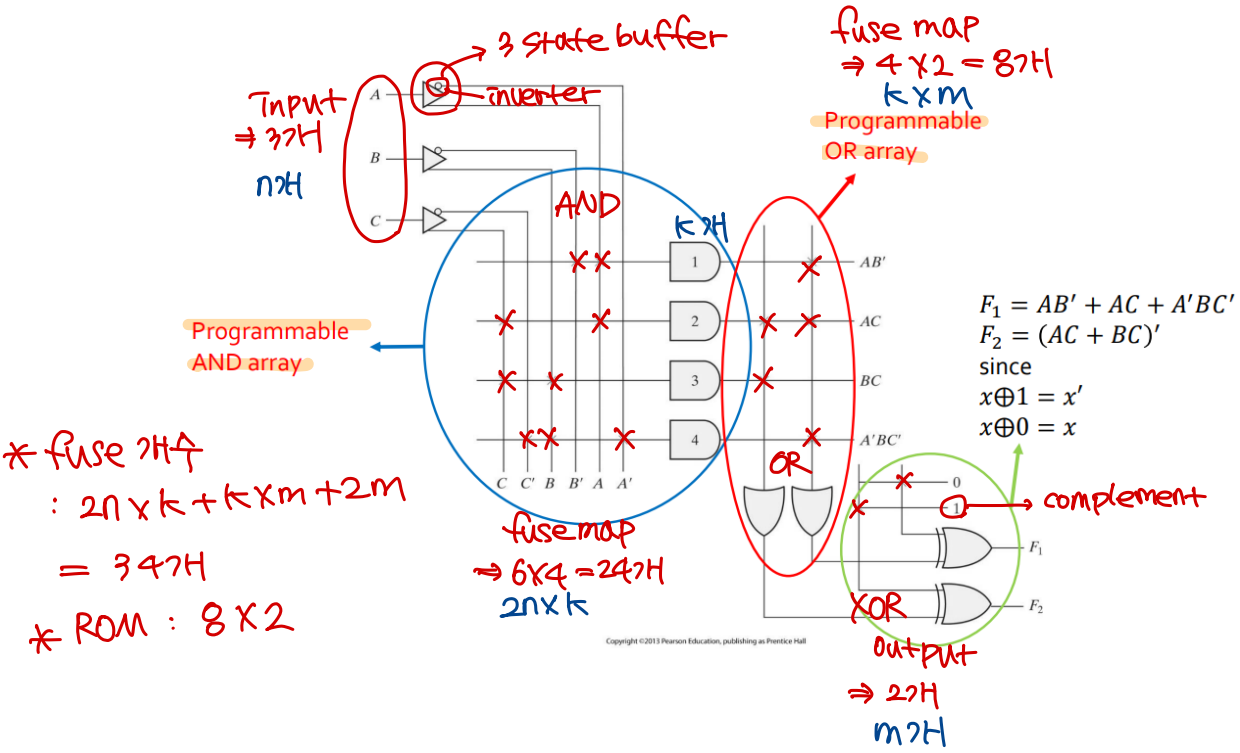
produce terms(AND gate) → k개

sum terms(OR gate) → m개

⇒ programmed fuses : 2n*k + k*m + 2m

↔ ROM : 2^n X m

product term개수가 중요!

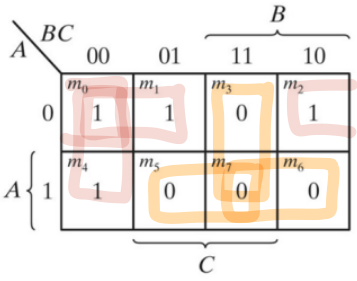


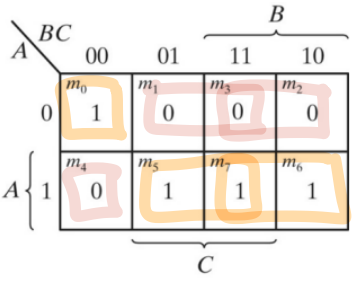
- **example 7.2**

PLA programming table

	Product term	Inputs A	B	C	Outputs (C) F_1	(T) F_2
AB	1	1	1	–	1	1
AC	2	1	–	1	1	1
BC	3	–	1	1	1	–
$A'B'C'$	4	0	0	0	–	1

개수 최소화





: 6개 ⇒ T

: 4개 ⇒ F

↳ 선택!

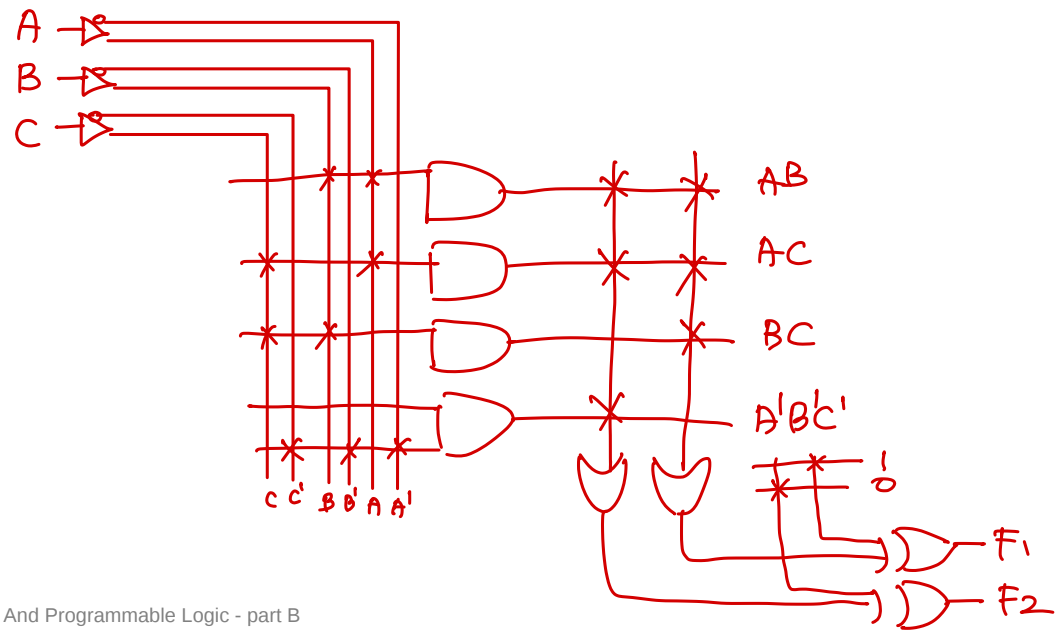
(T) $F_1 = A'B' + A'C' + B'C'$

(F) $F_1 = (AB + AC + BC)'$

(T) $F_2 = AB + AC + A'B'C'$

(F) $F_2 = (A'C + A'B + AB'C')'$

→ equation을 어떻게 설정하냐에 따라서 AND gate(Product term) 개수가 다름 ⇒ 최소화!



Programmable Array Logic(PAL)

programmable AND array

+ fixed OR array

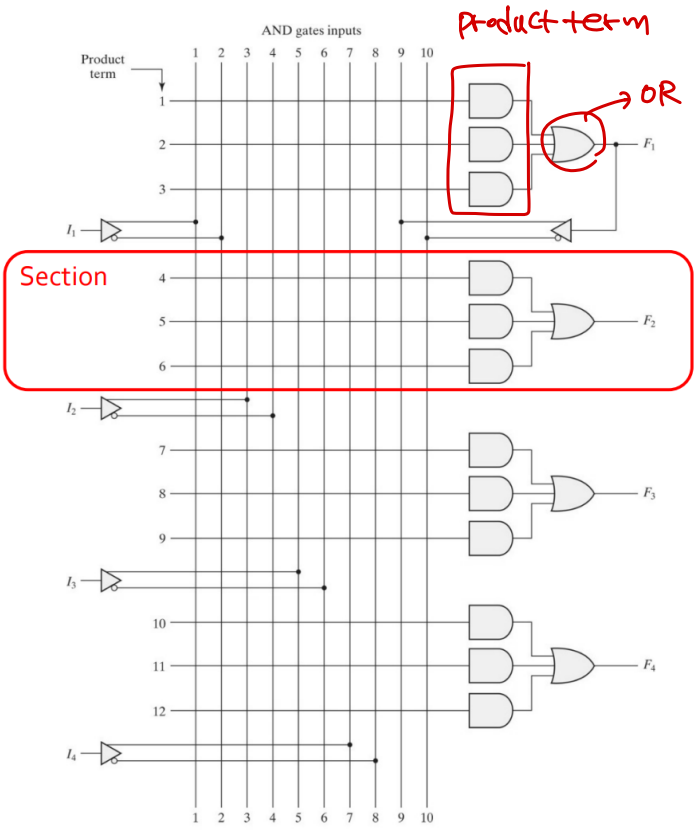
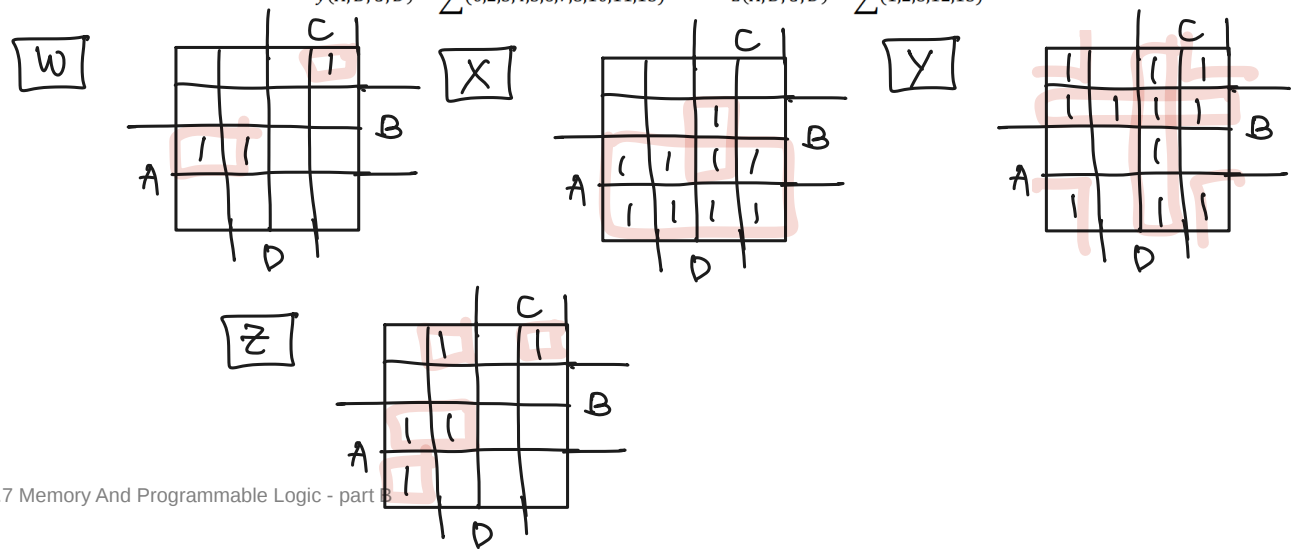


Table 7.6
PAL Programming Table

Product Term	AND Inputs A	B	C	D	w	Outputs
1	1	1	0	—	—	$w = ABC' + A'B'CD'$
2	0	0	1	0	—	
3	—	—	—	—	—	
4	1	—	—	—	—	$x = A + BCD$
5	—	1	1	1	—	
6	—	—	—	—	—	
7	0	1	—	—	—	$y = A'B + CD + B'D'$
8	—	—	1	1	—	
9	—	0	—	0	—	
10	—	—	—	—	1	$z = w + AC'D' + A'B'C'D$
11	1	—	0	0	—	
12	0	0	0	1	—	

$w(A,B,C,D) = \sum(2,12,13)$ $x(A,B,C,D) = \sum(7,8,9,10,11,12,13,14,15)$

$y(A,B,C,D) = \sum(0,2,3,4,5,6,7,8,10,11,15)$ $z(A,B,C,D) = \sum(1,2,8,12,13)$



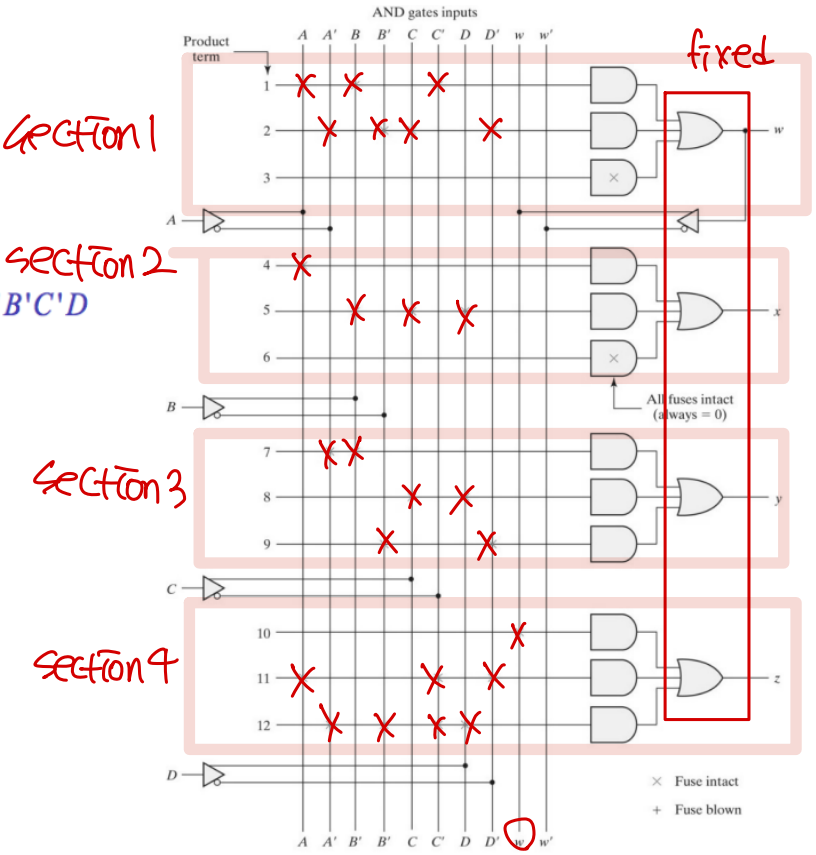
$w = ABC' + A'B'CD'$

$x = A + BCD$

$y = A'B + CD + B'D'$

$z = ABC' + A'B'CD' + AC'D' + A'B'C'D$

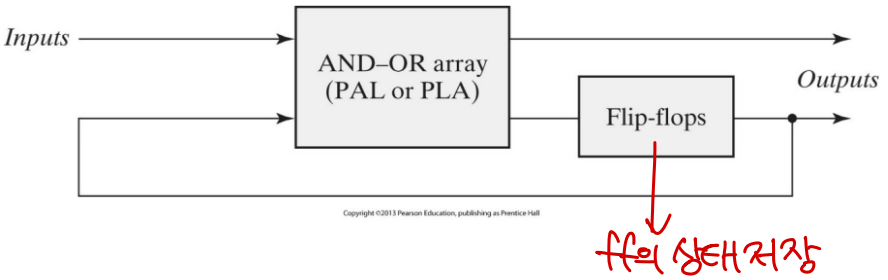
$= w + AC'D' + A'B'C'D$



↳ storage위치 구현

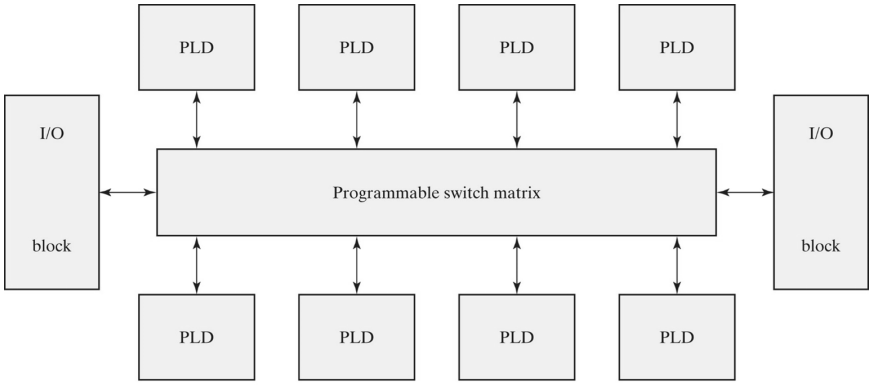
Sequential Programmable Devices(SPLD)

simple programmable logic device (ex. PROM, PLA, PAL, combinational PLD)



① Complex Programmable Logic Device(CPLD)

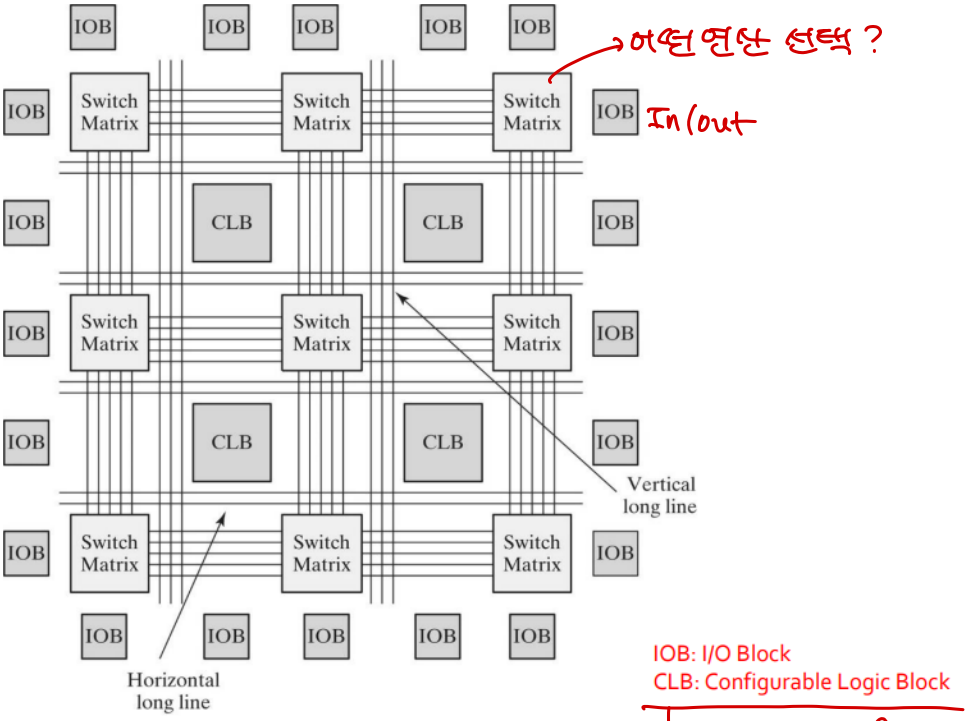
대규모로 계산하기 위해 gate 개수 늘린 것



⇒ 필요에 따라 PLD 선택해서 연산

② Field Programmable Gate Array(FPGA) → 현장에서 프로그래밍 가능

회로의 상태를 저장할 수 있는 ff → 용도에 맞게 회로 재설계 가능



CPLD vs. FPGA

	CPLD	FPGA
Data storage	EEPROM (Non-volatile)	SRAM (Volatile)
Term for data writing	'Program'	'Configure'
Structure	Logic gates	Look-up Table(Logic gate) + D-flipflop
Scale	~100,000 gates	~ 10,000,000 gates
Main Application	Simple combinational logic design	Memory, Complex IP, CPU design