

# Smart High-Side Power Switch

## Two Channels: 2 x 90mΩ

## Status Feedback

### Product Summary

Operating Voltage	$V_{bb}$	5.5...40V	
Active channels		one	two parallel
On-state Resistance	$R_{ON}$	90mΩ	45mΩ
Nominal load current	$I_{L(NOM)}$	3.7A	7.4A
Current limitation	$I_{L(SCR)}$	12A	12A

### Package



### General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology.
- Providing embedded protective functions

### Applications

- µC compatible high-side power switch with diagnostic feedback for 12V and 24V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

### Basic Functions

- Very low standby current
- CMOS compatible input
- Improved electromagnetic compatibility (EMC)
- Fast demagnetization of inductive loads
- Stable behaviour at undervoltage
- Wide operating voltage range
- Logic ground independent from load ground

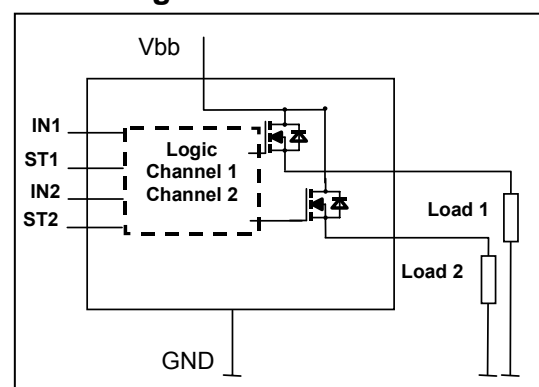
### Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of  $V_{bb}$  protection
- Electrostatic discharge protection (ESD)

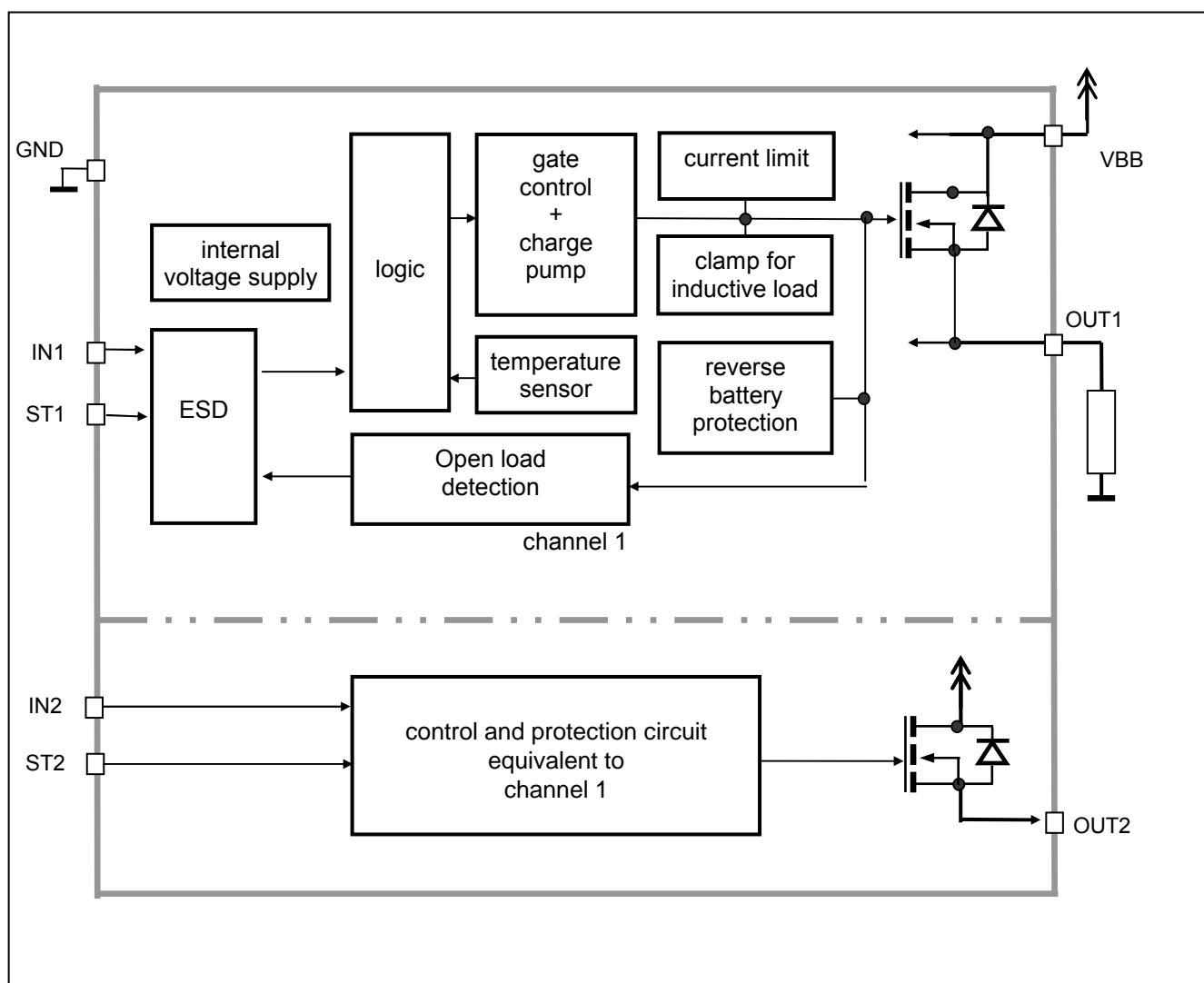
### Diagnostic Function

- Diagnostic feedback with open drain output
- Open load detection in OFF-state
- Feedback of thermal shutdown in ON-state

### Block Diagram



## Functional diagram

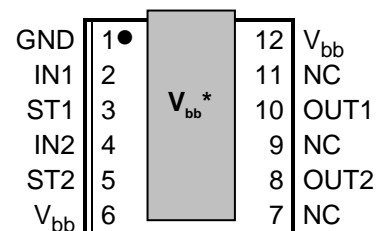


## Pin Definitions and Functions

Pin	Symbol	Function
1	GND	<b>Ground</b> of chip
2	IN1	<b>Input 1,2</b> activates channel 1,2 in case of logic high signal
4	IN2	
3	ST1	<b>Diagnostic feedback 1 &amp; 2</b> of channel 1,2 open drain, low on failure
5	ST2	
6,12, heat slug	$V_{bb}$	<b>Positive power supply voltage.</b> Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
7,9,11	NC	<b>Not Connected</b>
8	OUT2	<b>Output 1,2</b> protected high-side power output of channel 1 and 2. Design the wiring for the max. short circuit current
10	OUT1	

## Pin configuration

(top view)



\* heat slug

**Maximum Ratings** at  $T_j = 25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 6)	$V_{bb}$	43	V
Supply voltage for full short circuit protection $T_{j,start} = -40 \dots +150^\circ\text{C}$	$V_{bb}$	36	V
Load current (Short-circuit current, see page 6)	$I_L$	self-limited	A
Load dump protection <sup>1)</sup> $V_{LoadDump} = V_A + V_S$ , $V_A = 13.5\text{ V}$ $R_l^{2)} = 2\ \Omega$ , $t_d = 400\text{ ms}$ ; IN = low or high, each channel loaded with $R_L = 13.5\ \Omega$ ,	$V_{Load\ dump}^{3)}$	60	V
Operating temperature range	$T_j$	$-40 \dots +150$	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	$-55 \dots +150$	
Power dissipation (DC) <sup>4)</sup> $T_a = 25^\circ\text{C}$ : (all channels active) $T_a = 85^\circ\text{C}$ :	$P_{tot}$	3.1 1.6	W
Maximal switchable inductance, single pulse $V_{bb} = 12\text{V}$ , $T_{j,start} = 150^\circ\text{C}^{4)}$ , see diagrams on page 10 $I_L = 3.5\text{ A}$ , $E_{AS} = 178\text{ mJ}$ , $0\ \Omega$ one channel: $I_L = 7.0\text{ A}$ , $E_{AS} = 337\text{ mJ}$ , $0\ \Omega$ two parallel channels:	$Z_L$	21.3 10	mH
Electrostatic discharge capability (ESD) IN: (Human Body Model) ST: out to all other pins shorted: acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993 $R = 1.5\text{ k}\Omega$ ; $C = 100\text{ pF}$	$V_{ESD}$	1.0 4.0 8.0	kV
Input voltage (DC) see internal circuit diagram page 9	$V_{IN}$	$-10 \dots +16$	V
Current through input pin (DC)	$I_{IN}$	$\pm 0.3$	mA
Pulsed current through input pin <sup>5)</sup>	$I_{INp}$	$\pm 5.0$	
Current through status pin (DC)	$I_{ST}$	$\pm 5.0$	

1) Supply voltages higher than  $V_{bb(AZ)}$  require an external current limit for the GND and status pins (a  $150\ \Omega$  resistor for the GND connection is recommended).

2)  $R_l$  = internal resistance of the load dump test pulse generator

3)  $V_{Load\ dump}$  is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

4) Device on  $50\text{ mm} \times 50\text{ mm} \times 1.5\text{ mm}$  epoxy PCB FR4 with  $6\text{ cm}^2$  (one layer,  $70\ \mu\text{m}$  thick) copper area for  $V_{bb}$  connection. PCB is vertical without blown air. See page 14

5) only for testing



## Thermal Characteristics

Parameter and Conditions	Symbol	Values			Unit
		min	typ	max	
Thermal resistance junction - Case <sup>6)</sup> junction – ambient <sup>6)</sup> @ 6 cm <sup>2</sup> cooling area	each channel: $R_{thjC}$ $R_{thja}$ one channel active: all channels active:	-- -- -- --	-- -- 45 40	5 -- -- --	K/W

## Electrical Characteristics

Parameter and Conditions, each of the four channels at $T_j = -40...+150^{\circ}\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

## Load Switching Capabilities and Characteristics

On-state resistance ( $V_{bb}$ to OUT); $I_L = 2\text{ A}$ each channel, $T_j = 25^{\circ}\text{C}$ : $T_j = 150^{\circ}\text{C}$ : two parallel channels, $T_j = 25^{\circ}\text{C}$ : see diagram, page 11	$R_{ON}$	-- -- --	70 140 35	90 180 45	mΩ
Nominal load current one channel active: two parallel channels active: Device on PCB <sup>6)</sup> , $T_a = 85^{\circ}\text{C}$ , $T_j \leq 150^{\circ}\text{C}$	$I_{L(NOM)}$	3.7 7.4	4.7 9.5	--	A
Output current while GND disconnected or pulled up <sup>7)</sup> ; $V_{bb} = 32\text{ V}$ , $V_{IN} = 0$ , see diagram page 9	$I_{L(GNDhigh)}$	--	--	2	mA
Turn-on time <sup>8)</sup> IN  to 90% $V_{OUT}$ : Turn-off time IN  to 10% $V_{OUT}$ : $R_L = 12\text{ }\Omega$	$t_{on}$ $t_{off}$	-- --	100 100	250 270	μs
Slew rate on <sup>8)</sup> 10 to 30% $V_{OUT}$ , $R_L = 12\text{ }\Omega$ :	$dV/dt_{on}$	0.2	--	1.0	V/μs
Slew rate off <sup>8)</sup> 70 to 40% $V_{OUT}$ , $R_L = 12\text{ }\Omega$ :	$-dV/dt_{off}$	0.2	--	1.1	V/μs

<sup>6)</sup> Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70μm thick) copper area for  $V_{bb}$  connection. PCB is vertical without blown air. See page 14

<sup>7)</sup> not subject to production test, specified by design

<sup>8)</sup> See timing diagram on page 12.

Parameter and Conditions, each of the four channels at $T_j = -40...+150^{\circ}\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

### Operating Parameters

Operating voltage	$V_{bb(\text{on})}$	5.5	--	40	V
Undervoltage switch off <sup>9)</sup>	$T_j = -40^{\circ}\text{C}...25^{\circ}\text{C}$ : $V_{bb(\text{u so})}$	--	--	4.5	V
	$T_j = 125^{\circ}\text{C}$ :	--	--	4.5 <sup>10)</sup>	
Overvoltage protection <sup>11)</sup> $I_{bb} = 40\text{ mA}$	$V_{bb(\text{AZ})}$	41	47	52	V
Standby current <sup>12)</sup>	$T_j = -40^{\circ}\text{C}...25^{\circ}\text{C}$ : $I_{bb(\text{off})}$	--	4.5	10	$\mu\text{A}$
	$V_{IN} = 0$ ; see diagram page 11 $T_j = 150^{\circ}\text{C}$ :	--	--	15	
	$T_j = 125^{\circ}\text{C}$ :	--	--	10 <sup>10)</sup>	
Off-State output current (included in $I_{bb(\text{off})}$ ) $V_{IN} = 0$ ; each channel	$I_{L(\text{off})}$	--	1	5	$\mu\text{A}$
Operating current <sup>13)</sup> , $V_{IN} = 5\text{V}$ , one channel on: all channels on:	$I_{GND}$	-- --	0.6 1.2	1.2 2.4	mA

### Protection Functions<sup>14)</sup>

Current limit, $V_{out} = 0\text{V}$ , (see timing diagrams, page 12) $T_j = -40^{\circ}\text{C}$ : $T_j = 25^{\circ}\text{C}$ : $T_j = +150^{\circ}\text{C}$ :	$I_{L(\text{lim})}$	-- -- 9	-- 15 --	23 -- ----	A
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel two channels (see timing diagrams, page 12)	$I_{L(\text{SCR})}$	-- --	12 12	-- --	A
Initial short circuit shutdown time $T_{j,\text{start}} = 25^{\circ}\text{C}$ : $V_{out} = 0\text{V}$ (see timing diagrams on page 12)	$t_{\text{off}(\text{SC})}$	--	2	--	ms
Output clamp (inductive load switch off) <sup>15)</sup> at $V_{ON(\text{CL})} = V_{bb} - V_{OUT}$ , $I_L = 40\text{ mA}$	$V_{ON(\text{CL})}$	41	47	52	V
Thermal overload trip temperature	$T_{jt}$	150	--	--	$^{\circ}\text{C}$
Thermal hysteresis	$\Delta T_{jt}$	--	10	--	K

<sup>9)</sup> is the voltage, where the device doesn't change it's switching condition for 15ms after the supply voltage falling below the lower limit of  $V_{bb(\text{on})}$

<sup>10)</sup> not subject to production test, specified by design

<sup>11)</sup> Supply voltages higher than  $V_{bb(\text{AZ})}$  require an external current limit for the GND and status pins (a 150 $\Omega$  resistor for the GND connection is recommended). See also  $V_{ON(\text{CL})}$  in table of protection functions and circuit diagram on page 9.

<sup>12)</sup> Measured with load; for the whole device; all channels off

<sup>13)</sup> Add  $I_{ST}$ , if  $I_{ST} > 0$

<sup>14)</sup> Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

<sup>15)</sup> If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest  $V_{ON(\text{CL})}$

Parameter and Conditions, each of the four channels at $T_j = -40...+150^{\circ}\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	



### Reverse Battery

Reverse battery voltage <sup>16)</sup>	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ( $V_{out} > V_{bb}$ ) $I_L = -2.0\text{ A}$ , $T_j = +150^{\circ}\text{C}$	$-V_{ON}$	--	600	--	mV

### Diagnostic Characteristics

Open load detection voltage	$V_{OUT(OL)}$	1.7	2.8	4.0	V
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### Input and Status Feedback<sup>17)</sup>

Input resistance (see circuit page 9)	$R_i$	2.5	4.0	6.0	k $\Omega$
Input turn-on threshold voltage 	$V_{IN(T+)}$	--	--	2.5	V
Input turn-off threshold voltage 	$V_{IN(T-)}$	1.0	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.2	--	V
Status change after positive input slope <sup>18)</sup> with open load	$t_{d(STon)}$	--	10	20	$\mu\text{s}$
Status change after positive input slope <sup>18)</sup> with overload	$t_{d(STon)}$	30	--	--	$\mu\text{s}$
Status change after negative input slope with open load	$t_{d(SToff)}$	--	--	500	$\mu\text{s}$
Status change after negative input slope <sup>18)</sup> with overtemperature	$t_{d(SToff)}$	--	--	20	$\mu\text{s}$
Off state input current $V_{IN} = 0.4\text{ V}$ :	$I_{IN(off)}$	5	--	20	$\mu\text{A}$
On state input current $V_{IN} = 5\text{ V}$ :	$I_{IN(on)}$	10	35	60	$\mu\text{A}$
Status output (open drain)					
Zener limit voltage $I_{ST} = +1.6\text{ mA}$ :	$V_{ST(high)}$	5.4	--	--	V
ST low voltage $I_{ST} = +1.6\text{ mA}$ :	$V_{ST(low)}$	--	--	0.6	

<sup>16)</sup> Requires a 150  $\Omega$  resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 4 and circuit page 9).

<sup>17)</sup> If ground resistors  $R_{GND}$  are used, add the voltage drop across these resistors.

<sup>18)</sup> not subject to production test, specified by design

## Truth Table

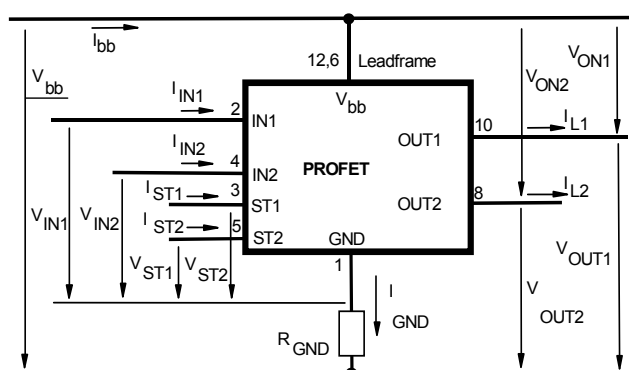
( each channel )

	IN	OUT	ST
Normal operation	L	L	H
	H	H	H
Open load	L	Z	L <sup>19)</sup>
	H	H	H
Overtemperature	L	L	H
	H	L	L

L = "Low" Level      X = don't care      Z = high impedance, potential depends on external circuit  
H = "High" Level      Status signal valid after the time delay shown in the timing diagrams

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel (see truth table). If switching channel 1 to 2 in parallel, the status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

## Terms



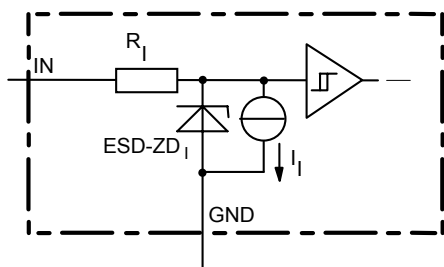
Leadframe ( $V_{bb}$ ) is connected to pin 6,12

External  $R_{GND}$  optional; single resistor  $R_{GND} = 150 \Omega$  for reverse battery protection up to the max. operating voltage.

<sup>19)</sup> L, if potential at the Output exceeds the OpenLoad detection voltage

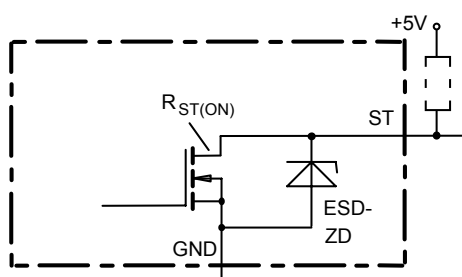


### Input circuit (ESD protection), IN1 or IN2



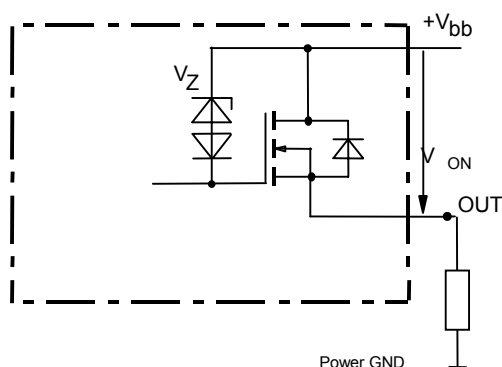
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

### Status output, ST1 or ST2



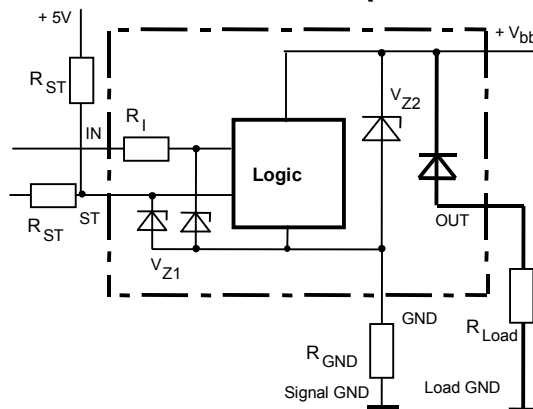
ESD-Zener diode: 6.1 V typ., max 0.3 mA;  $R_{ST(ON)} < 375 \Omega$  at 1.6 mA. The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

### Inductive and overvoltage output clamp, OUT1 or OUT2



$V_{ON}$  clamped to  $V_{ON(CL)} = 47 \text{ V typ.}$

### Overvolt. and reverse batt. protection



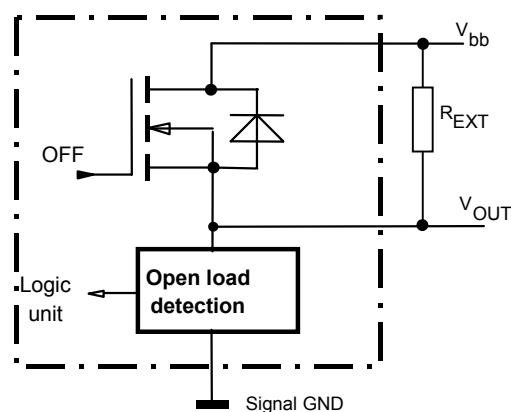
$V_{Z1} = 6.1 \text{ V typ.}$ ,  $V_{Z2} = 47 \text{ V typ.}$ ,  $R_{GND} = 150 \Omega$ ,  $R_{ST} = 15 \text{ k}\Omega$ ,  $R_I = 3.5 \text{ k}\Omega \text{ typ.}$

In case of reverse battery the load current has to be limited by the load. Temperature protection is not active

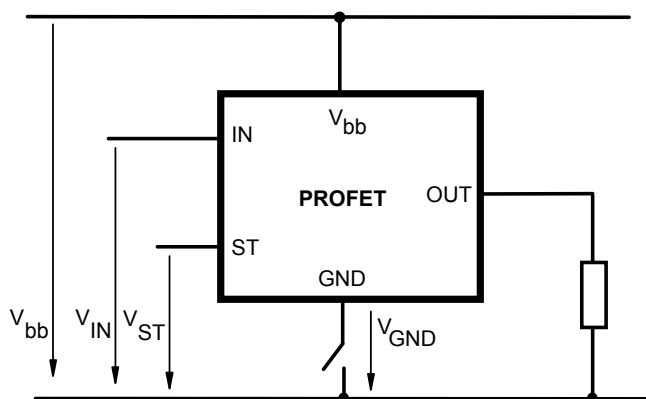
### Open-load detection, OUT1 or OUT2

OFF-state diagnostic condition:

Open Load, if  $V_{OUT} > 3 \text{ V typ.}$ ; IN low

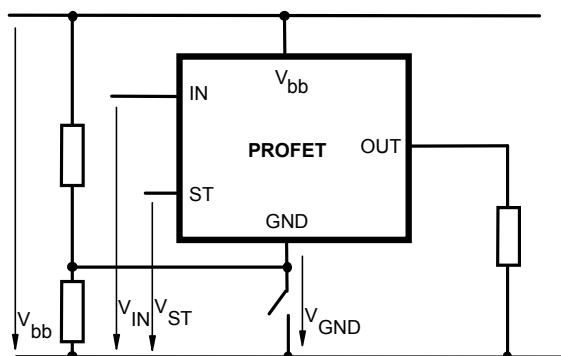


### GND disconnect



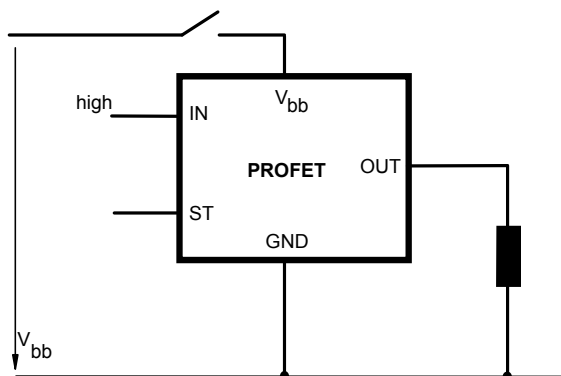
Any kind of load. In case of IN=high is  $V_{OUT} \approx V_{IN} - V_{IN(T+)}$ . Due to  $V_{GND} > 0$ , no  $V_{ST} = \text{low}$  signal available.

### GND disconnect with GND pull up



Any kind of load. If  $V_{GND} > V_{IN} - V_{IN(T+)}$  device stays off  
Due to  $V_{GND} > 0$ , no  $V_{ST}$  = low signal available.

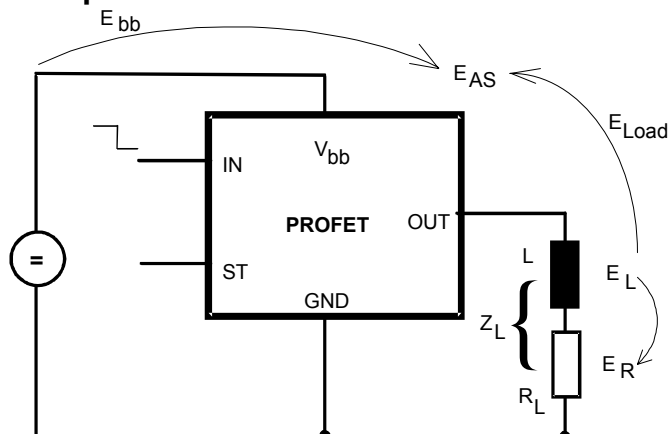
### Vbb disconnect with energized inductive load



For inductive load currents up to the limits defined by  $Z_L$  (max. ratings and diagram on page 10) each switch is protected against loss of  $V_{bb}$ .

Consider at your PCB layout that in the case of  $V_{bb}$  disconnection with energized inductive load all the load current flows through the GND connection.

### Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = \frac{1}{2} \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

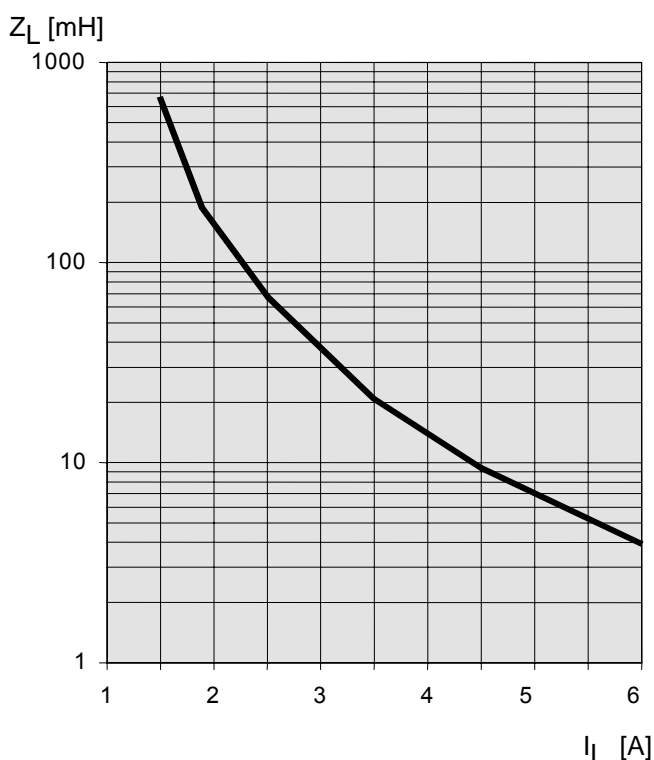
$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \cdot i_L(t) dt,$$

with an approximate solution for  $R_L > 0 \Omega$ :

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left( 1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

### Maximum allowable load inductance for a single switch off (one channel)<sup>4)</sup>

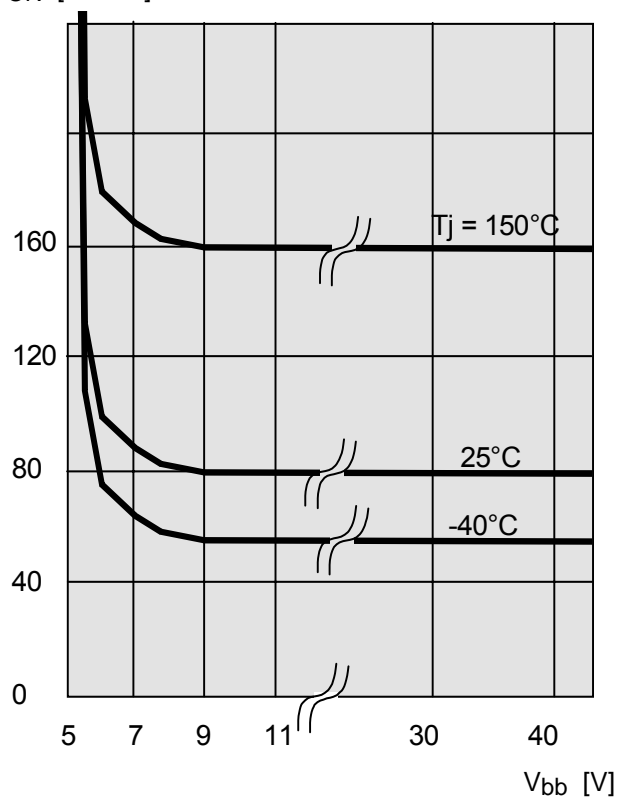
$L = f(I_L)$ ;  $T_{j,start} = 150^\circ\text{C}$ ,  $V_{bb} = 12\text{ V}$ ,  $R_L = 0 \Omega$



### Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j)$ ;  $I_L = 2\text{ A}$ ,  $I_N = \text{high}$

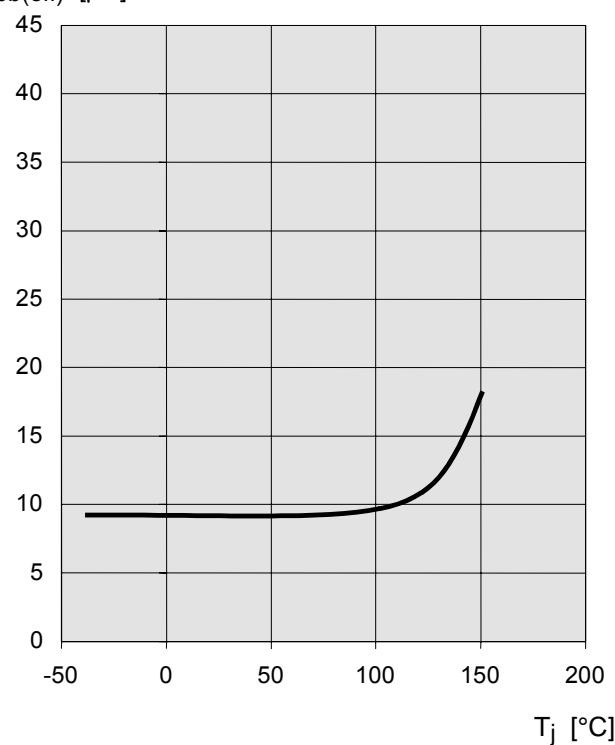
$R_{ON}$  [mOhm]



### Typ. standby current

$I_{bb(off)} = f(T_j)$ ;  $V_{bb} = 9 \dots 34\text{ V}$ ,  $I_{N1,2} = \text{low}$

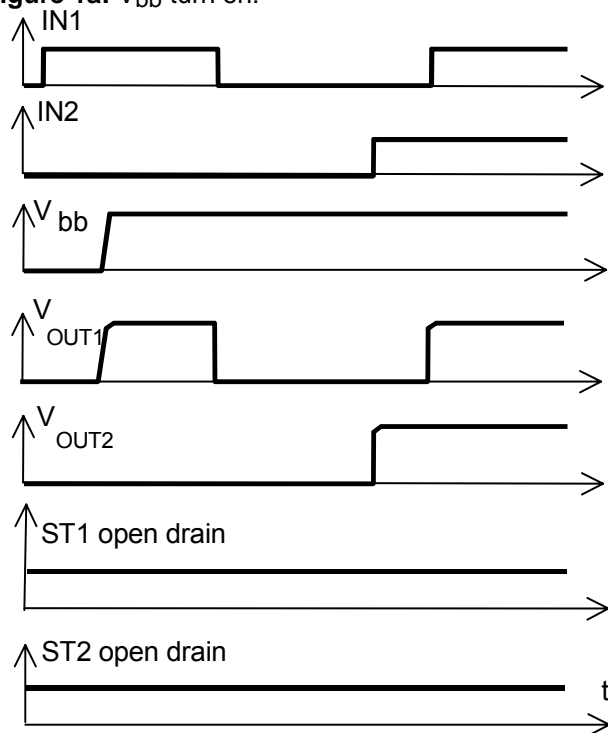
$I_{bb(off)}$  [ $\mu\text{A}$ ]



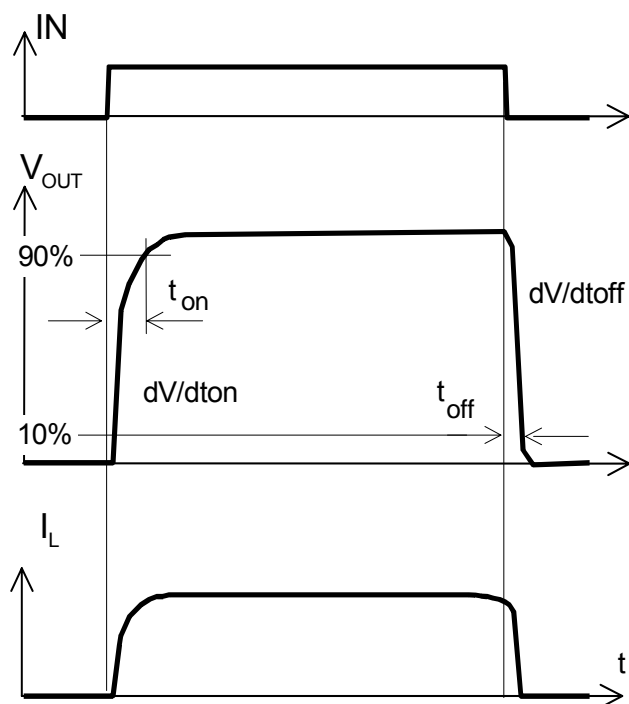
## Timing diagrams

All channels are symmetric and consequently the diagrams are valid for channel 1 to channel 4

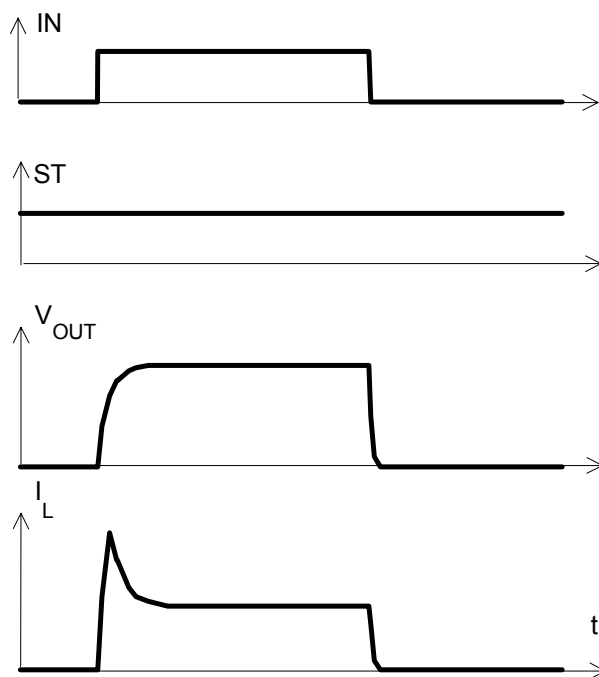
**Figure 1a:**  $V_{bb}$  turn on:



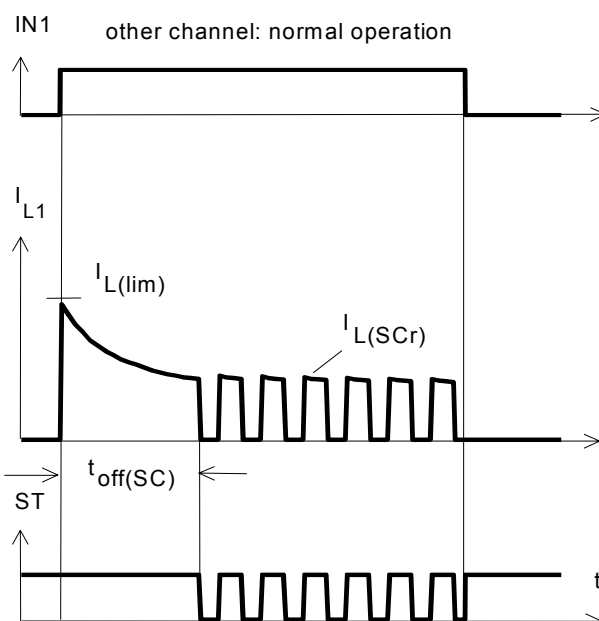
**Figure 2a:** Switching a resistive load, turn-on/off time and slew rate definition:



**Figure 2b:** Switching a lamp:

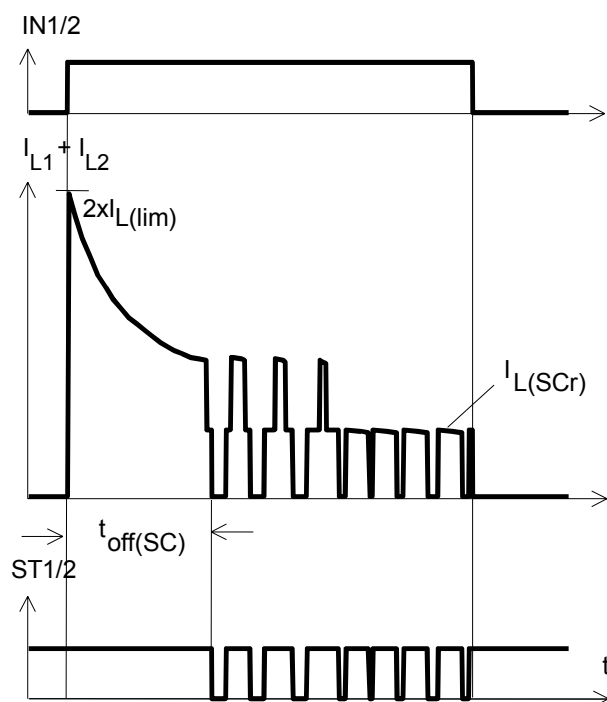


**Figure 3a:** Turn on into short circuit: shut down by overtemperature, restart by cooling



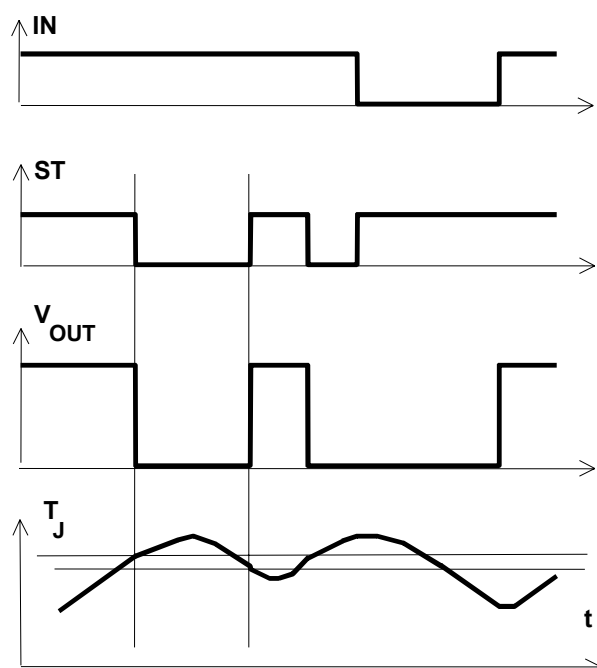
Heating up of the chip may require several milliseconds, depending on external conditions

**Figure 3b:** Turn on into short circuit:  
shut down by overtemperature, restart by cooling  
(two parallel switched channels 1 and 2)

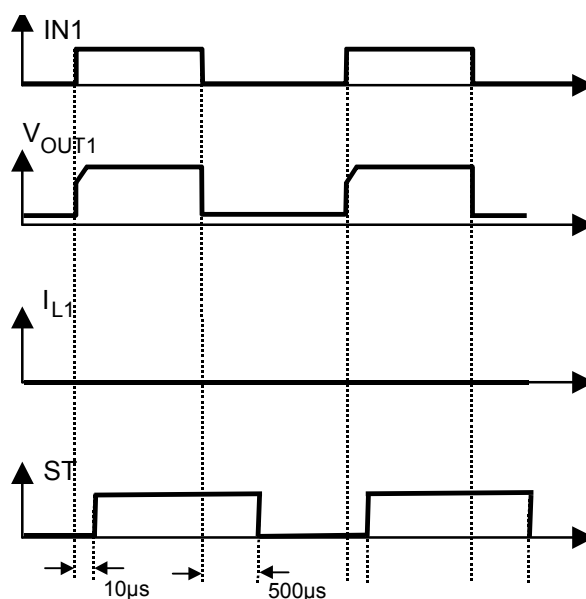


ST1 and ST2 have to be configured as a 'Wired OR' function  
ST1/2 with a single pull-up resistor.

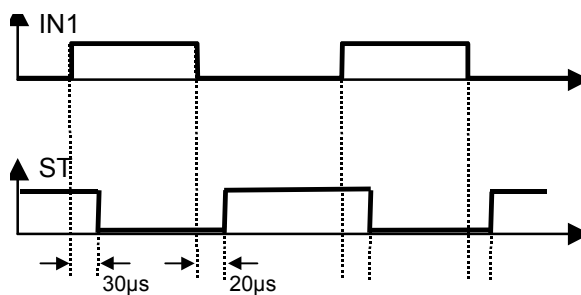
**Figure 4a:** Overtemperature:  
Reset if  $T_j < T_{jt}$



**Figure 5a:** Open load: detection in OFF-state, turn  
on/off to open load  
Open load of channel 1; other channels normal  
operation



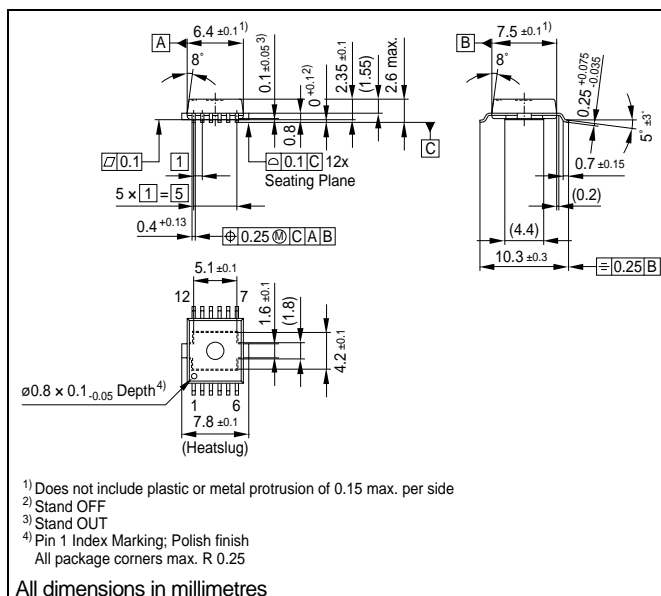
**Figure 6a:** Status change after, turn on/off to  
overtemperature  
Overtemperature of channel 1; other channels normal  
operation



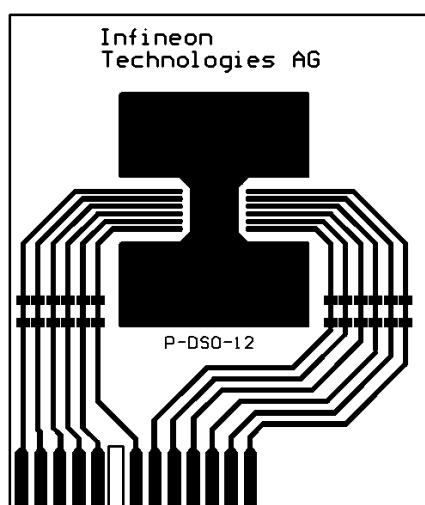
### Package and Ordering Code

**Standard: P-DSO-12-2**

Sales Code	BTS 5215L
Ordering Code	Q67060-S7023



Printed circuit board (FR4, 1.5mm thick, one layer 70 $\mu$ m, 6cm<sup>2</sup> active heatsink area) as a reference for max. power dissipation  $P_{tot}$ , nominal load current  $I_{L(NOM)}$  and thermal resistance  $R_{thja}$



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## Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

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