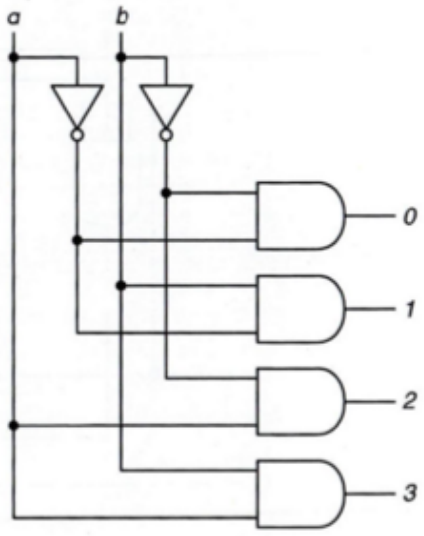
표 4.2a 활성-1 디코더 진리표

a	*b*	*0*	*1*	*2*	*3*
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

그림 4.8a 활성-1 디코더

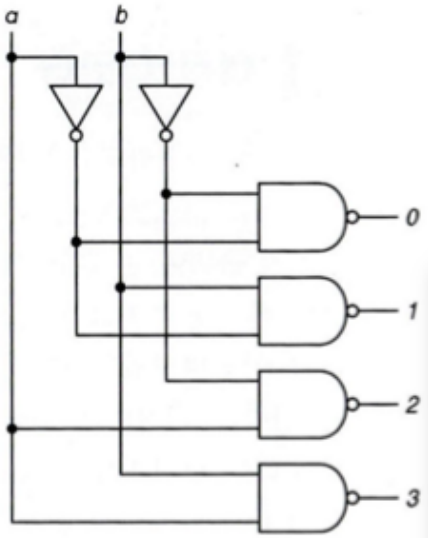


active high

표 4.2b 활성-0 디코더 진리표

a	*b*	*0*	*1*	*2*	*3*
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

그림 4.8b 활성-0 디코더



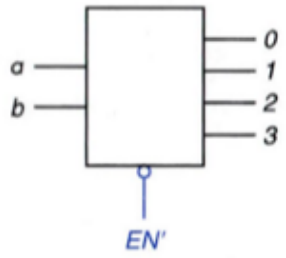
active low

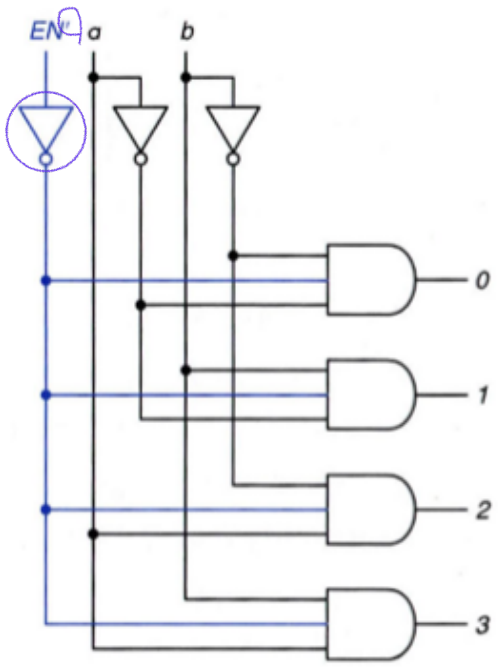
그림 4.9 enable 신호를 가지는 디코더

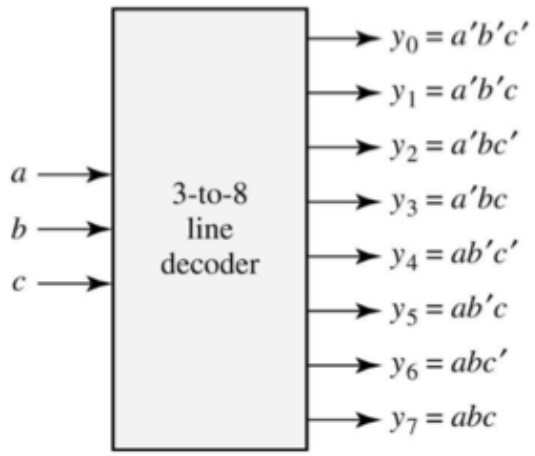
EN'	*a*	*b*	*0*	*1*	*2*	*3*
1	X	X	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

활성 1 출력

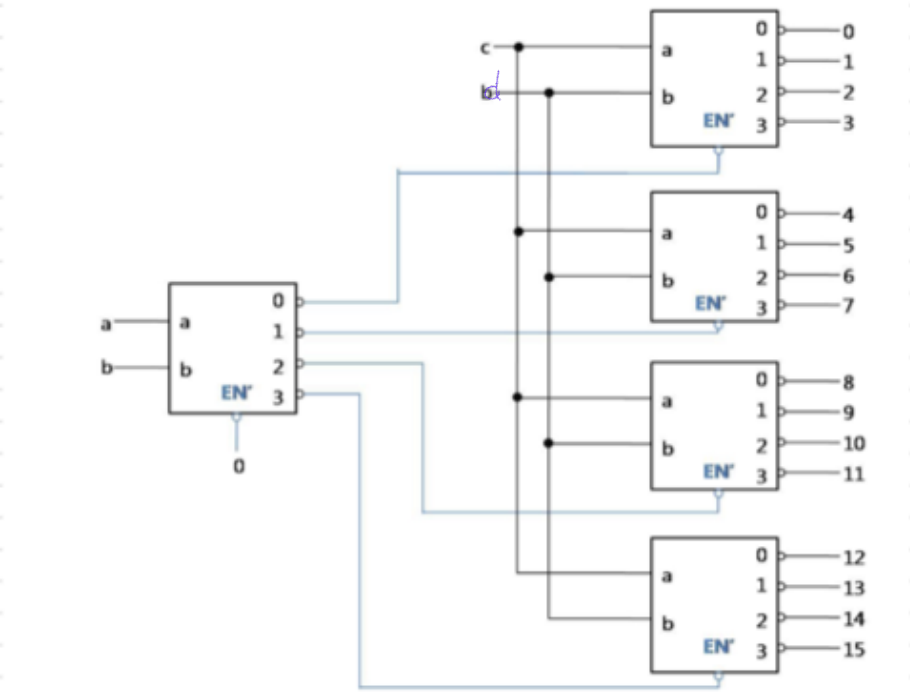
활성 0 enable





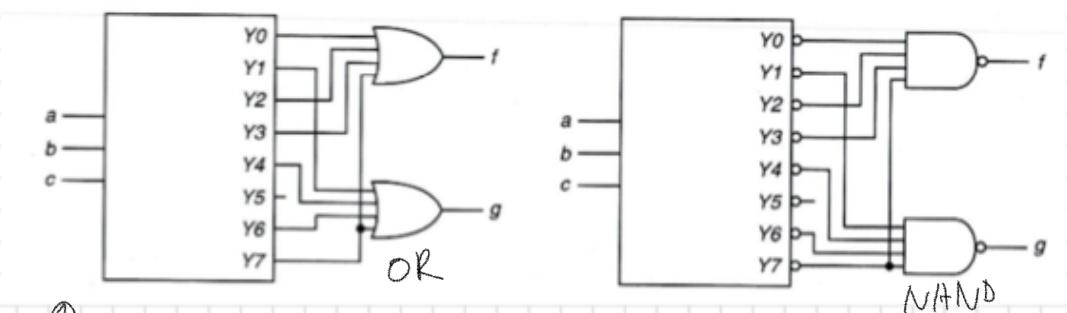


a	b	c	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1



└ active low 2-to-4 decoder 사용해 4 to 16 decoder

※ 디코더 이용 논리함수 구현



↑
한개 1 출력 = minterm

한개 0

$f = \Sigma m(0, 2, 3, 7)$

$g = \Sigma m(1, 4, 6, 7)$

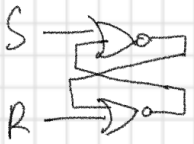
* Flip-flops

review $y = \begin{cases} G(Q, x) \rightarrow \text{Mandy} \\ G(Q) \rightarrow \text{Moore} \end{cases}$

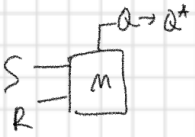
Sequential Circuit $\begin{cases} \text{Synchronous} & \text{using F/F} \\ \text{asynchronous} & \text{; no clock} \end{cases}$

A flip-flop is a binary cell capable of storing 1-bit information.
A flip-flop maintains a binary state until directed by clock pulse.

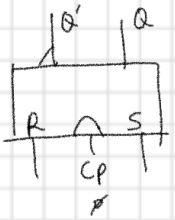
① basic latch



S	R	Q^*
0	0	Q
0	1	0
1	0	1
1	1	X



② SR flip-flop



Graphic symbol

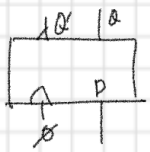
S	R	Q^*	Comments
0	0	Q	no change
0	1	0	clear
1	0	1	set
1	1	?	not allowed

characteristic table

Q	Q^*	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

excitation table

③ D flip-flop



D	Q^*	Comments
0	0	clear
1	1	set

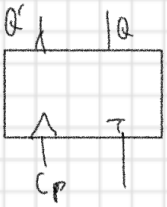
Q	Q^*	D
0	0	0
0	1	1
1	0	0
1	1	1

④ JK Flip-flop

J	K	Q^*	Comment
0	0	Q	no change
0	1	0	clear
1	0	1	Set
1	1	Q'	complement

Q	Q^*	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

⑤ T-flip flop



T	Q^*	Comments
0	Q	No change
1	Q'	Complement

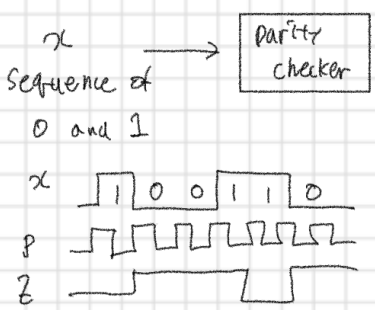
Q	Q^*	T
0	0	0
0	1	1
1	0	1
1	1	0

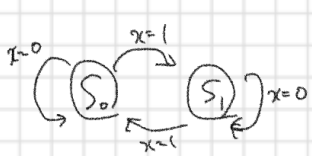
Parity Checker

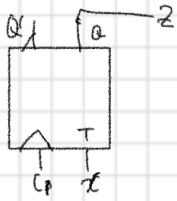
0 0 1 0 0 0 1 | 1

7-bit | parity bit

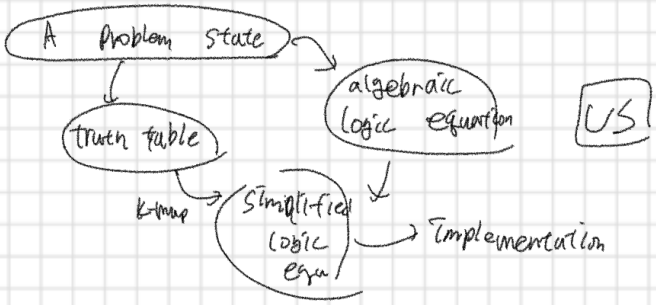
# of 1's even → 0
odd → 1





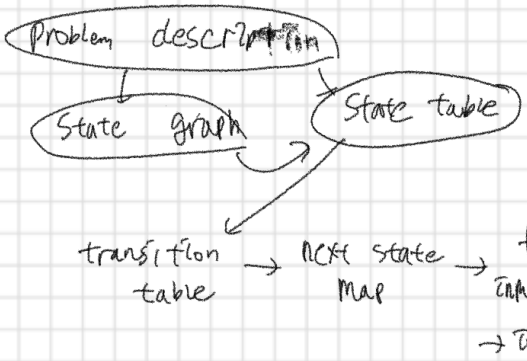


* Combinational Circuits Design



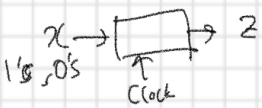
US

* Sequential Circuit Design



* Finite State Machine EX

"Sequence" Detector

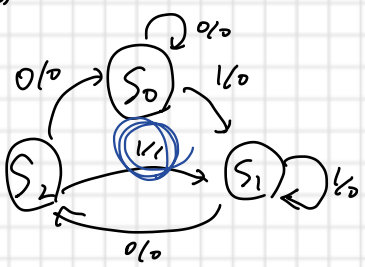


Any input sequence ending in 101 will produce an output z=1

x= 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0

z= 0 0 0 0 0 1 0 0 1 0 1 0 0

① State graph : we are looking for 101



3 States < 4

2 FFs are needed

② State Table

Current State	next state x=0	next state x=1	output x=0	output x=1
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

③ State assignment

$S_0 \rightarrow 0\,0$

$S_1 \rightarrow 0\,1$

$S_2 \rightarrow \underset{\text{A B}}{1\,0}$

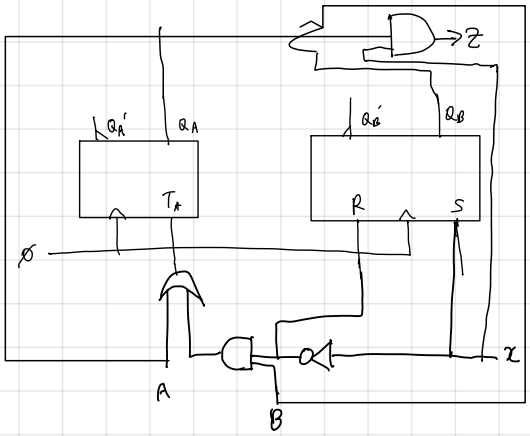
(T) (SR)

④ FFs Input detection

A	B	x	A^*	B^*	z	T_A	R_A	S_B
0	0	0	0	0	0	0	X	0
0	0	1	0	1	0	0	0	1
0	1	0	1	0	0	1	1	0
0	1	1	0	1	0	0	0	X
1	0	0	0	0	0	1	X	0
1	0	1	0	1	1	1	0	1

AB \ x	0	1
00		
01		
11	X	X
10		1

$z = Ax$



AB \ x	0	1
00	0	0
01	1	0
11	X	X
10	1	1

$T_A = A + x'B$

AB \ x	0	1
00	X	0
01	1	0
11	X	X
10	X	0

$R_B = x'$

AB \ x	0	1
00	0	1
01	0	X
11	X	X
10	0	1

$S_B = x$

Design Example

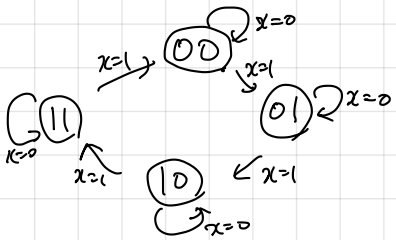
Design a clocked sequential circuit that goes through a sequential circuit that goes through a sequence of repeated binary states

00, 01, 10, 11 when x=1 the state of circuit

unchanged when x=0

0 → 1 → 2 → 3 → 0 → 1

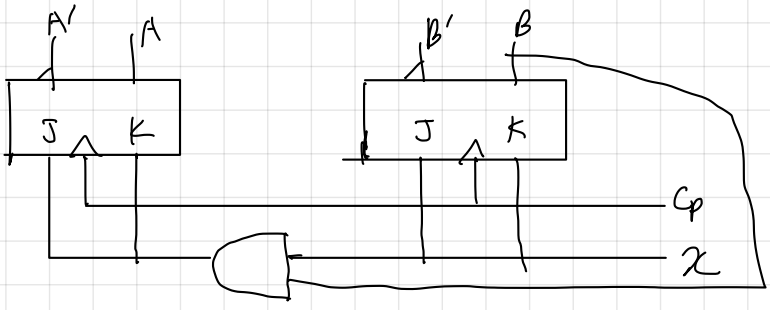
x=1 to count



J	K	Q^*
0	0	Q
0	1	0
1	0	1
1	1	Q'

2 JK Flipflop

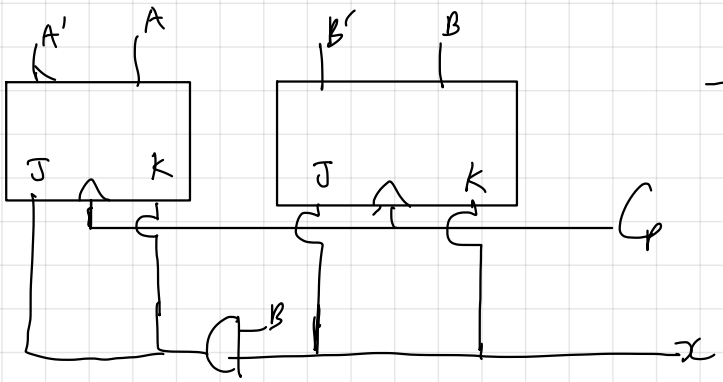
A	B	x	A^*	B^*	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	0	1	0	X	X	0
0	1	1	1	0	1	X	X	1
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1



↑ 11/20

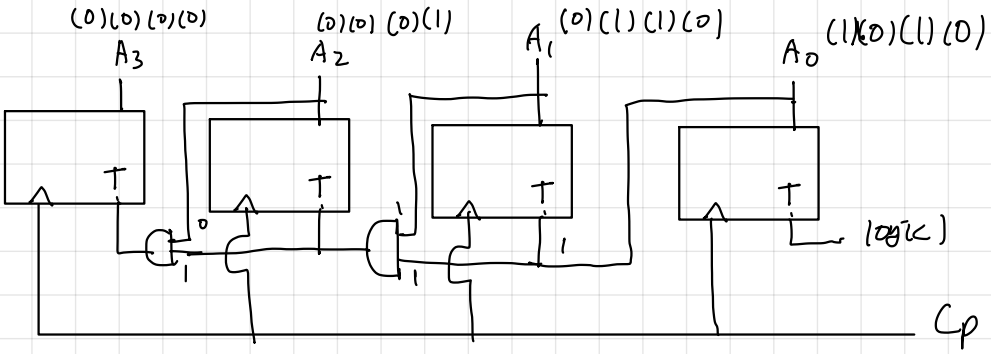
↓11/22

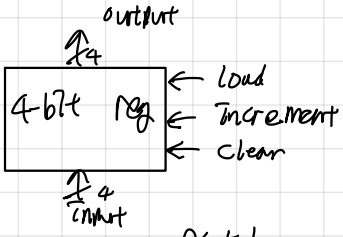
2.



→ (0, 0)
(0, 1)
(1, 0)
(1, 0)
(1, 1)
(0, 0)

Synchronous Counter



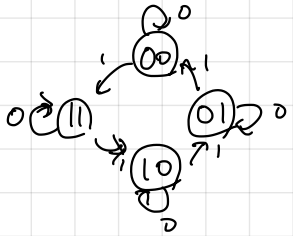


PC+1

(0000) → (0001) → (0010) → (0011) → (0100)

※ Design a two-bit Counter

when x=0 States do not change
when x=1 the sequence is
11, 10, 01, 00, 11 - ... and so on



JK | Q*	Q Q* | J K
char	필요 안

A	B	x	A*	B*	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	1	1	1	X	1	X
0	1	0	0	1	0	X	X	0
0	1	1	0	0	0	X	X	1
1	0	0	1	0	X	0	0	X
1	0	1	0	1	X	1	1	X
1	1	0	1	1	X	0	X	0
1	1	1	1	0	X	0	X	1

$J_A = Bx$ $K_A = B'x$

$J_B = x$ $K_B = x$

0 → 3 → 5 → 2 → 9 → 11 → 10