Zhiwei Zhong

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EDUCATION

Northwestern University, Evanston, USA Sept. 2021 – Present
Ph.D in Electrical and Computer Engineering (GPA: 3.84/4), expected Jun. 2026

Southeast University, Nanjing, China Sept. 2018 – Jun. 2021
M.E. in Information and Communication Engineering (GPA: 85.7/100)

Southeast University, Nanjing, China Sept. 2014 – Jun 2018
B.E. in Information Science and Engineering (GPA: 3.8/4)

RESEARCH INTERESTS

- Low-power SoC with machine learning (ML) for human-machine interface
- Physics-informed AI/ML in embedded systems
- VLSI design and ML optimization for digital communication

AWARDS

- Design Contest Award of ACM International Symposium on Low Power Electronics and Design. *2024*
- Second Place in the University Demo at the ACM/IEEE 61st Design Automation Conference. *2024*
- Highlight paper of IEEE Transactions on Circuits and Systems I. *2020*
- Silver Award of International Genetically Engineered Machine Competition, USA. *2019*

RESEARCH EXPERIENCE

Physics-Embedded Neural Network for Robot Control Northwestern University
Research Assistant *2021 – present*

- Developed an enhanced physics-embedded neural network for real-time robotic control in embedded systems. Implemented a Lagrangian neural network to extract hidden robot states and utilized a reinforcement learning-based agent for architectural optimization. Achieve 95% error reduction and 3X speed-up. (*MWSCAS'24*)
- Related publications: [C1] .

VLSI Design in Bio Systems Northwestern University
Research Assistant *2021 – present*

- Developed low-power SoC for brain computer interface (BCI) in VR/AR applications. Integrated with Teacher-Student CNN scheme with 55% energy saving and Instruction-based reconfigurable architecture for various BCI tasks. (*ISSCC'24*) [Demo Video]
- Developed human emotion based hardware system management on resource-limited edge devices. An affect-driven adaptive hardware video decoder was proposed achieving up to 23% power saving. (*DAC'22*)
- Related publications: [C2], [C3]

VLSI Design in Communication Systems Southeast University
Research Assistant *2018 – 2020*

- Developed a compiler to automatically generate target 5G polar encoders in Verilog HDL files, given code length, parallelism level, and stage number. The compiler is based on uniform formula representations of pipelined or stage-folded polar encoders. (*TCAS-I'20 Highlight Paper*)
- Developed a flexible permutation network for LDPC decoders and implemented it on ASIC, which increases throughput by 100% and clock frequency by 28% compared with the existing work. (*TCAS-II'20*)
- Related publications: [J1], [J2], [C4].

Deep Learning in Communication Systems Southeast University
Research Assistant *2017 – 2018*

- Applied gradient descent algorithm to accelerate convergence and improve the error-correction performance of the message passing detection algorithm in MIMO detection. (*GlobalSIP'18*)
- Applied convolutional neural networks as channel equalizer to recover transmitted signals from channel impairments: noise, inter-symbol interference, and non-linear distortion. (*ISWCS'18*)
- Related publications: [C5], [C6].

TECHNICAL SKILLS

Programming Languages: Python, PyTorch, Verilog, VHDL, C/C++

Software Tools: Cadence (Xcelium, Genus, Innovus, Virtuoso), CUDA, Arduino, Unity, MATLAB, Quartus, Xilinx Vivado

SELECTED PUBLICATIONS

Google Scholar

Journal

[J1] **Zhiwei Zhong**, Yongming Huang, Zaichen Zhang, Xiaohu You, and Chuan Zhang. "A flexible and high parallel permutation network for 5G LDPC decoders". *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)*, 2020.

[J2] **Zhiwei Zhong**, Warren J. Gross, Zaichen Zhang, Xiaohu You, and Chuan Zhang. "Polar compiler: auto-generator of hardware architectures for polar encoders". *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)*, 2020.

Conference

[C1] **Zhiwei Zhong**, Yuhao Ju, and Jie Gu. "Scalable Physics-Embedded Neural Networks for Real-Time Robotic Control in Embedded Systems". *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, Aug. 2024.

[C2] **Zhiwei Zhong***, Yijie Wei*, Lance Go, Jie Gu. "A Sub 1 uJ/class headset-integrated mind imagery and control SoC for VR/MR applications with teacher-student CNN and general-purpose instruction set architecture". *IEEE International Solid-State Circuits Conference (ISSCC)*. 2024. (∗Both authors contributed equally to this work)

[C3] Yijie Wei, **Zhiwei Zhong**, Jie Gu. "Human emotion based real-time memory and computation management on resource-limited edge devices". *Proceedings of the 59th ACM/IEEE Design Automation Conference (DAC)*, San Francisco, USA, Jul. 2022.

[C4] **Zhiwei Zhong**, Xiaohu You, and Chuan Zhang. "Auto-generation of pipelined hardware designs for polar encoder". *China Semiconductor Technology International Conference (CSTIC)*, Shanghai, China, March 2018.

[C5] Xiaosi Tan, **Zhiwei Zhong**, Zaichen Zhang, Xiaohu You, and Chuan Zhang. "Low-Complexity message passing MIMO detection algorithm with deep neural network". *IEEE Global Conference on Signal and Information Processing (GlobalSIP)*, Anaheim, USA, Nov. 2018.

[C6] Weihong Xu, **Zhiwei Zhong**, Yair Be'ery, Xiaohu You, and Chuan Zhang. "Joint neural network equalizer and decoder". *International Symposium on Wireless Communication Systems (ISWCS)*, Lisbon, Portugal, Aug. 2018.

PROFESSIONAL SERVICE

Reviewer: IEEE Journal of Solid-State Circuits. *2024*
Reviewer: ACM/IEEE International Conference on Computer-Aided Design. *2024*
Reviewer: IEEE Computer Society Annual Symposium on VLSI. *2024*