中国科学技术大学计算机学院

《数字电路实验》报告

实验题目：信号处理及有限状态机

学生姓名：张展翔

学生学号：PB20111669

完成日期：2021.12.16

计算机实验教学中心制

2020 年 09 月

【实验题目】

信号处理及有限状态机

【实验目的】

进一步熟悉 FPGA 开发的整体流程

掌握几种常见的信号处理技巧

掌握有限状态机的设计方法

能够使用有限状态机设计功能电路

【实验环境】

VLAB：vlab.ustc.eud.cn

FPGAOL:fpgaol.ustc.edu.cn

Logisim

Vivado

【实验练习】

题目 1

更改后的代码如下：

```
module test(
input clk,rst,
output led);
parameter C_0 = 2b'00;
parameter C_1 = 2b'01;
parameter C_2 = 2b'10;
parameter C_3 = 2b'11;
```

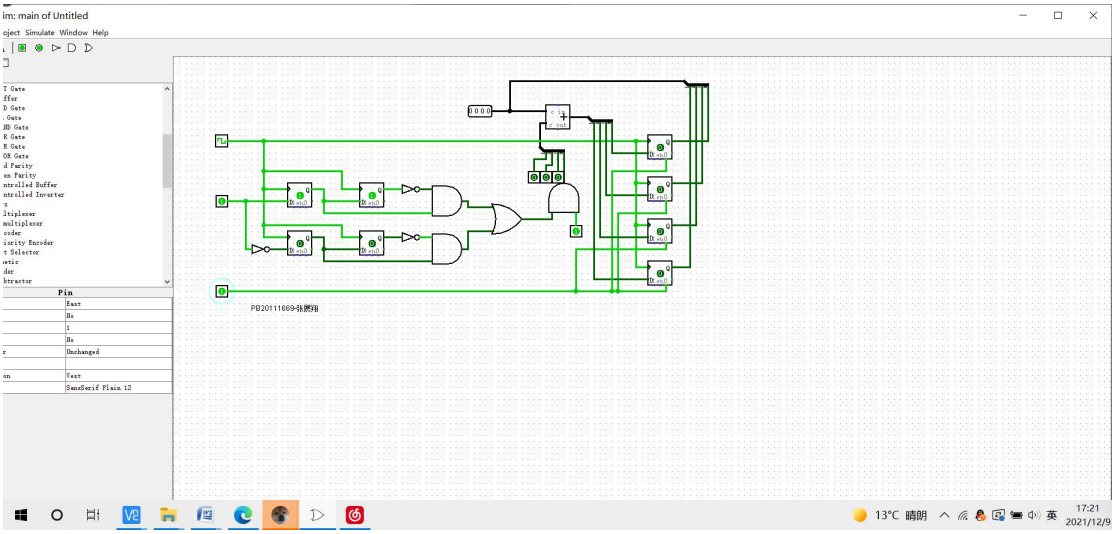
```
reg [1:0] cur;
reg [1:0] nex;
//part1
always@(*)
    begin
        case(cur)
        C_0: nex = C_1;
        C_1: nex = C_2;
        C_2: nex = C_3;
        C_3: nex = C_0;
        default: nex = C_0;
        endcase
    end
//part2
always@(posedge clk or posedge rst)
    begin
        if(rst)
            cur<=C_0;
        else
            cur<=nex;
    end
//part3
```

```
assign led = (cur == C_3)?1'b0:1'b1;

endmodule
```

题目 2

设计的计数器电路如下图所示



题目 3

设计文件如下所示：

```
module counter(
    input clk,rst,
    input sw,button,
    output reg [3:0] hexplay_data,
    output reg [2:0] hexplay_an
    );
    reg [7:0] data = 8'h1f;
    reg [32:0] hexplay_cnt;
    wire button_edge;
    reg [3:0]button_cnt;
```

```
    wire button_clean;
always@(posedge clk)begin
    if(button==1'b0)
        button_cnt <= 4'h0;
    else if(button_cnt<4'h8)
        button_cnt <= button_cnt + 1'b1;
end
assign button_clean = button_cnt[3];
always@(posedge clk) begin
    if (hexplay_cnt >= (2000000 / 8))
        hexplay_cnt <= 0;
    else
        hexplay_cnt <= hexplay_cnt + 1;
end
always@(posedge clk) begin
    if (hexplay_cnt == 0)begin
        if (hexplay_an == 1)
            hexplay_an <= 0;
        else
            hexplay_an <= hexplay_an + 1;
    end
end
```

```
always@(*) begin
    case(hexplay_an)
        0: hexplay_data <= data[3:0];
        1: hexplay_data <= data[7:4];
    endcase
end
cal_edge
cal_edge_1(.clk(clk),.button(button_clean),.button_edge(but
ton_edge));
always@(posedge clk) begin
    if (rst == 0) begin
        if(button_edge == 1) begin
            if (sw == 0) begin
                data <= data - 1;
            end
            else begin
                data <= data + 1;
            end
        end
    end
    else
        data <= 8'h1f;
```

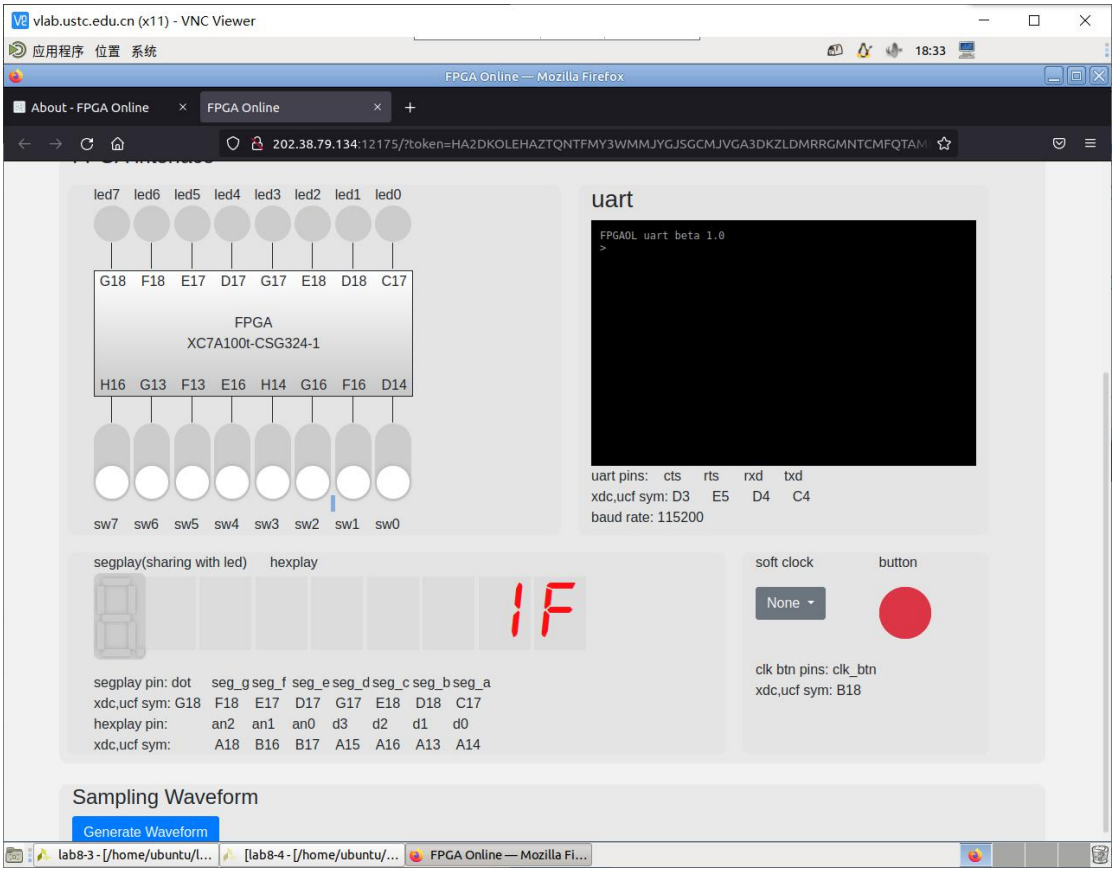
```
end
endmodule
module cal_edge (
    input button,clk,
    output button_edge
);
reg button_1,button_2;
always@(posedge clk)
    button_1 <= button;
always@(posedge clk)
    button_2 <= button_1;
assign button_edge = button_1 &(~button_2);
endmodule
```

xdc 约束文件如下：

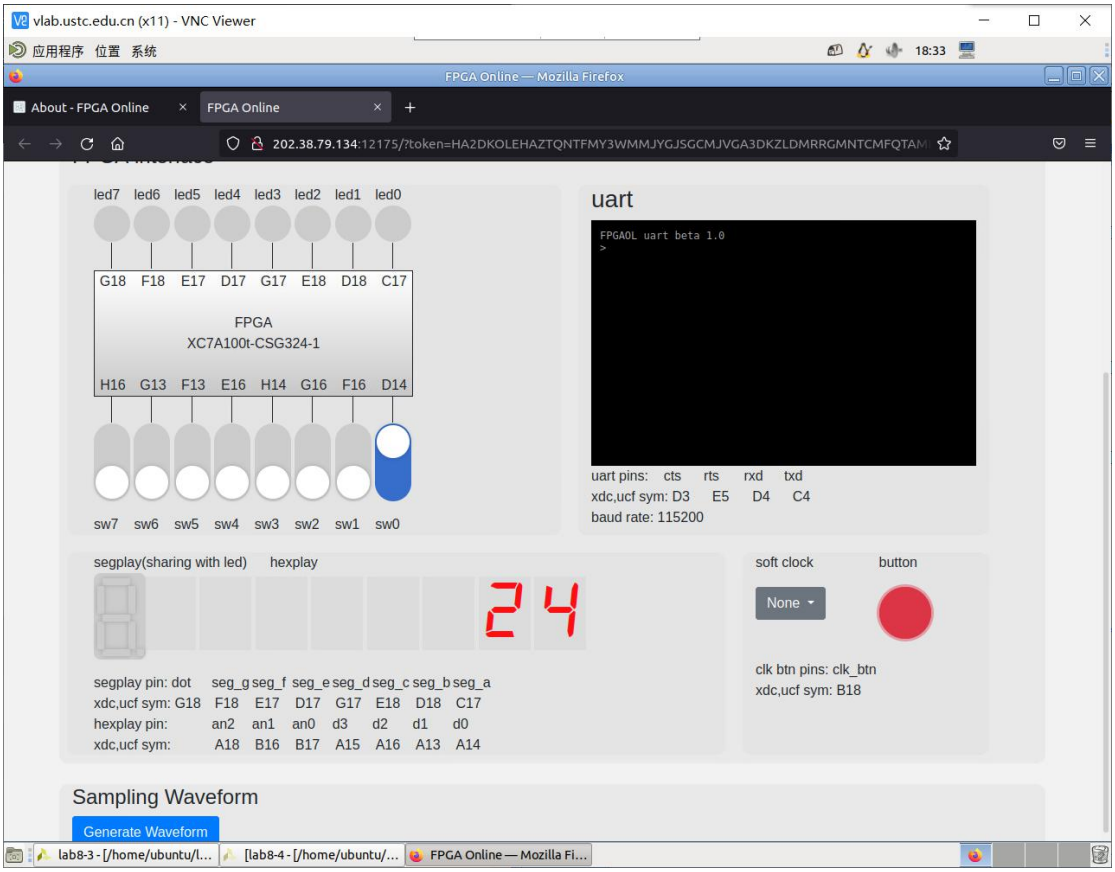
```
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 }
[get_ports {clk}]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 }
[get_ports { sw }];
set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[0] }];
set_property -dict { PACKAGE_PIN A13   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[1] }];
```

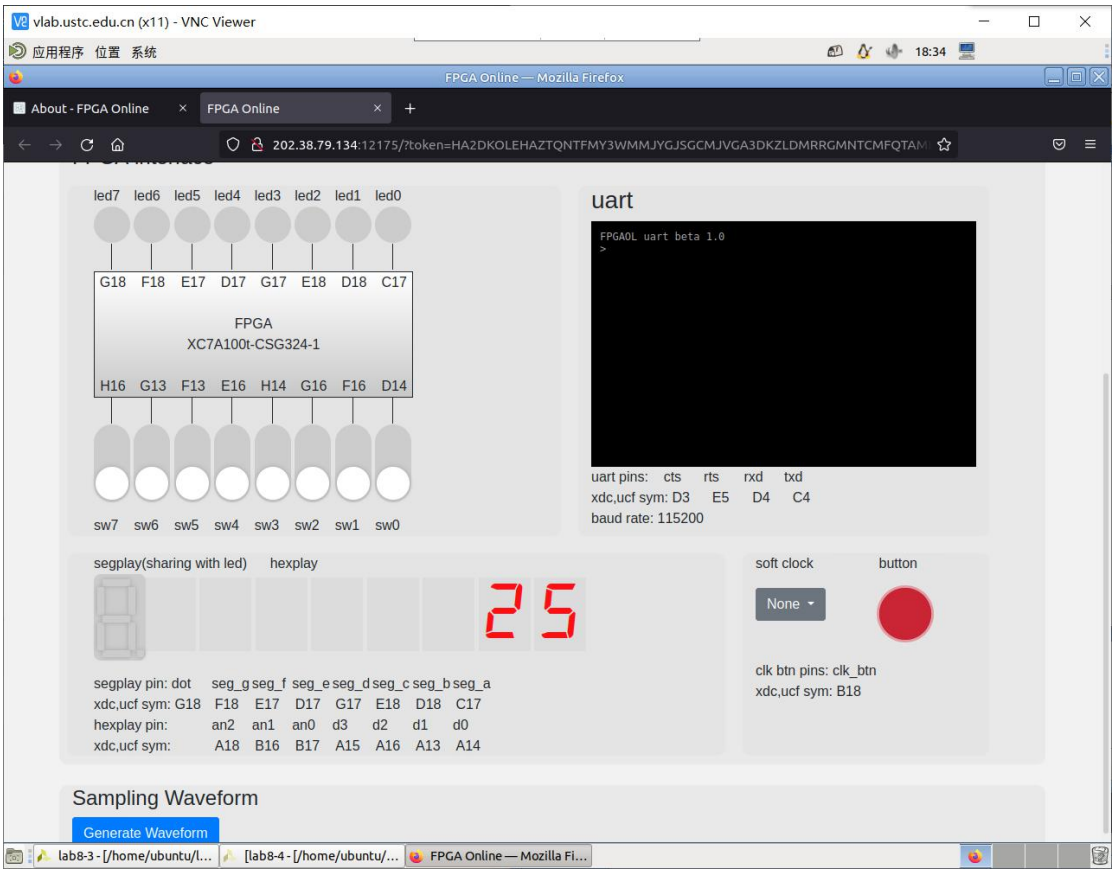
```
set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[2] }];
set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[3] }];
set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_an[0] }];
set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_an[1] }];
set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_an[2] }];
## FPGAOL BUTTON & SOFT_CLOCK
set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 }
[get_ports { button }];
set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 }
[get_ports { rst }];
```

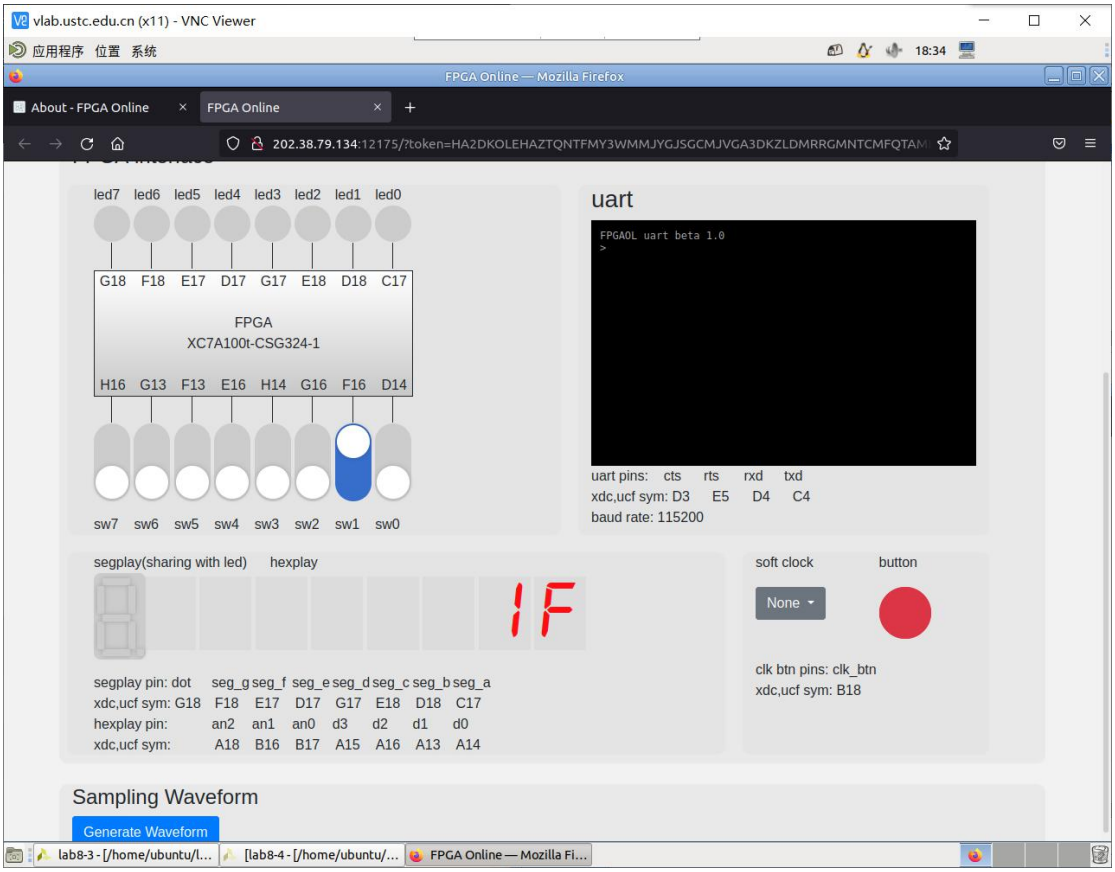
将其生成.bit 文件后传至 FPGA 平台烧写，得到以下的界面



当按下开关 sw0 时，点击按钮，每次 led 的数值加 1；关闭开关 sw0 时，点击按钮，每次 led 的数值减 1；打开 sw1 开关则进行复位

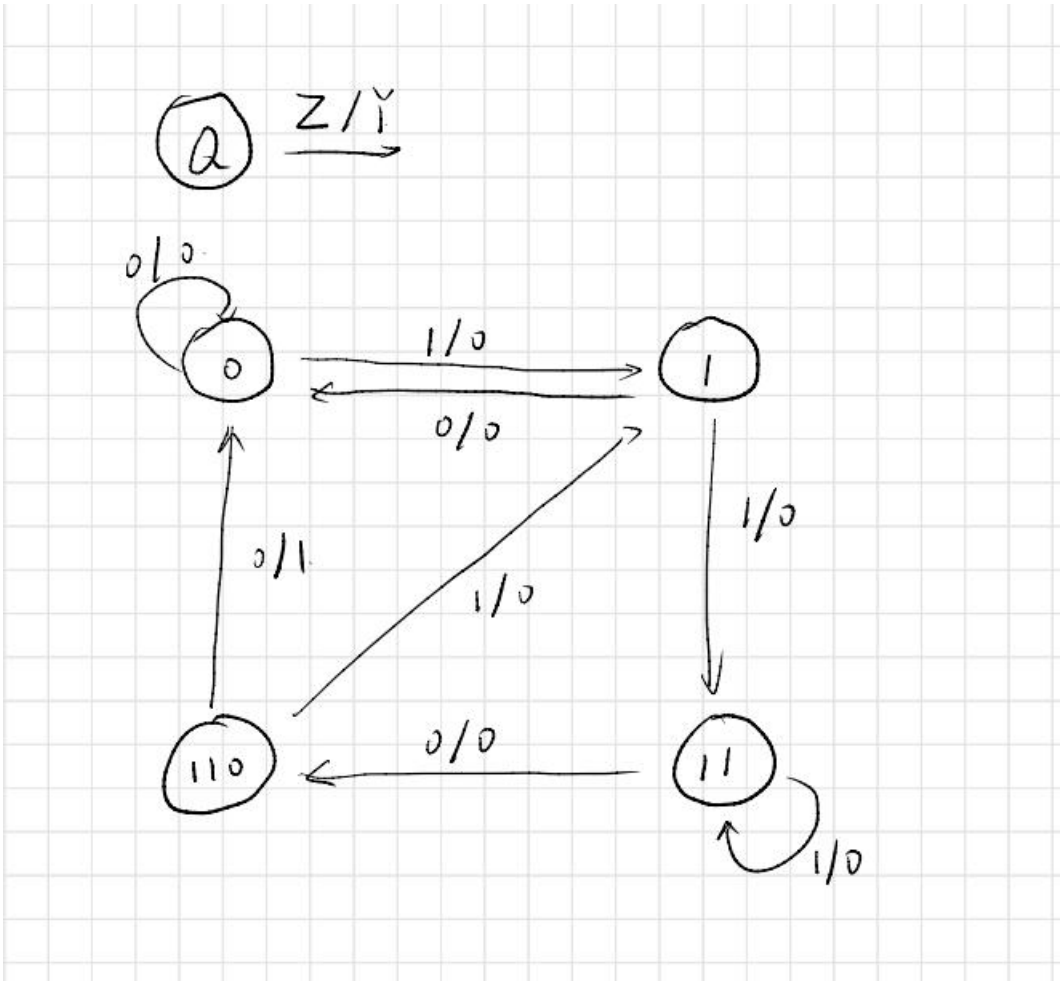

vlab.ustc.edu.cn (x11) - VNC Viewer
应用程序 位置 系统
18:33
FPGA Online — Mozilla Firefox
About - FPGA Online
FPGA Online
202.38.79.134:12175/?token=HA2DKOLEHAZTQNTFMY3WMMJYGJSGCMJVGA3DKZLDMRRGMNTCMFQTAM
led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
uart
FPGAOL uart beta 1.0
>
uart pins: cts rts rxd txd
xdc,ucf sym: D3 E5 D4 C4
baud rate: 115200
segplay(sharing with led) hexplay
24
segplay pin: dot seg_g seg_f seg_e seg_d seg_c seg_b seg_a
xdc,ucf sym: G18 F18 E17 D17 G17 E18 D18 C17
hexplay pin: an2 an1 an0 d3 d2 d1 d0
xdc,ucf sym: A18 B16 B17 A15 A16 A13 A14
soft clock
button
None
clk btn pins: clk_btn
xdc,ucf sym: B18
Sampling Waveform
Generate Waveform
lab8-3 - [/home/ubuntu/l...
[lab8-4 - [/home/ubuntu/...
FPGA Online — Mozilla Fi...


vlab.ustc.edu.cn (x11) - VNC Viewer
应用程序 位置 系统
18:34
FPGA Online — Mozilla Firefox
About - FPGA Online
FPGA Online
202.38.79.134:12175/?token=HA2DKOLEHAZTQNTFMY3WMMJYGJSGCMJVGA3DKZLDMRRGMNTCMFQTAM
led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
uart
FPGAOL uart beta 1.0
>
uart pins: cts rts rxd txd
xdc,ucf sym: D3 E5 D4 C4
baud rate: 115200
segplay(sharing with led) hexplay
25
segplay pin: dot seg_g seg_f seg_e seg_d seg_c seg_b seg_a
xdc,ucf sym: G18 F18 E17 D17 G17 E18 D18 C17
hexplay pin: an2 an1 an0 d3 d2 d1 d0
xdc,ucf sym: A18 B16 B17 A15 A16 A13 A14
soft clock
button
None
clk btn pins: clk_btn
xdc,ucf sym: B18
Sampling Waveform
Generate Waveform
lab8-3 - [/home/ubuntu/l...
[lab8-4 - [/home/ubuntu/...
FPGA Online — Mozilla Fi...


vlab.ustc.edu.cn (x11) - VNC Viewer
应用程序 位置 系统
18:34
FPGA Online — Mozilla Firefox
About - FPGA Online
FPGA Online
202.38.79.134:12175/?token=HA2DKOLEHAZTQNTFMY3WMMJYGJSGCMJVGA3DKZLDMRRGMNTCMFQTAM
led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
uart
FPGA0L uart beta 1.0
>
uart pins: cts rts rxd txd
xdc,ucf sym: D3 E5 D4 C4
baud rate: 115200
segplay(sharing with led)
hexplay
1F
segplay pin: dot seg_g seg_f seg_e seg_d seg_c seg_b seg_a
xdc,ucf sym: G18 F18 E17 D17 G17 E18 D18 C17
hexplay pin: an2 an1 an0 d3 d2 d1 d0
xdc,ucf sym: A18 B16 B17 A15 A16 A13 A14
soft clock
button
None
clk btn pins: clk_btn
xdc,ucf sym: B18
Sampling Waveform
Generate Waveform
lab8-3 - [/home/ubuntu/l...
[lab8-4 - [/home/ubuntu/...
FPGA Online — Mozilla Fi...

实验 4

状态图如下所示：



实现代码如下：

```
module check_bit(
input clk,
input sw,button,
output reg [3:0] hexplay_data,
output reg [2:0] hexplay_an
);
reg [3:0] data;
reg [3:0]count = 0;
reg [32:0] hexplay_cnt;
```

```
wire button_edge;
reg [3:0]button_cnt;
wire button_clean;
always@(posedge clk)begin
if(button==1'b0)
button_cnt <= 4'h0;
else if(button_cnt<4'h8)
button_cnt <= button_cnt + 1'b1;
end
assign button_clean = button_cnt[3];
parameter Idel = 4'b0000,
A = 4'b0001,
B = 4'b0010,
C = 4'b0100,
D = 4'b1000;
reg [3:0] current_s = Idel;
reg [3:0] next_s;
cal_edge
cal_edge_1(.clk(clk),.button(button_clean),.button_edge(but
ton_edge));
always@(posedge clk) begin
if (hexplay_cnt >= (2000000 / 8))
```

```
hexplay_cnt <= 0;
else
hexplay_cnt <= hexplay_cnt + 1;
end
always@(posedge clk) begin
if (hexplay_cnt == 0)begin
if (hexplay_an == 5)
hexplay_an <= 0;
else
hexplay_an <= hexplay_an + 1;
end
end
always@(*) begin
case(hexplay_an)
0: hexplay_data = data[0];
1: hexplay_data = data[1];
2: hexplay_data = data[2];
3: hexplay_data = data[3];
4: hexplay_data = count;
5: hexplay_data = current_s;
 endcase
end
```

```
always@(posedge clk)begin
if(button_edge == 1)begin
case(current_s)
Idel: if(sw == 1) next_s = A;
 else next_s = Idel;
A: if(sw == 1) next_s = B;
else next_s = Idel;
 B: if(sw == 1) next_s = B;
 else next_s = C;
C: if(sw == 1) next_s =A;
else begin
count <= count + 1;
next_s = D;
end
D: if(sw == 1) next_s = A;
else next_s = Idel;
default: next_s = Idel;
endcase
end
end
always@(posedge clk)begin
current_s <= next_s;
```

```
end
always@(posedge clk)
begin
if(button_edge == 1)begin
data[3] <= data[2];
data[2] <= data[1];
 data[1] <= data[0];
data[0] <= sw;
 end
end
endmodule

module cal_edge (
input button,clk,
output button_edge
);
reg button_1,button_2;
always@(posedge clk)
button_1 <= button;
always@(posedge clk)
button_2 <= button_1;
assign button_edge = button_1 &(~button_2);
```

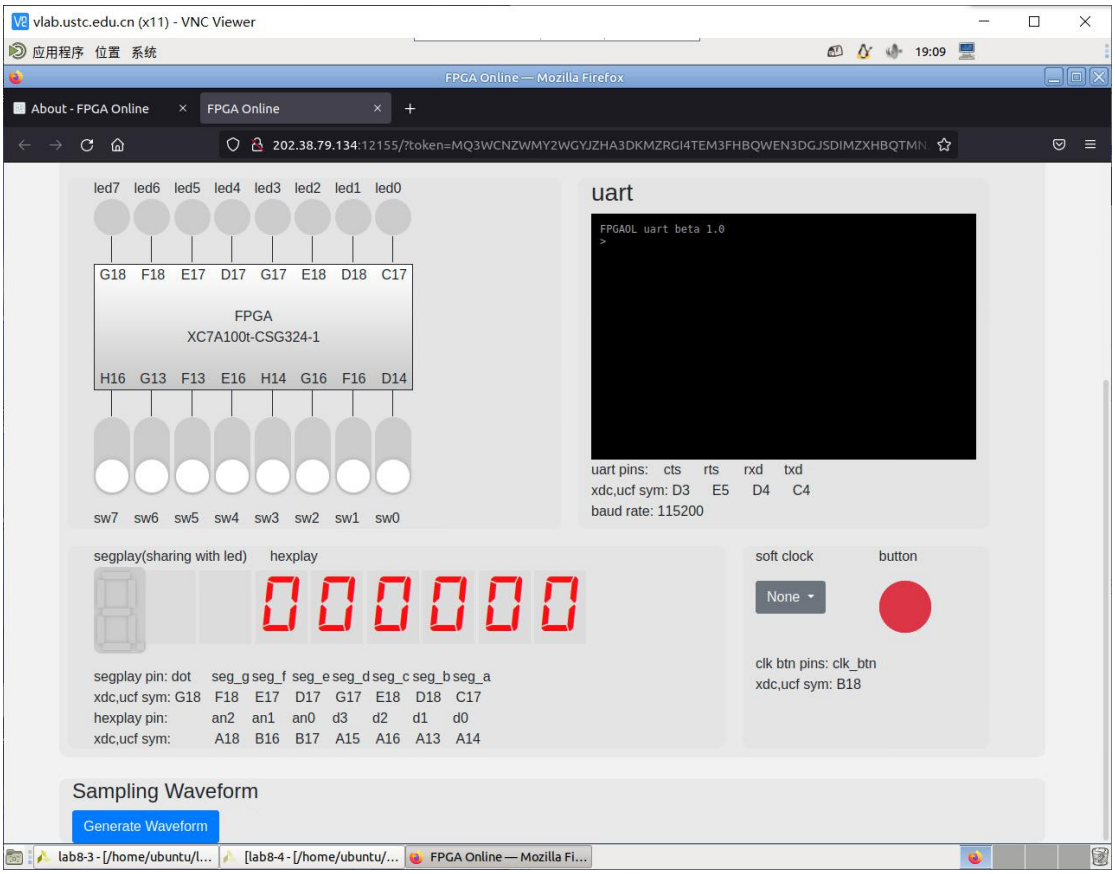
```
endmodule
```

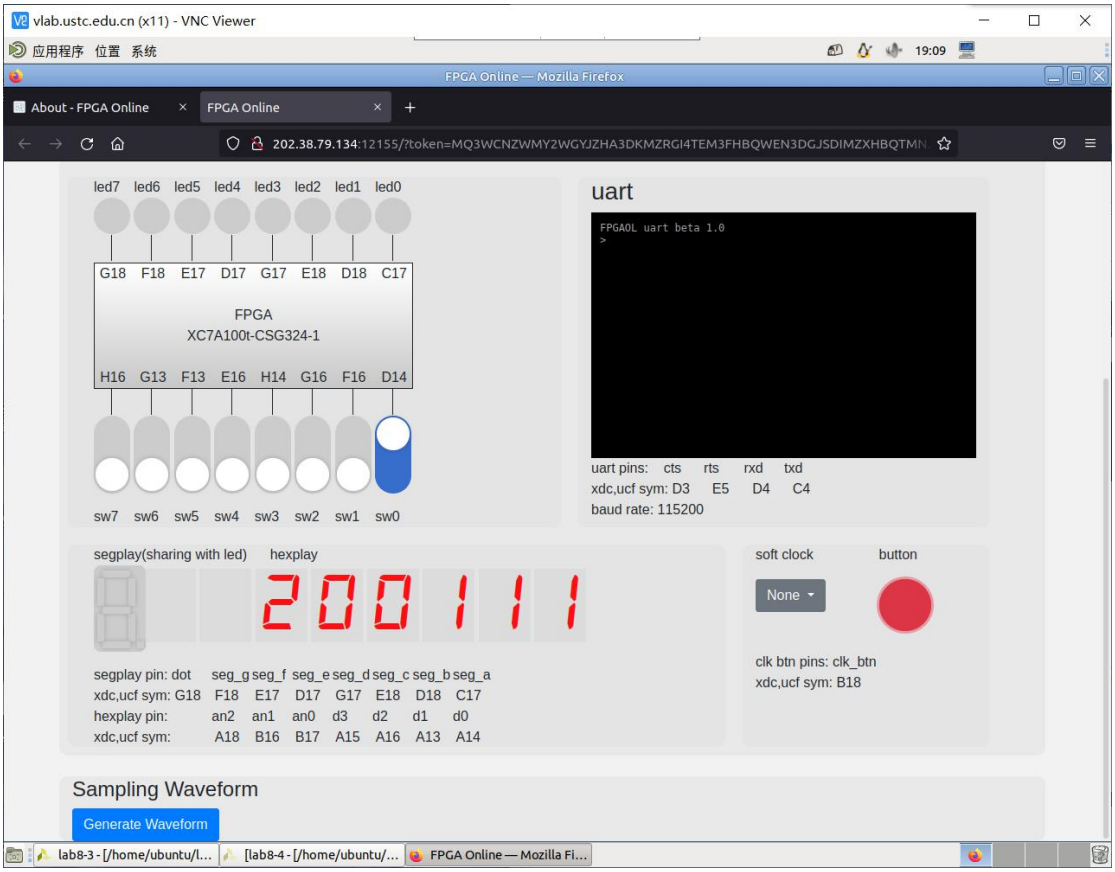
对应的 xdc 约束文件：

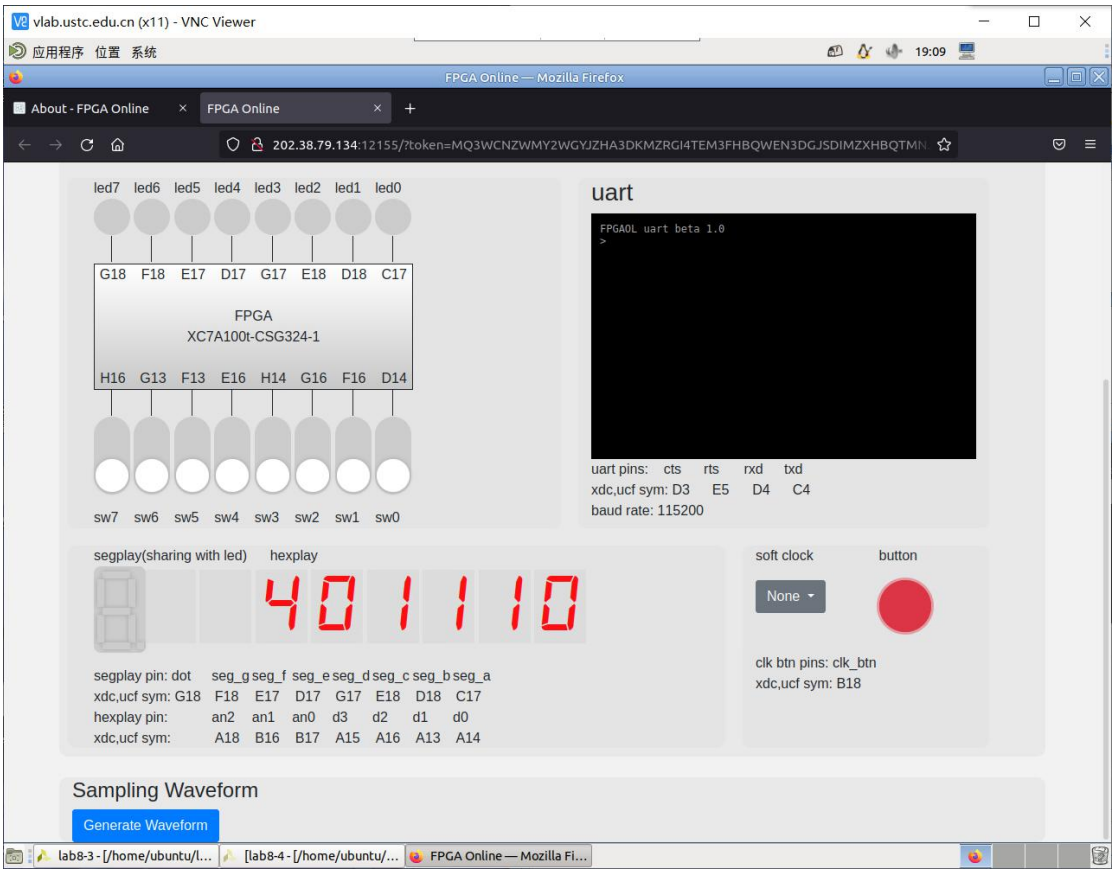
```
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 }
[get_ports { clk }];
set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 }
[get_ports { button }];
#FPGAOL SWITCH
set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 }
[get_ports { sw }];
#set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 }
[get_ports { rst }];
## FPGAOL HEXPLAY
set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[0] }];
set_property -dict { PACKAGE_PIN A13   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[1] }];
set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[2] }];
set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_data[3] }];
set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33 }
[get_ports { hexplay_an[0] }];
```

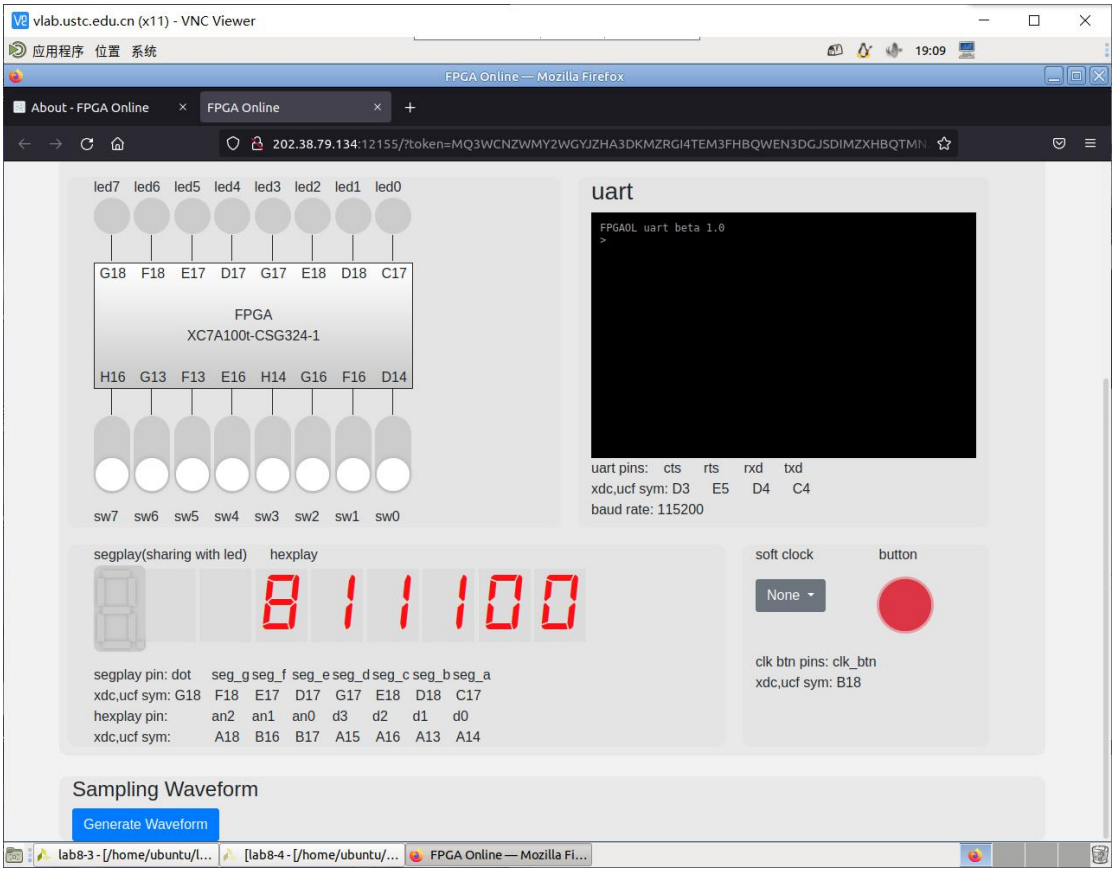
```
set_property -dict { PACKAGE_PIN B16    IOSTANDARD LVCMOS33 }
[get_ports { hexplay_an[1] }];
set_property -dict { PACKAGE_PIN A18    IOSTANDARD LVCMOS33 }
[get_ports { hexplay_an[2] }];
```

烧写后如下系列图所示，最左边的数字表示状态序号，第二个表示 1100 的次数，右四位表示当前状态。




vlab.ustc.edu.cn (x11) - VNC Viewer
应用程序 位置 系统
19:09
FPGA Online — Mozilla Firefox
About - FPGA Online
FPGA Online
202.38.79.134:12155/?token=MQ3WCNZWMY2WGYJZHA3DKMZRGI4TEM3FHBQWEN3DGJSDIMZXHBQTMN
led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
uart
FPGAOL uart beta 1.0
>
uart pins: cts rts rxd txd
xdc,ucf sym: D3 E5 D4 C4
baud rate: 115200
segplay(sharing with led)
hexplay
2 0 0 1 1 1
segplay pin: dot seg_g seg_f seg_e seg_d seg_c seg_b seg_a
xdc,ucf sym: G18 F18 E17 D17 G17 E18 D18 C17
hexplay pin: an2 an1 an0 d3 d2 d1 d0
xdc,ucf sym: A18 B16 B17 A15 A16 A13 A14
soft clock
button
None
clk btn pins: clk_btn
xdc,ucf sym: B18
Sampling Waveform
Generate Waveform
lab8-3 - [/home/ubuntu/l...
[lab8-4 - [/home/ubuntu/...
FPGA Online — Mozilla Fi...


vlab.ustc.edu.cn (x11) - VNC Viewer
应用程序 位置 系统
19:09
FPGA Online — Mozilla Firefox
About - FPGA Online
FPGA Online
202.38.79.134:12155/?token=MQ3WCNZWMY2WGYJZHA3DKMZRGI4TEM3FHBQWEN3DGJSDIMZXHBQTMN
led7 led6 led5 led4 led3 led2 led1 led0
G18 F18 E17 D17 G17 E18 D18 C17
FPGA
XC7A100t-CSG324-1
H16 G13 F13 E16 H14 G16 F16 D14
sw7 sw6 sw5 sw4 sw3 sw2 sw1 sw0
uart
FPGAOL uart beta 1.0
>
uart pins: cts rts rxd txd
xdc,ucf sym: D3 E5 D4 C4
baud rate: 115200
segplay(sharing with led)
hexplay
4 0 1 1 1 0
segplay pin: dot seg_g seg_f seg_e seg_d seg_c seg_b seg_a
xdc,ucf sym: G18 F18 E17 D17 G17 E18 D18 C17
hexplay pin: an2 an1 an0 d3 d2 d1 d0
xdc,ucf sym: A18 B16 B17 A15 A16 A13 A14
soft clock
button
None
clk btn pins: clk_btn
xdc,ucf sym: B18
Sampling Waveform
Generate Waveform
lab8-3 - [/home/ubuntu/l...
[lab8-4 - [/home/ubuntu/...
FPGA Online — Mozilla Fi...



【总结与思考】

本次实验任务量巨大，难度也比较大，本来想一中午加下午搞完结果翻车了（×）又搞了一个晚上（×，主要困难是生成.bit 文件经常失败，反反复复

不过通过本次实验，我学到了很多有用的知识，极大的提高了我写 verilog 代码和 debug 的能力，收获还是非常大的