

컴퓨터 공학 기초 실험2 보고서

실험제목: Simple Memory & Bus

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학 과: 컴퓨터공학과

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실습분반: 월요일 0, 1, 2

학 번: 2022202064

성 명: 최봉규

1. 제목 및 목적

A. 제목

Simple Memory & Bus

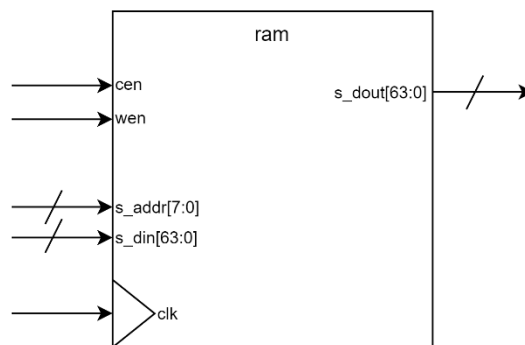
B. 목적

Memory는 address에 기반하여 데이터를 저장하는 hardware임을 이해한다. 또한 bus는 여러 component들 간에 데이터를 전송할 수 있도록 연결해주는 component임을 이해한다. 이처럼 Memory와 bus의 특성에 대해 이해하고, 이를 바탕으로 설계한다.

2. 원리(배경지식)

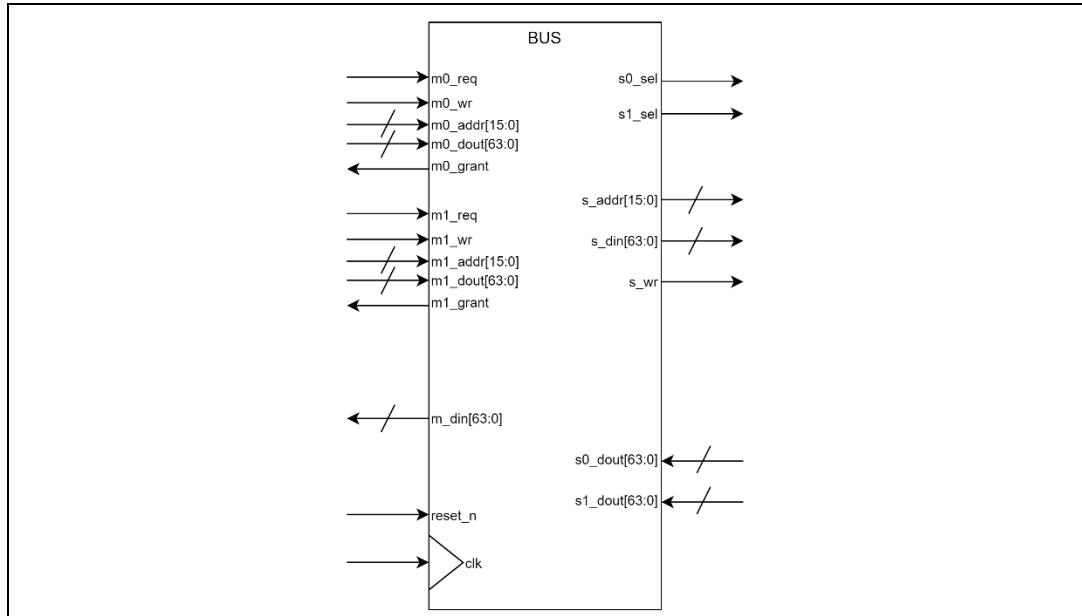
Simple memory

RAM(random access memory)은 임의의 address에 대해 data를 읽고 쓰는 memory를 의미한다. 이 프로젝트에서 지칭하는 memory는 모두 RAM을 의미한다. Memory는 Software를 hardware와 communicate를 하게 해주는 매개체 역할을 한다. 아래는 memory(ram)의 schematic symbol이다.



Bus

Bus는 여러 component들 간에 data를 전송(transfer)할 수 있도록 연결해주는 component이다. BUS는 새로운 component 들을 추가하기가 쉬우며, 가격이 저렴한 특징을 갖고 있다. 하나 이상의 IP components가 연결된 wire 덩어리이다. 오직 한 쌍의 IP component만 data를 bus를 통해 주고받을 수 있다. 한 쌍이 communicate를 할 때, 하나는 master, 또 다른 하나는 slave이다. 오직 master만이 bus를 통해 data transfer를 request 혹은 initiate가 가능하다. Slave는 단지 master에 의해 request된 data transfer를 주는 데이터를 받거나 혹은 데이터를 주는 역할을 한다. 아래는 BUS의 schematic symbol이다.



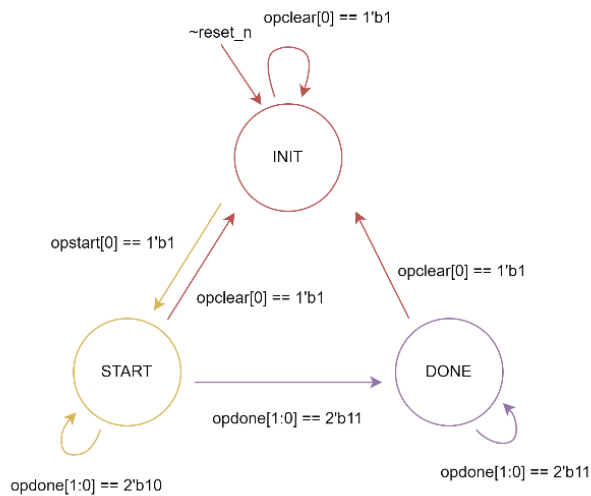
Bus가 master로부터 요청을 받으면, 내부에 있는 arbiter를 통해 slave0와 slave1 중 어떤 slave와 communicate할 지 결정한다. 이 때 어느 slave와 communicate할 지는 address를 통해 결정한다. 결정한 slave에는 m_dout과 m_addr를 건넨다. Slave에 연결된 컴포넌트로부터 output이 나오는데 이를 각 연결하여 그로부터 S0_dout과 S1_dout을 입력 받는다. Mux를 통해 m_din에 S0_dout과 S1_dout 둘 중 하나의 값을 선택하여 받게 된다. 이와 함께 선택된 값에는 m_grant는 1의 값을 갖게 되어 해당 마스터의 요청이 허가되었음을 알려준다. Master가 grant signal을 받은 후에는 request signal이 1인 동안에는 bus의 소유권을 빼앗기지 않고 data 전송을 계속 할 수 있다. 만약 두 개의 master 모두 request를 하고 있지 않다면 grant는 master0이 받는다.

3. 설계 세부사항

Simple memory		
Direction	Port name	Description
Input	clk	Clock
	cen	Chip enable
	wen	Write enable
	addr[4:0]	Address
Output	din[31:0]	Data in
	dout[31:0]	Data out

cen과 wen의 값이 모두 1'b1이 되면 address가 가리키는 memory에 din을 write한다. 이 때의 dout 은 0을 출력하도록 한다. 만약 cen = 1'b1이고, wen = 1'b0이면, address가

가리키는 memory의 값을 dout에 write한다. cen = 1'b0이면 dout은 0이 된다. 이로써, cen이 wen보다 우선순위를 갖는 것을 확인할 수 있다. 다음은 memory의 fsm이다.

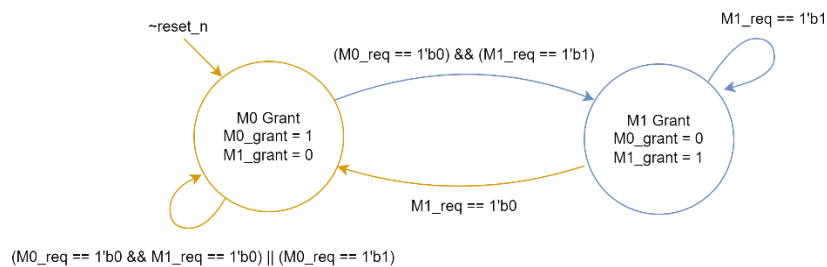
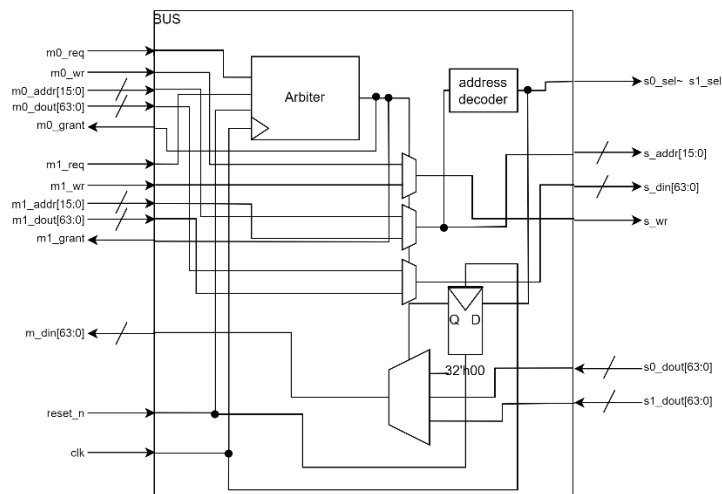


Bus		
Direction	Port name	Description
Input	clk	Clock
	reset_n	Active low reset
	m0_req	Master 0 request
	m0_wr	Master 0 write / read
	m0_address[7:0]	Master 0 address
	m0_dout[31:0]	Master 0 data output
	m1_req	Master 1 request
	m1_wr	Master 1 write / read
	m1_address[7:0]	Master 1 address
	m1_dout[31:0]	Master 1 data output
	s0_dout[31:0]	Slave 0 data out
	s1_dout[31:0]	Slave 1 data out
Output	m0_grant	Master 0 grant
	m1_grant	Master 1 grant
	m_din[31:0]	Master data input
	s0_sel	Slave 0 select
	s1_sel	Slave 1 select
	s_address[7:0]	Slave address
	s_wr	Slave write / read
	s_din[31:0]	Slave data input

2개의 master와 2개의 slave를 가지고 있다. Address의 bandwidth는 8bits이다. Data의 bandwidth는 32bit이다. 각 slave가 가지는 주소 범위는 다음과 같다.

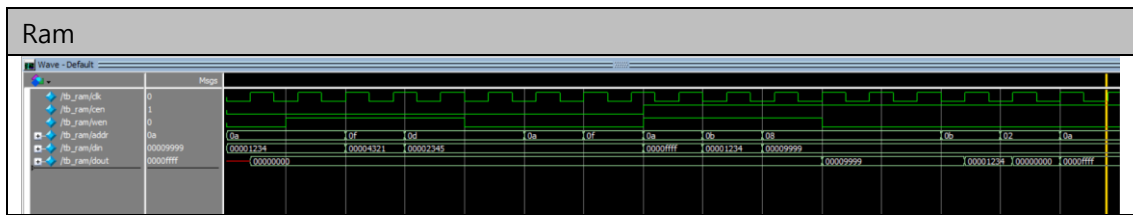
Memory map	
Slave 0	0x00 ~ 0x1F
Slave 1	0x20 ~ 0x3F

해당 주소들을 binary로 확대한다면, slave 0의 경우 8'b0000_0000 ~ 8'b0001_1111이고, slave 1의 경우 8'b0010_0000 ~ 8'b0011_1111으로 상위 3bit에 대해서 slave 0은 3'b000을 가지고, slave 1의 경우 3'b001을 갖게 된다. 다음은 bus의 design과 abitrator의 fsm을 보여주고 있다.

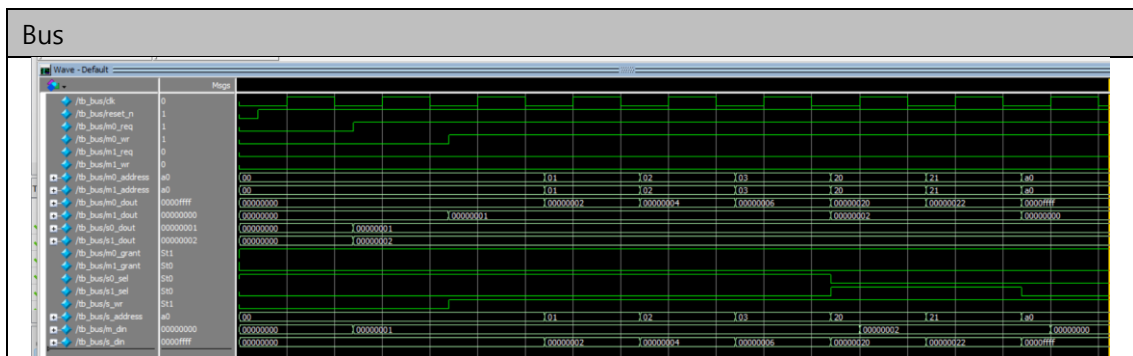


4. 설계 검증 및 실험 결과

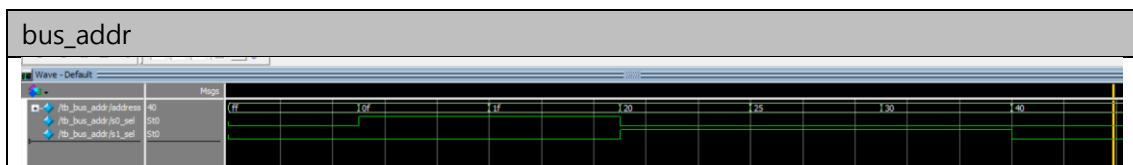
A. 시뮬레이션 결과



해당 waveform은 ram의 testbench로 `cen = 1'b0`일 때에는 `wen`과 `addr`가 아무리 바뀌어도 `dout`은 0의 값을 갖는 것을 확인할 수 있다. `cen = 1'b1`일 때에는 `wen = 1'b1`이 된 순간 `addr`를 바꾸면서 `d_in`으로 넣은 값들을 해당 인덱스에 저장을 한다. `wen = 1'b0`의 값을 갖게 하고, 주소를 변경한 결과 이전에 `d_in`으로 넣은 것들을 가지고 있음을 확인할 수 있다.

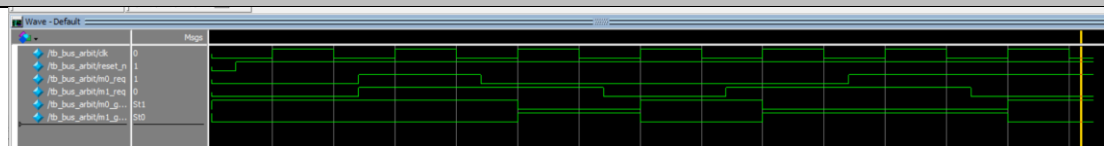


해당 waveform은 bus의 testbench이다. `m0`와 `m1`의 address를 동일 시 하고, 서로 다른 `dout`의 값을 줌으로 써, `s_din`으로 들어오는 값들이 어떤 것인지 확인했다. `m0_req = 1'b1`를 가지면서 `s_din`은 `m0_dout`의 값을 가지게 된다. 또한 `s_address`역시 `m0`의 것을 따라간다. Address를 8'h20이 되면서 `s1`을 선택하게 된다. `m_din`에는 `s_dout`의 값을 가져 가게 되었다. 이후 address를 8'ha0을 주면서 `s0`, `s1` 둘 모두 선택하지 않고, `m_din`은 32'h0000_0000의 값을 갖게 된다. 이와 같이 의도대로 잘 작동함을 알 수 있다.



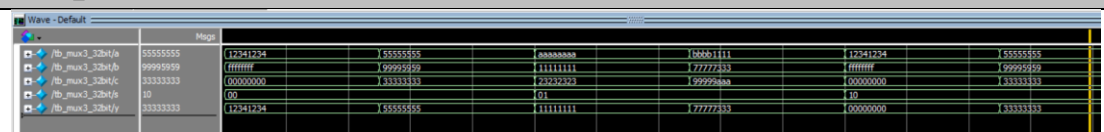
해당 waveform은 bus_addr의 testbench이다. 입력 address에 따라 `s0`와 `s1`이 선택되는 것을 확인할 수 있다. 앞서 설계한 대로 address가 0x00 ~ 0x1f인 경우 `s0`를 선택하고, 0x20 ~ 0x3f인 경우 `s1`을 택하게 한다. 이 외의 값에 대해서는 둘 모두 선택하지 않는데, 테스트 벤치를 보면 설계한 대로 잘 작동함을 확인할 수 있다.

bus_arbit



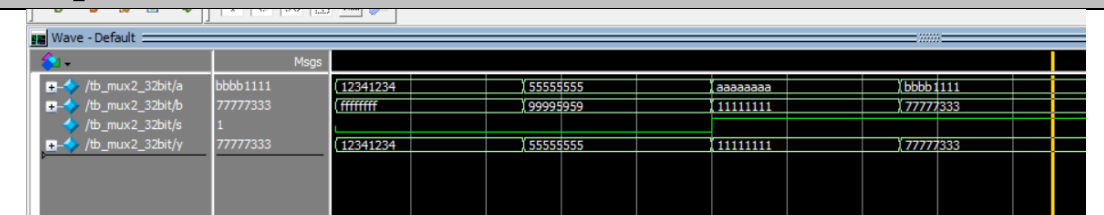
해당 waveform은 m0_req와 m1_req에 따라 m0_grant, m1_grant가 변하는 것을 확인할 수 있다. m0_req = 1'b1인 경우 m0_grant = 1'b1의 값을 갖는다. 이 후 m1_req = 1'b1이 되어도 m0_req = 1'b0이 되기 전에는 m0_grant를 택했다. 이후 m1_grant = 1'b1의 값을 갖는 것을 볼 수 있다. m1_grant가 1'b1이 되면서 m0_grant = 1'b0의 값으로 내려간다. 이후의 값들을 보더라도 의도대로 잘 동작하는 것을 확인할 수 있다.

mux3_32bit



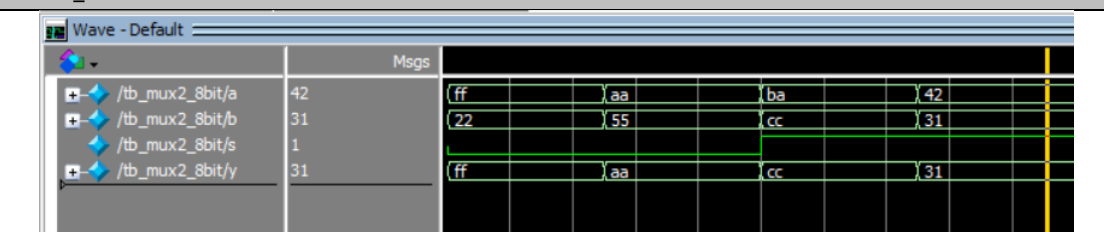
해당 waveform은 s에 따라 a, b, c의 값을 y로 이어준다. s = 2'b00인 경우 y = a의 값을 갖게 되고, s = 2'b01인 경우 y = b의 값을, s = 2'b10인 경우 y = c의 값을 갖도록 설계했다. 해당 결과를 잘 갖는 것을 testbench를 통해 확인할 수 있다.

mux2_32bit

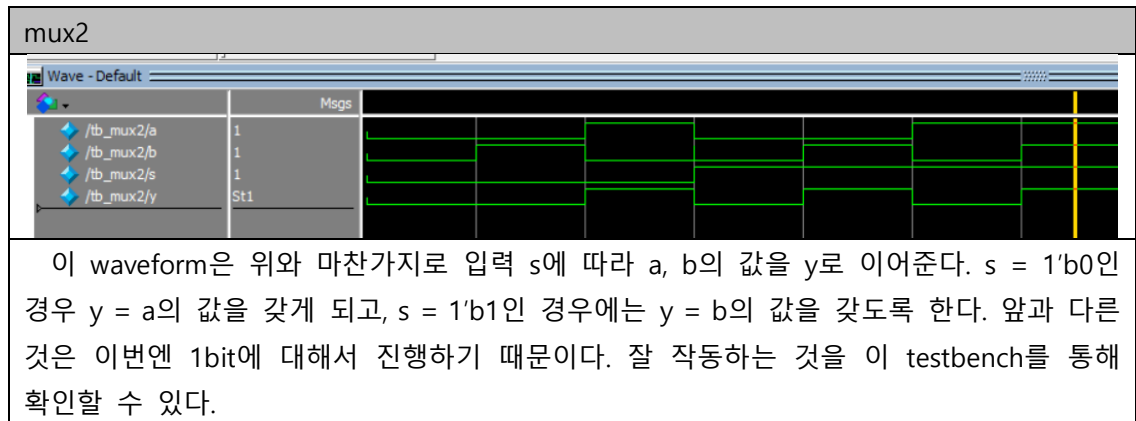


해당 waveform은 입력 s에 따라 a, b의 값을 y로 이어준다. s = 1'b0인 경우 y = a의 값을 갖게 되고, s = 1'b1인 경우에는 y = b의 값을 갖도록 한다. 의도한대로 잘 작동하는 것을 이 testbench를 통해 확인할 수 있다.

mux2_8bit



이 waveform은 위와 마찬가지로 입력 s에 따라 a, b의 값을 y로 이어준다. s = 1'b0인 경우 y = a의 값을 갖게 되고, s = 1'b1인 경우에는 y = b의 값을 갖도록 한다. 앞과 다른 것은 이번엔 8bit에 대해서 진행하기 때문이다. 잘 작동하는 것을 이 testbench를 통해 확인할 수 있다.



B. 합성(synthesis) 결과

Ram

Flow Summary


<<Filter>>

Flow Status	Successful - Sun Nov 19 01:31:32 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	ram
Top-level Entity Name	ram
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	527 / 41,910 (1 %)
Total registers	1056
Total pins	72 / 499 (14 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

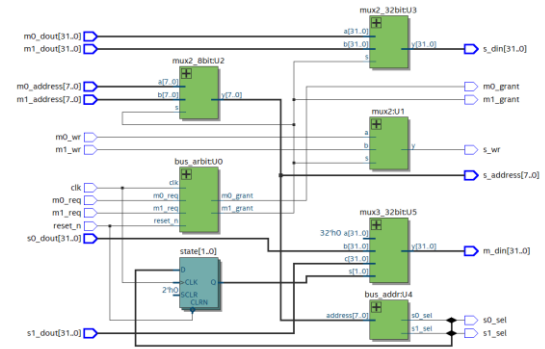
해당 flow summary는 ram의 것으로, Logic utilization은 527, total registers는 1056, total pins는 72인 것을 확인할 수 있다.

해당 RTL map viewer는 ram의 것이다.

Bus

Flow Summary	
 <<Filter>>	
Flow Status	Successful - Sun Nov 19 01:48:19 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	bus
Top-level Entity Name	bus
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	39 / 41,910 (< 1 %)
Total registers	3
Total pins	227 / 499 (45 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

해당 flow summary는 bus의 것으로, Logic utilization은 39, total registers는 3, total pins는 227인 것을 확인할 수 있다.



The diagram shows the RTL map for the 'bus' entity. It features several multiplexers (mux2_00bits12, mux2_00bits13, mux2_00bits14, mux2_00bits15, mux2_00bits16, mux2_00bits17, mux2_00bits18, mux2_00bits19, mux2_00bits20, mux2_00bits21, mux2_00bits22, mux2_00bits23, mux2_00bits24, mux2_00bits25, mux2_00bits26, mux2_00bits27, mux2_00bits28, mux2_00bits29, mux2_00bits30, mux2_00bits31, mux2_00bits32, mux2_00bits33, mux2_00bits34, mux2_00bits35, mux2_00bits36, mux2_00bits37, mux2_00bits38, mux2_00bits39, mux2_00bits40, mux2_00bits41, mux2_00bits42, mux2_00bits43, mux2_00bits44, mux2_00bits45, mux2_00bits46, mux2_00bits47, mux2_00bits48, mux2_00bits49, mux2_00bits50, mux2_00bits51, mux2_00bits52, mux2_00bits53, mux2_00bits54, mux2_00bits55, mux2_00bits56, mux2_00bits57, mux2_00bits58, mux2_00bits59, mux2_00bits60, mux2_00bits61, mux2_00bits62, mux2_00bits63, mux2_00bits64, mux2_00bits65, mux2_00bits66, mux2_00bits67, mux2_00bits68, mux2_00bits69, mux2_00bits70, mux2_00bits71, mux2_00bits72, mux2_00bits73, mux2_00bits74, mux2_00bits75, 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mux2_00bits140, mux2_00bits141, mux2_00bits142, mux2_00bits143, mux2_00bits144, mux2_00bits145, mux2_00bits146, mux2_00bits147, mux2_00bits148, mux2_00bits149, mux2_00bits150, mux2_00bits151, mux2_00bits152, mux2_00bits153, mux2_00bits154, mux2_00bits155, mux2_00bits156, mux2_00bits157, mux2_00bits158, mux2_00bits159, mux2_00bits160, mux2_00bits161, mux2_00bits162, mux2_00bits163, mux2_00bits164, mux2_00bits165, mux2_00bits166, mux2_00bits167, mux2_00bits168, mux2_00bits169, mux2_00bits170, mux2_00bits171, mux2_00bits172, mux2_00bits173, mux2_00bits174, mux2_00bits175, mux2_00bits176, mux2_00bits177, mux2_00bits178, mux2_00bits179, mux2_00bits180, mux2_00bits181, mux2_00bits182, mux2_00bits183, mux2_00bits184, mux2_00bits185, mux2_00bits186, mux2_00bits187, mux2_00bits188, mux2_00bits189, mux2_00bits190, mux2_00bits191, mux2_00bits192, mux2_00bits193, mux2_00bits194, mux2_00bits195, mux2_00bits196, mux2_00bits197, mux2_00bits198, mux2_00bits199, mux2_00bits200, mux2_00bits201, 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5. 고찰 및 결론

A. 고찰

bus에서 사용하는 I/O port가 많아서 자료를 좀 꼼꼼히 봐야 어디에 연결할지 감이 잡히는 것이 힘들었다. testbench를 만들면서 port를 잘 instance를 못해 몇몇의 포트 결과가 z로 되는 걸 보면서 무슨 port를 빠뜨렸는지 확인하면서 top module을 정의할 때, 옆에 있는 것으로 쓰면 빠지는 port 없이 잘 연결할 수 있겠다는 생각이 들었다. 해당 방법을 이용하여 일일이 testbench에서 top module을 instance할 때 걸리는 시간을 줄이고 헛갈리지 않게 잘 연결할 수 있었다.

B. 결론

이번 실습을 진행하면서 Verilog 에서의 for 반복문을 처음 써보았다. c/c++과 다를 것은 크게 없었는데, for문 증감식에서 ++, -- 같은 표현을 사용하지 않는 것이 조금 불편하게 다가왔다. 해당 과제를 진행하면서 bus에 대해, 그리고도 memory를 만드는 법에 대해 알아가면서 프로젝트에서 사용할 bus와 memory에 대해서 크게 어려움 없이 만들 수 있을 것 같다는 생각이 들었다. 또한 loop문을 사용하면서 이를 testbench를 만드는 데에 적용하면 많은 경우의 수에 대해 간결하게 확인할 수 있지 않을까 생각이 들었다.

6. 참고문헌

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