Q1: How to use CH7025/26?
A1: Chrontel provides PCB reference design and programming guide together with the datasheet, please follow reference design to set up your hardware and follow the steps in programming guide to program CH7025/26. Also, we provide sample code for some embedded platforms, you could get it from Chrontel AE department.

Q2: What kinds of input format does CH7025/26 support?
A2: CH7025/26 supports progressive, interlaced and CPU interface input: The progressive and interlaced input are just the LCD interface including data, H/V Sync, pixel clock and DE (data enable, which is not necessary); the CPU interface is like memory interface, please check Q4 for details.

The content of video data could be RGB or YcbCr format.

Q3: What kinds of output format and signal does CH7025/26 support?
A3: The output formats CH7025/26 supports are:

SDTV (NTSC&PAL)
VGA (D-Sub)
HDTV (480p, 576p, 720p, 1080i)

The signals CH7025/26 support are as following:

SDTV:	Single, dual and triple CVBS
	S-Video
	S-Video and single CVBS
	RGB+CSync (SCART mode)
VGA:	RGB + H/V Sync
	RGB + CSync
HDTV:	YPbPr

Please check CH7025/26 datasheet for details.

Q4: How is the input data format for CPU interface?
A4: The input signals for CPU interface include:

VSYNC:	Frame flag
CSB:	Chip select
WEB:	Write enable
DATA:	Video data

Please reference Figure1 below for example:

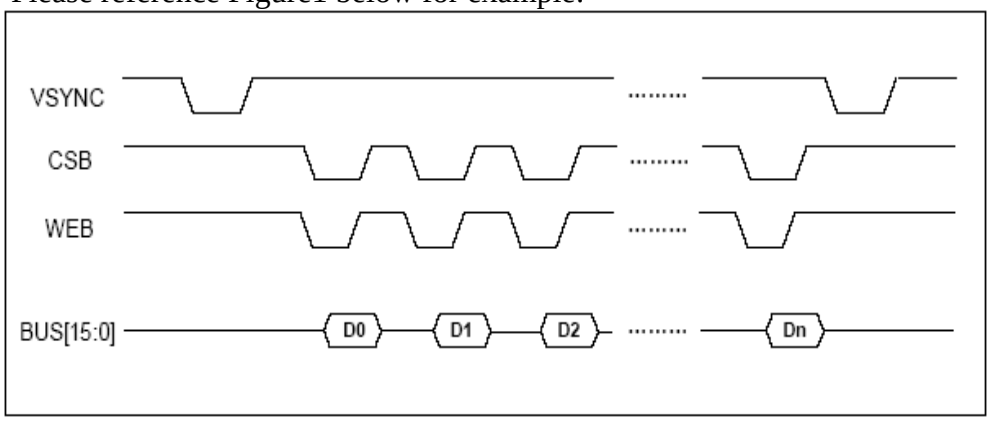

Figure1: Frame Data Transfer Timing

Q7: How to adjust output image size to fit my screen? Is there any limitation?
A7: You could adjust HAO and VAO parameters to adjust it. Bigger HAO bring lager horizontal size, Bigger VAO bring lager vertical size. In bypass mode, the image size could not be adjusted, and keep the same size with input image.

When using CH7025/26, horizontal size of output image (HAO) MUST be bigger than (or equal to) that of input image (HAI): HAO >= HAI. In vertical, there is no this limitation.

Q8: When startup, there is some garbage in TV (VGA) display?
A8: Please add following operation at the end of CH7025/26 initialization:

1) Set bit 1 and bit 0 of 06h to 1
2) Set bit 1 of 06h to 0
3) Set bit 0 of 06h to 0

The up-to-date programming guide tool of CH7025/26 resolved this problem.

Q10: How to set up internal test pattern of CH7025/26?
A10: Please reference Appendix C of programming guide document.

Q11: How about SCART mode of CH7025/26?
A11: CH7025/26 supports SCART output mode, which includes RGB and C sync signals, and the level of the signals are all 3.3V. For standard SCART mode, the level of C sync should be about 1V, this is the difference. The format of SCART mode is same with TV format, just as NTSC_M or PAL_B, so it is interlaced video format.

When using CH7025/26 in SCART mode, we suggest that:

Firstly you should confirm if your panel supports this mode, and if there is any special requirement for the input. If the panel's requirement could not be met, it says CH7025/26 can not be used with this output mode here.

Secondly, we commend that you could configure CH7025/26 to send out CVBS signal at start up, if it works well, then configure CH7025/26 to send out RGB+C sync signals to your panel. At this time, the video stream should be correct, if image could not display on your panel correctly, it is the circuit or the panel who caused the problem.

Q12: Is there is any power sequence shall be followed when turn ON/OFF CH7026?
A12: To turn on CH7025/26 should follow a sequence, which will be embedded in the register-setting file generated by programming tool. To turn off CH7025/26, there is no sequence required.

Q13: For CPU interface support, how to configure CH7026's VSYNC (frame flag) on CPU?
A13: For CPU interface, the input signals of CH7025/26 should be as Figure 1, please generate VSYNC signal following Figure 1. Please check Q4 for details.

Q14: Can we ignore frame flag on CPU side? If yes, how to ensure the VSO and HSO is correct when VGA out?
A14: No. VSYNC signal must be generated and sent to CH7025/26 when using CPU interface input format of CH7025/26.

Q15: What is the acceptable of external clock input? 19.2MHz clock input is OK?
A15: The range is 2.3MHz ~ 64MHz, so 19.2MHz clock input is acceptable. Please see datasheet of CH7025/26.

Q16: Do you have recommended crystal and its part number?
A16: No. Any crystal with the acceptable frequency could be used.

Q17: Does the crystal clock can be shut down during input data is activated when DE/CSB is low?
Q17: There is two conditions:

a. When using crystal (make the “Using Crystal” check button in programming tool checked), the crystal will act as drive clock of CH7025/26, so the crystal clock can not be shut down during input data is activated.

b. When not using crystal (make the “Using Crystal” check button unchecked), the input pixel clock (GCLK) will act as the drive clock of CH7025/26, the crystal clock can be shut down at this time.

There are two usage of the crystal connected to XI/XO, one as mentioned above, the other is to use the crystal to generate sub-carrier.

Q18: Is I2C interface alive or not when disable external crystal clock input?
Q18: I2C interface will alive when 3.3V main power is supplied, it has no relationship with external clock inputs (crystal and GCLK).

Q19: Can we shut down specific power when CH7026 is disabled but its input is toggling? If yes, which power plane we can turn off?
A19: Yes. The power not in use could be shut down to save power. The programming guide tool will turn off the power not in use automatically.

Q20: What is the purpose of composite sync output and how to use this signal?
A20: Some panels require composite sync signal.

Q21: Refer to CH7013BG integrated experience, can we use common LPF to support CVBS, S-Video and VGA? If yes, please give advice.
A21: Chrontel will provide PCB reference design for using CH7025/26. Please refer it.

Q22: Base on power saving consideration, does CH7026 can auto detect TV be plugged-out during TV OUT activation?
A22: No. CH7025/26 has DAC-detect function, but it should be used manually.

Writing History

Rev.	Date	Description
0.01	04/16/2008	Add Q1 ~ Q11
0.02	04/29/2008	Add Q12 ~ Q22