CH7025/CH7026 TV/VGA Encoder

Features

- TV encoder targets for handheld device, surveillance camera and automobile market.
- Supports multiple output formats such as analog TV (NTSC and PAL), VGA and HDTV (480p,576p,720p, 1080i). Sync signals can be provided in separated or composite manner.
- Three on-chip 10-bit high speed DACs providing flexible output capabilities such as single, double or triple CVBS output, YPbPr output, RGB output and simultaneous CVBS and S-video output.
- 90/180/270 degree image rotation and vertical or horizontal flip.
- 16-Mbit SDRAM is used as a frame buffer for frame rate conversion.
- Flexible up and down scaling.
- Programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supports various RGB (RGB888, RGB666, RGB565 and etc), YCbCr (4:4:4 YcbCr, ITU656) and 2x or 3x multiplexed input. CPU interface is also supported.
- Supports flexible input resolution up to 800x800 and 1024x680.
- Pixel by pixel brightness, contrast, hue and saturation adjustment for each output is supported. (For RGB output, only brightness and contrast adjustment is supported).
- Pixel by pixel horizontal position adjustment and line by line vertical position adjustment.
- Supports Macrovision™ 7.1 L1 in CH7025. CH7026 is a Non-Macrovision version of the CH7025
- Supports Macrovision™ copy protection for progressive scan TV (480p, 576p) in CH7025
- Supports CGMS-A for analog TV and HDTV
- TV/Monitor connection detection capability. DAC can be switched off based on detection result.
- Programmable power management.
- Flexible pixel clock frequency from graphics controller is supported. (2.3MHz –120MHz)
- Flexible input clock from crystal or oscillator is supported. (2.3MHz – 64MHz)
- Supports slave input clock mode only.
- Fully programmable through serial port.
- IO and SPC/SPD voltage supported is from 1.2V to 3.3V.
- Offered in BGA or QFP package.

General Description

The CH7025/CH7026 is a semiconductor device targeting for handheld market, surveillance camera and automobile multimedia system. This device accepts digital video signals through its 24-bit input bus and generates NTSC, PAL, VGA or HDTV (480p, 576p, 720p and 1080i) video signal by its 10-bit DACs. In addition, CH7025/26 has an embedded 16-Mbit SDRAM to support the CPU interface.

CH7025/26 has incorporated an advanced technology that can perform real-time video rotations and frame rate conversions for incoming video stream. These complicated tasks are achieved by storing video data to the internal SDRAM and applying scaling process if required. CH7025/26 provides great flexibility for accepting different video data formats including RGB and YcbCr (e.g. RGB565, RGB 666, RGB 888, ITU 656).

The CH7025/26 is available in BGA or QFP package.

Note: the above feature list is subject to change without notice. Please contact Chrontel for more information and current updates.

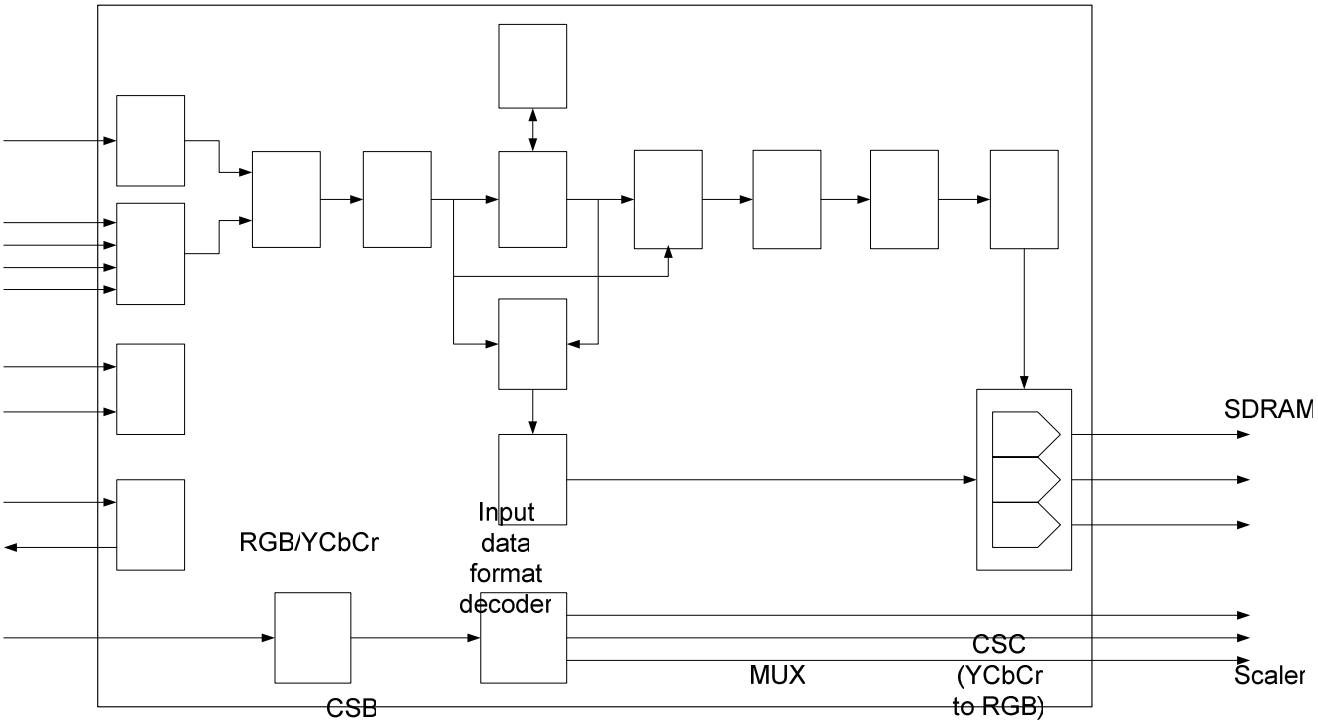

Figure 1. CH7025/CH7026 block diagram

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1.1 Package diagram

1.1.1 The 80-pin BGA Package Diagram

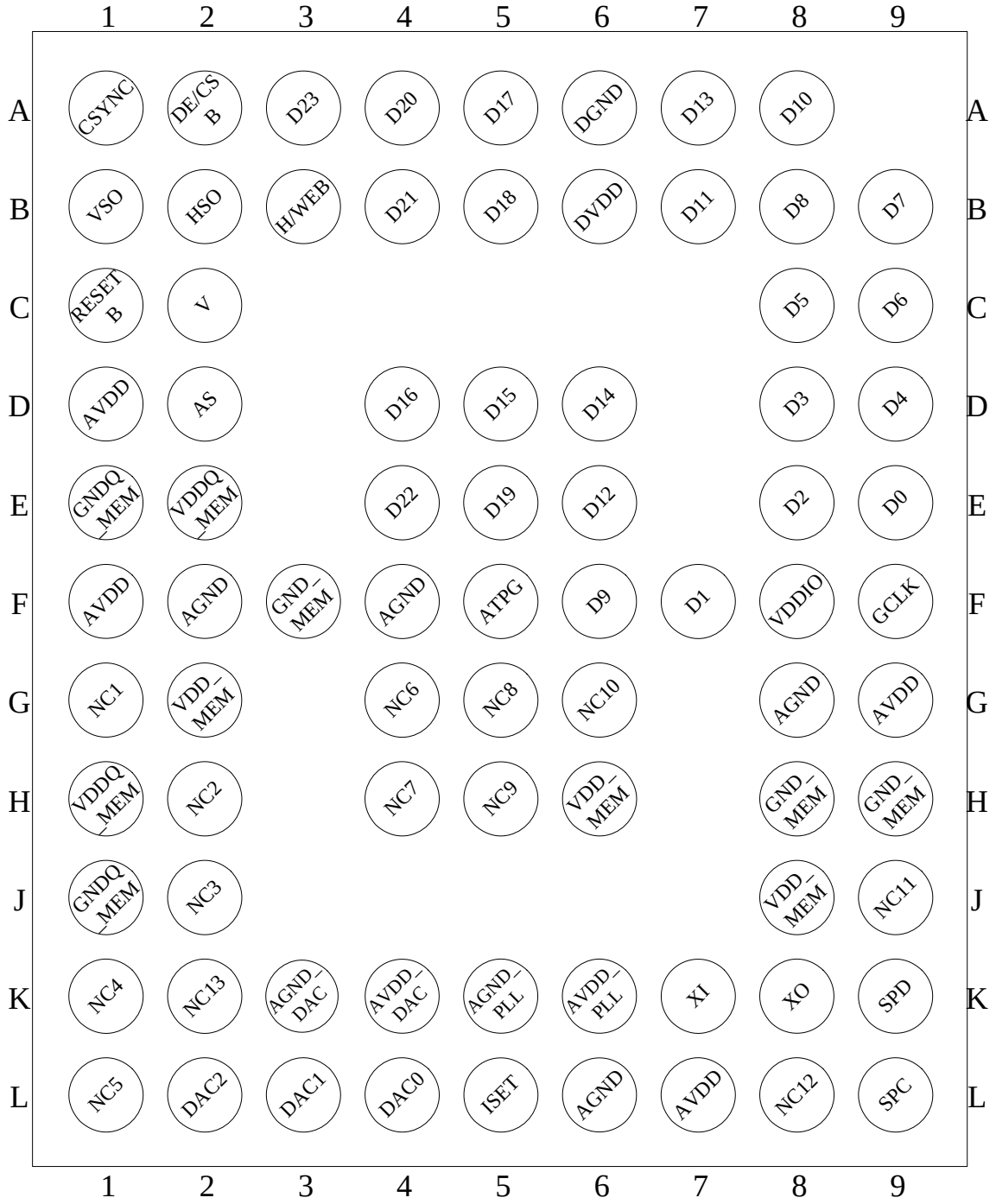

Figure 2: 80-pin BGA package

1.1.2 The 80-pin LQFP Package Diagram

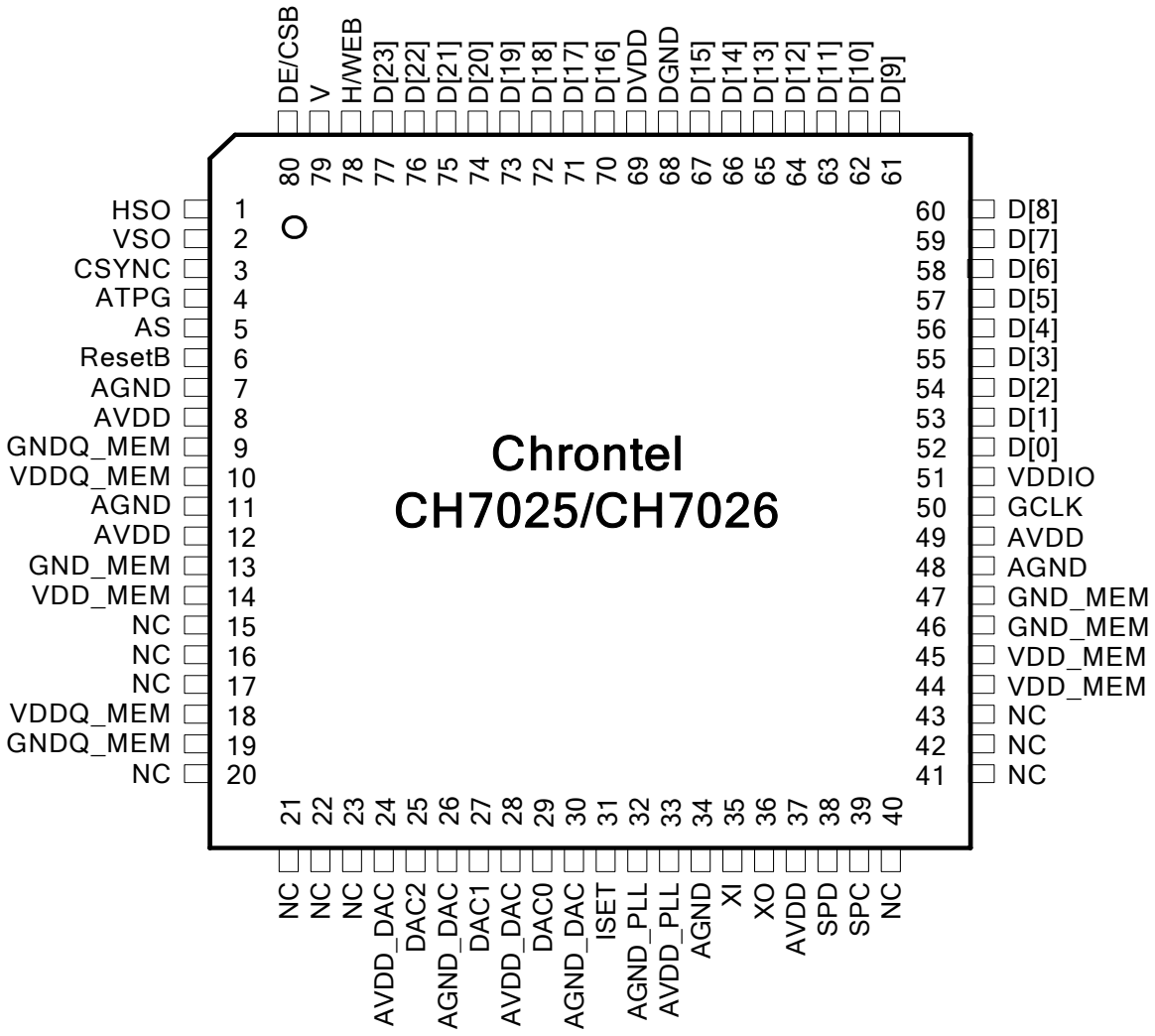

Figure 3: 80-pin LQFP package

1.2 Pin description

Table 1: Pin name description (BGA package)

Pin #	Type	Symbol	Description
A3, E4, B4, A4, E5, B5, A5, D4, D5, D6, A7, E6, B7, A8, F6, B8, B9, C9, C8, D9, D8, E8, F7, E9	In(F)	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
C2	Inout	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
B3	Inout	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
A2	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also the CSB signal of CPU interface The amplitude will be 0 to VDDIO.
D2	In	AS	Address select
F5	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V. Reserved pin.
C1	In	ResetB	Reset * Input When this pin is low, the device is held in the hardware reset condition. When this pin is high, reset is controlled through the serial port.
K9	Inout	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resister is required.
L9	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resister is required.
L4	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
L3	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v

Pin #	Type	Symbol	Description
L2	Out	DAC2	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
L5	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
K7	In	XI	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
K8	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
F9	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
B1	Out	VSO	Vertical sync signal output
B2	Out	HSO	Horizontal sync signal output
A1	Out	CSYNC	Composite sync output
F8	Power	VDDIO	IO supply voltage (1.2-3.3V)
B6	Power	DVDD	Digital supply voltage (1.8V)
D1, F1, L7, G9	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
K6	Power	AVDD_PLL	PLL supply voltage (1.8V)
K4	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
E2, H1	Power	VDDQ_MEM	SDRAM output buffer supply voltage (1.8V or 2.5V)
G2, J8, H6	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
A6	Power	DGND	Digital supply ground
F4, F2, L6, G8	Power	AGND	Analog supply ground
K5	Power	AGND_PLL	PLL supply ground
K3	Power	AGND_DAC	DAC supply ground
E1, J1	Power	GNDQ_MEM	SDRAM output buffer supply ground
F3, H9, H8	Power	GND_MEM	SDRAM device supply ground

Table 2: Pin name descriptions (LQFP80 package)

Pin #	Type	Symbol	Description
52 - 67 70 - 77	In	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
79	Inout	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
78	Inout	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
80	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. CSB signal input of CPU interface The amplitude will be 0 to VDDIO.
5	In	AS	Chip address select 0: 76h 1: 75h
4	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V. Reserved pin.
6	In	ResetB	Reset * Input When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
38	Inout	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resister is required.
39	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resister is required.
29	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
27	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
25	Out	DAC2	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
31	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
35	In	XI	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel

Pin #	Type	Symbol	Description
			resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
36	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
50	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
2	Out	VSO	Vertical sync signal output, The amplitude of this pin is from 0 to AVDD
1	Out	HSO	Horizontal sync signal output, The amplitude of this pin is from 0 to AVDD
3	Out	CSYNC	Composite sync output, The amplitude of this pin is from 0 to AVDD
51	Power	VDDIO	IO supply voltage (1.2-3.3V)
69	Power	DVDD	Digital supply voltage (1.8V)
8 12 37 49	Power	AVDD	Analog supply voltage
33	Power	AVDD_PLL	PLL supply voltage
24 28	Power	AVDD_DAC	DAC power supply
10 18	Power	VDDQ_MEM	SDRAM output buffer supply voltage
14 44 45	Power	VDD_MEM	SDRAM device supply voltage
68	Power	DGND	Digital supply ground
7 11 34 48	Power	AGND	Analog supply ground
32	Power	AGND_PLL	PLL supply ground
26 30	Power	AGND_DAC	DAC supply ground
9 19	Power	GNDQ_MEM	SDRAM output buffer supply ground
13 46 47	Power	GND_MEM	SDRAM device supply ground

2.0 Functional description

2.1 Input interface

2.1.1 Overview

Five distinct methods of transferring data to the CH7025/CH7026 are described. They are:

1. Unitary data, clock input at 1X the pixel rate
2. Multiplexed data, clock input at 1X of pixel rate
3. Multiplexed data, clock input at 2X of pixel rate
4. Multiplexed data, clock input at 3X of pixel rate
5. 8/16/24 bit CPU interface

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7025/CH7026 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X or 3X pixel rate the data applied to the CH7025/CH7026 is latched with one edge of the clock (also known as single edge transfer mode or SDR). For the unitary data, clock at 1X pixel rate, the data applied to the CH7025/CH7026 is latched with one edge of the clock .The polarity of the pixel clock can be reversed under serial port control. Hsync and Vsync can be input individually or embedded into data signal such as BT656 input format.

2.1.2 Input Clock and Data Timing Diagram

Figure 6 below shows the timing diagram for input data and clocks. The first XCLK waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in later section.

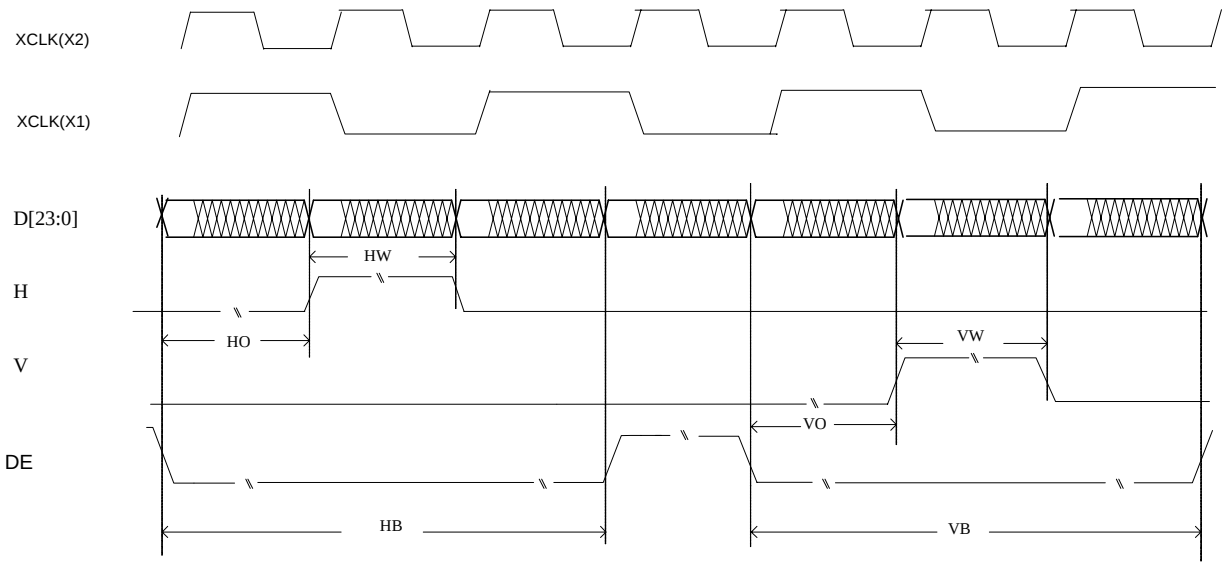

Figure 4: Clock, Data and Interface Timing

2.1.3 Input data voltage

The voltage level of input pins D[23:0], H/WEB, V, DE/CSB, SPC, SPD are from 0 to VDDIO. These pins support two input mode, one is CMOS mode, and the other is pseudo differential mode. The default is CMOS mode with CMOS level on these pins. When control bit **DIFFEN** is high, the input is pseudo differential mode that uses a reference voltage (VREF) to compare with input voltage and decide input logic value. The VREF value can be 80%, 70%, 60% and 50% of VDDIO value, referring to **VRTM[1:0]**. The pseudo differential mode can accept the wide range of the input voltage level from 1.2v to 3.3v, while the CMOS mode can accept 1.8v to 3.3v input voltage.

2.1.4 Input data format

The following table indicates the supported input data format by CH7025/CH7026.

Table 3: Input data format

MULTI		IDF	D[23:16]	D[15:8]	D[7:0]
0		0	R[7:0]	G[7:0]	B[7:0]
		1	2'b00,R[5:0]	2'b00,G[5:0]	2'b00,B[5:0]
		2	3'b000,R[4:0]	2'b00,G[5:0]	3'b000,B[4:0]
		3	3'b000,R[4:0]	3'b000,G[4:0]	3'b000,B[4:0]
		4	R[7:3],G[7:5]	R[2:0],G[1],G[4:2], B[7]	B[6:3],G[0],B[2:0]
		5	8'h00	Y[7:0]	C[7:0]
		6	4'h0, Y[9:6]	Y[5:0],C[9:8]	C[7:0]
		7	Y[7:0]	Cb[7:0]	Cr[7:0]
		9	6'h00, R[5:4]	R[3:0],G[5:2]	G[1:0],B[5:0]
		10	8'h00	R[4:0],G[5:3]	G[2:0],B[4:0]
		11	8'h00	1'b0, R[4:0],G[4:3]	G[2:0],B[4:0]
1	PA	0		4’h0, R[7:4]	R[3:0],G[7:4]
	PB			4’h0, G[3:0]	B[7:0]
	PA	1		7’h00, R[5]	R[4:0],G[5,3]
	PB			7’h00, G[2]	G[1:0],B[5:0]
	PA	2			R[4:0],G[5,3]
	PB				G[2:0],B[4:0]
	PA	3			1’b0,R[4:0],G[4,3]
	PB				G[2:0],B[4:0]
	PA	4		4’h0, R[7:4]	R[3],G[7:5],R[2:0],G[1]
	PB			4’h0, G[4:2], B [7]	B[6:3],G[0],B[2:0]
	PA	5			Y[7:0]
	PB				C[7:0]
	PA	6		6’h00, Y[9:8]	Y[7:0]
	PB			6’h00, C[9:8]	C[7:0]
	PA	7		4’h0, Y[7:4]	Y[3:0],Cb[7:4]
	PB			4’h0, Cb[3:0]	Cr[7:0]
2	PA	0			R[7:0]
	PB				G[7:0]
	PC				B[7:0]
	PA	7			Y[7:0]
	PB				Cb[7:0]
	PC				Cr[7:0]

(PA,PB,PC represent the parts of one pixel data)

IDF[3:0] describes the major input data format that CH7025/CH7026 accepts. They are:

IDF = 0: 888 RGB input
IDF = 1: 666 RGB input
IDF = 2: 565 RGB input
IDF = 3: 555 RGB input
IDF = 4: DVO input
IDF = 5: 8-bit YCbCr4:2:2 input
IDF = 6: 10-bit YCbCr4:2:2 input
IDF = 7: 8-bit YCbCr4:4:4 input
IDF = 9: Consecutive aligned 666 RGB input
IDF = 10: Consecutive aligned 565 RGB input
IDF = 11: Consecutive aligned 555 RGB input

Table 3 above describe the 24-bit input data format under unitary mode. For multiplexed input, input data needs to be de-multiplexed to unitary input first then this table can be applied. The multiplexed input data format is shown in figure below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCbCr formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; PA and PB) will contain a complete pixel. (3X input has the similar feature)

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (PA) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCbCr data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCbCr formats.

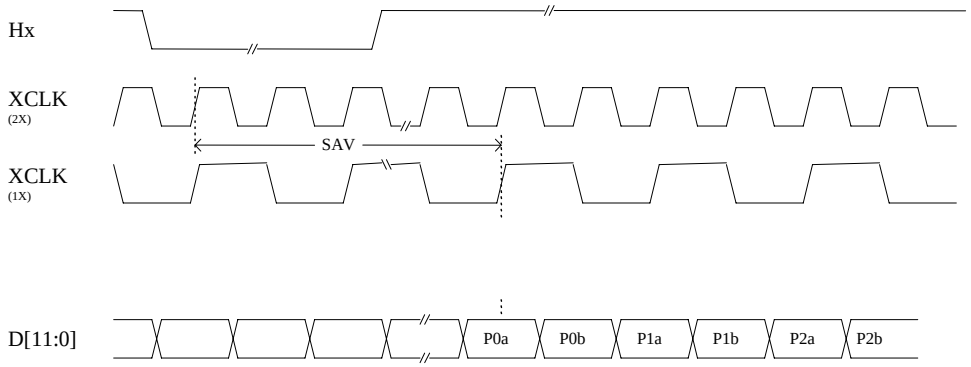

Figure 5: 12-bit Multiplexed Input Data Formats

In YCbCr 4:2:2 with embedded sync mode, the hardware can detect the connect error and correct it automatically, for example, if the input P14 and P15 are a group, but you take P13 and P14 as a group, the hardware can detect this error and correct it by run-in code.

2.2 Chip output

2.2.1 TV output

The CH7025/CH7026 support the following output formats:

Table 4: Supported SDTV standards

No.	Standards	Field Rate (Hz)	Total	Scan Type
0	NTSC-M	60/1.001	858x525	Interlaced
1	NTSC-J	60/1.001	858x525	Interlaced
2	NTSC-443	60/1.001	858x525	Interlaced
3	PAL-B/D/G/H/I	50	864x625	Interlaced
4	PAL-M	60/1.001	858x525	Interlaced
5	PAL_N	50	864x625	Interlaced
6	PAL-Nc	50	864x625	Interlaced
7	PAL_60	60/1.001	858x525	Interlaced

Table 5: Supported EDTV/HDTV standards

Standards		Field/Frame Rate(Hz)	Total	Active	Clock(MHz)	Scan Type
480/60p	SMPTE293M EIA770.2A	60/1.001	858x525 or 1716x525	720x480	27 or 54	Progressive
576/50p	ITU-R BT1358	50	864x625 or 1728x625	720x576	27 or 54	Progressive
720/60p	SMPTE296M	60 or 60/1.001	1650x750	1280x720	74.25 or 74.176	Progressive
720/50p	SMPTE296M	50	1980x750	1280x720	74.25	Progressive
1080/60i	SMPTE274M	60 or 60/1.001	2200x1125	1920x1080	74.25 or 74.176	Interlaced
1080/50i	SMPTE274M	50	2640x1125	1920x1080	74.25	Interlaced
1080/50i	SMPTE295M	50	2376x1250	1920x1080	74.25	Interlaced

CVBS, S-video, YPbPr and analog RGB output are supported, when output analog RGB, composite sync output is available.

2.2.2 VGA output

CH7025/CH7026 also supports analog RGB output through video DACs. Typically used resolution is 800x600, 856x480, 800x480 or 640x480. Vertical sync and horizontal sync signal can be provided. Composite sync output is also supported. The type of composite sync can be programmed through register map.

Table 6: Composite sync type

CSSEL[2:0]	Composite sync type
0	Vsync XOR Hsync
1	Vsync OR Hsync
2	Vsync AND Hsync

2.2.3 Video DAC output

The DAC output is configured by the register bits **VFMT[2:0]**. **DACS[1:0]** bits are used to control the multiple output format i.e. dual or triple CVBS output, dual CVBS and S-Video output and etc. **DACSP[2:0]** bits are to swap the DAC output sequence such as CVBS, S-Video or S-Video, CVBS. Detailed information of these bits are described in register bits description section of this document. **Table 7** below lists the DAC output configurations of the CH7025/CH7026:

Table 7: Video DAC Configurations for CH7025/CH7026

DAC0	DAC1	DAC2
CVBS	Y	C
CVBS	CVBS	0
CVBS	CVBS	CVBS
Y(R)	Pb(G)	Pr(B)

2.2.4 DAC single/double termination

The DAC output of CH7025/CH7026 can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the effect of the cable. See also the description of register bit **SEL_R**.

2.2.5 TV connection detect

CH7025/CH7026 can detect the TV connection by setting register SPPSNS. It can detect which DAC are connected, short to ground or not connected.

2.2.6 Picture enhancement

The CH7025/CH7026 has the capability of vertical and horizontal output picture position adjustment. It can automatically put the picture in the display center, and the vertical or horizontal position is also programmable through user input. And also it can provide brightness, contrast, hue, saturation adjustment and text enhancement functions. (For analog RGB output, only brightness and contrast adjustment is available).

CH7025/CH7026 also supports vertical or horizontal flip and rotation (0, 90, 180 and 270 degree) functions.

2.2.7 Color Sub-carrier Generation

CH7025/CH7026 has two ways to generate the color sub-carrier frequency. If the **GCLK** from the graphics controller has a steady center frequency and very small jitters, the sub-carrier can be derived from the **GCLK**. However, since even a ±0.01% sub-carrier frequency variation is enough to cause some TV to lose color lock, CH7025/CH7026 has the ability to generate the sub-carrier frequency from the crystal when the **GCLK** from the graphics device cannot meet the requirement. In this case, the crystal has to be present. In other words, the only configuration where the off-chip crystal can be removed is when slave mode is used and the graphics controller provides **GCLK** with required characteristics.

In addition, CH7025/CH7026 has the capability to gen-lock the color sub-carrier with Vsync. Also, it has the ability to operate in a “stop dot crawl” mode for NTSC CVBS output when the first sub-carrier generation method is used.

2.2.8 ITU-R BT.470 Compliance

The SDTV output of CH7025/CH7026 is mostly compliant with ITU-R BT.470 standard except for the items below.

- The frequencies of horizontal sync, vertical sync, and color sub-carrier depend on the quality of **GCLK** from graphics controller and/or the off-chip crystal.
- It is assumed that gamma correction, if required, is performed in the graphics device.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements. However, they may have a small variation depending on the actual input and output format.
- The actual bandwidths of the luminance and chrominance signals depend on the input resolution and the filter selection.

2.3 Testing Functions

2.3.1 Test pattern select

Setting TSTP[4:0] of 04h on the second page of register map can select different video patterns that go through datapath, according to the following table (TEST bit5 of 04h on the second page has to be 1 to enable test mode). TSYNC is to select which sync will be used internally generated sync or external input sync.

Table 8: Test pattern selection

TSTP[3:0]	Test pattern
0	Black
1	White
2	Vertical ramp
3	Horizontal ramp
4	Color bar
5	One pixel wide color bar
6	Zigzag
7	Reserved
8	One black and one white frame
9	Black lines on white background

When TSTP = 9, TSTW[2:0] is used to determine the interval in lines between two black lines with white background.

2.3.2 SDRAM power down

Generally, SDRAM can have two kinds of power down modes. One is power down mode, the other is deep power down mode. For power down mode, by dropping the CKE signal from high to low and holding CS signal high, then SDRAM goes into the power down mode. All data contents will be held in the bank. For deep power down mode, a command is required to issued. There is a bit called MEMPD in register map. It can be used to enable the deep power mode. During deep power mode, all the data in memory banks will be lost, and the SDRAM leakage current is less than 1uA. **An very important thing required to be noted here is that not all the SDRAM parts support either power down or deep power down mode**. In these cases, even CH7025/CH7026 enters into power down, the leakage current is still large (>100uA). This current is primarily derived from the SDRAM die. For detailed information about power down of SDRAM, please refer to SDRAM vendors' specifications.

3.0 Register control

The CH7025/CH7026 is controlled via a serial control port. The serial bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written into under all power down modes. The device should retain all register values during power down modes.

3.1 Control Registers Index

Table 9: Control Registers Index

Name	Description	Address	Page
A1[31:0]	Divider ratio for A/2^32	4Dh – 50H	1
A2[7:0]	Divider ratio for 1/A	51h	1
ACIV	Sub-carrier generation method	41h	1
AH_LB	Multiplexed input data alignment	0Bh	1
BLK_H[6:0]	Define the ceiling integer of HAI/16 , set it when HAI larger than 720	69h	1
BPSEL	TV bypass clock selection	55h	1
BRI[7:0]	Brightness control value	31h	1
CBW	Chroma filter bandwidth selection	3Dh	1
CFBP	Chroma filter bypass enable	3Fh	1
CGMSDATA[13:0]	CGMS data 14bits	6Dh – 71H	1
CGMSEN	CGMS enable	5FH	1
CKINV	Clock inversion bit for latch clock	75h	1
CPUEN	CPU interface enable	0Bh	1
CSBINV	Inversion bit for CSB signal of CPU interface	0Eh	1
CSSEL[2:0]	Composite sync type selector	08h	1
CTA[6:0]	Contrast control value	30h	1
DACAT0[1:0]	DAC connection status for DAC0	7Fh	1
DACAT1[1:0]	DAC connection status for DAC1	7Fh	1
DACAT2[1:0]	DAC connection status for DAC2	7Fh	1
DACS[1:0]	Multiple TV output configuration	0Ah	1
DBP	Dither function bypass	3Eh	1
DACPD[2:0]	DAC power down bits	04h	1
DACSP[2:0]	DAC output sequence swap bits	0Ah	1
DEPO_I	Input DE signal polarity	07h	1
DEPO_O	Output DE signal polarity	07h	1
DES	Using encoded sync	09h	1
DID[7:0]	Device ID	00h	1
DIFFEN[1:0]	Differential input mode enable	76h	1
DISPON	Clock signal selection for DAC detection	7Dh	1
DNSMPEN	4:3 down sample enable	0Eh	1
DOTB	Dot crawl enable	40h	1
DPCKN4	Divider value	53h	1
DPSEL[1:0]	Pixel and latching clock selection	55h	1
DPD	Digital power down	04h	1
DVALID	SDRAM ready signal	7Eh	1
EDGE_ENH	Sharpen the edge of output picture	12h	1
FIELDSW	Switch the turn of odd/even field of input video	15H	1
FPD	Full power down	04h	1
GSEL	Graphics clock selection	55h	1
HAI[10:0]	Input total active pixels per line	0Fh, 10h	1

Name	Description	Address	Page
HAO[10:0]	Output total active pixels per line	1Bh, 1Ch	1
HDTVEN	HDTV output enable	12h	1
HDVDOFMT[4:0]	HDTV output video format	5Ch	1
HEND[10:0]	Horizontal end position for image zoom feature	27h, 29h	1
HFLIP	Horizontal flip	2Dh	1
HFLN_EN	Enable half line difference for TV scaling	32h	1
HIGH	Non-multiplexed input data alignment	0Ch	1
HO[10:0]	Input horizontal sync offset value	12h, 13h	1
HOO[10:0]	Output horizontal sync offset value	1Eh, 1Fh	1
HP[11:0]	Horizontal position adjustment value	35h – 36h	1
HPO_I	Input HS polarity	07h	1
HPO_O	Output HS polarity	07h	1
HREPT	Enable non-interpolation mode for horizontal scaling	0Fh	1
HST[10:0]	Horizontal start position for image zoom feature	27h, 28h	1
HTI[10:0]	Input total pixels per line	0Fh, 11h	1
HTO[11:0]	Output total pixels per line	1Bh, 1Dh	1
HUE[6:0]	HUE adjustment value	2Eh	1
HVAUTO	Using self countered timing values	0Fh	1
HW[10:0]	Input horizontal sync width	12h, 14h	1
HWO[10:0]	Output horizontal sync width	1Eh, 20h	1
IDF[3:0]	Input data format	0Ch	1
IMGZOOM	Image zoom feature enable	27h	1
INTLACE	Interlaced input indicator	0Bh	1
LNSEL[1:0]	The number of line used for vertical scaling selection	09h	1
MEMINIT	Reset SDRAM to initialization state	06h	1
MEMPD	Memory deep power enable	05h	1
MONOB	Mono output enable	3Dh	1
MULTI[1:0]	Multiplexed input type selection	0Bh	1
MVMOD[1:0]	Macrovision mode selection	56h	1
MVTSTEN	Macrovision test enable	56h	1
N0[7:0]	N0 value for MV	57h	1
N1[5:0]	N1 value for MV	58h	1
N10[[5:0]	N10 value for MV	61h	1
N11[14:0]	N11 value for MV	62h – 63h	1
N12[14:0]	N12 value for MV	64h – 65h	1
N13[7:0]	N13 value for MV	66h	1
N14[7:0]	N14 value for MV	67h	1
N15[7:0]	N15 value for MV	68h	1
N16	N16 value for MV	69h	1
N17[3:0]	N17 value for MV	6Ah	1
N18[3:0]	N18 value for MV	6Bh	1
N19[3:0]	N19 value for MV	6Ch	1
N2[5:0]	N2 value for MV	59h	1
N20[2:0]	N20 value for MV	6Dh	1
N21[9:0]	N21 value for MV	6Eh, 6Fh	1
N22	N22 value for MV	6Eh	1
N3[5:0]	N3 value for MV	5Ah	1
N4[5:0]	N4 value for MV	5Bh	1
N5[2:0]	N5 value for MV	5Ch	1
N6[2:0]	N6 value for MV	5Dh	1

Name	Description	Address	Page
N7[1:0]	N7 value for MV	5Eh	1
N8[5:0]	N8 value for MV	5Fh	1
N9[5:0]	N9 value for MV	60h	1
PBPREN	YPBPR output enable	0Dh	1
PEN	Enable customize SDTV format to decrease flicker	58h	1
PLL1N1[2:0]	PLL1 pre-divider ratio control	52h	1
PLL1N2[2:0]	PLL1 feedback divider 2 control	52h	1
PLL1N3[2:0]	PLL1 feedback divider 3 control	53h	1
PLL2N5[2:0]	PLL2 post-divider ratio control	53h	1
PLL3N6[1:0]	PLL3 pre-divider ratio control	54h	1
PLL3N7	PLL3 to DPCK divider 7 ratio control	54h	1
PLL3N8[1:0]	PLL3 to DPCK divider 8 ratio control	54h	1
POS3X[1:0]	3x input data position select	0Bh	1
DAC0C1[6:0]	A value of AX+B on DAC0	37h	1
DAC0C2[7:0]	B value of AX+B on DAC0	38h	1
DAC1C1[6:0]	A value of AX+B on DAC1	39h	1
DAC1C2[7:0]	B value of AX+B on DAC1	3Ah	1
DAC2C1[6:0]	A value of AX+B adjustment on DAC2	3Bh	1
DAC2C2[7:0]	B value of AX+B adjustment on DAC2	3Ch	1
RGBEN	Enable RGB output of SDTV	32h	1
RESETDB	Device reset	02h	1
REVERSE	Input data is LSB first	0Bh	1
RFLOPEN	Rotation control	06h	1
ROTATE[1:0]	Rotation selection	2Dh	1
SAT[6:0]	Saturation control value	2Fh	1
SCREQ[26:0]	Value for calculate sub-carrier frequency from crystal	42h – 45h	1
SEL_R	Single or double termination selection	77h	1
SETEN	Enable to manually set de-flicker filter	21H	1
SPPSNS	DAC detection enable	7Dh	1
STOP	Stop signal	06h	1
SWAP[2:0]	Swapping bit for RGB sequence	0Ch	1
SWP_PAPB	P0a or P0b first selector	0Eh	1
SWP_CBCR	Swap CbCr for BT656 input	0Eh	1
SWRDIM	Enable immediately switch bank for SDRAM reading	06h	1
SYO	Enabling sync output	09h	1
TE[2:0]	Text enhancement	32h	1
TV_BP	TV bypass enable	15H	1
VAI[10:0]	Input total active lines per frame	15h, 16h	1
VAO[10:0]	Output total active lines per frame	21h, 22h	1
VEND[10:0]	Vertical end position for image zoom feature	2Ah, 2Bh	1
VFFSPP[2:0]	Vertical scaling filter selection	3Dh	1
VFLIP	Vertical flip	2Dh	1
VFMT[3:0]	Output video format	0Dh	1
VID[7:0]	Revision ID	01h	1
VO[10:0]	Input vertical sync offset	18h, 19h	1
VOO[10:0]	Output vertical sync offset	24h, 25h	1
VP[11:0]	Vertical position adjustment value	33h – 34h	1
VPO_I	Input VS polarity	07h	1
VPO_O	Output VS polarity	07h	1
VREPT	enable non-interpolation mode for vertical scaling.	30h	1

Name	Description	Address	Page
VRTM[1:0]	IO differential mode vref trimming	76h	1
VSINV	Inversion for VSYNC signal of CPU interface	0Eh	1
VST[10:0]	Vertical start position for image zoom feature	2Ah, 2Bh	1
VTI[10:0]	Input total lines per frame	15h, 17h	1
VTO[10:0]	Output total lines per frame	21h, 23h	1
VW[10:0]	Input vertical sync width	18h, 19h	1
VWO[10:0]	Output vertical sync width	24h, 26h	1
WEBINV	Inversion for WEB signal of CPU interface	0Eh	1
WRFAST	Frame write fast indicator	0Dh	1
WSSEN	WSS enable	5FH	1
XCH	Multiplexed and non-multiplex clock selector	55h	1
XSEL	Using external crystal as reference to generate sub-carrier	41h	1
XTAL[3:0]	Crystal frequency selection	41h	1
YC2RGB	YCbCr to RGB output enable	0Dh	1
YCV[2:0]	CVBS luma filter select	3Eh	1

3.2 Control Registers Map

Table 10: Serial Port Register Map (Page 1)

REG	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
01h	VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]
02h							RESETIB	RESETDB
03h								PG
04h			DACPD[2]	DACPD[1]	DACPD[0]		DPD	FPD
05h						MEMPD		
06h				RFLOPEN	SWRDIM		MEMINIT	STOP
07h			DEPO_O	HPO_O	VPO_O	DEPO_I	HPO_I	VPO_I
08h		CSSEL[2]	CSSEL[1]	CSSEL[0]				
09h	LNSEL[1]	LNSEL[0]			SYO	DES		
0Ah				DACS[1]	DACS[0]	DACSP[2]	DACSP[1]	DACSP[0]
0Bh	INTLACE	CPUEN	POS3X[1]	POS3X[0]	MULTI[1]	MULTI[0]	AH_LB	REVERSE
0Ch	HIGH	SWAP[2]	SWAP[1]	SWAP[0]	IDF[3]	IDF[2]	IDF[1]	IDF[0]
0Dh	WRFAST	PBPREN	YC2RGB		VFMT[3]	VFMT[2]	VFMT[1]	VFMT[0]
0Eh	CSBINV	VSINV	WEBINV	SWP_CBCR	SWP_PAPB	DNSMPEN		
0Fh	HVAUTO	HREPT	HTI[10]	HTI[9]	HTI[8]	HAI[10]	HAI[9]	HAI[8]
10h	HAI[7]	HAI[6]	HAI[5]	HAI[4]	HAI[3]	HAI[2]	HAI[1]	HAI[0]
11h	HTI[7]	HTI[6]	HTI[5]	HTI[4]	HTI[3]	HTI[2]	HTI[1]	HTI[0]
12h	HDTVEN	EDGE_ENH	HW[10]	HW[9]	HW[8]	HO[10]	HO[9]	HO[8]
13h	HO[7]	HO[6]	HO[5]	HO[4]	HO[3]	HO[2]	HO[1]	HO[0]
14h	HW[7]	HW[6]	HW[5]	HW[4]	HW[3]	HW[2]	HW[1]	HW[0]
15h	FIELDSW	TV_BP	VTI[10]	VTI[9]	VTI[8]	VAI[10]	VAI[9]	VAI[8]
16h	VAI[7]	VAI[6]	VAI[5]	VAI[4]	VAI[3]	VAI[2]	VAI[1]	VAI[0]
17h	VTI[7]	VTI[6]	VTI[5]	VTI[4]	VTI[3]	VTI[2]	VTI[1]	VTI[0]
18h			VW[10]	VW[9]	VW[8]	VO[10]	VO[9]	VO[8]
19h	VO[7]	VO[6]	VO[5]	VO[4]	VO[3]	VO[2]	VO[1]	VO[0]
1Ah	VW[7]	VW[6]	VW[5]	VW[4]	VW[3]	VW[2]	VW[1]	VW[0]
1Bh		HTO[11]	HTO[10]	HTO[9]	HTO[8]	HAO[10]	HAO[9]	HAO[8]

REG	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1Ch	HAO[7]	HAO[6]	HAO[5]	HAO[4]	HAO[3]	HAO[2]	HAO[1]	HAO[0]
1Dh	HTO[7]	HTO[6]	HTO[5]	HTO[4]	HTO[3]	HTO[2]	HTO[1]	HTO[0]
1Eh			HWO[10]	HWO[9]	HWO[8]	HOO[10]	HOO[9]	HOO[8]
1Fh	HOO[7]	HOO[6]	HOO[5]	HOO[4]	HOO[3]	HOO[2]	HOO[1]	HOO[0]
20h	HWO[7]	HWO[6]	HWO[5]	HWO[4]	HWO[3]	HWO[2]	HWO[1]	HWO[0]
21h		SETEN	VTO[10]	VTO[9]	VTO[8]	VAO[10]	VAO[9]	VAO[8]
22h	VAO[7]	VAO[6]	VAO[5]	VAO[4]	VAO[3]	VAO[2]	VAO[1]	VAO[0]
23h	VTO[7]	VTO[6]	VTO[5]	VTO[4]	VTO[3]	VTO[2]	VTO[1]	VTO[0]
24h			VWO[10]	VWO[9]	VWO[8]	VOO[10]	VOO[9]	VOO[8]
25h	VOO[7]	VOO[6]	VOO[5]	VOO[4]	VOO[3]	VOO[2]	VOO[1]	VOO[0]
26h	VWO[7]	VWO[6]	VWO[5]	VWO[4]	VWO[3]	VWO[2]	VWO[1]	VWO[0]
27h	IMGZOOM		HEND[10]	HEND[9]	HEND[8]	HST[10]	HST[9]	HST[8]
28h	HST[7]	HST[6]	HST[5]	HST[4]	HST[3]	HST[2]	HST[1]	HST[0]
29h	HEND[7]	HEND[6]	HEND[5]	HEND[4]	HEND[3]	HEND[2]	HEND[1]	HEND[0]
2Ah			VEND[10]	VEND[9]	VEND[8]	VST[10]	VST[9]	VST[8]
2Bh	VST[7]	VST[6]	VST[5]	VST[4]	VST[3]	VST[2]	VST[1]	VST[0]
2Ch	VEND[7]	VEND[6]	VEND[5]	VEND[4]	VEND[3]	VEND[2]	VEND[1]	VEND[0]
2Dh					VFLIP	HFLIP	ROTATE[1]	ROTATE[0]
2Eh		HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]
2Fh		SAT[6]	SAT[5]	SAT[4]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
30h	VREPT	CTA[6]	CTA[5]	CTA[4]	CTA[3]	CTA[2]	CTA[1]	CTA[0]
31h	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]
32h	RGBEN	HFLN_EN				TE[2]	TE[1]	TE[0]
33h					VP[11]	VP[10]	VP[9]	VP[8]
34h	VP[7]	VP[6]	VP[5]	VP[4]	VP[3]	VP[2]	VP[1]	VP[0]
35h					HP[11]	HP[10]	HP[9]	HP[8]
36h	HP[7]	HP[6]	HP[5]	HP[4]	HP[3]	HP[2]	HP[1]	HP[0]
37h		DAC0C1[6]	DAC0C1[5]	DAC0C1[4]	DAC0C1[3]	DAC0C1[2]	DAC0C1[1]	DAC0C1[0]
38h	DAC0C2[7]	DAC0C2[6]	DAC0C2[5]	DAC0C2[4]	DAC0C2[3]	DAC0C2[2]	DAC0C2[1]	DAC0C2[0]
39h		DAC1C1[6]	DAC1C1[5]	DAC1C1[4]	DAC1C1[3]	DAC1C1[2]	DAC1C1[1]	DAC1C1[0]
3Ah	DAC1C2[7]	DAC1C2[6]	DAC1C2[5]	DAC1C2[4]	DAC1C2[3]	DAC1C2[2]	DAC1C2[1]	DAC1C2[0]
3Bh		DAC2C1[6]	DAC2C1[5]	DAC2C1[4]	DAC2C1[3]	DAC2C1[2]	DAC2C1[1]	DAC2C1[0]
3Ch	DAC2C2[7]	DAC2C2[6]	DAC2C2[5]	DAC2C2[4]	DAC2C2[3]	DAC2C2[2]	DAC2C2[1]	DAC2C2[0]
3Dh	MONOB		CBW			VFFSPP[2]	VFFSPP[1]	VFFSPP[0]
3Eh	DBP					YCV[2]	YCV[1]	YCV[0]
3Fh	CFBP							
40h					DOTB			
41h	XSEL	XTAL[3]	XTAL[2]	XTAL[1]	XTAL[0]	ACIV		
42h						SCREQ[26]	SCREQ[25]	SCREQ[24]
43h	SCREQ[23]	SCREQ[22]	SCREQ[21]	SCREQ[20]	SCREQ[19]	SCREQ[18]	SCREQ[17]	SCREQ[16]
44h	SCREQ[15]	SCREQ[14]	SCREQ[13]	SCREQ[12]	SCREQ[11]	SCREQ[10]	SCREQ[9]	SCREQ[8]
45h	SCREQ[7]	SCREQ[6]	SCREQ[5]	SCREQ[4]	SCREQ[3]	SCREQ[2]	SCREQ[1]	SCREQ[0]
4Dh	A1[31]	A1[30]	A1[29]	A1[28]	A1[27]	A1[26]	A1[25]	A1[24]
4Eh	A1[23]	A1[22]	A1[21]	A1[20]	A1[19]	A1[18]	A1[17]	A1[16]
4Fh	A1[15]	A1[14]	A1[13]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
50h	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
51h	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]	A2[2]	A2[1]	A2[0]
52h			PLL1N2[2]	PLL1N2[1]	PLL1N2[0]	PLL1N1[2]	PLL1N1[1]	PLL1N1[0]
53h		DPCKN4	PLL2N5[2]	PLL2N5[1]	PLL2N5[0]	PLL1N3[2]	PLL1N3[1]	PLL1N3[0]
54h				PLL3N8[1]	PLL3N8[0]	PLL3N7	PLL3N6[1]	PLL3N6[0]

REG	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
55h				XCH	BPSEL	DPSEL[1]	DPSEL[0]	GSEL
56h					MVTSTEN		MVMOD[1]	MVMOD[0]
57h	N0[7]	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]
58h	PEN		N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
59h			N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
5Ah			N3[5]	N3[4]	N3[3]	N3[2]	N3[1]	N3[0]
5Bh			N4[5]	N4[4]	N4[3]	N4[2]	N4[1]	N4[0]
5Ch	HDVDOFMT [4]	HDVDOFMT [3]	HDVDOFMT [2]	HDVDOFMT [1]	HDVDOFMT [0]	N5[2]	N5[1]	N5[0]
5Dh						N6[2]	N6[1]	N6[0]
5Eh							N7[1]	N7[0]
5Fh	CGMSEN[5]	CGMSEN[4]	N8[5]	N8[4]	N8[3]	N8[2]	N8[1]	N8[0]
60h	CGMSEN[3]	CGMSEN[2]	N9[5]	N9[4]	N9[3]	N9[2]	N9[1]	N9[0]
61h	CGMSEN[1]	CGMSEN[0]	N10[5]	N10[4]	N10[3]	N10[2]	N10[1]	N10[0]
62h		N11[14]	N11[13]	N11[12]	N11[11]	N11[10]	N11[9]	N11[8]
63h	N11[7]	N11[6]	N11[5]	N11[4]	N11[3]	N11[2]	N11[1]	N11[0]
64h		N12[14]	N12[13]	N12[12]	N12[11]	N12[10]	N12[9]	N12[8]
65h	N12[7]	N12[6]	N12[5]	N12[4]	N12[3]	N12[2]	N12[1]	N12[0]
66h	N13[7]	N13[6]	N13[5]	N13[4]	N13[3]	N13[2]	N13[1]	N13[0]
67h	N14[7]	N14[6]	N14[5]	N14[4]	N14[3]	N14[2]	N14[1]	N14[0]
68h	N15[7]	N15[6]	N15[5]	N15[4]	N15[3]	N15[2]	N15[1]	N15[0]
69h	BLK_H[6]	BLK_H[5]	BLK_H[4]	BLK_H[3]	BLK_H[2]	BLK_H[1]	BLK_H[0]	N16
6Ah					N17[3]	N17[2]	N17[1]	N17[0]
6Bh					N18[3]	N18[2]	N18[1]	N18[0]
6Ch					N19[3]	N19[2]	N19[1]	N19[0]
6Dh	CGMSDATA[13]	CGMSDATA[12]	CGMSDATA[11]	CGMSDATA[10]	CGMSDATA[9]	N20[2]	N20[1]	N20[0]
6Eh	N22	CGMSDATA[8]	CGMSDATA[7]	CGMSDATA[6]	CGMSDATA[5]	CGMSDATA[4]	N21[9]	N21[8]
6Fh	N21[7]	N21[6]	N21[5]	N21[4]	N21[3]	N21[2]	N21[1]	N21[0]
70h	CGMSDATA[3]	CGMSDATA[2]						
71h	CGMSDATA[1]	CGMSDATA[0]						
75h								CKINV
76h					VRTM[1]	VRTM[0]	DIFFEN[1]	DIFFEN[0]
77h		SEL_R						
7Dh							DISPON	SPPSNS
7Eh					DVALID			
7Fh			DACAT2[1]	DACAT2[0]	DACAT1[1]	DACAT1[0]	DACAT0[1]	DACAT0[0]

Table 11: Serial Port Register Map (Page 2)

REG	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h								PG
04h			TEST	TSYNC	TSTP[3]	TSTP[2]	TSTP[1]	TSTP[0]

3.3 Register Descriptions

Device ID Register **Address: 00h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	1	0	1	0	1	0	1

DID[7:0] (bits 7-0) is the device ID. It is read-only and the value is 55h for CH7025. 54h for CH7026.

Revision ID Register **Address: 01h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

VID[7:0] (bits 7-0) is the revision ID.

Reset Register **Address: 02h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RESETIB	RESETDB
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	1

RESETIB (bit 1) resets all control registers. When RESETIB is '0' the control registers are reset to the default values. When RESETIB is '1' the control registers operate normally. The control registers are also reset at power on by an internally generated power on reset signal.

RESETDB (bit 0) resets the datapath. When RESETDB is '0' the datapath is reset. When RESETDB is '1' the datapath is enabled. The datapath is also reset at power on by an internally generated power-on-reset signal.

Page selection Register **Address: 03h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PG
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

PG (bit 0) is for page selection. This register is physically the same for both page 1 and page 2.

0: 1st page

1: 2nd page

Power state Register 1 **Address: 04h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	DACPD[2]	DACPD[1]	DACPD[0]	Reserved	DPD	FPD
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

DACPD[2:0] (bit 5-3) is power down control bits for DACs, referred as following table.

Table 12 : DAC power down control bits

DACSP[2:0]	DAC0	DAC1	DAC2
0	DACPD[0]	DACPD[1]	DACPD[2]
1	DACPD[1]	DACPD[0]	DACPD[2]
2	DACPD[0]	DACPD[2]	DACPD[1]
3	DACPD[2]	DACPD[0]	DACPD[1]
4	DACPD[1]	DACPD[2]	DACPD[0]
5	DACPD[2]	DACPD[1]	DACPD[0]

DPD (bit 1) is power down control for digital path. When DPD is "1", digital path is powered down.

FPD (bit 0) controls the power on/off state. When FPD is "0", the CH7025/CH7026 is in power-up state. When FPD is "1", the CH7025/CH7026 is in power-down state. At power-down state, the CH7025/CH7026 accepts SPP access.

Power state Register 2 **Address: 05h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	MEMPD	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

MEMPD (bit 2) is the memory power down enable bit. Once it's high. SDRAM will enter into deep power down mode.

SDRAM and Scaler enable Register **Address: 06h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	RFLOPEN	SWRDIM	Reserved	MEMINIT	STOP
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	1	0	0	1	1

RFLOPEN(bit 4) is to enable rotation and flip to be implemented between writing frame buffer and reading frame buffer in back and forth mode. When input frame active line is bigger than 720, then should disable the bit.

SWRDIM(bit3) is to enable immediately switch bank for SDRAM reading. When input frame line is bigger than 720, then should enable the bit.

MEMINIT (bit 1) is to set SDRAM in initialization state. Once it goes low, initialization sequence is beginning.

STOP (bit 0) is to stop the scaler and SDRAM control operation. When it's high, these logics are stopped. This bit is required for programming the chip.

Sync configuration Register **Address: 07h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	DEPO_O	HPO_O	VPO_O	DEPO_I	HPO_I	VPO_I
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	1	1	1

DEPO_O (bit 5) is to indicate the polarity for output DE signal. When it is “1”, the polarity of DE is high. Otherwise, the polarity is low.

HPO_O (bit 4) is to indicate the polarity for output H signal. When it is “1”, the polarity of H is high. Otherwise, the polarity is low.

VPO_O (bit 3) is to indicate the polarity for output V signal. When it is “1”, the polarity of V is high. Otherwise, the polarity is low.

DEPO_I (bit 2) is to indicate the polarity for input DE signal. When it is “1”, the polarity of DE is high. Otherwise, the polarity is low.

HPO_I (bit 1) is to indicate the polarity for input H signal. When it is “1”, the polarity of H is high. Otherwise, the polarity is low.

VPO_I (bit 0) is to indicate the polarity for input V signal. When it is “1”, the polarity of V is high. Otherwise, the polarity is low.

SYNC output configuration Register **Address: 08h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	CSSEL[2]	CSSEL[1]	CSSEL[0]	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

CSSEL[2:0] (bit 6 – 4) is to select the composite sync type. Please refer to **Table 6**.

SYNC selection Register **Address: 09h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	LNSEL[1]	LNSEL[0]	Reserved	Reserved	SYO	DES	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

LNSEL[1:0] (bit 7 – 6) is to select the number of lines used for vertical scaling. Default is 0: 4 lines; 1: 3 lines; 2 or 3: 2 lines.

SYO (bit 3) is to enable generating internal sync to VGA controller. When it is “1”, enable this feature.

DES (bit 2) is embedded sync selection signal. If the sync information is embedded into input data, this bit will be high.

DAC output configuration Register **Address: 0Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	DACS[1]	DACS[0]	DACSP[2]	DACSP[1]	DACSP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DACS[1:0] (bit 4 – 3) is to configure the multiple TV output feature.

Table 13: Multiple TV output configuration

DACS[1:0]	Output
0	CVBS and S-Video output
1	Dual CVBS output
2	Triple CVBS output

DACSP[2:0] (bit 2 – 0) is to swap the DAC output sequence.

Table 14: DAC output swapping sequence

DACSP[2:0]	DAC0	DAC1	DAC2
0	R or Y or CVBS	G or PB or YS	B or PR or CS
1	R or Y or CVBS	B or PR or CS	G or PB or YS
2	G or PB or YS	R or Y or CVBS	B or PR or CS
3	G or PB or YS	B or PR or CS	R or Y or CVBS
4	B or PR or CS	R or Y or CVBS	G or PB or YS
5	B or PR or CS	G or PB or YS	R or Y or CVBS

(note: YS and CS is Luma and chroma of S-Video when DACS set zero, otherwise YS and CS equal CVBS)

Input data format Register 1 Address: 0Bh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	INTLACE	CPUEN	POS3X[1]	POS3X[0]	MULTI[1]	MULTI[0]	AH_LB	REVERSE
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

INTLACE (bit 7) is to indicate if the input is interlaced. Active high.

CPUEN (bit 6) is the enable signal for data transmitted through CPU interface. Once it's high, this feature is enabled.

POS3X[1:0] (bit 5 – 4) is to configure where the 3x input data is located in 24 bit data input pins. If it is "0", the lower 8 bits will be used; If it is "1", the middle 8 bits will be used; If it is "2", using the upper 8 bits.

MULTI[1:0] (bit 3 – 2) is to select the 1x, 2x or 3x input. When it is "0", input data is 1x: When it is "1", input data is 2x; When it is "2", input data is 3x. Detailed information refer to Table 3.

AH_LB (bit 1) is to choose if multiplexed input data is aligned to higher or lower 12 bits among D[23:0]. If it is "1", align to D[23:12]; If it is "0", align to D[11:0].

REVERSIE (bit 0) is to choose if input data is MSB first or LSB first. If it is "1", input data is LSB first. Otherwise, input is MSB first.

Input data format Register 2 Address: 0Ch

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HIGH	SWAP[2]	SWAP[1]	SWAP[0]	IDF[3]	IDF[2]	IDF[1]	IDF[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HIGH (bit 7) is to choose whether the non-multiplexed data is aligned to higher or lower bits among D[23:0], or 2x multiplexed data is aligned to higher or lower bits among D[11:0]. When it is "1", data is aligned to higher bits. Otherwise, align to lower bits.

SWAP[2:0] (bit 6 – 4) is to swap the data input sequence.

Table 15 : HIGH,SWAP format

REVERSE	SWAP[2:0]	D[23:16]	D[15:8]	D[7:0]
0	0	R[7:0]	G[7:0]	B[7:0]
	1	R[7:0]	B[7:0]	G[7:0]
	2	G[7:0]	R[7:0]	B[7:0]
	3	G[7:0]	B[7:0]	R[7:0]
	4	B[7:0]	R[7:0]	G[7:0]
	5	B[7:0]	G[7:0]	R[7:0]
1	0	R[0:7]	G[0:7]	B[0:7]
	1	R[0:7]	B[0:7]	G[0:7]
	2	G[0:7]	R[0:7]	B[0:7]
	3	G[0:7]	B[0:7]	R[0:7]
	4	B[0:7]	R[0:7]	G[0:7]
	5	B[0:7]	G[0:7]	R[0:7]

IDF[3:0] (bit 3 – 0) is to configure the input data format. For details, please refer to **Table 3**.

Output video format Register Address: 0Dh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	WRFAST	PBPREN	YC2RGB	Reserved	VFMT[3]	VFMT[2]	VFMT[1]	VFMT[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

WRFAST (bit 7) is to indicate the input frame rate is higher than output frame rate. Active high.

PBPREN (bit 6) is to enable the YPBPR output.

YC2RGB (bit 5) is to indicate YCbCr input mode. When it is “1”, input data is YCbCr.

VFMT[3:0] is to select output format.

Table 16: SDTV/VGA Output format

VFMT[3:0]	Output format
0	NTSC_M
1	NTSC_J
2	NTSC_443
3	PAL_B/D/G/H/I
4	PAL_M
5	PAL_N
6	PAL_Nc
7	PAL_60
8	VGA out
9	VGA out (bypass scaler)

MISC control Register Address: 0Eh

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CSBINV	VSINV	WEBINV	SWP_CBCR	SWP_PAPB	DNSMPEN	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	0	0	0

CSBINV (bit 7) is to invert the CSB signal of CPU interface, active low.

VSINV (bit 6) is to invert the VSYNC signal of CPU interface, active low.

WEBINV (bit 5) is to invert the WEB signal of CPU interface, active low.

SWP_CBCR (bit 4) is to swap the CbCr signal under BT656 input format.

SWP_PAPB (bit 3) is to select in 2x multiplexed input mode P0a is first or P0b is first.

DNSMPEN (bit 2) is to enable the 4:3 down sampling feature. Active high.

Input timing Register 1 **Address: 0Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HVAUTO	HREPT	HTI[10]	HTI[9]	HTI[8]	HAI[10]	HAI[9]	HAI[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	1

HVAUTO (bit 7) is to select the self countered timing values. Active high.

HREPT(bit 6) is to enable non-interpolation mode for horizontal scaling.

HTI[10:8] (bits 5-3) combine with HTI[7:0] to define HTI[10:0], the Input Horizontal Total Pixels.

HAI[10:8] (bits 2-0) combine with HAI[7:0] to define HAI[10:0], the Input Horizontal Active Pixels.

Input timing Register 2 **Address: 10h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HAI[7]	HAI[6]	HAI[5]	HAI[4]	HAI[3]	HAI[2]	HAI[1]	HAI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HAI[7:0] (bits 7-0) combine with HAI[10:8] to define HAI[10:0], the Input Horizontal Active Pixels.

Input timing Register 3 **Address: 11h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HTI[7]	HTI[6]	HTI[5]	HTI[4]	HTI[3]	HTI[2]	HTI[1]	HTI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	1	1	0	1

HTI[7:0] (bits 7-0) combine with HTI[10:8] to define HTI[10:0], the Input Horizontal Total Pixels.

Input timing Register 4 **Address: 12h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HDTVEN	EDGE_ENH	HW[10]	HW[9]	HW[8]	HO[10]	HO[9]	HO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HDTVEN (bits 7) HDTV output enable.

EDGE_ENH (bits 7) sharpen the edge of output picture.

HW[10:8] (bits 5-3) combine with HW[7:0] to define HW[10:0], the Input Horizontal Sync Width.

HO[10:8] (bits 2-0) combine with HO[7:0] to define HO[10:0], the Input Horizontal Sync Offset.

Input timing Register 5 **Address: 13h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HO[7]	HO[6]	HO[5]	HO[4]	HO[3]	HO[2]	HO[1]	HO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HO[7:0] (bits 7-0) combine with HO[10:8] to define HO[10:0], the Input Horizontal Sync Offset.

Input timing Register 6 **Address: 14h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HW[7]	HW[6]	HW[5]	HW[4]	HW[3]	HW[2]	HW[1]	HW[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

HW[7:0] (bits 7-0) combine with HW[10:8] to define HW[10:0], the Input Horizontal Sync Width

Input timing Register 7 **Address: 15h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	FIELDSW	TV_BP	VTI[10]	VTI[9]	VTI[8]	VAI[10]	VAI[9]	VAI[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

FIELDSW(bits 7) **s**witch the turn of odd/even field of input video.

TV_BP(bits 6) TV bypass enable.

VTI[10:8] (bits 5-3) combine with VTI[7:0] to define VTI[10:0], the Input Vertical Total Pixels.

VAI[10:8] (bits 2-0) combine with VAI[7:0] to define VAI[10:0], the Input Vertical Active Pixels.

Input timing Register 8 **Address: 16h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VAI[7]	VAI[6]	VAI[5]	VAI[4]	VAI[3]	VAI[2]	VAI[1]	VAI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	1	0	0	0	0

VAI[7:0] (bits 7-0) combine with VAI[10:8] to define VAI[10:0], the Input Vertical Active Pixels.

Input timing Register 9 **Address: 17h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VTI[7]	VTI[6]	VTI[5]	VTI[4]	VTI[3]	VTI[2]	VTI[1]	VTI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	1	1	1	1	1

VTI[7:0] (bits 7-0) combine with VTI[10:8] to define VTI[10:0], the Input Vertical Total Pixels.

Input timing Register 10 **Address: 18h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VW[10]	VW[9]	VW[8]	VO[10]	VO[9]	VO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VW[10:8] (bits 5-3) combine with VW[7:0] to define VW[10:0], the Input Vertical Sync Width.

VO[10:8] (bits 2-0) combine with VO[7:0] to define VO[10:0], the Input Vertical Sync Offset.

Input timing Register 11 **Address: 19h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VO[7]	VO[6]	VO[5]	VO[4]	VO[3]	VO[2]	VO[1]	VO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	0	0	0

VO[7:0] (bits 7-0) combine with VO[10:8] to define VO[10:0], the Input Vertical Sync Offset.

Input timing Register 12 **Address: 1Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VW[7]	VW[6]	VW[5]	VW[4]	VW[3]	VW[2]	VW[1]	VW[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	1

VW[7:0] (bits 7-0) combine with VW[10:8] to define VW[10:0], the Input Horizontal Sync Width

Output timing Register 1 **Address: 1Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	HTO[11]	HTO[10]	HTO[9]	HTO[8]	HAO[10]	HAO[9]	HAO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	1	0	1	0	1

HTO[11:8] (bits 5-3) combine with HTO[7:0] to define HTO[11:0], the Output Horizontal Total Pixels.

HAO[10:8] (bits 2-0) combine with HAO[7:0] to define HAO[10:0], the Output Horizontal Active Pixels.

Output timing Register 2 **Address: 1Ch**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HAO[7]	HAO[6]	HAO[5]	HAO[4]	HAO[3]	HAO[2]	HAO[1]	HAO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	1	1	0

HAO[7:0] (bits 7-0) combine with HAO[10:8] to define HAO[10:0], the Output Horizontal Active Pixels.

Output timing Register 3 **Address: 1Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HTO[7]	HTO[6]	HTO[5]	HTO[4]	HTO[3]	HTO[2]	HTO[1]	HTO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	1	0	1	0	0

HTO[7:0] (bits 7-0) combine with HTO[10:8] to define HTO[10:0], the Output Horizontal Total Pixels.

Output timing Register 4 **Address: 1Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	HWO[10]	HWO[9]	HWO[8]	HOO[10]	HOO[9]	HOO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HWO[10:8] (bits 5-3) combine with HWO[7:0] to define HWO[10:0], the Output Horizontal Sync Width.

HOO[10:8] (bits 2-0) combine with HOO[7:0] to define HOO[10:0], the Output Horizontal Sync Offset.

Output timing Register 5 **Address: 1Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HOO[7]	HOO[6]	HOO[5]	HOO[4]	HOO[3]	HOO[2]	HOO[1]	HOO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HOO[7:0] (bits 7-0) combine with HOO[10:8] to define HOO[10:0], the Output Horizontal Sync Offset.

Output timing Register 6 **Address: 20h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HWO[7]	HWO[6]	HWO[5]	HWO[4]	HWO[3]	HWO[2]	HWO[1]	HWO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	0	0	0	0

HWO[7:0] (bits 7-0) combine with HWO[10:8] to define HWO[10:0], the Output Horizontal Sync Width

Output timing Register 7 **Address: 21h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	SETEN	VTO[10]	VTO[9]	VTO[8]	VAO[10]	VAO[9]	VAO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	1	0	0	0	1

SETEN(bits 6) enable to manually set de-flicker filter.

VTO[10:8] (bits 5-3) combine with VTO[7:0] to define VTO[10:0], the Output Vertical Total Pixels.

VAO[10:8] (bits 2-0) combine with VAO[7:0] to define VAO[10:0], the Output Vertical Active Pixels.

Output timing Register 8 **Address: 22h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VAO[7]	VAO[6]	VAO[5]	VAO[4]	VAO[3]	VAO[2]	VAO[1]	VAO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	0	0	0

VAO[7:0] (bits 7-0) combine with VAO[10:8] to define VAO[10:0], the Output Vertical Active Pixels.

Output timing Register 9 **Address: 23h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VTO[7]	VTO[6]	VTO[5]	VTO[4]	VTO[3]	VTO[2]	VTO[1]	VTO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	1	0	1

VTO[7:0] (bits 7-0) combine with VTO[10:8] to define VTO[10:0], the Output Vertical Total Pixels.

Output timing Register 10 **Address: 24h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VWO[10]	VWO[9]	VWO[8]	VOO[10]	VOO[9]	VOO[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VWO[10:8] (bits 5-3) combine with VWO[7:0] to define VWO[10:0], the Output Vertical Sync Width.

VOO[10:8] (bits 2-0) combine with VOO[7:0] to define VOO[10:0], the Output Vertical Sync Offset.

Output timing Register 11 **Address: 25h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VOO[7]	VOO[6]	VOO[5]	VOO[4]	VOO[3]	VOO[2]	VOO[1]	VOO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	0	0	0

VOO[7:0] (bits 7-0) combine with VOO[10:8] to define VOO[10:0], the Output Vertical Sync Offset.

Output timing Register 12 **Address: 26h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VWO[7]	VWO[6]	VWO[5]	VWO[4]	VWO[3]	VWO[2]	VWO[1]	VWO[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	1	1

VWO[7:0] (bits 7-0) combine with VWO[10:8] to define VWO[10:0], the Output Horizontal Sync Width

Image zooming Register 1 **Address: 27h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	IMGZOOM	Reserved	HEND[10]	HEND[9]	HEND[8]	HST[10]	HST[9]	HST[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

IMGZOOM (bit 7) is to enable the image zoom feature. Active high.

HEND[10:8] (bit 5 – 3) combine with HEND[7:0] to define HEND[10:0], the Horizontal End position.

HST[10:8] (bit 2 – 0) combine with HST[7:0] to define HST[10:0], the Horizontal Start position.

Image zooming Register 2 **Address: 28h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HST[7]	HST[6]	HST[5]	HST[4]	HST[3]	HST[2]	HST[1]	HST[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

HST[7:0] (bit 7 – 0) combine with HST[10:8] to define HST[10:0], the Horizontal Start position.

Image zooming Register 3 **Address: 29h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HEND[7]	HEND[6]	HEND[5]	HEND[4]	HEND[3]	HEND[2]	HEND[1]	HEND[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HEND[7:0] (bit 7 – 0) combine with HEND[10:8] to define HEND[10:0], the Horizontal End position.

Image zooming Register 4 **Address: 2Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	VEND[10]	VEND[9]	VEND[8]	VST[10]	VST[9]	VST[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VEND[10:8] (bit 5 – 3) combine with VEND[7:0] to define VEND[10:0], the Vertical End position.

VST[10:8] (bit 2 – 0) combine with VST[7:0] to define VST[10:0], the Vertical Start position.

Image zooming Register 5 **Address: 2Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VST[7]	VST[6]	VST[5]	VST[4]	VST[3]	VST[2]	VST[1]	VST[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	1

VST[7:0] (bit 7 – 0) combine with VST[10:8] to define VST[10:0], the Vertical Start position.

Image zooming Register 6 **Address: 2Ch**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VEND[7]	VEND[6]	VEND[5]	VEND[4]	VEND[3]	VEND[2]	VEND[1]	VEND[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	1	0	0	0	0

VEND[7:0] (bit 7 – 0) combine with VEND[10:8] to define VEND[10:0], the Vertical End position.

Image rotation and flip Register **Address: 2Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	VFLIP	HFLIP	ROTATE[1]	ROTATE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VFLIP (bit 3) is the vertical flip bit.

HFLIP (bit 2) is the horizontal flip bit.

ROTATE[1:0] (bit 1 – 0) is the image rotation bit. When it is “00”, no rotation; When it is “01”, 90 degree rotation; When it is “10”, 180 degree rotation; When it is “11”, 270 degree rotation.

Hue adjustment Register **Address 2Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

HUE[6:0] (bits 6-0) define the TV Hue control HUE[6:0]. The adjusted angle in the color space is (HUE[6:0]-64)/2 degrees, positive angle is toward magenta color, negative angle is toward green color.

Saturation adjustment Register **Address: 2Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	SAT[6]	SAT[5]	SAT[4]	SAT[3]	SAT[2]	SAT[1]	SAT[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	1	1	1

SAT[6:0] (bits 6-0) define the TV Color Saturation control SAT[6:0]. The Color Saturation is multiplied by SAT[6:0]/64.

Contrast adjustment Register **Address 30h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VREPT	CTA[6]	CTA[5]	CTA[4]	CTA[3]	CTA[2]	CTA[1]	CTA[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

VREPT (bit 7) is to enable non-interpolation mode for vertical scaling.

CTA[6:0] (bits 6-0) define the TV contrast control CTA[6:0]. The luma is multiplied by CTA[6:0]/64.

Brightness adjustment Register **Address 31h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

BRI[7:0] (bits 7-0) define the TV brightness control BRI[7:0]. The Brightness will be adjusted by (BRI[7:0]-128).

Text enhancement Register **Address 32h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	RGBEN	HFLN_EN	Reserved	Reserved	Reserved	TE[2]	TE[1]	TE[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	1	0	1	0	0

RGBEN(bit 7) is to enable RGB output of TV format

HFLN_EN(bit 6) is to enable half line difference for TV scaling.

TE[2:0] (bits 2-0) define TV Sharpness control (Text Enhancement) TE[2:0]. TE[2:0]=100 means no enhancement. Larger setting than 100 boosts the high frequency band of the picture. Smaller setting than 100 smoothes the image.

Vertical position adjustment Register 1 **Address 33h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	VP[11]	VP[10]	VP[9]	VP[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

VP[11:8] (bits 3-0) combine with VP[7:0] to define the TV horizontal position adjustment VP[11:0].

Vertical position adjustment Register 2 **Address 34h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	VP[7]	VP[6]	VP[5]	VP[4]	VP[3]	VP[2]	VP[1]	VP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

VP[7:0] (bits 7-0) combine with VP[11:8] to define the TV vertical position adjustment VP[11:0]. The number of lines that is adjusted is determined by VP[11:0]-2048. If the value is positive, the output picture is moved upward; if the value is negative, the output picture is moved downward.

Horizontal position adjustment Register 1 **Address 35h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	HP[11]	HP[10]	HP[9]	HP[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

HP[11:8] (bits 3-0) combine with HP[7:0] to define the TV horizontal position adjustment HP[11:0].

Horizontal position adjustment Register 2 **Address: 36h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HP[7]	HP[6]	HP[5]	HP[4]	HP[3]	HP[2]	HP[1]	HP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HP[7:0] (bits 7-0) combine with HP[11:8] to define TV horizontal position adjustment HP[11:0]. The number of pixels that is adjusted is determined by HP[11:0]-2048. If the value is positive, the output picture is moved to the right; if the value is negative, the output picture is moved to the left.

AX + B adjustment Register 1 **Address: 37h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DAC0C1[6]	DAC0C1 [5]	DAC0C1 [4]	DAC0C1 [3]	DAC0C1 [2]	DAC0C1 [1]	DAC0C1 [0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

DAC0C1 [6:0] (bit 6 – 0) is the A value of AX/64+B on DAC0.

AX + B adjustment Register 2 **Address: 38h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DAC0C2 [7]	DAC0C2 [6]	DAC0C2 [5]	DAC0C2 [4]	DAC0C2 [3]	DAC0C2 [2]	DAC0C2 [1]	DAC0C2 [0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DAC0C2 [7:0] (bit 7 – 0) is the B value of AX/64+B on DAC0.

AX + B adjustment Register 3 **Address: 39h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DAC1C1[6]	DAC1C1 [5]	DAC1C1 [4]	DAC1C1 [3]	DAC1C1 [2]	DAC1C1 [1]	DAC1C1 [0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

DAC1C1 [6:0] (bit 6 – 0) is the A value of AX/64+B on DAC1.

AX + B adjustment Register 4 **Address: 3Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DAC1C2[7]	DAC1C2[6]	DAC1C2[5]	DAC1C2[4]	DAC1C2[3]	DAC1C2[2]	DAC1C2[1]	DAC1C2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DAC1C2 [7:0] (bit 7 – 0) is the B value of AX/64+B on DAC1.

AX + B adjustment Register 5 **Address: 3Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DAC2C1[6]	DAC2C1[5]	DAC2C1[4]	DAC2C1[3]	DAC2C1[2]	DAC2C1[1]	DAC2C1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

DAC2C1 [6:0] (bit 6 – 0) is the A value of AX/64+B on DAC2.

AX + B adjustment Register 6 **Address: 3Ch**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DAC2C2[7]	DAC2C2[6]	DAC2C2[5]	DAC2C2[4]	DAC2C2[3]	DAC2C2[2]	DAC2C2[1]	DAC2C2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

DAC2C2 [7:0] (bit 7 – 0) is the B value of AX/64+B on DAC2.

Filter setting Register 1 **Address: 3Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	MONOB	Reserved	CBW	Reserved	Reserved	VFFSPP[2]	VFFSPP[1]	VFFSPP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	1	1	1	0	0

MONOB (bit 7) is the display mono image. Active low.

CBW (bit 5) increases TV Chroma bandwidth, when CBW='1'; otherwise decrease the Chroma bandwidth.

VFFSPP[2:0] (bits 2-0) define the TV Adaptive Flicker Filter Control VFFSPP[2:0]. Allowed values are 0 to 6 (7 is reserved). Larger setting has stronger De-flicker effect, but the picture are less clear.

Filter setting Register 2 **Address: 3Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	DBP	Reserved	Reserved	Reserved	Reserved	YCV[2]	YCV[1]	YCV[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	1	0	0	0	0	1

DBP (bit 7) is the dither function bypass control.

YCV[2:0] (bit 2 - 0) define the Composite Luma channel bandwidth control YCV[2:0]. YCV[2:0] can be set to 0, 1, 2, 3, 4, 5. Smaller YCV value results in higher luma channel bandwidth.

Filter bypass register **Address: 3Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CFBP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

CFBP (bit 7) bypasses TV Chroma filter, when CFBP='1'; otherwise enable the filter.

Burst setting Register **Address: 40h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	DOTB	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

DOTB (bit 3) enables TV Dot Crawl reduction when set to '1'. '0' disables Dot Crawl reduction.

Sub-carrier generation method Register **Address: 41h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	XSEL	XTAL[3]	XTAL[2]	XTAL[1]	XTAL[0]	ACIV	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	1	0	0	1	0

XSEL (bit 7): whether the crystal frequency is predefined or not. When the crystal frequency is predefined, some registers, such as SCFREQ, will be calculated inside the chip to save programming effort.

1: using predefined values;
0: using other values.

XTAL[3:0] (bits 6 - 3): predefined crystal frequencies.

0: 3.6864MHz,
1: 3.579545MHz,
2: 4MHz,
3: 12MHz,
4: 13MHz,
5: 13.5MHz,
6: 14.318MHz,
7: 14.7456MHz,
8: 16MHz,
9: 18.432MHz,
10: 20MHz,
11: 26MHz,
12: 27MHz,
13: 32MHz,
14: 40MHz,
15: 49MHz.

ACIV(bit 2) controls whether the FSCI value is used to set the sub-carrier frequency, or the automatically calculated (CIV) value. When the ACIV value is '1', the number calculated and present at the SCFREQ registers will automatically be used as the increment value for sub-carrier generation.

Sub-carrier frequency setting Register 1 **Address: 42h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	SCREQ[26]	SCREQ[25]	SCREQ[24]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

SCFREQ[26:24] (bit 2 – 0) combine with SCFREQ[23:16], SCFREQ[15:8], and SCFREQ[7:0] to define SCFREQ[26:0], the Sub-carrier Frequency Value.

Sub-carrier frequency setting Register 2 **Address: 43h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCREQ[23]	SCREQ[22]	SCREQ[21]	SCREQ[20]	SCREQ[19]	SCREQ[18]	SCREQ[17]	SCREQ[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

SCFREQ[23:16] (bit 7 – 0) combine with SCFREQ[26:24], SCFREQ[15:8], and SCFREQ[7:0] to define SCFREQ[26:0], the Sub-carrier Frequency Value.

Sub-carrier frequency setting Register 3 **Address: 44h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCREQ[15]	SCREQ[14]	SCREQ[13]	SCREQ[12]	SCREQ[11]	SCREQ[10]	SCREQ[9]	SCREQ[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

SCFREQ[15:8] (bit 7 – 0) combine with SCFREQ[26:24], SCFREQ[23:16], and SCFREQ[7:0] to define SCFREQ[26:0], the Sub-carrier Frequency Value.

Sub-carrier frequency setting Register 4 **Address: 45h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	SCREQ[7]	SCREQ[6]	SCREQ[5]	SCREQ[4]	SCREQ[3]	SCREQ[2]	SCREQ[1]	SCREQ[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

SCFREQ[7:0] (bit 7 – 0) combine with SCFREQ[26:24], SCFREQ[23:16], and SCFREQ[15:8] to define SCFREQ[26:0], the Sub-carrier Frequency Value, the detailed value refer to Programming Guide.

Digital divider settings Register 1 **Address: 4Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[31]	A1[30]	A1[29]	A1[28]	A1[27]	A1[26]	A1[25]	A1[24]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	1	0	0	0

A1[31:24](bits7-0) combine with A1[23:16], A1[15:8] and A1[7:0] to define the clock divider for UCLK. (For its value, refer to the Programming Guide of CH7026).

Digital divider settings Register 2 **Address: 4Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[23]	A1[22]	A1[21]	A1[20]	A1[19]	A1[18]	A1[17]	A1[16]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

See Register 4Dh.

Digital divider settings Register 3 **Address: 4Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[15]	A1[14]	A1[13]	A1[12]	A1[11]	A1[10]	A1[9]	A1[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

See Register 4Dh.

Digital divider settings Register 4 **Address: 50h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A1[7]	A1[6]	A1[5]	A1[4]	A1[3]	A1[2]	A1[1]	A1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

See Register 4Dh.

Digital divider settings Register 5 **Address: 51h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	A2[7]	A2[6]	A2[5]	A2[4]	A2[3]	A2[2]	A2[1]	A2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

A2[7:0](bit 7 - 0) is to define the clock divider for MCLK. (For its value, refer to the Programming Guide of CH7026).

Analog divider setting Register 1 **Address: 52h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	PLL1N2[2]	PLL1N2[1]	PLL1N2[0]	PLL1N1[2]	PLL1N1[1]	PLL1N1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	1

PLL1N2[2:0] (bit 5 - 3): control the video PLL1 feedback-divider 1 value. Other values are not allowed. For single edge rate (SDR) input mode, the value of PLL1N2 is equal to PLL1N1. For dual edge rate (DDR) input mode, PLL1N2 is equal to twice of PLL1N1. (The value refer to the Programming Guide of CH7026).

PLL1N1[2:0] (bit 2 – 0) control the pre-divider of PLL1. It makes sure that the frequency range input the PFD of PLL1 is from 2.3 to 4.6MHz. (For its value, refer to the Programming Guide of CH7026).

Analog divider setting Register 2 **Address: 53h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	DPCKN4	PLL2N5[2]	PLL2N5[1]	PLL2N5[0]	PLL1N3[2]	PLL1N3[1]	PLL1N3[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	1	1	1	0	0

DPCKN4 (bit 6) control the divider ratio for multiplexed input(when XCH set 1). When it is "1", ratio is 1/3; Otherwise ratio is 1/2. For 2x input mode, DPCKN4 is 0; For 3x input mode, DPCKN4 is 1.

PLL2N5[2:0] (bit 5 – 4)control the divider after the output from PLL2's VCO. (The value refer to the Programming Guide of CH7026).

PLL1N3[2:0] (bit 2 - 0): control the video PLL1 feedback-divider 2 value. (The value refer to the Programming Guide of CH7026).

Analog divider setting Register 3 **Address: 54h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	PLL3N8[1]	PLL3N8[0]	PLL3N7	PLL3N6[1]	PLL3N6[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

PLL3N8[1:0] (bit 4 – 3) is the post divider 1 ratio after PLL3. (The value refer to the Programming Guide of CH7026).

PLL3N7 (bit 2) is the post divider 2 ratio after PLL3. When it is "1", ratio is 1/3;Otherwise 1/1. (The value refer to the Programming Guide of CH7026).

The value of PLL3N7 and PLL3N8 can be determined flexibly. This is to derive a clock signal which is larger than the clock frequency (WEB) of CPU interface. (The value refer to the Programming Guide of CH7026).

PLL3N6[1:0] (bit 1 – 0) is the post divider 3 ratio after PLL3. (The value refer to the Programming Guide of CH7026).

Clock selection Register **Address: 55h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	XCH	BPSEL	DPSEL[1]	DPSEL[0]	GSEL
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	1	1	0	0	1	0	0

XCH (bit 4) is to select the pixel clock to driver digital logic. When under 2x or 3x multiplexed input mode, XCH is 1. Otherwise 0.

BPSEL (bit 3) is. Under 2x/3x input and TV bypass mode, BPSEL is 1. Otherwise 0. (The value refer to the Programming Guide of CH7026).

DPSEL (bit 2 – 1) is to select the clock for analog latching. When it is "0x", select input pixel clock after PLL; When it is "10", select input GCLK directly; When it is "11", select memory clock. (The value refer to the Programming Guide of CH7026).

GSEL (bit 0) is to select the clock source for generating UCLK. When it is "1", select crystal; Otherwise select input GCLK. When input GCLK is lower than 2MHz and a crystal or oscillator (> 2.3MHz) is presented on XI/XO pins, GSEL needs to be 1, otherwise 0. (The value refer to the Programming Guide of CH7026).

MV mode level Register **Address: 56h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	MVTSTEN	Reserved	MVMOD[1]	MVMOD[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	0	0	0	0	0	0

MVTSTEN (bit 3) controls the Macrovision N values setting. When MVTSTEN='0', Macrovision N values are from internal setting. When MVTSTEN='1', Macrovision N values are input manually from Registers 41h through Register 5Ah.

MVMODE (bits 1-0) define Macrovision level mode as the follow table.

Table 17: Macrovision level mode MVMODE[1:0]

MVMODE[1:0]	Macrovision level mode
00	Macrovision off
01	AGC only
10	AGC + 2-line Color stripe
11	AGC + 4-line Color stripe

MV Control Register 1 **Address: 57h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N0[7]	N0[6]	N0[5]	N0[4]	N0[3]	N0[2]	N0[1]	N0[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N0[7:0] (Bits 7-0) defines N0[7:0].

MV Control Register 2 **Address: 58h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	PEN	Reserved	N1[5]	N1[4]	N1[3]	N1[2]	N1[1]	N1[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

PEN (bit 7) is to enable customize SDTV format for decreasing flicker.

N1[5:0] (bits 5-0) define N1[5:0].

MV Control Register 3 **Address: 59h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	N2[5]	N2[4]	N2[3]	N2[2]	N2[1]	N2[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N2[5:0] (bits 5-0) define N2[5:0].

MV Control Register 4 **Address: 5Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	N3[5]	N3[4]	N3[3]	N3[2]	N3[1]	N3[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT	0	0	0	0	0	0	0	0

N3[5:0] (bits 5-0) define N3[5:0].

MV Control Register 5 **Address: 5Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	N4[5]	N4[4]	N4[3]	N4[2]	N4[1]	N4[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N4[5:0] (bits 5-0) define N4[5:0].

MV Control Register 6 **Address: 5Ch**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	HDVDOFM[4]	HDVDOFM[3]	HDVDOFM[2]	HDVDOFM[1]	HDVDOFM[0]	N5[2]	N5[1]	N5[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

HDVDOFM[4:0] (bits 7-3) HDTV output video format

Table 18 : EDTV/HDTV output format

HDVDOFM[4:0]	Output format
0	480p
1	480p double sample
2	576p
3	576p double sample
4	720p(60Hz)
5	720p(50Hz)
6	1080i(60Hz)
7	1080i(50Hz, SMPTE 274M)
8	1080i(50Hz, SMPTE 295M)

N5[2:0] (bits 2-0) define N5[2:0].

MV Control Register 7 **Address: 5Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	N6[2]	N6[1]	N6[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	0	0

N6[2:0] (bits 2 - 0) define N6[2:0].

MV Control Register 8 **Address: 5Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	N7[1]	N7[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	0	0	0

N7[1:0] (bits 1 - 0) define N7[1:0].

MV Control Register 9 **Address: 5Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CGMSEN	WSSEN	N8[5]	N8[4]	N8[3]	N8[2]	N8[1]	N8[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

CGMSEN (bit 7) CGMS enable.

WSSEN (bit 6) WSS enable.

N8[5:0] (bits 5-0) define N8[5:0].

MV Control Register 10 **Address: 60h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	N9[5]	N9[4]	N9[3]	N9[2]	N9[1]	N9[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N9[5:0] (bits 5-0) define N9[5:0].

MV Control Register 11 **Address: 61h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	N10[5]	N10[4]	N10[3]	N10[2]	N10[1]	N10[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N10[5:0] (bits 5-0) define N10[5:0].

MV Control Register 12 **Address: 62h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	N11[14]	N11[13]	N11[12]	N11[11]	N11[10]	N11[9]	N11[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N11[14:8] (bits 6-0) combine with N11[7:0] to define N11[14:0].

MV Control Register 13 **Address: 63h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N11[7]	N11[6]	N11[5]	N11[4]	N11[3]	N11[2]	N11[1]	N11[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N11[7:0] (bits 7-0) combine with N11[14:8] to define N11[14:0].

MV Control Register 14 **Address: 64h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	N12[14]	N12[13]	N12[12]	N12[11]	N12[10]	N12[9]	N12[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N12[14:8] (bits 6-0) combine with N12[7:0] to define N12[14:0].

MV Control Register 15 **Address: 65h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N12[7]	N12[6]	N12[5]	N12[4]	N12[3]	N12[2]	N12[1]	N12[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N12[7:0] (bits 7-0) combine with N12[14:8] to define N12[14:0].

MV Control Register 16 **Address: 66h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N13[7]	N13[6]	N13[5]	N13[4]	N13[3]	N13[2]	N13[1]	N13[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N13[7:0] (bits 7-0) define N13[7:0].

MV Control Register 17 **Address: 67h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N14[7]	N14[6]	N14[5]	N14[4]	N14[3]	N14[2]	N14[1]	N14[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N14[7:0] (bits 7-0) define N14[7:0].

MV Control Register 18 **Address: 68h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N15[7]	N15[6]	N15[5]	N15[4]	N15[3]	N15[2]	N15[1]	N15[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N15[7:0] (bits 7-0) define N15[7:0].

MV Control Register 19 **Address: 69h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	BLK_H[6]	BLK_H[5]	BLK_H[4]	BLK_H[3]	BLK_H[2]	BLK_H[1]	BLK_H[0]	N16
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	1	1	0	1	0

BLK_H[6:0](bit 7-1) Define the ceiling integer of HAI/16, set it when HAI larger than 720 , otherwise use default value.

N16 (bit 0) defines N16.

MV Control Register 20 **Address: 6Ah**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	N17[3]	N17[2]	N17[1]	N17[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N17[3:0] (bits 3 - 0) define N17[3:0].

MV Control Register 21 **Address: 6Bh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	N18[3]	N18[2]	N18[1]	N18[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N18[3:0] (bits 3 - 0) define N18[3:0].

MV Control Register 22 **Address: 6Ch**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	N19[3]	N19[2]	N19[1]	N19[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N19[3:0] (bits 3 - 0) define N19[3:0].

MV Control Register 23 **Address: 6Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	CGMSDATA[13]	CGMSDATA[12]	CGMSDATA[11]	CGMSDATA[10]	CGMSDATA[9]	N20[2]	N20[1]	N20[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

CGMSDATA[13:0] CGMS signal

N20[2:0] (bits 2-0) define N20[2:0].

MV Control Register 24 **Address: 6Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N22	CGMSDATA[9]	CGMSDATA[9]	CGMSDATA[9]	CGMSDATA[9]	CGMSDATA[9]	N21[9]	N21[8]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N22 (bit 7) defines N22.

N21[9:8] (bits 1-0) combine with N21[7:0] to define N21[9:0].

MV Control Register 25 **Address: 6Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	N21[7]	N21[6]	N21[5]	N21[4]	N21[3]	N21[2]	N21[1]	N21[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	0	0	0

N21[7:0] (bits 7-0) combine with N21[9:8] to define N21[9:0].

Clock inversion Register **Address: 75h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CKINV
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	1	0	1	0	0	0	1	0

CKINV (bit 0) is to invert the GCLK.

IO input setting Register **Address: 76h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	VRTM[1]	VRTM[0]	DIFFEN[1]	DIFFEN[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	1	1	0	0

VRTM[1:0] (bit 1 - 0) control the trimming settings of the voltage reference generator

VRTM1	VRTM0	VREF
0	0	about 50% of VDDIO
0	1	about 60% of VDDIO
1	0	about 70% of VDDIO
1	1	about 80% of VDDIO

DIFFEN [1:0] (bit 1 – 0) enable the differential input mode of data and GCLK buffer. DIFFEN [1] is used to set data buffer, the other is for GCLK buffer

DAC trimming Register **Address: 77h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	SEL_R	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	0	0	0	0	1	1

SEL_R (bit 6) is to select the single or double termination.

SDRAM test and DAC sense Register **Address: 7Dh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DISPON	SPPSNS
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	1	1	0	0	0	0	0

DISPON (bit 1) is to select the clock source for DAC, if it is '1', select dcore backend clock, otherwise, select crystal clock. It is suggested to be set '1'.

SPPSNS (bit 0) is the DAC sense signal for connection detect.

SDRAM Status Register **Address: 7Eh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	Reserved	Reserved	DVALID	Reserved	Reserved	Reserved
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

DVALID (bit 3) is the read only bit. If it is "1", it will indicate that SDRAM has been initialized.

Attach Display Register **Address: 7Fh**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	DACAT2[1]	DACAT2[0]	DACAT1[1]	DACAT1[0]	DACAT0[1]	DACAT0[0]
TYPE:	R	R	R	R	R	R	R	R
DEFAULT:	0	0	0	0	0	0	0	0

DACAT2[1:0] (bits 5-4) return attach information for DAC3 channel according to the table below.
DACAT1[1:0] (bits 3-2) return attach information for DAC2 channel according to the table below.
DACAT0[1:0] (bits 1-0) return attach information for DAC1 channel according to the table below.

Table 19: Attached Display Mapping

DACAT0[1:0]	Attached Display
00	No Attached Display
01	Connected
11	Short to ground
10	Reserved

Below are the descriptions for registers of page 2.

Test Pattern Selection Register **Address: 04h**

BIT:	7	6	5	4	3	2	1	0
SYMBOL:	Reserved	Reserved	TEST	TSYNC	TSTP[3]	TSTP[2]	TSTP[1]	TSTP[0]
TYPE:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DEFAULT:	0	0	0	0	0	1	0	0

TEST (bit 5) is the test pattern selection enable.

TSYNC (bit 4) is to select the internally generated test sync.

TSTP[3:0] (bit 3 – 0) is to select different test patterns. For details, please refer to Table 8.

4.0 Electrical specifications

4.1 Absolute maximum rating

Symbol	Description	Min	Typ	Max	Units
	All 1.8V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		2.5 5.0	V
	Input voltage of all digital pins (see note[3])	GND – 0.5		VDDIO+0.5	V
TAMB	Ambient operating temperature	-40		85	°C
TSTOR	Storage temperature	-40		150	°C
TJ	Junction temperature			150	°C
TVPS	Vapor phase soldering (5 second) Vapor phase soldering (11 second) Vapor phase soldering (1 minute)			260 245 225	°C

Note:
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce permanent damage.
3. The digital input voltage will follow the I/O supply voltage (VDDIO), the I/O supply voltage range is from 1.2V to 3.3V.

4.2 Recommended operating conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Crystal and I/O Power Supply Voltage	2.5	3.3	3.5	V
AVDD_DAC	DAC Power Supply Voltage	2.5	3.3	3.5	V
AVDD_PLL	PLL Power Supply Voltage	1.71	1.8	1.89	V
DVDD	Digital Power Supply Voltage	1.71	1.8	1.89	V
VDDIO	Data I/O supply voltage	1.14		3.5	V
RL1	Output load to DAC Current Reference		1.2k		Ω
R_{L2}	Output load to DAC Outputs		37.5		Ω
VDDQ_MEM	Memory data interface supply	2.375	2.5	2.625	V
VDD_MEM	Memory core supply	2.375	2.5	2.625	V
VDD18	Generic for all 1.8V supplies	1.71	1.8	1.89	V
VDD33	Generic for all 3.3V supplies	2.5	3.3	3.5	V

4.3 Electrical characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD18=1.8V± 5%, VDD33 =2.5V – 3.5V)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		38		mA
	Video level error			10	%
I_{VDD18}	Total VDD18 supply current (1.8V supplies)		35		mA
I_{VDD33} (1)	Total VDD33 supply current (3.3V supplies) (see note)		30		mA
I_{VDDQ}	Memory data interface supply current		0.1		mA
I_{VDD_MEM}	Memory core supply current		20		mA
I_{PD}	Total Power Down Current		<20		uA

Notes:
1. Applies for one DAC and single 75Ohm termination. The current of every DAC is less than 25mA for single termination and less than 50mA for double termination.
2. Some memories do not support deep power down mode.

4.4 Digital inputs / outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 3.0 mA	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD33 + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{DATAIH}	Data I/O (1) High Voltage		VDDIO/2 +0.25		VDDIO + 0.5	V
V_{DATAIL}	Data I/O Low Voltage		GND-0.5		VDDIO/2 -0.25	V
V_{MISCIH}	Miscellaneous Input High Voltage (2)		VDD33 – 0.5		VDD33 + 0.5	V
V_{MISCIL}	Miscellaneous Input Low Voltage (2)		GND-0.5		0.6	V
V_{SYNCOH}	Miscellaneous Output High Voltage (3)		VDD33 x 0.8			V
V_{SYNCOL}	Miscellaneous Output Low Voltage (3)				0.3	V
I_{MISCPU}	Miscellaneous Input Pull Up Current (2)	V_{IN} = 0	0.5		5.0	uA
I_{MISCPD}	Miscellaneous Input Pull Down Current (2)	V_{IN} = VDD33	0.1		1.1	uA

Notes:
1. Applies to D[23:0], GCLK, H, V and DE. VDDIO is the I/O supply, ranging from 1.2V to 3.3V.
2. Applies to AS, RESETB and ATPG.
3. Applies to HSO, VSO, CSYNC.

4.5 AC specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$f_{CRYSTAL}$	Input (CRYSTAL) frequency		2.3		64	MHz
f_{GCLK}	Input (GCLK) frequency		1.5		120	MHz
DC_{GCLK}	Input (GCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{GJIT}	GCLK clock jitter tolerance			10		ns
t_S	Setup Time: D[23:0], H, V and DE to GCLK	GCLK to D[23:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[23:0], H, V and DE to GCLK	D[23:0], H, V, DE = Vref to GCLK	0.5			ns
t_{STEP}	De-skew time increment		50		80	ps

5.0 Package Dimensions

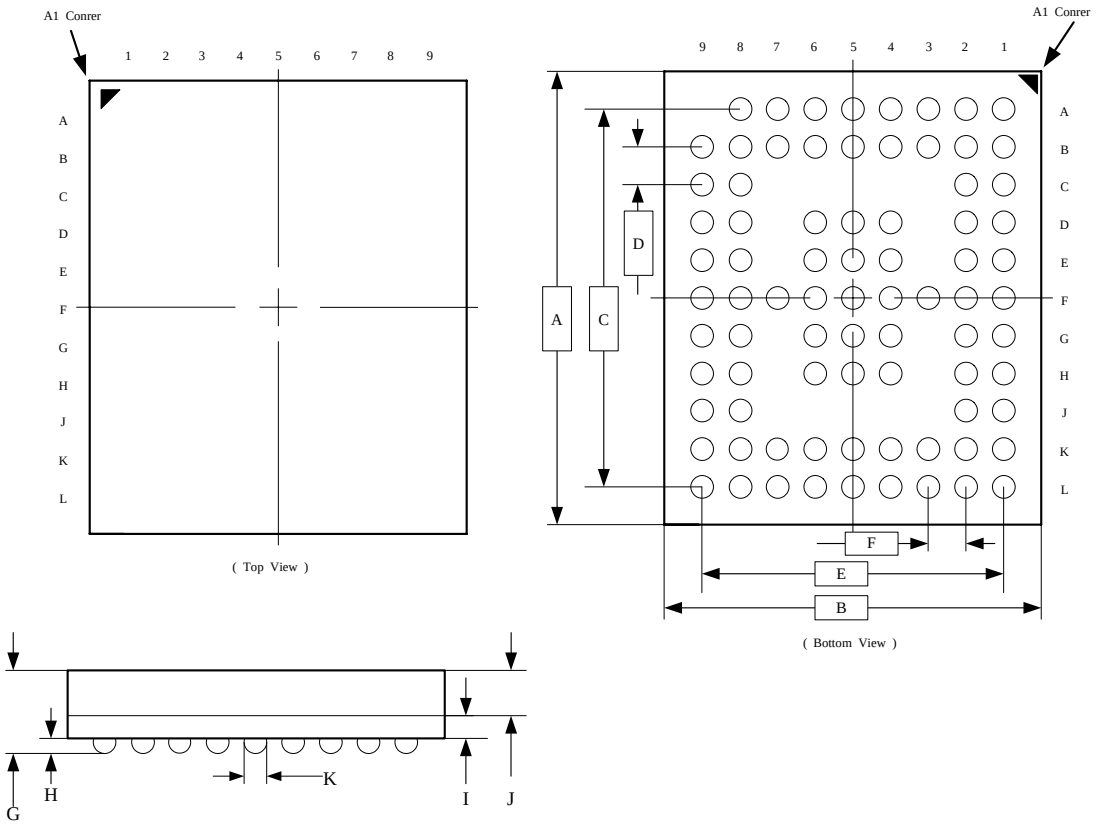

Figure 6: 80 Pin BGA Package

Table of Dimensions

No. of Leads		SYMBOL										
80 (5 X 6 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	Min	6.00	5.00	5.00	0.50	4.00	0.50		0.22	0.30	0.60	0.30
	Max							1.20	0.30			

Notes:

1. All dimensions conform to JEDEC standard MO-216.

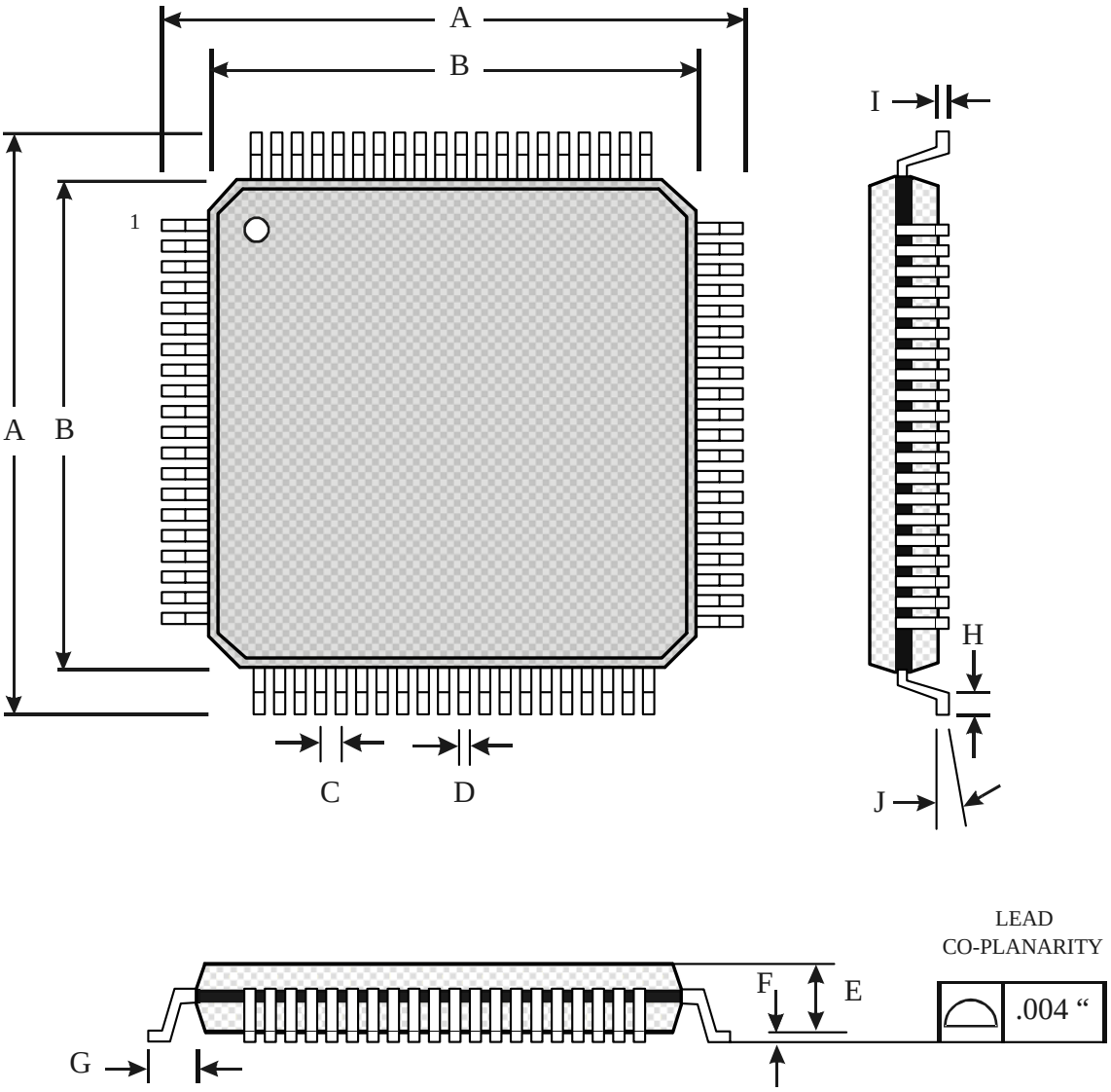

Figure 7: 80 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
80 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	11.90	9.90	0.40	0.13	1.35	0.05	1.00	0.45	0.09	0°
	MAX	12.10	10.10		0.23	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

6.0 Revision history

Rev. #	Date	Section	Description
1.0	3/5/2008	All	Official release.

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ORDERING INFORMATION

Part Number	Package Type	Copy Protection	Operating Temperature Range
CH7025B-GF	80TFBGA, Lead-free	Macrovision™	Commercial : -20 to 70°C
CH7025B-GFI	80TFBGA, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7025B-TF	80LQFP, Lead-free	Macrovision™	Commercial : -20 to 70°C
CH7025B-TFI	80LQFP, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7026B-GF	80TFBGA, Lead-free	None	Commercial : -20 to 70°C
CH7026B-GFI	80TFBGA, Lead-free	None	Industrial : -40 to 85°C
CH7026B-TF	80LQFP, Lead-free	None	Commercial : -20 to 70°C
CH7026B-TFI	80LQFP, Lead-free	None	Industrial : -40 to 85°C

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