PCB Layout and Design Guide for CH7025 TV Encoder

1.0 Introduction

The CH7025 is a device targeting handheld and similar systems which accept a digital input signal, and encodes and transmits data through three 10-bit DACs. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards. Analog RGB output and composite SYNC signal are also supported. The device accepts different data formats including RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.). 16Mbit SDRAM can is embedded in package, so Frame rate conversion is possible.

This application note focuses only on the basic PCB layout and design guidelines for CH7025 TV encoder. Guidelines in component placement, power supply decoupling, grounding, input/output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 76-pin BGA package of the CH7025. Please refer to the CH7025 datasheet for the details of the pin assignments.

2.0 Component Placement and Design Considerations

Components associated with the CH7025 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1uF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C3, C4, C5, C6) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7025 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7025 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7025 ground pins should be connected to its respective decoupling capacitor ground lead directly, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

There are four power supply pins, AVDD, AVDD_DAC, AVDD_PLL, VDDIO, DVDD, VDDQ, VDD_MEM. See **Table 1** for the Power supply pins assignment. See **Figure 1** for Power Supply Decoupling

Table 1: Power Supply Pins Assignment of the CH7025

Pin Assignment	# of Pins	Type	Symbol	Description
B5	1	Power	VDDIO	IO supply voltage (1.2-3.3V)
E3	1	Power	DVDD	Digital supply voltage (1.8V)
J5, J7, B6, C7	4	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
D9	1	Power	AVDD_PLL	PLL supply voltage (1.8V)
F9,	1	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
J6, J8	2	Power	VDDQ	SDRAM output buffer supply voltage (1.8V or 2.5V)
A7, A8, H8	3	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
E4	1	Ground	DGND	Digital supply ground
H5, H7, D7, A6	4	Ground	AGND	Analog supply ground
D8	1	Ground	AGND_PLL	PLL supply ground
F8	1	Ground	AGND_DAC	DAC supply ground
J9, H6,	2	Ground	GNDQ	SDRAM output buffer supply ground
B7, B8, G7	3	Ground	GND_MEM	SDRAM device supply ground

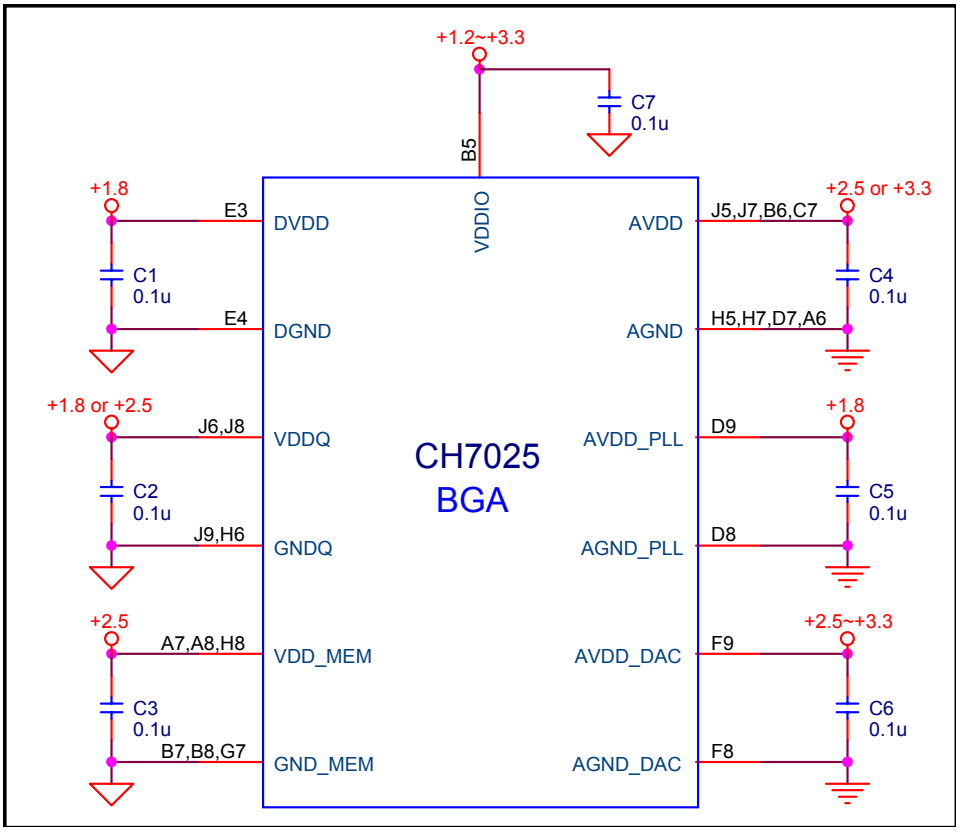

Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ω at DC; 23 Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.

2.2 Internal Reference Pins

• ISET pin

This pin sets the DAC current. A 1.2 KW, 1% tolerance resistor should be connected between ISET and AGND_DAC as shown in **Figure 2**. A smaller resistance will create more DAC current, resulting brighter TV out images. This resistor should be placed with short and wide traces as much as possible to CH7025.

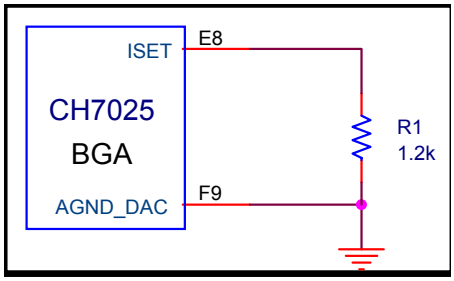

Figure 2: ISET pin connection

2.3 General Control Pins

• RESETB

This pin is the chip reset pin for CH7025. RESETB pin, which is internally pulled-up, places the device in the power on reset condition when this pin is low. A power reset switch can be placed on the RESETB pin on the PCB as a hardware reset for CH7025 as shown in **Figure 3**. When the pin is high, the reset function can also be controlled through the serial port.

• XI and XO

CH7025 has capability to accept external clocks with frequencies from 0.7 MHz to 71.6 MHz. However, we recommend predefined crystal frequencies as stated in the CH7025 datasheet for the crystal or oscillator.

Predefined crystal frequencies used for CH7025 are shown in **Table 2.** The crystal selection register is located at Register 41h.

Table 2: Predefined Crystal Frequencies

XTAL[3:0]	Frequency
0	3.6864MHz
1	3.579545MHz
2	4MHz
3	12MHz
4	13MHz
5	13.5MHz
6	14.318MHz
7	14.7456MHz
8	16MHz
9	18.432MHz
10	20MHz
11	26MHz
12	27MHz
13	32MHz
14	40MHz
15	49MHz

The crystal load capacitance, C_L, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors **Figure 3** gives a reference design for crystal circuit design.

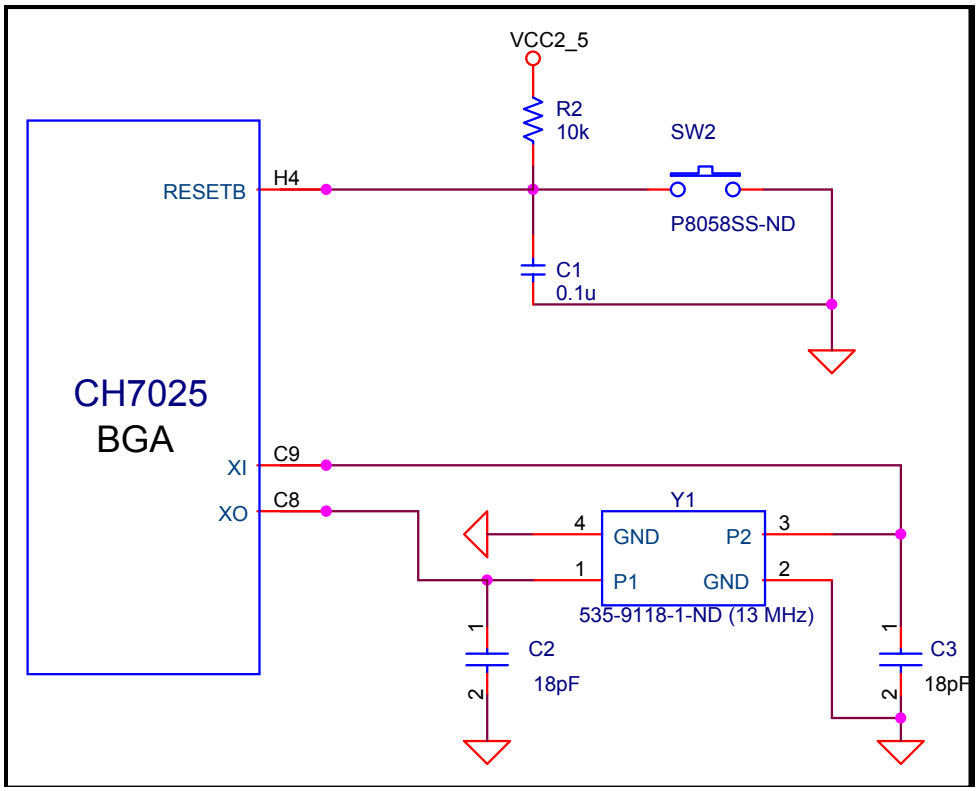

Figure 3: General Control Pins

• Reference Crystal Oscillator

CH7025 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7025. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7025 (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

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Note that the XI and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$$C_{ext} = (2 \times C_L) - C_{int} - 2C_S$$

where

C_{ext} = external load capacitance required on XI and XO pins.

C_L = crystal load capacitance specified by crystal manufacturer.

C_{int} = capacitance internal to CH7025 (approximately 10-15 pF on each of XI and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that
$C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int}$=2C L - (2C S + C_{int})

Therefore C L must be specified greater than C_{int} /2 + C_S in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

2.4 Serial Port Control for CH7025

• SPC and SPD

SPD and SPC function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC pins are pulled up to VDDIO (+1.2V ~ +3.3V) with 6.8kΩ resistors as shown in **Figure 4**.

• AS

This pin determines the serial port address of CH7025. Address = 75h when AS is high. Address = 76h when AS is low. See **Figure 4** for detail. For BGA package, the serial port address is 76h.

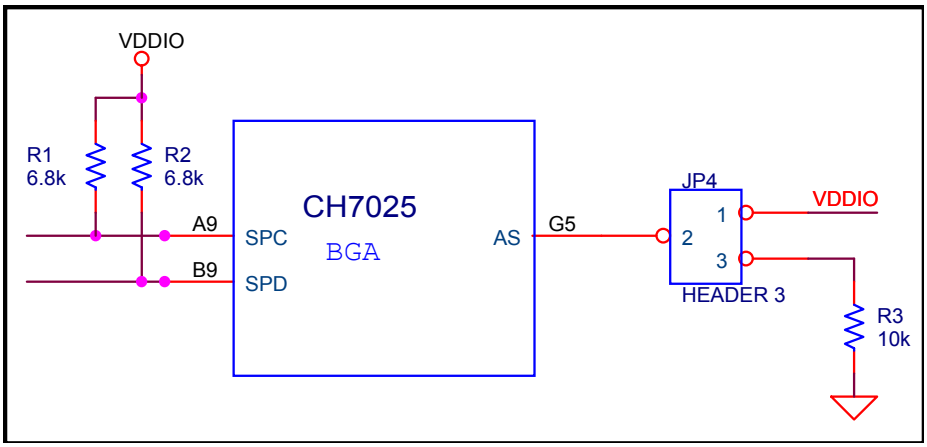


Figure 4: Serial Port Control

2.5 Input Pins

• Data Inputs

CH7025 can accept up to 24 data inputs, as shown in **Figure 5**, from a digital video port of a graphics controller. The swing is defined by VDDIO (1.2 ~ 3.3V).

• H/V Sync Pins

The horizontal/vertical sync pins can be used as inputs when the sync slave mode is used as shown in **Figure 5**.

• DE/CSB

The DE/CSB pin is used as a data input indicator (See **Figure 5**). When the pin is high, the input data is active. When the pin is low, the input data is blanking.

• GCLK

The GCLK input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.

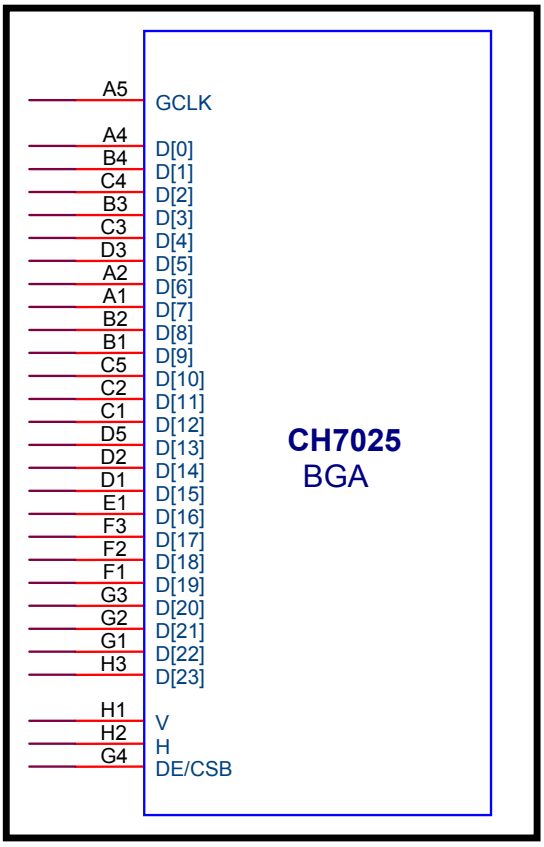


Figure 5: CH7025 Input Pins

2.6 Miscellaneous Pins

• ATPG

The ATPG pin should be left open or pulled low with a 10k Ω resister in the application as shown in **Figure 6**.

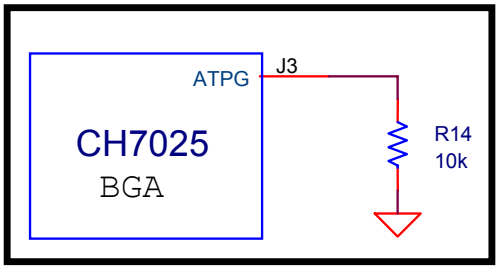


Figure 6: ATPG Pin

2.7 TV Video Outputs

- **DAC0~2**

Three on-chip 10-bit high speed DACs providing flexible output capabilities. Such as single, double or triple CVBS output, YPbPR output, RGB output and simultaneous CVBS and S-video output. If the DAC requires a double termination, a 75 Ω resistor should be placed between the CVBS pin and the ground as shown in **Figure 7**.

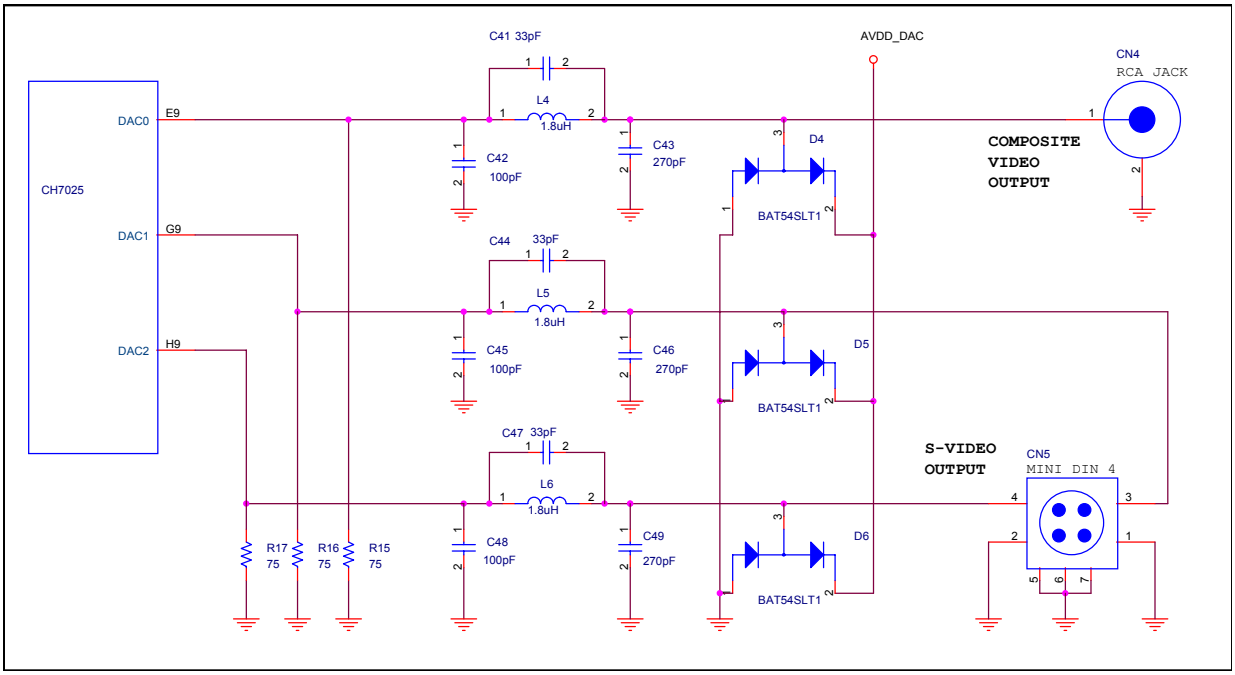


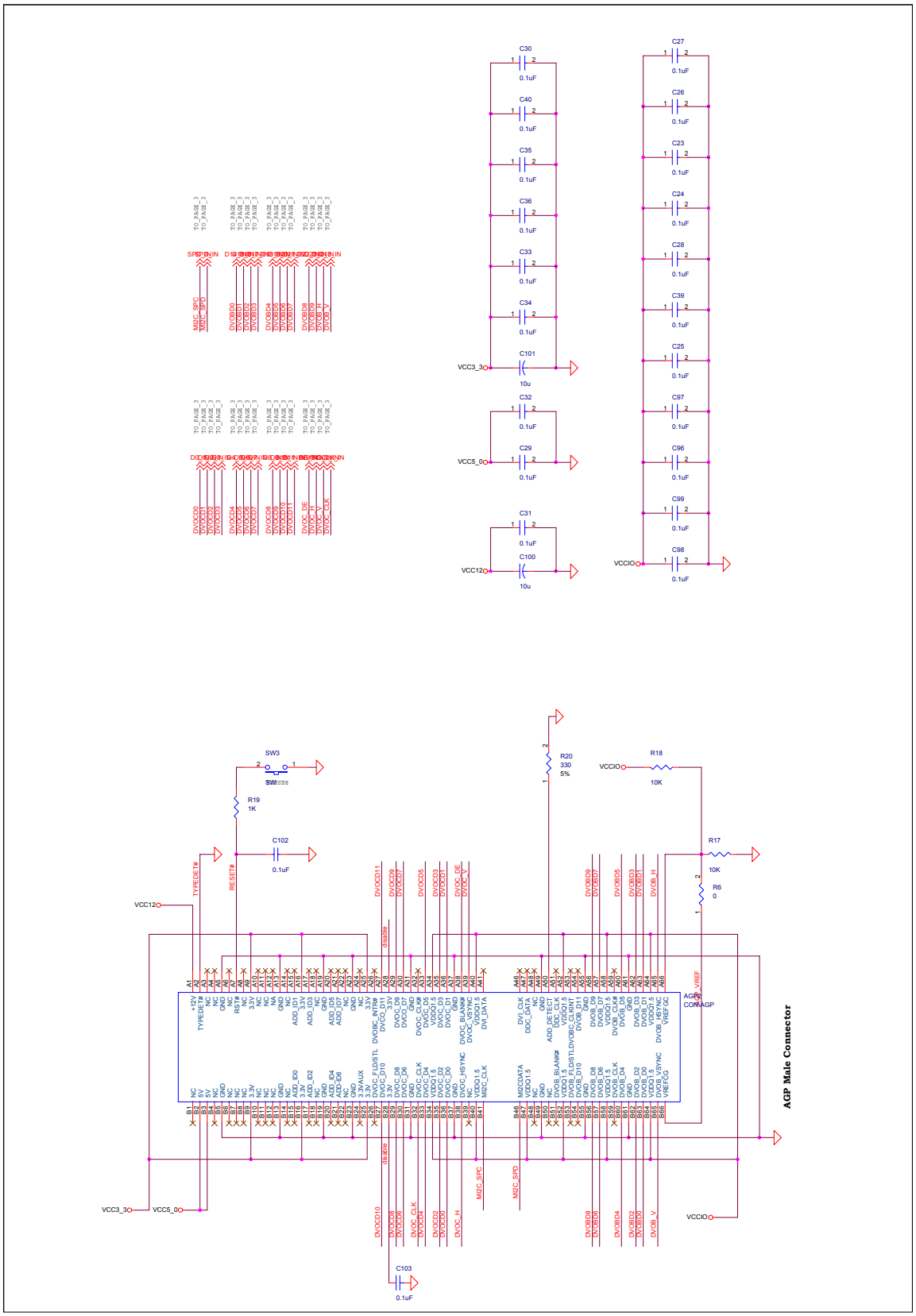
Figure 7: CH7025 BGA Video Output

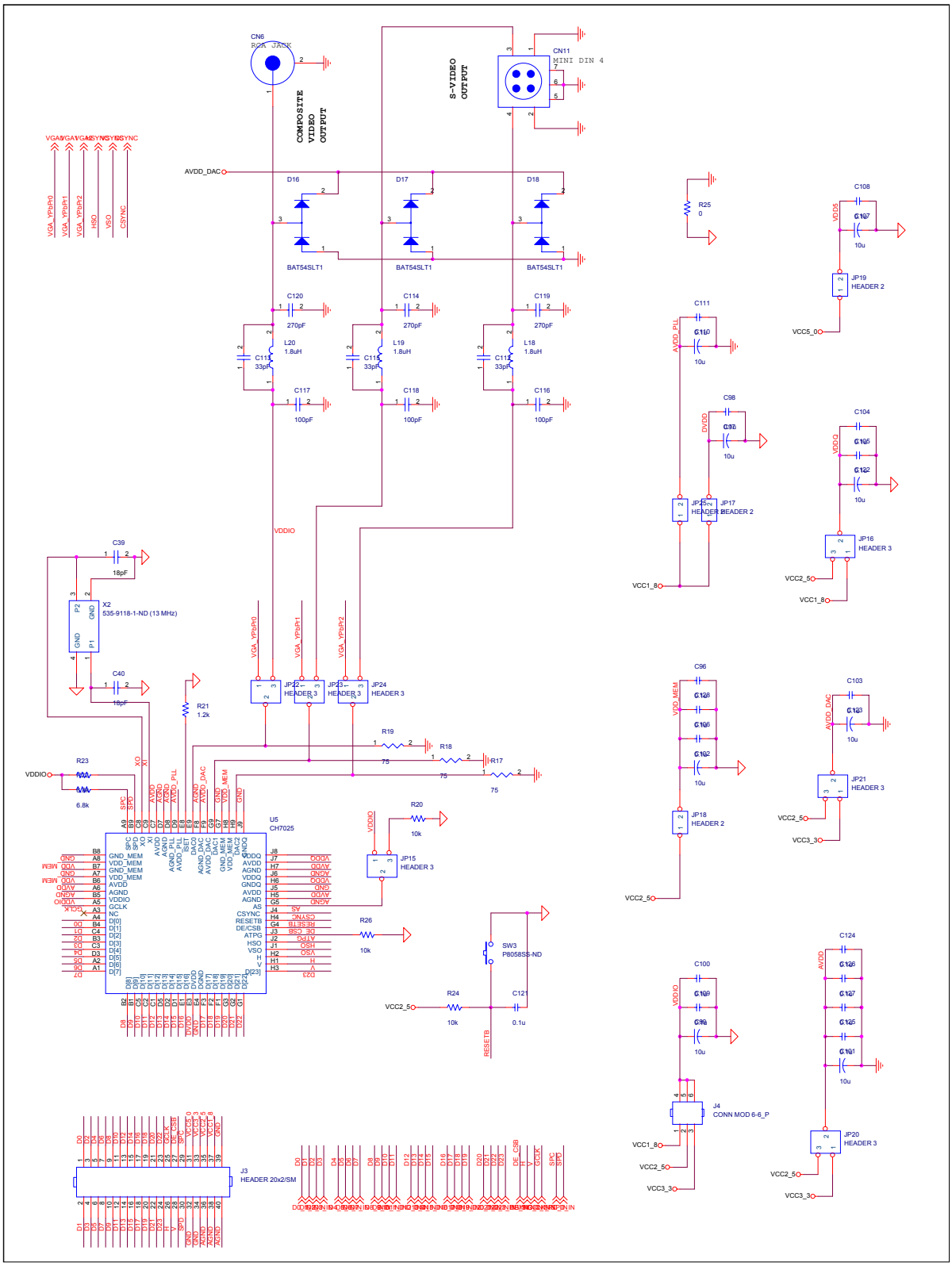
In order to minimize the hazard of ESD, a set of protection diodes are highly recommended for each HDMI Output (data and clock).

3.0 Reference Design Example

3.1 Reference Schematic

Figure 8 is the reference schematic of CH7025 BGA. This schematic is provided here for design reference only. We encourage those who will engage in an application design with CH7025 to contact Chrontel Applications group. **Table 3** provides the BOM list for **Figure 8** reference schematic.


C30
C40
C35
C36
C33
C34
C101
C32
C29
C31
C100
C27
C26
C23
C24
C28
C39
C25
C97
C96
C99
C98
0.1uF
10u
VCC3_3
VCC5_0
VCC12
VCCIO
SW3
R19
1K
R20
330
5%
R18
10K
R17
10K
R6
0
C102
C103
RESET#
TYPEDET#
AGP Male Connector


CN6
RCA JACK
COMPOSITE VIDEO OUTPUT
S-VIDEO OUTPUT
CN11
MINI DIN 4
AVDD_DAC
D16
D17
D18
BAT54SLT1
C120
C114
C119
270pF
L20
L19
L18
1.8uH
C115
C113
33pF
C117
C118
C116
100pF
VDDIO
C39
18pF
X2
535-9118-1-ND (13 MHz)
C40
R21
1.2k
R23
6.8k
R19
R18
R17
75
R20
10k
R26
10k
R24
10k
C121
0.1u
SW3
P8058SS-ND
RESETB
U5
CH7025
J3
HEADER 20x2/SM
JP15
JP22
JP23
JP24
HEADER 3
R25
0
C108
JP19
HEADER 2
VCC5_0
C111
AVDD_PLL
C98
DVDD
JP25
JP17
VCC1_8
C104
VDDIO
JP16
VCC2_5
C96
VDD_MEM
JP18
C103
AVDD_DAC
JP21
VCC3_3
C100
J4
CONN MOD 6-6_P
C124
AVDD
JP20

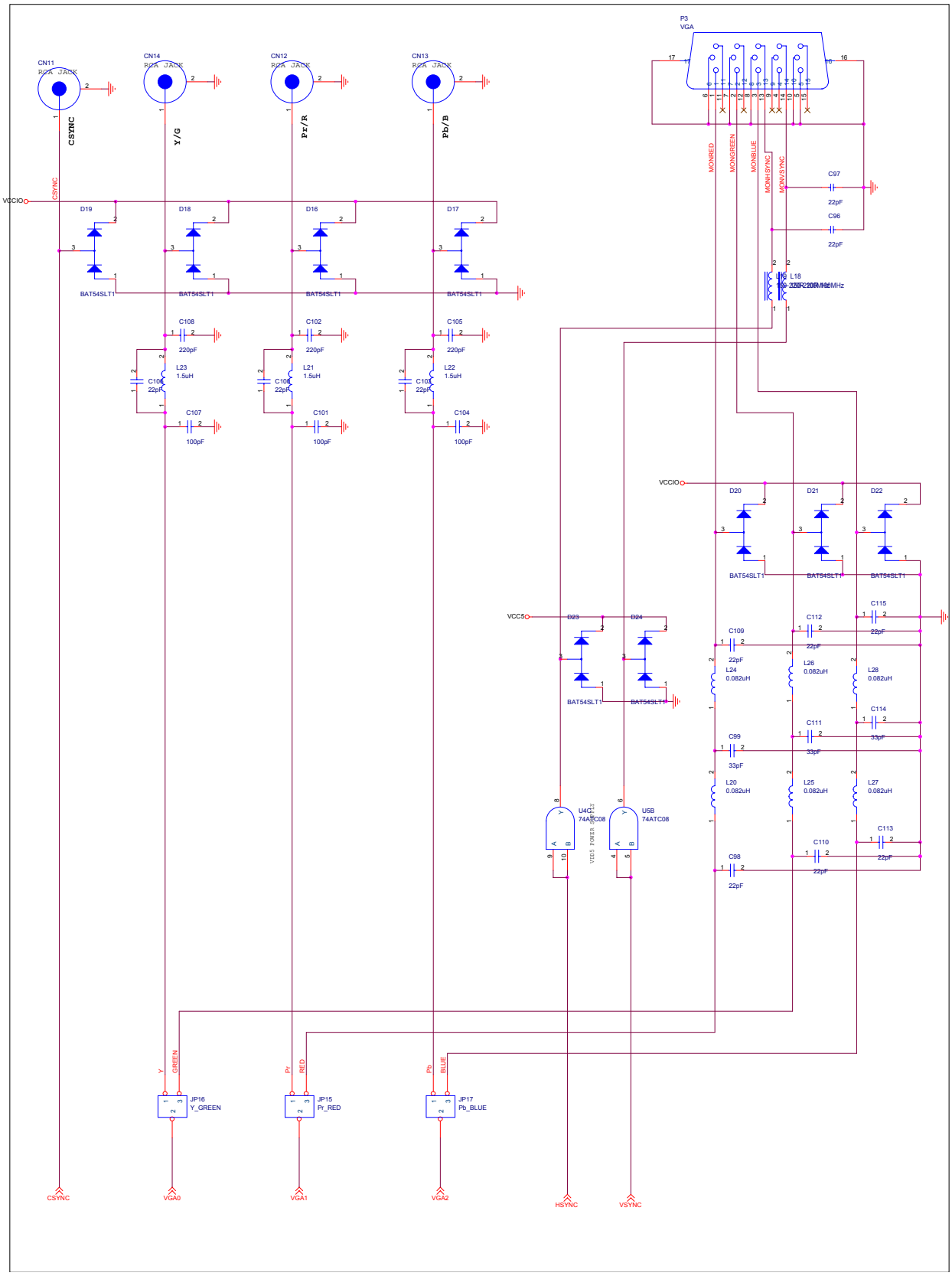


Figure 8:CH7025 BGA reference schematic

3.2 Reference Board Preliminary BOM

Table 3: CH7025 Reference Design BOM List

Item	Quantity	Reference	Part
1	1	AGP1	CON\AGP
2	5	CN4,CN7,CN8,CN9,CN10	RCA Jack
3	1	CN5	S-Video interface
4	22	C1,C2,C3,C4,C5,C6,C7,C8, C9,C10,C11,C12,C13,C14, C15,C16,C17,C18,C19,C20, C21,C22	0.1uF
5	1	C37	18pF
6	12	C38,C66,C69,C72,C75,C77, C78,C80,C81,C83,C84,C85	22pF
7	6	C41,C44,C47,C76,C79,C82	33pF
8	6	C42,C45,C48,C67,C70,C73	100pF
9	3	C43,C46,C49	270pF
10	16	C50,C51,C52,C53,C54,C55, C56,C57,C59,C60,C61,C63, C64,C65,C88,C93	0.1u
11	10	C58,C62,C86,C87,C89,C90, C91,C92,C94,C95	10u
12	3	C68,C71,C74	220pF
13	12	D4,D5,D6,D7,D8,D9,D10, D11,D12,D13,D14,D15	BAT54SLT1
14	7	JP1,JP2,JP3,JP4,JP6,JP9, JP12	HEADER 3
15	1	JP5	
16	4	JP7,JP10,JP11,JP14	HEADER 2
17	1	JP8	HEADER 3
18	1	JP13	HEADER 3
19	1	J1	HEADER 20x2/SM
20	1	J2	HEADER 3x2/SM
21	3	L4,L5,L6	1.8uH
22	3	L7,L8,L9	1.5uH
23	6	L10,L11,L12,L13,L14,L15	0.082uH
24	2	L16,L17	FB 150-220R 100MHz
25	1	P1	VGA
26	1	R1	1K
27	1	R2	330
28	5	R3,R5,R9,R12,R13	10k
29	2	R4,R16	0
30	1	R7	1.2k
31	3	R8,R10,R11	75ohm
32	2	R14,R15	6.8k
33	1	SW1	SW
34	1	SW2	SW
35	1	U3	CH7025
36	1	U4	74ATC08
37	1	X1	535-9118-1-ND (13 MHz)

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