CH7025/CH7026 TV/VGA Encoder

Features

- TV encoder targets for handheld device, surveillance camera and automobile market.
- Supports multiple output formats such as analog TV (NTSC and PAL), VGA and HDTV (480p,576p,720p, 1080i). Sync signals can be provided in separated or composite manner.
- Three on-chip 10-bit high speed DACs providing flexible output capabilities such as single, double or triple CVBS output, YPbPr output, RGB output and simultaneous CVBS and S-video output.
- 90/180/270 degree image rotation and vertical or horizontal flip.
- 16-Mbit SDRAM is used as a frame buffer for frame rate conversion.
- Flexible up and down scaling.
- Programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supports various RGB (RGB888, RGB666, RGB565 and etc), YCbCr (4:4:4 YcbCr, ITU656) and 2x or 3x multiplexed input. CPU interface is also supported.
- Supports flexible input resolution up to 800x800 and 1024x680.
- Pixel by pixel brightness, contrast, hue and saturation adjustment for each output is supported. (For RGB output, only brightness and contrast adjustment is supported).
- Pixel by pixel horizontal position adjustment and line by line vertical position adjustment.
- Supports Macrovision^{TM} 7.1 L1 in CH7025. CH7026 is a Non-Macrovision version of the CH7025
- Supports Macrovision^{TM} copy protection for progressive scan TV (480p, 576p) in CH7025
- Supports CGMS-A for analog TV and HDTV
- TV/Monitor connection detection capability. DAC can be switched off based on detection result.
- Programmable power management.
- Flexible pixel clock frequency from graphics controller is supported. (2.3MHz –120MHz)
- Flexible input clock from crystal or oscillator is supported. (2.3MHz – 64MHz)
- Supports slave input clock mode only.
- Fully programmable through serial port.
- IO and SPC/SPD voltage supported is from 1.2V to 3.3V.
- Offered in BGA or QFP package.

General Description

The CH7025/CH7026 is a semiconductor device targeting for handheld market, surveillance camera and automobile multimedia system. This device accepts digital video signals through its 24-bit input bus and generates NTSC, PAL, VGA or HDTV (480p, 576p, 720p and 1080i) video signal by its 10-bit DACs. In addition, CH7025/26 has an embedded 16-Mbit SDRAM to support the CPU interface.

CH7025/26 has incorporated an advanced technology that can perform real-time video rotations and frame rate conversions for incoming video stream. These complicated tasks are achieved by storing video data to the internal SDRAM and applying scaling process if required. CH7025/26 provides great flexibility for accepting different video data formats including RGB and YcbCr (e.g. RGB565, RGB 666, RGB 888, ITU 656).

The CH7025/26 is available in BGA or QFP package.

Note: the above feature list is subject to change without notice. Please contact Chrontel for more information and current updates.

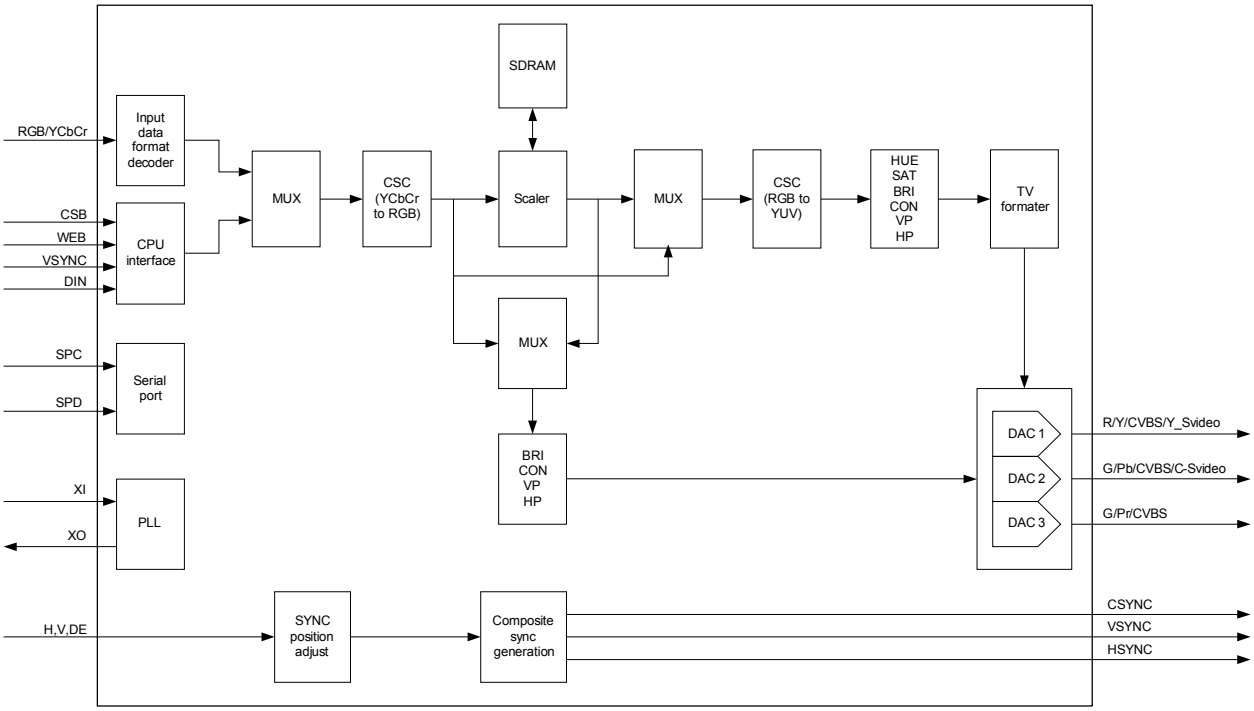

Figure 1: CH7025/CH7026 block diagram

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1.0 Pin-out

1.1 Package diagram

1.1.1 The 80-pin BGA Package Diagram

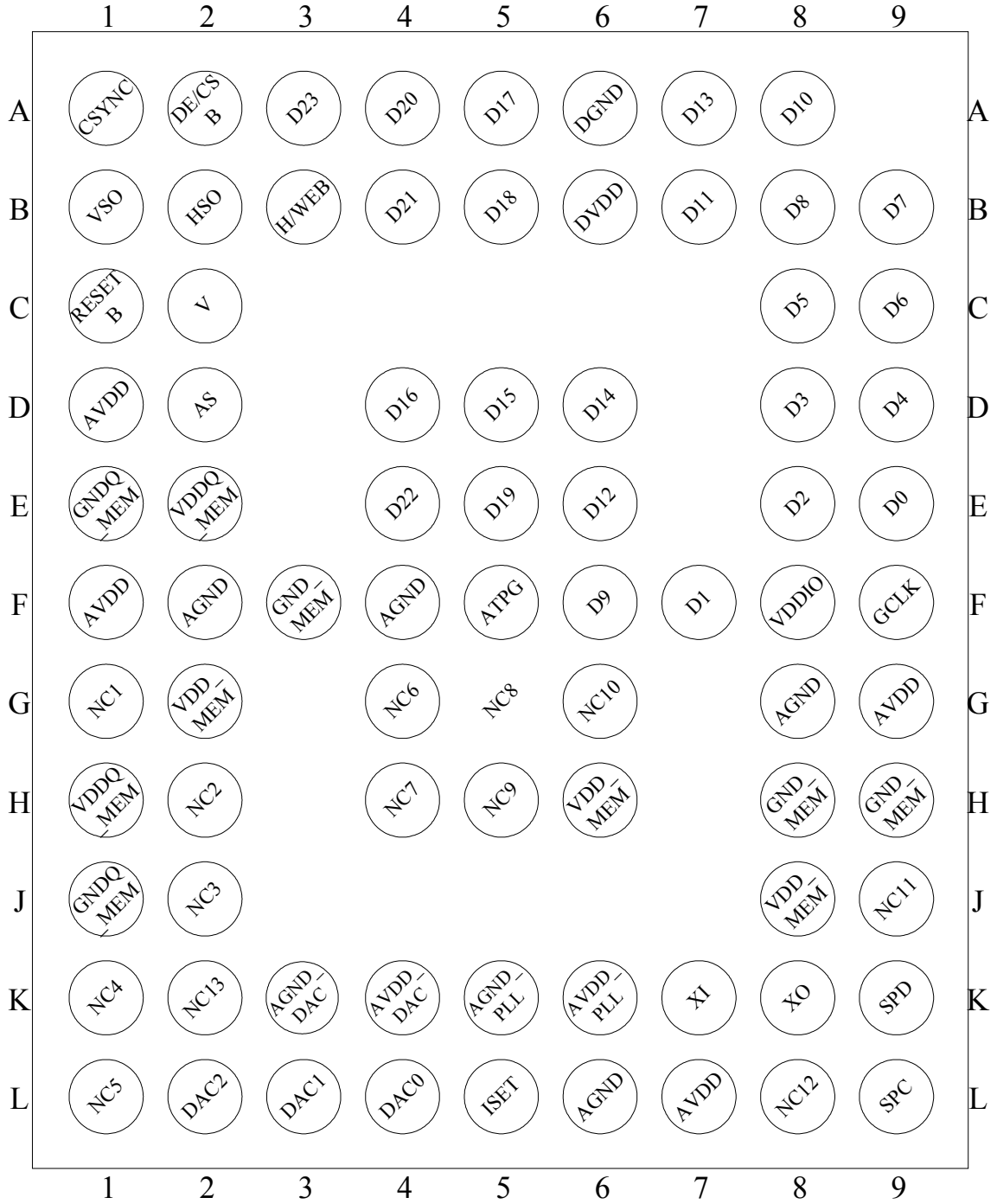

Figure 2: 80-pin BGA package

1.1.2 The 80-pin LQFP Package Diagram

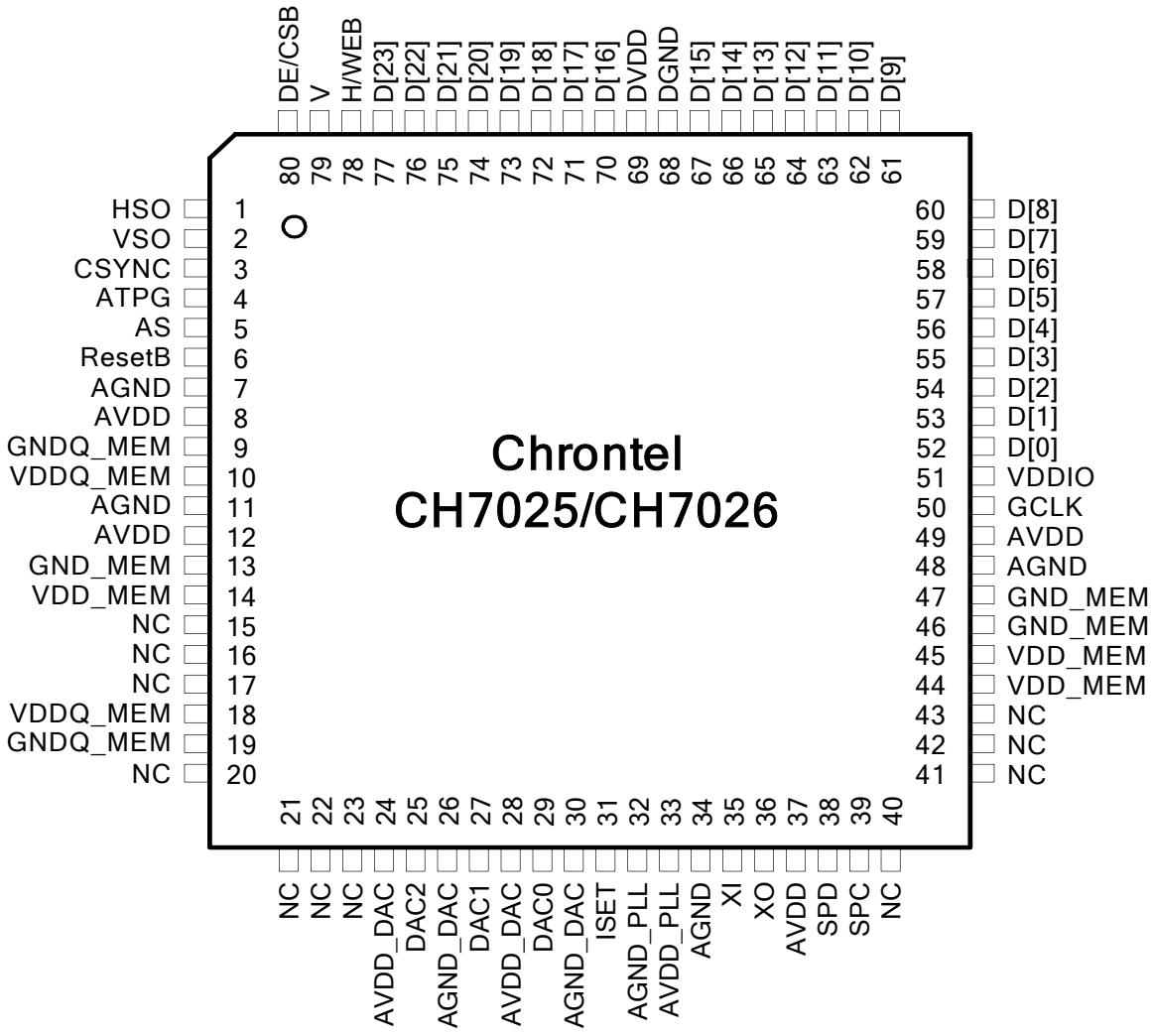

Figure 3: 80-pin LQFP package

1.2 Pin description

Table 1: Pin name description (BGA package)

Pin #	Type	Symbol	Description
A3, E4, B4, A4, E5, B5, A5, D4, D5, D6, A7, E6, B7, A8, F6, B8, B9, C9, C8, D9, D8, E8, F7, E9	In(F)	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
C2	Inout	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
B3	Inout	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
A2	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also the CSB signal of CPU interface The amplitude will be 0 to VDDIO.
D2	In	AS	Address select
F5	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V. Reserved pin.
C1	In	ResetB	Reset * Input When this pin is low, the device is held in the hardware reset condition. When this pin is high, reset is controlled through the serial port.
K9	Inout	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resister is required.
L9	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resister is required.
L4	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
L3	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v

Pin #	Type	Symbol	Description
L2	Out	DAC2	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
L5	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
K7	In	XI	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
K8	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
F9	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
B1	Out	VSO	Vertical sync signal output
B2	Out	HSO	Horizontal sync signal output
A1	Out	CSYNC	Composite sync output
F8	Power	VDDIO	IO supply voltage (1.2-3.3V)
B6	Power	DVDD	Digital supply voltage (1.8V)
D1, F1, L7, G9	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
K6	Power	AVDD_PLL	PLL supply voltage (1.8V)
K4	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
E2, H1	Power	VDDQ_MEM	SDRAM output buffer supply voltage (1.8V or 2.5V)
G2, J8, H6	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
A6	Power	DGND	Digital supply ground
F4, F2, L6, G8	Power	AGND	Analog supply ground
K5	Power	AGND_PLL	PLL supply ground
K3	Power	AGND_DAC	DAC supply ground
E1, J1	Power	GNDQ_MEM	SDRAM output buffer supply ground
F3, H9, H8	Power	GND_MEM	SDRAM device supply ground

Table 2: Pin name descriptions (LQFP80 package)

Pin #	Type	Symbol	Description
52 - 67 70 - 77	In	D[23:0]	Data[0] through Data[23] Inputs These pins accept the 24 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
79	Inout	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
78	Inout	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
80	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. CSB signal input of CPU interface The amplitude will be 0 to VDDIO.
5	In	AS	Chip address select 0: 76h 1: 75h
4	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be low. Voltage level is 0 to 3.3V. Reserved pin.
6	In	ResetB	Reset * Input When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
38	Inout	SPD	Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port. External pull-up resister is required.
39	In	SPC	Serial Port Clock Input This pin functions as the clock pin of the serial port. External pull-up resister is required.
29	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
27	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
25	Out	DAC2	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3v
31	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
35	In	XI	Crystal Input / External Reference Input For master mode and some situation of the slave mode, a parallel

Pin #	Type	Symbol	Description
			resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
36	Out	XO	Crystal Output For master mode and some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
50	In	GCLK	External Clock Inputs The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
2	Out	VSO	Vertical sync signal output, The amplitude of this pin is from 0 to AVDD
1	Out	HSO	Horizontal sync signal output, The amplitude of this pin is from 0 to AVDD
3	Out	CSYNC	Composite sync output, The amplitude of this pin is from 0 to AVDD
51	Power	VDDIO	IO supply voltage (1.2-3.3V)
69	Power	DVDD	Digital supply voltage (1.8V)
8 12 37 49	Power	AVDD	Analog supply voltage
33	Power	AVDD_PLL	PLL supply voltage
24 28	Power	AVDD_DAC	DAC power supply
10 18	Power	VDDQ_MEM	SDRAM output buffer supply voltage
14 44 45	Power	VDD_MEM	SDRAM device supply voltage
68	Power	DGND	Digital supply ground
7 11 34 48	Power	AGND	Analog supply ground
32	Power	AGND_PLL	PLL supply ground
26 30	Power	AGND_DAC	DAC supply ground
9 19	Power	GNDQ_MEM	SDRAM output buffer supply ground
13 46 47	Power	GND_MEM	SDRAM device supply ground

2.0 Functional description

2.1 Input interface

2.1.1 Overview

Five distinct methods of transferring data to the CH7025/CH7026 are described. They are:

1. Unitary data, clock input at 1X the pixel rate
2. Multiplexed data, clock input at 1X of pixel rate
3. Multiplexed data, clock input at 2X of pixel rate
4. Multiplexed data, clock input at 3X of pixel rate
5. 8/16/24 bit CPU interface

For the multiplexed data, clock at 1X pixel rate, the data applied to the CH7025/CH7026 is latched with both edges of the clock (also referred to as dual edge transfer mode or DDR). For the multiplexed data, clock at 2X or 3X pixel rate the data applied to the CH7025/CH7026 is latched with one edge of the clock (also known as single edge transfer mode or SDR). For the unitary data, clock at 1X pixel rate, the data applied to the CH7025/CH7026 is latched with one edge of the clock .The polarity of the pixel clock can be reversed under serial port control. Hsync and Vsync can be input individually or embedded into data signal such as BT656 input format.

2.1.2 Input Clock and Data Timing Diagram

Figure 6 below shows the timing diagram for input data and clocks. The first XCLK waveform represents the input clock for single edge transfer (SDR) methods. The second XCLK waveform represents the input clock for the dual edge transfer (DDR) method. The timing requirements are given in later section.

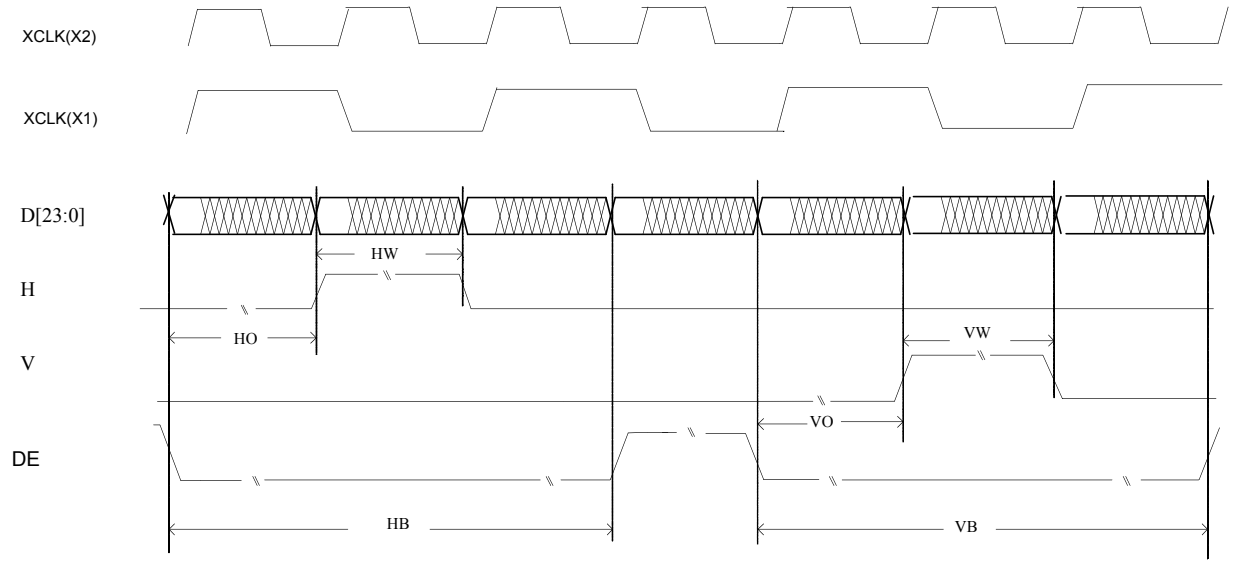

Figure 4: Clock, Data and Interface Timing

2.1.3 Input data voltage

The voltage level of input pins D[23:0], H/WEB, V, DE/CSB, SPC, SPD are from 0 to VDDIO. These pins support two input mode, one is CMOS mode, and the other is pseudo differential mode. The default is CMOS mode with CMOS level on these pins. When control bit **DIFFEN** is high, the input is pseudo differential mode that uses a reference voltage (VREF) to compare with input voltage and decide input logic value. The VREF value can be 80%, 70%, 60% and 50% of VDDIO value, referring to **VRTM[1:0]**. The pseudo differential mode can accept the wide range of the input voltage level from 1.2v to 3.3v, while the CMOS mode can accept 1.8v to 3.3v input voltage.

2.1.4 Input data format

The following table indicates the supported input data format by CH7025/CH7026.

Table 3: Input data format

MULTI		IDF	D[23:16]	D[15:8]	D[7:0]
0		0	R[7:0]	G[7:0]	B[7:0]
		1	2'b00,R[5:0]	2'b00,G[5:0]	2'b00,B[5:0]
		2	3'b000,R[4:0]	2'b00,G[5:0]	3'b000,B[4:0]
		3	3'b000,R[4:0]	3'b000,G[4:0]	3'b000,B[4:0]
		4	R[7:3],G[7:5]	R[2:0],G[1],G[4:2], B[7]	B[6:3],G[0],B[2:0]
		5	8'h00	Y[7:0]	C[7:0]
		6	4'h0, Y[9:6]	Y[5:0],C[9:8]	C[7:0]
		7	Y[7:0]	Cb[7:0]	Cr[7:0]
		9	6'h00, R[5:4]	R[3:0],G[5:2]	G[1:0],B[5:0]
		10	8'h00	R[4:0],G[5:3]	G[2:0],B[4:0]
		11	8'h00	1'b0, R[4:0],G[4:3]	G[2:0],B[4:0]
1	PA	0		4’h0, R[7:4]	R[3:0],G[7:4]
	PB			4’h0, G[3:0]	B[7:0]
	PA	1		7’h00, R[5]	R[4:0],G[5,3]
	PB			7’h00, G[2]	G[1:0],B[5:0]
	PA	2			R[4:0],G[5,3]
	PB				G[2:0],B[4:0]
	PA	3			1’b0,R[4:0],G[4,3]
	PB				G[2:0],B[4:0]
	PA	4		4’h0, R[7:4]	R[3],G[7:5],R[2:0],G[1]
	PB			4’h0, G[4:2], B [7]	B[6:3],G[0],B[2:0]
	PA	5			Y[7:0]
	PB				C[7:0]
	PA	6		6’h00, Y[9:8]	Y[7:0]
	PB			6’h00, C[9:8]	C[7:0]
	PA	7		4’h0, Y[7:4]	Y[3:0],Cb[7:4]
	PB			4’h0, Cb[3:0]	Cr[7:0]
2	PA	0			R[7:0]
	PB				G[7:0]
	PC				B[7:0]
	PA	7			Y[7:0]
	PB				Cb[7:0]
	PC				Cr[7:0]

(PA,PB,PC represent the parts of one pixel data)

IDF[3:0] describes the major input data format that CH7025/CH7026 accepts. They are:

IDF = 0: 888 RGB input
IDF = 1: 666 RGB input
IDF = 2: 565 RGB input
IDF = 3: 555 RGB input
IDF = 4: DVO input
IDF = 5: 8-bit YCbCr4:2:2 input
IDF = 6: 10-bit YCbCr4:2:2 input
IDF = 7: 8-bit YCbCr4:4:4 input
IDF = 9: Consecutive aligned 666 RGB input
IDF = 10: Consecutive aligned 565 RGB input
IDF = 11: Consecutive aligned 555 RGB input

Table 3 above describe the 24-bit input data format under unitary mode. For multiplexed input, input data needs to be de-multiplexed to unitary input first then this table can be applied. The multiplexed input data format is shown in figure below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCbCr formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (e.g.; PA and PB) will contain a complete pixel. (3X input has the similar feature)

It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (PA) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCbCr data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per ITU-R BT.656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in ITU-R BT.656). All non-active pixels should be 0 in RGB formats, and 16 for Y, 128 for Cr and Cb in YCbCr formats.

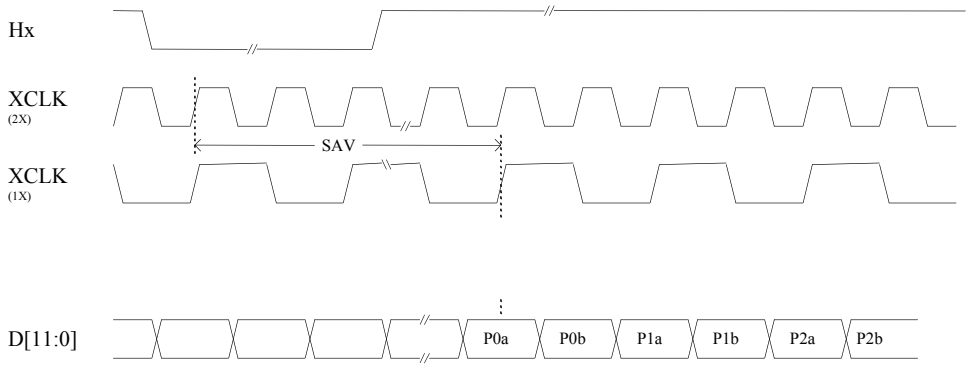

Figure 5: 12-bit Multiplexed Input Data Formats

In YCbCr 4:2:2 with embedded sync mode, the hardware can detect the connect error and correct it automatically, for example, if the input P14 and P15 are a group, but you take P13 and P14 as a group, the hardware can detect this error and correct it by run-in code.

2.2 Chip output

2.2.1 TV output

The CH7025/CH7026 support the following output formats:

Table 4: Supported SDTV standards

No.	Standards	Field Rate (Hz)	Total	Scan Type
0	NTSC-M	60/1.001	858x525	Interlaced
1	NTSC-J	60/1.001	858x525	Interlaced
2	NTSC-443	60/1.001	858x525	Interlaced
3	PAL-B/D/G/H/I	50	864x625	Interlaced
4	PAL-M	60/1.001	858x525	Interlaced
5	PAL_N	50	864x625	Interlaced
6	PAL-Nc	50	864x625	Interlaced
7	PAL_60	60/1.001	858x525	Interlaced

Table 5: Supported EDTV/HDTV standards

Standards		Field/Frame Rate(Hz)	Total	Active	Clock(MHz)	Scan Type
480/60p	SMPTE293M EIA770.2A	60/1.001	858x525 or 1716x525	720x480	27 or 54	Progressive
576/50p	ITU-R BT1358	50	864x625 or 1728x625	720x576	27 or 54	Progressive
720/60p	SMPTE296M	60 or 60/1.001	1650x750	1280x720	74.25 or 74.176	Progressive
720/50p	SMPTE296M	50	1980x750	1280x720	74.25	Progressive
1080/60i	SMPTE274M	60 or 60/1.001	2200x1125	1920x1080	74.25 or 74.176	Interlaced
1080/50i	SMPTE274M	50	2640x1125	1920x1080	74.25	Interlaced
1080/50i	SMPTE295M	50	2376x1250	1920x1080	74.25	Interlaced

CVBS, S-video, YPbPr and analog RGB output are supported, when output analog RGB, composite sync output is available.

2.2.2 VGA output

CH7025/CH7026 also supports analog RGB output through video DACs. Typically used resolution is 800x600, 856x480, 800x480 or 640x480. Vertical sync and horizontal sync signal can be provided. Composite sync output is also supported. The type of composite sync can be programmed through register map.

Table 6: Composite sync type

CSSEL[2:0]	Composite sync type
0	Vsync XOR Hsync
1	Vsync OR Hsync
2	Vsync AND Hsync

2.2.3 Video DAC output

The DAC output is configured by the register bits **VFMT[2:0]**. **DACS[1:0]** bits are used to control the multiple output format i.e. dual or triple CVBS output, dual CVBS and S-Video output and etc. **DACSP[2:0]** bits are to swap the DAC output sequence such as CVBS, S-Video or S-Video, CVBS. Detailed information of these bits are described in register bits description section of this document. **Table 7** below lists the DAC output configurations of the CH7025/CH7026:

Table 7: Video DAC Configurations for CH7025/CH7026

DAC0	DAC1	DAC2
CVBS	Y	C
CVBS	CVBS	0
CVBS	CVBS	CVBS
Y(R)	Pb(G)	Pr(B)

2.2.4 DAC single/double termination

The DAC output of CH7025/CH7026 can be single terminated or double terminated. Using single termination will save power consumption while double termination is likely to minimize the effect of the cable. See also the description of register bit **SEL_R**.

2.2.5 TV connection detect

CH7025/CH7026 can detect the TV connection by setting register SPPSNS. It can detect which DAC are connected, short to ground or not connected.

2.2.6 Picture enhancement

The CH7025/CH7026 has the capability of vertical and horizontal output picture position adjustment. It can automatically put the picture in the display center, and the vertical or horizontal position is also programmable through user input. And also it can provide brightness, contrast, hue, saturation adjustment and text enhancement functions. (For analog RGB output, only brightness and contrast adjustment is available).

CH7025/CH7026 also supports vertical or horizontal flip and rotation (0, 90, 180 and 270 degree) functions.

2.2.7 Color Sub-carrier Generation

CH7025/CH7026 has two ways to generate the color sub-carrier frequency. If the **GCLK** from the graphics controller has a steady center frequency and very small jitters, the sub-carrier can be derived from the **GCLK**. However, since even a ±0.01% sub-carrier frequency variation is enough to cause some TV to lose color lock, CH7025/CH7026 has the ability to generate the sub-carrier frequency from the crystal when the **GCLK** from the graphics device cannot meet the requirement. In this case, the crystal has to be present. In other words, the only configuration where the off-chip crystal can be removed is when slave mode is used and the graphics controller provides **GCLK** with required characteristics.

In addition, CH7025/CH7026 has the capability to gen-lock the color sub-carrier with Vsync. Also, it has the ability to operate in a “stop dot crawl” mode for NTSC CVBS output when the first sub-carrier generation method is used.

2.2.8 ITU-R BT.470 Compliance

The SDTV output of CH7025/CH7026 is mostly compliant with ITU-R BT.470 standard except for the items below.

- The frequencies of horizontal sync, vertical sync, and color sub-carrier depend on the quality of **GCLK** from graphics controller and/or the off-chip crystal.
- It is assumed that gamma correction, if required, is performed in the graphics device.

- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements. However, they may have a small variation depending on the actual input and output format.
- The actual bandwidths of the luminance and chrominance signals depend on the input resolution and the filter selection.

2.3 Testing Functions

2.3.1 Test pattern select

Setting TSTP[4:0] of 04h on the second page of register map can select different video patterns that go through datapath, according to the following table (TEST bit5 of 04h on the second page has to be 1 to enable test mode). TSYNC is to select which sync will be used internally generated sync or external input sync.

Table 8: Test pattern selection

TSTP[3:0]	Test pattern
0	Black
1	White
2	Vertical ramp
3	Horizontal ramp
4	Color bar
5	One pixel wide color bar
6	Zigzag
7	Reserved
8	One black and one white frame
9	Black lines on white background

When TSTP = 9, TSTW[2:0] is used to determine the interval in lines between two black lines with white background.

2.3.2 SDRAM power down

Generally, SDRAM can have two kinds of power down modes. One is power down mode, the other is deep power down mode. For power down mode, by dropping the CKE signal from high to low and holding CS signal high, then SDRAM goes into the power down mode. All data contents will be held in the bank. For deep power down mode, a command is required to issued. There is a bit called MEMPD in register map. It can be used to enable the deep power mode. During deep power mode, all the data in memory banks will be lost, and the SDRAM leakage current is less than 1uA. **An very important thing required to be noted here is that not all the SDRAM parts support either power down or deep power down mode**. In these cases, even CH7025/CH7026 enters into power down, the leakage current is still large (>100uA). This current is primarily derived from the SDRAM die. For detailed information about power down of SDRAM, please refer to SDRAM vendors' specifications.

3.0 Electrical specifications

3.1 Absolute maximum rating

Symbol	Description	Min	Typ	Max	Units
	All 1.8V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		2.5 5.0	V
	Input voltage of all digital pins (see note[3])	GND – 0.5		VDDIO+0.5	V
TAMB	Ambient operating temperature	-40		85	°C
TSTOR	Storage temperature	-40		150	°C
TJ	Junction temperature			150	°C
TVPS	Vapor phase soldering (5 second) Vapor phase soldering (11 second) Vapor phase soldering (1 minute)			260 245 225	°C

Note:
1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce permanent damage.
3. The digital input voltage will follow the I/O supply voltage (VDDIO), the I/O supply voltage range is from 1.2V to 3.3V.

3.2 Recommended operating conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Crystal and I/O Power Supply Voltage	2.5	3.3	3.5	V
AVDD_DAC	DAC Power Supply Voltage	2.5	3.3	3.5	V
AVDD_PLL	PLL Power Supply Voltage	1.71	1.8	1.89	V
DVDD	Digital Power Supply Voltage	1.71	1.8	1.89	V
VDDIO	Data I/O supply voltage	1.14		3.5	V
RL1	Output load to DAC Current Reference		1.2k		Ω
R_{L2}	Output load to DAC Outputs		37.5		Ω
VDDQ_MEM	Memory data interface supply	2.375	2.5	2.625	V
VDD_MEM	Memory core supply	2.375	2.5	2.625	V
VDD18	Generic for all 1.8V supplies	1.71	1.8	1.89	V
VDD33	Generic for all 3.3V supplies	2.5	3.3	3.5	V

3.3 Electrical characteristics

(Operating Conditions: T_A = 0°C – 70°C, VDD18=1.8V± 5%, VDD33 =2.5V – 3.5V)

Symbol	Description	Min	Typ	Max	Units
	Video D/A Resolution	10	10	10	bits
	Full scale output current		38		mA
	Video level error			10	%
I_{VDD18}	Total VDD18 supply current (1.8V supplies)		35		mA
I_{VDD33} (1)	Total VDD33 supply current (3.3V supplies) (see note)		30		mA
I_{VDDQ}	Memory data interface supply current		0.1		mA
I_{VDD_MEM}	Memory core supply current		20		mA
I_{PD}	Total Power Down Current		<20		uA

Notes:
1. Applies for one DAC and single 75Ohm termination. The current of every DAC is less than 25mA for single termination and less than 50mA for double termination.
2. Some memories do not support deep power down mode.

3.4 Digital inputs / outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 3.0 mA	GND-0.5		0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD33 + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		**0.4**	V
V_{HYS}	Hysteresis of Serial Port Input		0.25			V
V_{DATAIH}	Data I/O (1) High Voltage		VDDIO/2 +0.25		VDDIO + 0.5	V
V_{DATAIL}	Data I/O Low Voltage		GND-0.5		VDDIO/2 -0.25	V
V_{MISCIH}	Miscellaneous Input High Voltage (2)		VDD33 – 0.5		VDD33 + 0.5	V
V_{MISCIL}	Miscellaneous Input Low Voltage (2)		GND-0.5		0.6	V
V_{SYNCOH}	Miscellaneous Output High Voltage (3)		VDD33 x 0.8			V
V_{SYNCOL}	Miscellaneous Output Low Voltage (3)				0.3	V
I_{MISCPU}	Miscellaneous Input Pull Up Current (2)	V_{IN} = 0	0.5		5.0	uA
I_{MISCPD}	Miscellaneous Input Pull Down Current (2)	V_{IN} = VDD33	0.1		1.1	uA

Notes:
1. Applies to D[23:0], GCLK, H, V and DE. VDDIO is the I/O supply, ranging from 1.2V to 3.3V.
2. Applies to AS, RESETB and ATPG.
3. Applies to HSO, VSO, CSYNC.

3.5 AC specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$f_{CRYSTAL}$	Input (CRYSTAL) frequency		2.3		64	MHz
f_{GCLK}	Input (GCLK) frequency		1.5		120	MHz
DC_{GCLK}	Input (GCLK) Duty Cycle	$T_S + T_H < 1.2ns$	30		70	%
t_{GJIT}	GCLK clock jitter tolerance			10		ns
t_S	Setup Time: D[23:0], H, V and DE to GCLK	GCLK to D[23:0], H, V, DE = Vref	0.35			ns
t_H	Hold Time: D[23:0], H, V and DE to GCLK	D[23:0], H, V, DE = Vref to GCLK	0.5			ns
t_{STEP}	De-skew time increment		50		80	ps

4.0 Package Dimensions

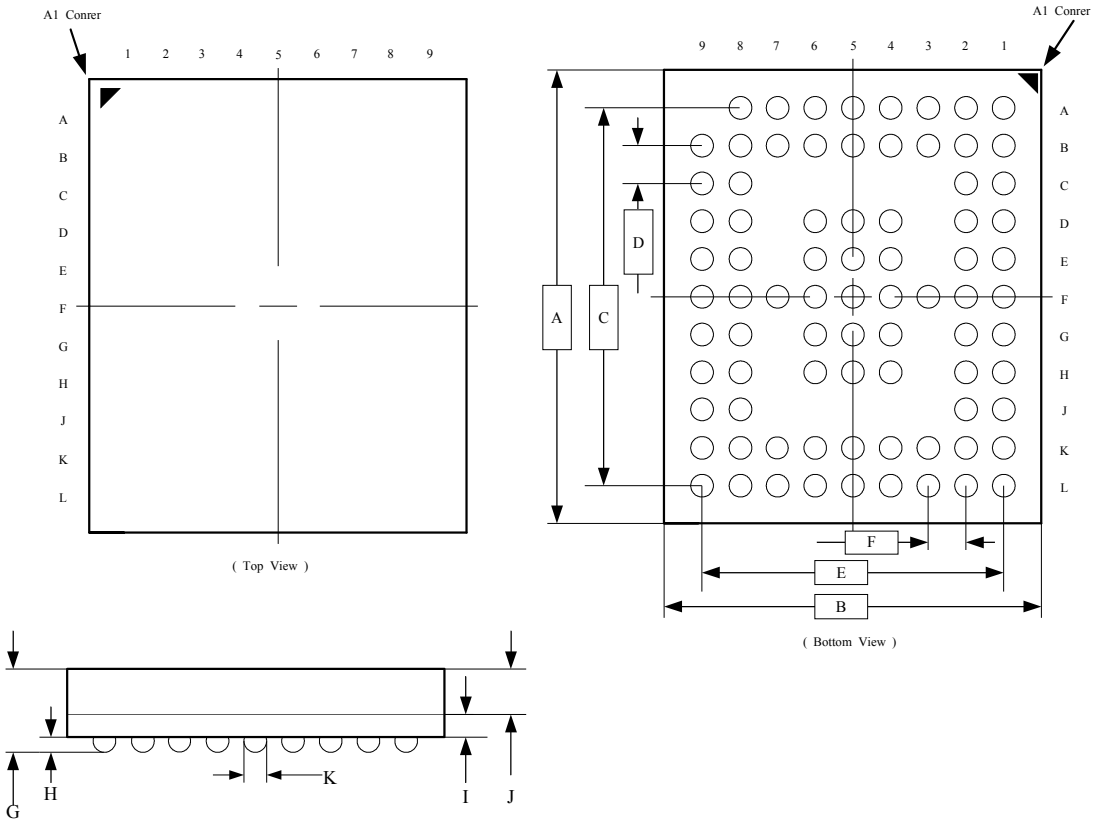

Figure 6: 80 Pin BGA Package

Table of Dimensions

No. of Leads		SYMBOL										
80 (5 X 6 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	Min	6.00	5.00	5.00	0.50	4.00	0.50		0.22	0.30	0.60	0.30
	Max							1.20	0.30			

Notes:

1. All dimensions conform to JEDEC standard MO-216.

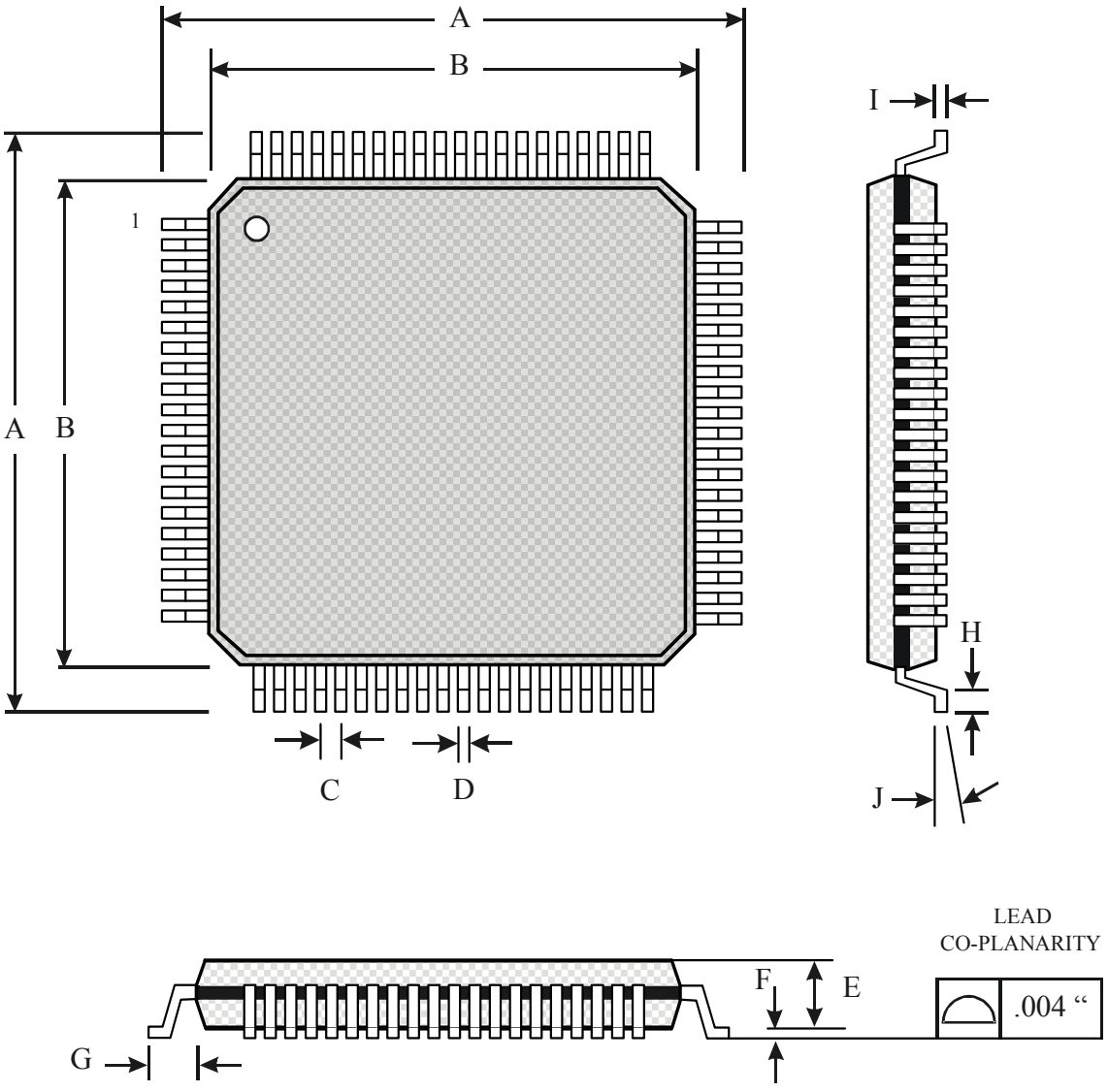

Figure 7: 80 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
80 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	11.90	9.90	0.40	0.13	1.35	0.05	1.00	0.45	0.09	0°
	MAX	12.10	10.10		0.23	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

5.0 Revision history

Rev. #	Date	Section	Description
1.0	3/5/2008	All	Official release.

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ORDERING INFORMATION

Part Number	Package Type	Copy Protection	Operating Temperature Range
CH7025B-GF	80TFBGA, Lead-free	Macrovision™	Commercial : -20 to 70°C
CH7025B-GFI	80TFBGA, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7025B-TF	80LQFP, Lead-free	Macrovision™	Commercial : -20 to 70°C
CH7025B-TFI	80LQFP, Lead-free	Macrovision™	Industrial : -40 to 85°C
CH7026B-GF	80TFBGA, Lead-free	None	Commercial : -20 to 70°C
CH7026B-GFI	80TFBGA, Lead-free	None	Industrial : -40 to 85°C
CH7026B-TF	80LQFP, Lead-free	None	Commercial : -20 to 70°C
CH7026B-TFI	80LQFP, Lead-free	None	Industrial : -40 to 85°C

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