**LAB 2 PLAN AND RUBRIC**

**Date:** 21 April 2020

**Subject:** Computer Systems Design

**Topic:** Hardware optimization to PPA constraints

**Objectives:**

* Students can design hardware logic according to multi-cycle approach
* Students can design hardware logic according to pipelined approach
* Students can use Xilinx Vivado Design Suite to gather metrics from implemented design
* Students understand how to achieve PPA trade-off using multi-cycle and pipelined approaches

**PLANNING**

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| timing | activities | resources | aim of activity |
| 10 min | **Introduction.** Outline the lab. | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Prepare the students to the lab |
| 5 min | **Practice.** Understanding the task variant | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Understand the lab variant and discuss it with the instructors. |
| 20 min | **Practice.** Designing multi-cycle implementation of hardware design | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Developing the skill of designing multi-cycle implementation of hardware design |
| 10 min | **Practice.** Debugging multi-cycle implementation of hardware design in simulation | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Developing the skill of debugging multi-cycle implementation of hardware design in simulation |
| According to the schedule | **Break** | | |
| 20 min | **Practice.** Uploading and debugging multi-cycle implementation of hardware design on FPGA board | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Developing the skill of uploading and debugging multi-cycle implementation of hardware design on FPGA board |
| 5 min | **Practice.** Gathering performance and area metrics of the multi-cycle implementation | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Understand how to gather performance and area metrics using Xilinx Vivado Design Suite |
| 20 min | **Practice.** Checking the results   1. Demonstration of the results to the instructors 2. Getting questions from the instructors | - | Checking the students results and grading.  Giving the questions and the practical task for understanding. It is needed to evaluate the students results. |
| According to the schedule | **Break** | | |
| 20 min | **Practice.** Designing pipelined implementation of hardware design | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Developing the skill of designing pipelined implementation of hardware design |
| 10 min | **Practice.** Debugging pipelined implementation of hardware design in simulation | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Developing the skill of debugging pipelined implementation of hardware design in simulation |
| 10 min | **Practice.** Uploading and debugging pipelined implementation of hardware design on FPGA board | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Developing the skill of uploading and debugging pipelined implementation of hardware design on FPGA board. |
| 5 min | **Practice.** Gathering performance and area metrics of the pipelined design and comparing them with multi-cycle implementation | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Understand performance and area differences between multi-cycle and pipelined implementations of hardware. |
| According to the schedule | **Break** | | |
| 10 min | **Practice.** Gathering and comparing power metrics of the multi-cycle and pipelined implementations (auxiliary task) | Study guide  (The section with Lab2 Task and Lab 2 Guide) | Understand power differences between multi-cycle and pipelined implementations of hardware. |
| 20 min | **Evaluation.** Checking the task for understanding | - | Checking the task for understanding and grading |
| 15 min | **Conclusion part.** Summarization of the lab | Study guide  (The section with Lab 2) | Summarize the main points of the lab. Structuring of the given knowledge and trained skills. |

**RUBRIC**

The rubric of the lab is focused on the overall performance, and it enables overall judgement of the student work. The result grade is depended on the result of practice part, the answers on the questions about the obtained results and the results of the task for understanding given after practical part. For the lab the students can get maximum 10 points.

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| Grade, points | Description |
| 0-5 | Students have partially completed the practical task |
| 6 | Students have successfully completed the practical task |
| 8 | Students have successfully completed the practical task and correctly answered the questions |
| 10 | Students have successfully completed the practical task, correctly answered the questions and done the auxiliary task |