QuTech Quantum Error Correction Challenge

Description:
In this challenge, participants will be tasked with using the available noisy intermediate-scale quantum (NISQ) hardware to implement a program that makes use of quantum error detection/correction (QED/QEC) techniques. The team at QuTech proposes a particular topic around a fundamental building block of quantum error correction, Quantum Parity Measurements (QPM). Nevertheless, any project that makes use of QED/QEC will be admissible, and scoring will be adapted on a case-by-case basis to assess all projects fairly.

Background:
Besides quantum communication, which participants will be able to explore in the QuTech Quantum Encryption challenge, another outstanding goal of QuTech is the development of fault-tolerant quantum computing. In honoring this tradition, we present a challenge around the implementation of QPMs, projective measurements used to stabilize quantum information, allowing the detection and, potentially, correction of quantum errors. These form the basis of quantum error correction, and their implementation is, therefore, fundamental to move us from the NISQ era into fully fault-tolerant quantum computing.

Goal:
The proposed goal of this challenge is the implementation of high-fidelity QPMs. It will be the responsibility of participants to define a set of relevant metrics, either from existing literature or of their own making, to assess the performance of their implementations. Furthermore, participants will be challenged to iteratively improve on their original implementation of QPMs through error mitigation strategies, in such a way as to develop an understanding of the fundamental error channels inherent to NISQ hardware.

Scoring:
Points will be assigned based on five different criteria:

- technical merit demonstrated in the implementation of quantum parity measurements, definition of circuit benchmarks or in exploiting other concepts from quantum mechanics to achieve the stated goal;
- creativity in the specification of new circuit benchmarks or in studying the most prominent error channels present in the available hardware platforms;
- utility of the concepts developed;
- relevance and novelty of the participants approach to addressing the stated goals;
- clarity in the communication of concepts and motivation for the chosen approach.

Quantum Parity Measurements:
In an actively corrected quantum memory, quantum information is distributed among many elementary degrees of freedom. QPMs are a procedure used to actively gather information about which (or whether) errors took place, particularly in stabilizer codes, by measuring subsets of qubits in Pauli matrix bases. An ideal QPM provides a discretization of the set of errors that occurred in the qubits over which quantum information was distributed.

Participants are encouraged to read parts of reference [1] for a theoretical framework of the concepts. Furthermore, curious participants can read about the experimental implementation of various QPMs in the context of recent experiments on quantum error correction codes, the Bacon-Shor code [2], the color code [3], the repetition code [4] and the surface code [5].

Benchmarking and performance metrics:
Participants should choose and/or create different metrics to assess the performance of the implemented circuits and determine the effectiveness of any methods employed to further improve the performance of their circuits. In particular, participants could consider metrics on the fidelity of the parity assessment, the average assignment probability being a trivial example, or more involved metrics on, for example, the back-action of the parity measurement.

Error mitigation and NISQ hardware:
Participants are encouraged to augment their projects through the exploration of error mitigation strategies, to determine whether they can be employed to further improve the implemented circuits. Examples of these could range from dynamical decoupling to more involved approaches, such as randomized compiling. Furthermore, participants are encouraged to draw information from these experiments to study the effects of specific error channels inherent to the NISQ hardware platforms used in the event, whether through direct measurement or matching with simulation results.

Bibliography:
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