CC1310 SimpleLink™ 超低功耗低于 1GHz 无线 MCU

1 器件概述

1.1 特性

- 微控制器
  - 强大的 ARM® Cortex®-M3 处理器
  - EEMBC CoreMark®评分：142
  - EEMBC ULPBench™评分：158
  - 时钟速率最高可达 48MHz
  - 32KB、64KB 和 128KB 系统内可编程闪存
  - 8KB 缓存静态随机存取存储器 (SRAM)（或用作通用 RAM）
  - 20KB 超低泄漏 SRAM
  - 2 引脚 cJTAG 和 JTAG 调试
  - 支持无线 (OTA) 升级
- 超低功耗传感器控制器
  - 可独立于系统其余部分自主运行
  - 16 位架构
  - 2KB 超低泄漏代码和数据 SRAM
- 有效的代码尺寸架构，在 ROM 中放置 TI-RTOS、驱动程序、引导加载程序的部件
- 与 RoHS 兼容的封装
  - 7mm × 7mm RGZ VQFN48 封装（30 个通用输入/输出 (GPIO)）
  - 5mm × 5mm RHB VQFN32 封装（15 个 GPIO）
  - 4mm × 4mm RSM VQFN32 封装（10 个 GPIO）
- 外设
  - 所有数字外设引脚均可连接任意 GPIO
  - 四个通用定时器模块（8 × 16 位或 4 × 32 位，均采用脉宽调制 (PWM)）
  - 12 位模数转换器 (ADC)、200MSPS、8 通道模拟多路复用器
  - 持续时间比较器
  - 超低功耗时钟比较器
  - 可编程电流源
  - UART
  - 2 个同步串行接口 (SSI)（SPI、MICROWIRE 和 TI）
  - I^2C、I2S
  - 实时时钟 (RTC)
  - AES-128 安全模块
  - 真随机数发生器 (TRNG)
  - 支持八个电容感测按钮
  - 集成温度传感器
- 外部系统
  - 片上内部 DC-DC 转换器
  - 无缝集成 SimpleLink™CC1190 范围扩展器
- 低功耗
  - 宽电源电压范围：1.8 至 3.8V
  - RX：5.4mA
  - TX（+10dBm 时）：13.4mA
  - Coremark 运行时的 48MHz 有源模式微控制器 (MCU)：2.5mA (51µA/MHz)
  - 有源模式 MCU：48.5 CoreMark/mA
  - 有源模式传感器控制器（24 MHz）：0.4mA + 8.2µA/MHz
  - 传感器控制器，每秒唤醒一次来执行一次 12 位 ADC 采样：0.95µA
  - 待机电流：0.7µA（实时时钟 (RTC) 运行，RAM 和 CPU 保持）
  - 关断电流：185nA（发生外部事件时唤醒）
- 射频 (RF) 部分
  - 出色的接收器灵敏度：远距离模式下为 -124dBm；50kbps 时为 -110dBm（低于 1GHz）
  - 出色的可选择性 (±100kHz)：56dB
  - 出色的阻断性能 (±10MHz)：90dB
  - 可编程输出功率：时最高可达 +9dBm
  - 单端或差分 RF 接口
  - 适用于符合全球射频规范的系统
    - ETSI EN 300 220 和 EN 303 204（欧洲）
    - FCC CFR47 第 15 部分（美国）
    - ARIB STD-T108（日本）
  - 无线 M 总线以及所选 IEEE®802.15.4g PHY
- 工具和开发环境
  - 功能全面的低成本开发套件
  - 针对不同 RF 配置的多种参考设计
  - 数据包监听器 PC 软件
  - Sensor Controller Studio
  - SmartRF™Studio
  - SmartRF Flash Programmer2
  - IAR Embedded Workbench®（用于 ARM）
  - Code Composer Studio™

1.2 应用

- 315、433、470、500、779、868、915、920MHz 工业、科学和医疗 (ISM) 及短程设备 (SRD) 系统
- 信道间隔为 50kHz 至 5MHz 的低功耗无线系统
- 家庭和楼宇自动化
- 无线警报和安全系统
- 工业用监控和控制
- 智能电网和自动抄表
- 无线医疗保健 应用
- 无线传感器网络
- 有源 RFID
- IEEE 802.15.4g、支持 IP 的智能对象 (6LoWPAN)、无线仪表总线、KNX 系统、Wi-SUN™及专有系统
- 能量收集 应用
- 电子货架标签 (ESL)
- 远距离传感器 应用
- 热量分配表

1.3 说明

CC1310 属于德州仪器 (TI) CC26xx 和 CC13xx 系列器件中的 经济高效型超低功耗 2.4GHz 和低于 1GHz 的 RF 器件。™。它具有极低的有源 RF 和微控制器 (MCU) 电流消耗，除了灵活的低功耗模式外，可确保卓越的电池使用寿命，适用于由小型纽扣电池供电的远距离操作以及能源采集型 应用。

CC1310 是经济高效型、超低功耗无线 MCU 中低于 1GHz 系列的首款器件。CC1310 器件在支持多个物理层和 RF 标准的平台中将灵活的超低功耗 RF 收发器和强大的 48MHz Cortex®-M3 微控制器相结合。专用无线控制器 (Cortex®-M0) 处理 ROM 或 RAM 中存储的低层 RF 协议命令，从而确保超低功耗和灵活度。CC1310 器件不会以牺牲 RF 性能为代价来实现低功耗；CC1310 器件具有出色的灵敏度和稳定性（可选择性和阻断）性能。

CC1310 器件是一款高度集成、真正的单片解决方案，其整合了一套完整的 RF 系统及一个片上 DC-DC 转换器。

传感器可由专用的超低功耗自主 MCU 以超低功耗方式进行处理，该 MCU 可配置为处理模拟和数字传感器，因此主 MCU (Cortex-M3) 能够最大限度地延长休眠时间。

CC1310 电源和时钟管理以及无线系统需要采用特定配置并由软件处理才能正确运行，这一切均已在 TI-RTOS 中实现。TI 建议将此软件框架应用于针对器件的全部应用程序开发过程。完整的 TI-RTOS 和器件驱动程序以源代码形式免费提供。

器件信息(1)

产品型号	封装	封装尺寸（标称值）
CC1310F128RGZ	VQFN (48)	7.00mm x 7.00mm
CC1310F128RHB	VQFN (32)	5.00mm x 5.00mm
CC1310F128RSM	VQFN (32)	4.00mm x 4.00mm
CC1310F64RGZ	VQFN (48)	7.00mm x 7.00mm
CC1310F64RHB	VQFN (32)	5.00mm x 5.00mm
CC1310F64RSM	VQFN (32)	4.00mm x 4.00mm
CC1310F32RGZ	VQFN (48)	7.00mm x 7.00mm
CC1310F32RHB	VQFN (32)	5.00mm x 5.00mm
CC1310F32RSM	VQFN (32)	4.00mm x 4.00mm

(1) 详细信息请见节 9。

1.4 功能框图

图 1-1 所示为 CC1310 器件框图。

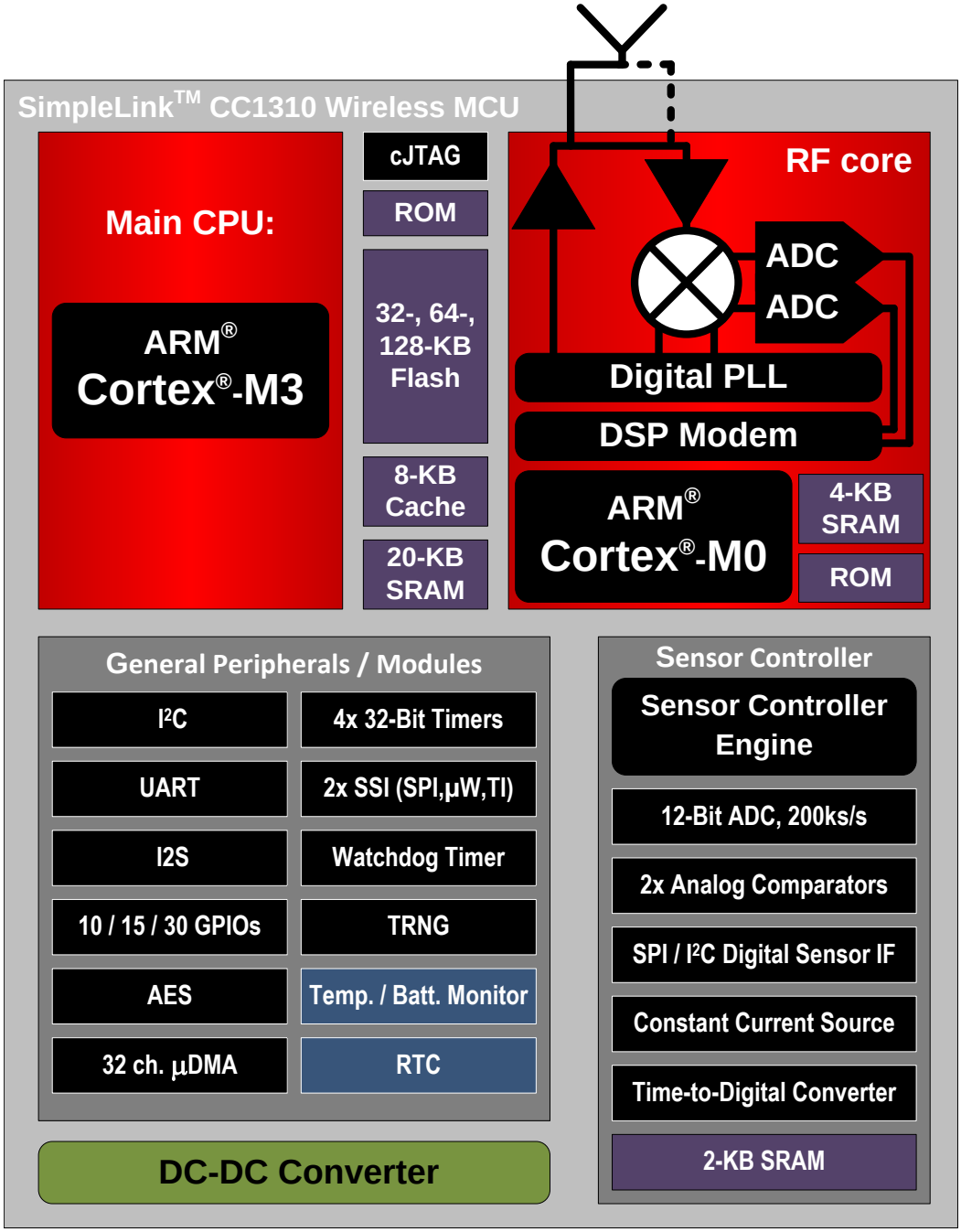


图 **1-1. CC1310** 框图

内容

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from October 28, 2015 to October 27, 2016 **Page**

- 已添加 32KB 和 64KB 至系统内可编程闪存的*特性*要点 1
- 已更改 至正确引脚数（位于*特性*要点 与 *RoHS 兼容的封装* 1
- 已更改 CC1310 框图 3
- Changed Figure 4-2, corrected typo in pin name 9
- Changed the table note in Section 5.1 from: VDDS to: ground 14
- Changed ESD ratings for all pins in Section 5.2 14
- Added OOK modulation power consumption to Section 5.4 15
- Added OOK modulation sensitivity to Section 5.6 17
- Added receive parameters for 431-MHz to 527-MHz band in Section 5.7 17
- Added transmit parameters for 431-MHz to 527-MHz band in Section 5.9 20
- Changed ADC reference voltage to correct value in Section 5.11 21
- Added thermal characteristics for RHB and RSM packages in Section 5.18 24
- Changed Figure 5-5 by extending the temperature 28
- Changed BOD restriction footnote in Table 6-2—restriction does not apply to die revision B and later 36
- Added Section 6.10 39
- 已更改 图 8-1 42

Changes from September 30, 2015 to October 28, 2015 **Page**

- Added the RSM and RHB packages 7

Changes from August 31, 2015 to September 30, 2015 **Page**

- 已更改 器件状态，从“产品预览”更改为“量产数据” 1
- Removed the RSM and RHB packages 7

3 Device Comparison

Table 3-1 lists the device family overview.

Table 3-1. Device Family Overview

DEVICE	PHY SUPPORT	FLASH (KB)	RAM (KB)	GPIOs	PACKAGE SIZE
CC1310F128RGZ	Proprietary, Wireless M-Bus, IEEE 802.15.4g	128	20	30	7 mm × 7 mm
CC1310F64RGZ	Proprietary, Wireless M-Bus, IEEE 802.15.4g	64	16	30	
CC1310F32RGZ	Proprietary, Wireless M-Bus, IEEE 802.15.4g	32	16	30	
CC1310F128RHB	Proprietary, Wireless M-Bus, IEEE 802.15.4g	128	20	15	5 mm × 5 mm
CC1310F64RHB	Proprietary, Wireless M-Bus, IEEE 802.15.4g	64	16	15	
CC1310F32RHB	Proprietary, Wireless M-Bus, IEEE 802.15.4g	32	16	15	
CC1310F128RSM	Proprietary, Wireless M-Bus, IEEE 802.15.4g	128	20	10	4 mm × 4 mm
CC1310F64RSM	Proprietary, Wireless M-Bus, IEEE 802.15.4g	64	16	10	
CC1310F32RSM	Proprietary, Wireless M-Bus, IEEE 802.15.4g	32	16	10	

3.1 Related Products

Wireless Connectivity The wireless connectivity portfolio offers a wide selection of low-power RF solutions suitable for a broad range of application. The offerings range from fully customized solutions to turnkey offerings with precertified hardware and software (protocol).

Sub-1 GHz Long-range, low power wireless connectivity solutions are offered in a wide range of Sub-1 GHz ISM bands.

Companion Products Review products that are frequently purchased or used with this product.

Reference Designs for CC1310 The TI Designs Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump-start your system design, all TI Designs include schematic or block diagrams, BOMs and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

4 Terminal Configuration and Functions

4.1 Pin Diagram – RSM Package

Figure 4-1 shows the RSM pinout diagram.

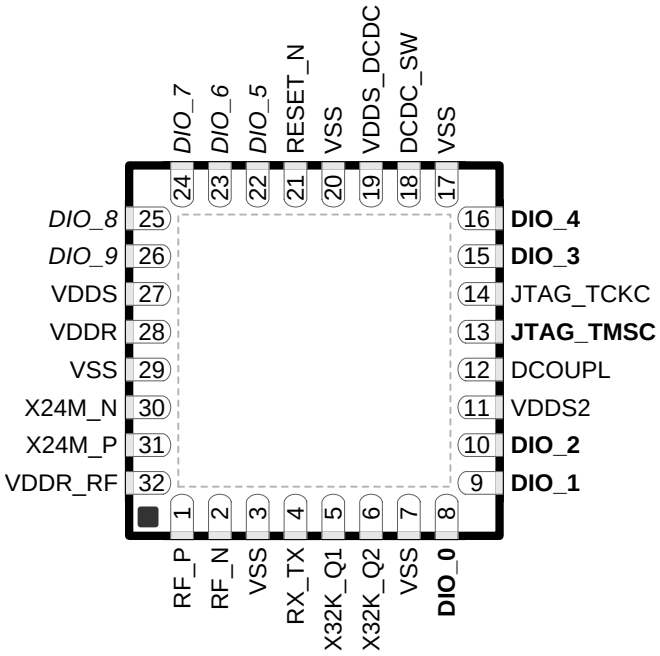


Figure 4-1. RSM (4-mm × 4-mm) Pinout, 0.4-mm Pitch
Top View

I/O pins marked in Figure 4-1 in **bold** have high-drive capabilities; they are as follows:

- Pin 8, DIO_0
- Pin 9, DIO_1
- Pin 10, DIO_2
- Pin 13, JTAG_TMSC
- Pin 15, DIO_3
- Pin 16, DIO_4

I/O pins marked in Figure 4-1 in *italics* have analog capabilities; they are as follows:

- Pin 22, DIO_5
- Pin 23, DIO_6
- Pin 24, DIO_7
- Pin 25, DIO_8
- Pin 26, DIO_9

4.2 Signal Descriptions – RSM Package

Table 4-1. Signal Descriptions – RSM Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	18	Power	Output from internal DC-DC(1)
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling capacitor(2)
DIO_0	8	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_1	9	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_2	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_3	15	Digital I/O	GPIO, high-drive capability, JTAG_TDO
DIO_4	16	Digital I/O	GPIO, high-drive capability, JTAG_TDI
DIO_5	22	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_6	23	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_7	24	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_8	25	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_9	26	Digital or analog I/O	GPIO, Sensor Controller, analog
EGP	–	Power	Ground; exposed ground pad
JTAG_TMSC	13	Digital I/O	JTAG TMSC
JTAG_TCKC	14	Digital I/O	JTAG TCKC
RESET_N	21	Digital input	Reset, active low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RX_TX	4	RF I/O	Optional bias pin for the RF LNA
VDDS	27	Power	1.8-V to 3.8-V main chip supply(1)
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply(1)
VDDS_DCDC	19	Power	1.8-V to 3.8-V DC-DC supply
VDDR	28	Power	1.7-V to 1.95-V supply, connect to output of internal DC-DC(2)(3)
VDDR_RF	32	Power	1.7-V to 1.95-V supply, connect to output of internal DC-DC(2)(4)
VSS	3, 7, 17, 20, 29	Power	Ground
X32K_Q1	5	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	6	Analog I/O	32-kHz crystal oscillator pin 2
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2

(1) See the technical reference manual listed in 节 8.3 for more details.
(2) Do not supply external circuitry from this pin.
(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.3 Pin Diagram – RHB Package

Figure 4-2 shows the RHB pinout diagram.

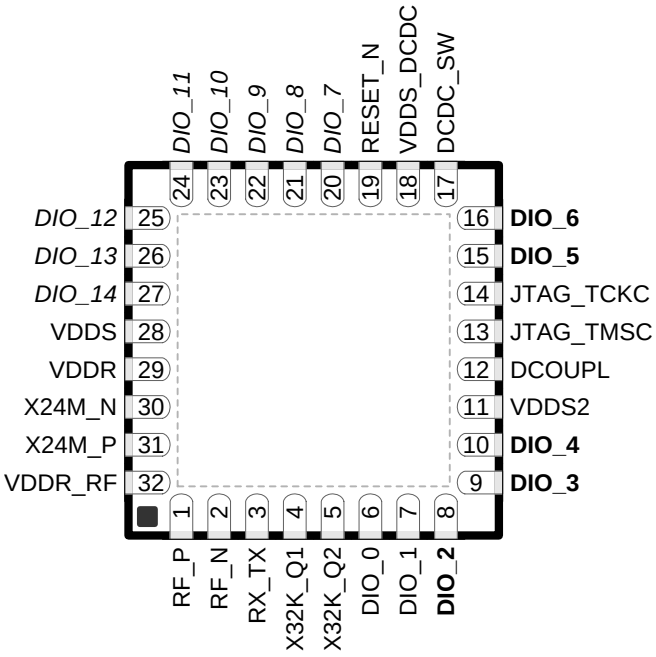


Figure 4-2. RHB (5-mm × 5-mm) Pinout, 0.5-mm Pitch
Top View

I/O pins marked in Figure 4-2 in **bold** have high-drive capabilities; they are as follows:

- Pin 8, DIO_2
- Pin 9, DIO_3
- Pin 10, DIO_4
- Pin 15, DIO_5
- Pin 16, DIO_6

I/O pins marked in Figure 4-2 in *italics* have analog capabilities; they are as follows:

- Pin 20, DIO_7
- Pin 21, DIO_8
- Pin 22, DIO_9
- Pin 23, DIO_10
- Pin 24, DIO_11
- Pin 25, DIO_12
- Pin 26, DIO_13
- Pin 27, DIO_14

4.4 Signal Descriptions – RHB Package

Table 4-2. Signal Descriptions – RHB Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	17	Power	Output from internal DC-DC (1)
DCOUPL	12	Power	1.27-V regulated digital-supply decoupling (2)
DIO_0	6	Digital I/O	GPIO, Sensor Controller
DIO_1	7	Digital I/O	GPIO, Sensor Controller
DIO_2	8	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_3	9	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_4	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_5	15	Digital I/O	GPIO, high-drive capability, JTAG_TDO
DIO_6	16	Digital I/O	GPIO, high-drive capability, JTAG_TDI
DIO_7	20	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_8	21	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_9	22	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_10	23	Digital or analog I/O	GPIO, Sensor Controller, Analog
DIO_11	24	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_12	25	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_13	26	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_14	27	Digital or analog I/O	GPIO, Sensor Controller, analog
EGP	–	Power	Ground; exposed ground pad
JTAG_TMSC	13	Digital I/O	JTAG TMSC, high-drive capability
JTAG_TCKC	14	Digital I/O	JTAG TCKC
RESET_N	19	Digital input	Reset, active low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
VDDR	29	Power	1.7-V to 1.95-V supply, connect to output of internal DC-DC (2) (3)
VDDR_RF	32	Power	1.7-V to 1.95-V supply, connect to output of internal DC-DC (2) (4)
VDDS	28	Power	1.8-V to 3.8-V main chip supply (1)
VDDS2	11	Power	1.8-V to 3.8-V GPIO supply (1)
VDDS_DCDC	18	Power	1.8-V to 3.8-V DC-DC supply
X24M_N	30	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	31	Analog I/O	24-MHz crystal oscillator pin 2
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2

(1) For more details, see the technical reference manual listed in 节 8.3.
(2) Do not supply external circuitry from this pin.
(3) If internal DC-DC is not used, this pin is supplied internally from the main LDO.
(4) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

4.5 Pin Diagram – RGZ Package

Figure 4-3 shows the RGZ pinout diagram.

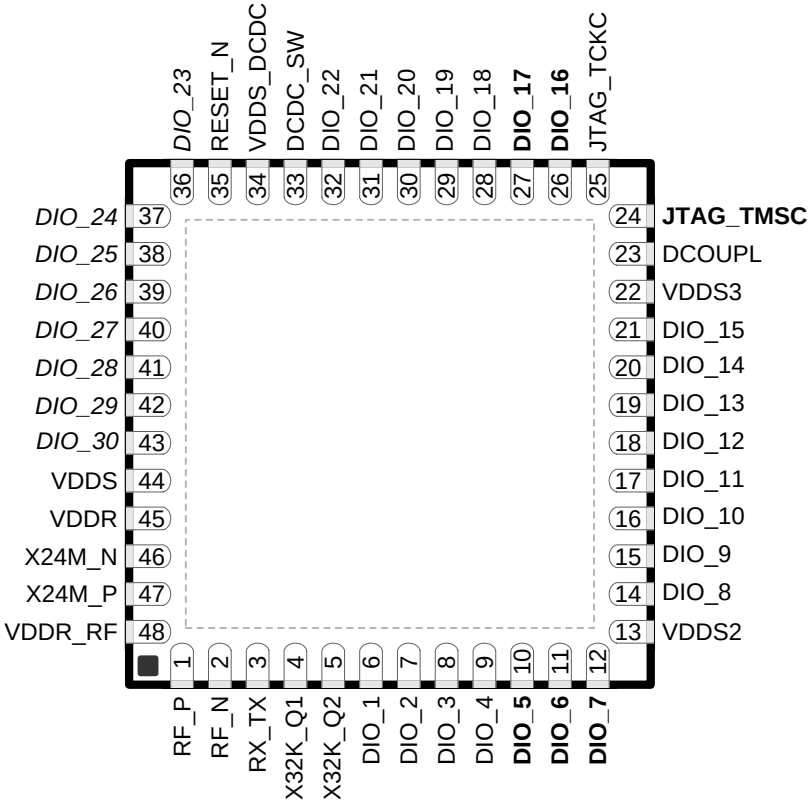


Figure 4-3. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch
Top View

I/O pins marked in Figure 4-3 in **bold** have high-drive capabilities; they are as follows:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

I/O pins marked in Figure 4-3 in *italics* have analog capabilities; they are as follows:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30

4.6 Signal Descriptions – RGZ Package

Table 4-3. Signal Descriptions – RGZ Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
DCDC_SW	33	Power	Output from internal DC-DC (1) (2)
DCOUPL	23	Power	1.27-V regulated digital-supply (decoupling capacitor) (2)
DIO_1	6	Digital I/O	GPIO, Sensor Controller
DIO_2	7	Digital I/O	GPIO, Sensor Controller
DIO_3	8	Digital I/O	GPIO, Sensor Controller
DIO_4	9	Digital I/O	GPIO, Sensor Controller
DIO_5	10	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_6	11	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_7	12	Digital I/O	GPIO, Sensor Controller, high-drive capability
DIO_8	14	Digital I/O	GPIO
DIO_9	15	Digital I/O	GPIO
DIO_10	16	Digital I/O	GPIO
DIO_11	17	Digital I/O	GPIO
DIO_12	18	Digital I/O	GPIO
DIO_13	19	Digital I/O	GPIO
DIO_14	20	Digital I/O	GPIO
DIO_15	21	Digital I/O	GPIO
DIO_16	26	Digital I/O	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	Digital I/O	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	Digital I/O	GPIO
DIO_19	29	Digital I/O	GPIO
DIO_20	30	Digital I/O	GPIO
DIO_21	31	Digital I/O	GPIO
DIO_22	32	Digital I/O	GPIO
DIO_23	36	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_24	37	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_25	38	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_26	39	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_27	40	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_28	41	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_29	42	Digital or analog I/O	GPIO, Sensor Controller, analog
DIO_30	43	Digital or analog I/O	GPIO, Sensor Controller, analog
EGP	–	Power	Ground; exposed ground pad
JTAG_TMSC	24	Digital I/O	JTAG TMSC, high-drive capability
JTAG_TCKC	25	Digital I/O	JTAG TCKC (3)
RESET_N	35	Digital input	Reset, active-low. No internal pullup.
RF_N	2	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
RF_P	1	RF I/O	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
VDDR	45	Power	1.7-V to 1.95-V supply, connect to output of internal DC-DC (2) (4)

(1) See technical reference manual listed in 节 8.3 for more details.
(2) Do not supply external circuitry from this pin.
(3) For design consideration regrading noise immunity for this pin, see the *JTAG Interface* chapter in the *CC13xx, CC26xx SimpleLink™ Wireless MCU Technical Reference Manual*.
(4) If internal DC-DC is not used, this pin is supplied internally from the main LDO.

Table 4-3. Signal Descriptions – RGZ Package (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
VDDR_RF	48	Power	1.7-V to 1.95-V supply, connect to output of internal DC-DC (2) (5)
VDDS	44	Power	1.8-V to 3.8-V main chip supply (1)
VDDS2	13	Power	1.8-V to 3.8-V DIO supply (1)
VDDS3	22	Power	1.8-V to 3.8-V DIO supply (1)
VDDS_DCDC	34	Power	1.8-V to 3.8-V DC-DC supply
X24M_N	46	Analog I/O	24-MHz crystal oscillator pin 1
X24M_P	47	Analog I/O	24-MHz crystal oscillator pin 2
RX_TX	3	RF I/O	Optional bias pin for the RF LNA
X32K_Q1	4	Analog I/O	32-kHz crystal oscillator pin 1
X32K_Q2	5	Analog I/O	32-kHz crystal oscillator pin 2

(5) If internal DC-DC is not used, this pin must be connected to VDDR for supply from the main LDO.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
VDDS, VDDS2, and VDDS3	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin(3)		–0.3	VDDSn + 0.3, max 4.1	V
	Voltage on crystal oscillator pins X32K_Q1, X32K_Q2, X24M_N, and X24M_P		–0.3	VDDR + 0.3, max 2.25	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDDS	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
	Input RF level			10	dBm
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Each pin is referenced to a specific VDDSn (VDDS, VDDS2 or VDDS3). For a pin-to-VDDS mapping table, see Table 6-3.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	All pins	±3000	V
		Charged device model (CDM), per JESD22-C101(2)	All pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Ambient temperature		–40	85	°C
Operating supply voltage (VDDS)	For operation in battery-powered and 3.3-V systems (internal DC-DC can be used to minimize power consumption)	1.8	3.8	V
Rising supply voltage slew rate		0	100	mV/µs
Falling supply voltage slew rate		0	20	mV/µs
Falling supply voltage slew rate, with low-power flash setting(1)			3	mV/µs
Positive temperature gradient in standby(2)	No limitation for negative temperature gradient, or outside standby mode		5	°C/s

(1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-µF VDDS input capacitor must be used to ensure compliance with this slew rate.
(2) Applications using RCOSC_LF as sleep timer must also consider the drift in frequency caused by a change in temperature (see Section 5.19.3.4).

5.4 Power Consumption Summary

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design unless otherwise noted. T_c = 25°C, V_{DDS} = 3.6 V with DC-DC enabled, unless otherwise noted. Using boost mode (increasing VDDR to 1.95 V), will increase currents in this table by 15% (does not apply to TX 14-dBm setting where this current is already included).

PARAMETER		TEST CONDITIONS	TYP	UNIT
I_{core}	Core current consumption	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	100	nA
		Shutdown. No clocks running, no retention	185	
		Standby. With RTC, CPU, RAM, and (partial) register retention. RCOSC_LF	0.7	µA
		Standby. With RTC, CPU, RAM, and (partial) register retention. XOSC_LF	0.8	
		Idle. Supply Systems and RAM powered.	570	
		Active. MCU running CoreMark at 48 MHz	1.2 mA + 25.5 µA/MHz	
		Active. MCU running CoreMark at 48 MHz	2.5	mA
		Active. MCU running CoreMark at 24 MHz	1.9	
		Radio RX	5.5	mA
		Radio TX, 10-dBm output power, (G)FSK, 868 MHz	13.4	mA
		Radio TX, OOK modulation, 10-dBm output power, AVG	11.2	mA
		Radio TX, boost mode (VDDR = 1.95 V), 14-dBm output power, (G)FSK, 868 MHz	23.5	mA
		Radio TX, OOK modulation, boost mode (VDDR = 1.95 V), 14-dBm, AVG	14.8	mA
		Radio TX, boost mode (VDDR = 1.95 V), 15-dBm output power, (G)FSK, measured on CC1310EM-7XD-4251, 433.92 MHz	25.1	mA
		Radio TX, 10-dBm output power, measured on CC1310EM-7XD-4251, 433.92 MHz	13.2	mA
PERIPHERAL CURRENT CONSUMPTION (1)(2)(3)				
I_{peri}	Peripheral power domain	Delta current with domain enabled	20	µA
	Serial power domain	Delta current with domain enabled	13	
	RF core	Delta current with power domain enabled, clock enabled, RF core idle	237	
	µDMA	Delta current with clock enabled, module idle	130	
	Timers	Delta current with clock enabled, module idle	113	
	I^2C	Delta current with clock enabled, module idle	12	
	I2S	Delta current with clock enabled, module idle	36	
	SSI	Delta current with clock enabled, module idle	93	
	UART	Delta current with clock enabled, module idle	164	

(1) Adds to core current I_{core} for each peripheral unit activated
(2) I_{peri} is not supported in standby or shutdown modes.
(3) Measured at 3.0 V

5.5 RF Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands (1)	(287)		(351)	MHz
	(359)		(439)	
	431		527	
	(718)		(878)	
	861		1054	

(1) For more information, see the *CC1310 SimpleLink Wireless MCU Silicon Errata*.

5.6 Receive (RX) Parameters, 861 MHz to 1054 MHz

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data rate			50		kbps
Data rate offset tolerance, IEEE 802.15.4g PHY	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-3}		1600		ppm
Data rate step size			1.5		bps
Digital channel filter programmable bandwidth	Using VCO divide by 5 setting	40		4000	kHz
Receiver sensitivity, 50 kbps	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2} 868 MHz and 915 MHz. Measured on CC1310EM-7XD-7793.		–110		dBm
Receiver saturation	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		10		dBm
Selectivity, ±200 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		43, 45		dB
Selectivity, ±400 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		48, 53		dB
Blocking ±1 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		59, 62		dB
Blocking ±2 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		64, 65		dB
Blocking ±5 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		67, 68		dB
Blocking ±10 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		76, 76		dB
Spurious emissions 1 GHz to 13 GHz (VCO leakage at 3.5 GHz) and 30 MHz to 1 GHz	Radiated emissions measured according to ETSI EN 300 220		–70		dBm
Image rejection (image compensation enabled, the image compensation is calibrated in production)	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		44		dB
RSSI dynamic range	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode). Starting from the sensitivity limit. This range will give an accuracy of ±2 dB.		95		dB
RSSI accuracy	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode). Starting from the sensitivity limit across the given dynamic range.		±2		dB
Receiver sensitivity, long-range mode 625 bps	10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHz.		–124		dBm

Receive (RX) Parameters, 861 MHz to 1054 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, ±100 kHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		52, 52		dB
Selectivity, ±200 kHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		61, 61		dB
Blocking ±1 MHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		73, 77		dB
Blocking ±2 MHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		79, 79		dB
Blocking ±10 MHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		91, 91		dB
Receiver sensitivity, OOK 4.8 kbps	4.8 kbps, OOK, 40-kHz RX bandwidth, BER = 10^{-2} 868 MHz and 915 MHz. Measured on CC1310EM-7XD-7793.		–115		dBm

5.7 Receive (RX) Parameters, 431 MHz to 527 MHz

Measured on the Texas Instruments CC1310EM-7XD-4251 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 433.92 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. This frequency band is supported on die Revision B and later.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity, 50 kbps	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		–110		dBm
Receiver saturation	50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		10		dBm
Selectivity, ±200 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		40, 42		dB
Selectivity, ±400 kHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		42, 50		dB
Blocking ±1 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		53, 58		dB
Blocking ±2 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		59, 60		dB
Blocking ±10 MHz, 50 kbps	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		74, 74		dB
Spurious emissions 1 GHz to 13 GHz (VCO leakage at 3.5 GHz) and 30 MHz to 1 GHz	Radiated emissions measured according to ETSI EN 300 220		–74		dBm

Receive (RX) Parameters, 431 MHz to 527 MHz *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-4251 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 433.92 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. This frequency band is supported on die Revision B and later.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Image rejection (image compensation enabled, the image compensation is calibrated in production)	Wanted signal 3 dB above sensitivity limit. 50 kbps, GFSK, 25-kHz deviation, 100-kHz RX bandwidth (same modulation format as IEEE 802.15.4g mandatory mode), BER = 10^{-2}		43		dB
Receiver sensitivity, long-range mode 625 bps	10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}. 868 MHz and 915 MHZ.		–124		dBm
Selectivity, ±100 kHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		57, 58		dB
Selectivity, ±200 kHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		56, 60		dB
Blocking ±1 MHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		68, 73		dB
Blocking ±2 MHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		74, 74		dB
Blocking ±10 MHz, long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		88, 89		dB
Image rejection (image compensation enabled, the image compensation is calibrated in production), long-range mode 625 bps	Wanted signal 3 dB above sensitivity limit. 10 ksym/s, GFSK, 5-kHz deviation, FEC (half rate), DSSS = 8, 40-kHz RX bandwidth, BER = 10^{-2}		55		dB

5.8 Transmit (TX) Parameters, 861 MHz to 1054 MHz

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 868 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output power, boost mode		VDDR = 1.95 V Minimum VDDS for boost mode is 2.1 V 868 MHz and 915 MHz		14		dBm
Maximum output power		868 MHz and 915 MHz		12		dBm
Output power programmable range				24		dB
Output power variation		Tested at +10-dBm setting		±0.9		dB
Output power variation, boost mode		+14 dBm		±0.5		dB
Spurious emissions (excluding harmonics)(1)	30 MHz to 1 GHz	Transmitting +14 dBm ETSI restricted bands		<–59		dBm
		Transmitting +14 dBm outside ETSI restricted bands		<–51		
	1 GHz to 12.75 GHz	Transmitting +14 dBm measured in 1-MHz bandwidth (ETSI)		<–37		
Harmonics	Second harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–52, –55		dBm
	Third harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–58, –55		
	Fourth harmonic	Transmitting +14 dBm, conducted 868 MHz, 915 MHz		–56, –56		
Spurious emissions out-of-band, 915 MHz(1)	30 MHz to 88 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–66		dBm
	88 MHz to 216 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–65		
	216 MHz to 960 MHz (within FCC restricted bands)	Transmitting +14 dBm, conducted		<–65		
	960 MHz to 2390 MHz and above 2483.5 MHz (within FCC restricted band)	Transmitting +14 dBm, conducted		<–52		
	1 GHz to 12.75 GHz (outside FCC restricted bands)	Transmitting +14 dBm, conducted		<–43		
Spurious emissions out-of-band, 920.6 MHz(1)	Below 710 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–50		dBm
	710 MHz to 900 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–60		
	900 MHz to 915 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–57		
	930 MHz to 1000 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–57		
	1000 MHz to 1215 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–59		
	Above 1215 MHz (ARIB T-108)	Transmitting +14 dBm, conducted		<–45		

(1) Suitable for systems targeting compliance with EN 300 220, EN 54-25, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

5.9 Transmit (TX) Parameters, 431 MHz to 527 MHz

Measured on the Texas Instruments CC1310EM-7XD-4251 reference design with T_c = 25°C, V_{DDS} = 3.0 V, DC-DC enabled, f_{RF} = 433.92 MHz, unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. This frequency band is supported on die Revision B and later.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum output power, boost mode		VDDR = 1.95 V Minimum VDDS for boost mode is 2.1 V		15		dBm
Maximum output power				14		dBm
Spurious emissions (excluding harmonics)(1)	30 MHz to 1 GHz	Transmitting +10 dBm, 433 MHz Inside ETSI restricted bands		<–63		dBm
		Transmitting +10 dBm, 433 MHz Outside ETSI restricted bands		<–39		
	1 GHz to 12.75 GHz	Transmitting +10 dBm, 433 MHz Outside ETSI restricted bands, measured in 1-MHz bandwidth (ETSI)		<–52		
		Transmitting +10 dBm, 433 MHz Inside ETSI restricted bands, measured in 1-MHz bandwidth (ETSI)		<–58		

(1) Suitable for systems targeting compliance with EN 300 220, EN 54-25, EN 303 204, FCC CFR47 Part 15, ARIB STD-T108.

5.10 PLL Parameters

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise in the 868-MHz band	±100-kHz offset		–101		dBc/Hz
	±200-kHz offset		–108		
	±400-kHz offset		–115		
	±1000-kHz offset		–124		
	±2000-kHz offset		–131		
	±10000-kHz offset		–140		
Phase noise in the 915-MHz band	±100-kHz offset		–98		dBc/Hz
	±200-kHz offset		–106		
	±400-kHz offset		–114		
	±1000-kHz offset		–122		
	±2000-kHz offset		–130		
	±10000-kHz offset		–140		

5.11 ADC Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, DC-DC disabled. Input voltage scaling enabled, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		V_{DDS}	V
	Resolution			12		Bits
	Sample rate				200	ksamples/s
	Offset	Internal 4.3-V equivalent reference(2)		2.1		LSB
	Gain error	Internal 4.3-V equivalent reference(2)		–0.14		LSB
DNL(3)	Differential nonlinearity			>–1		LSB
INL(4)	Integral nonlinearity			±2		LSB

(1) Using IEEE Std 1241™ 2010 for terminology and test methods.
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V. Applied voltage must be within the absolute maximum ratings (see Section 5.1) at all times.
(3) No missing codes. Positive DNL typically varies from 0.3 to 1.7, depending on the device (see Figure 5-7).
(4) For a typical example, see Figure 5-6.

ADC Characteristics *(continued)*

T_c = 25°C, V_{DDS} = 3.0 V, DC-DC disabled. Input voltage scaling enabled, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		10.0		Bits
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		10.2		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		11.1		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		–65		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		–72		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		–75		
SINAD and SNDR	Signal-to-noise and distortion ratio	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		62		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		63		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		69		
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference(2), 200 ksamples/s, 9.6-kHz input tone		74		dB
		VDDS as reference, 200 ksamples/s, 9.6-kHz input tone		75		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 ksamples/s, 300-Hz input tone		75		
	Conversion time	Including sampling time		5		µs
	Current consumption	Internal 4.3-V equivalent reference(2)		0.66		mA
	Current consumption	VDDS as reference		0.75		mA
	Reference voltage	Equivalent fixed internal reference(voltage scaling enabled) (2) For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1.		4.3		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). (2) For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V
	Reference voltage	VDDS as reference (Also known as RELATIVE) (input voltage scaling enabled)		VDDS		V
	Reference voltage	VDDS as reference (Also known as RELATIVE) (input voltage scaling disabled)		VDDS / 2.82		V
	Input Impedance	200 ksamples/s, voltage scaling enabled. Capacitive input, input impedance depends on sampling frequency and sampling time		>1		MΩ

5.12 Temperature Sensor

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			4		°C
Range		–40		85	°C
Accuracy			±5		°C
Supply voltage coefficient(1)			3.2		°C/V

(1) Automatically compensated when using supplied driver libraries.

5.13 Battery Monitor

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			50		mV

Battery Monitor *(continued)*

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Range		1.8		3.8	V
Accuracy			13		mV

5.14 Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
External reference voltage		0		V_{DDS}	V
Internal reference voltage	DCOUPL as reference		1.27		V
Offset			3		mV
Hysteresis			<2		mV
Decision time	Step from –10 mV to 10 mV		0.72		µs
Current consumption when enabled(1)			8.6		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.15 Low-Power Clocked Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DDS}	V
Clock frequency			32.8		kHz
Internal reference voltage, VDDS / 2			1.49 to 1.51		V
Internal reference voltage, VDDS / 3			1.01 to 1.03		V
Internal reference voltage, VDDS / 4			0.78 to 0.79		V
Internal reference voltage, DCOUPL / 1			1.25 to 1.28		V
Internal reference voltage, DCOUPL / 2			0.63 to 0.65		V
Internal reference voltage, DCOUPL / 3			0.42 to 0.44		V
Internal reference voltage, DCOUPL / 4			0.33 to 0.34		V
Offset			<2		mV
Hysteresis			<5		mV
Decision time	Step from –50 mV to 50 mV		1		clock-cycle
Current consumption when enabled			362		nA

5.16 Programmable Current Source

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range			0.25 to 20		µA
Resolution			0.25		µA
Current consumption(1)	Including current source at maximum programmable output		23		µA

(1) Additionally, the bias module must be enabled when running in standby mode.

5.17 DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 1.8 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only	1.32	1.54		V

DC Characteristics *(continued)*

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.26	0.32	V
GPIO VOH at 4-mA load	IOCURR = 1	1.32	1.58		V
GPIO VOL at 4-mA load	IOCURR = 1		0.21	0.32	V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		71.7		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		21.1		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		0.88		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.07		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.74		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 voltage transition points		0.33		V
T_A = 25°C, V_{DDS} = 3.0 V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.68		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.33		V
GPIO VOH at 4-mA load	IOCURR = 1		2.72		V
GPIO VOL at 4-mA load	IOCURR = 1		0.28		V

DC Characteristics *(continued)*

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		277		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		113		µA
GPIO high/low input transition, no hysteresis	IH = 0, transition between reading 0 and reading 1		1.67		V
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.94		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.54		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 voltage transition points		0.4		V
VIH	Lowest GPIO input voltage reliably interpreted as a *High*			0.8	VDDS(1)
VIL	Highest GPIO input voltage reliably interpreted as a *Low*	0.2			VDDS(1)

(1) Each GPIO is referenced to a specific VDDS pin. See the technical reference manual listed in 节 8.3 for more details.

5.18 Thermal Characteristics

THERMAL METRIC(1)		CC1310			UNIT(2)
		RSM (VQFN)	RHB (VQFN)	RGZ (VQFN)	
		32 PINS	32 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.9	32.8	29.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.3	24.0	15.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	6.8	6.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.3	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	6.8	6.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	1.9	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.

5.19 Timing and Switching Characteristics

5.19.1 Reset Timing

	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

5.19.2 Switching Characteristics: Wakeup and Timing

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted. The times listed here do not include RTOS overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Idle → Active			14		µs
MCU, Standby → Active			174		µs
MCU, Shutdown → Active			1097		µs

5.19.3 Clock Specifications

5.19.3.1 24-MHz Crystal Oscillator (XOSC_HF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	MIN	TYP	MAX	UNIT
Crystal frequency		24		MHz
ESR equivalent series resistance		20	60	Ω
L_M motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)		$< 1.6 \times 10^{-24} / C_L^2$		H
C_L crystal load capacitance	5		9	pF
Start-up time(2)		150		µs

(1) Probing or otherwise stopping the crystal while the DC-DC converter is enabled may cause permanent damage to the device.
(2) The crystal start-up time is low because it is *kick-started* by using the RCOSC_HF oscillator (temperature and aging compensated) that is running at the same frequency.

5.19.3.2 32.768-kHz Crystal Oscillator (XOSC_LF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.(1)

	MIN	TYP	MAX	UNIT
Crystal frequency		32.768		kHz
ESR equivalent series resistance		30	100	kΩ
Crystal load capacitance (C_L)	6		12	pF

(1) Probing or otherwise stopping the crystal while the DC-DC converter is enabled may cause permanent damage to the device.

5.19.3.3 48-MHz RC Oscillator (RCOSC_HF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1%		
Calibrated frequency accuracy(1)		±0.25%		
Startup time		5		µs

(1) Accuracy relative to the calibration source (XOSC_HF)

5.19.3.4 32-kHz RC Oscillator (RCOSC_LF)

Measured on the Texas Instruments CC1310EM-7XD-7793 reference design with T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency(1)		32.768		kHz
Temperature coefficient		50		ppm/°C

(1) The frequency accuracy of the Real Time Clock (RTC) is not directly dependent on the frequency accuracy of the 32-kHz RC Oscillator. The RTC can be calibrated to an accuracy within ±500 ppm of 32.768 kHz by measuring the frequency error of RCOSC_LF relative to XOSC_HF and compensating the RTC tick speed.

5.19.4 Flash Memory Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported flash erase cycles before failure		100			k Cycles
Flash page or sector erase current	Average delta current		12.6		mA
Flash page or sector erase time(1)			8		ms
Flash page or sector size			4		KB
Flash write current	Average delta current, 4 bytes at a time		8.15		mA
Flash write time(1)	4 bytes at a time		8		µs

(1) This number is dependent on flash aging and increases over time and erase cycles.

5.19.5 Synchronous Serial Interface (SSI) Characteristics

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	system clocks
S2(1)	t_{clk_high}	SSIClk high time		0.5 × t_{clk_per}		
S3(1)	t_{clk_low}	SSIClk low time		0.5 × t_{clk_per}		

(1) See the SSI timing diagrams, Figure 5-1, Figure 5-2, and Figure 5-3.

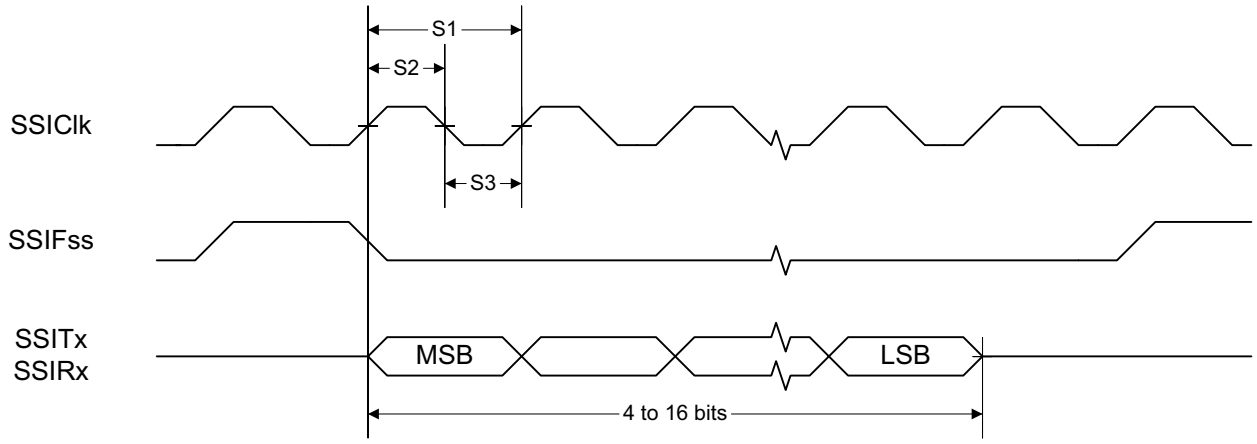


Figure 5-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

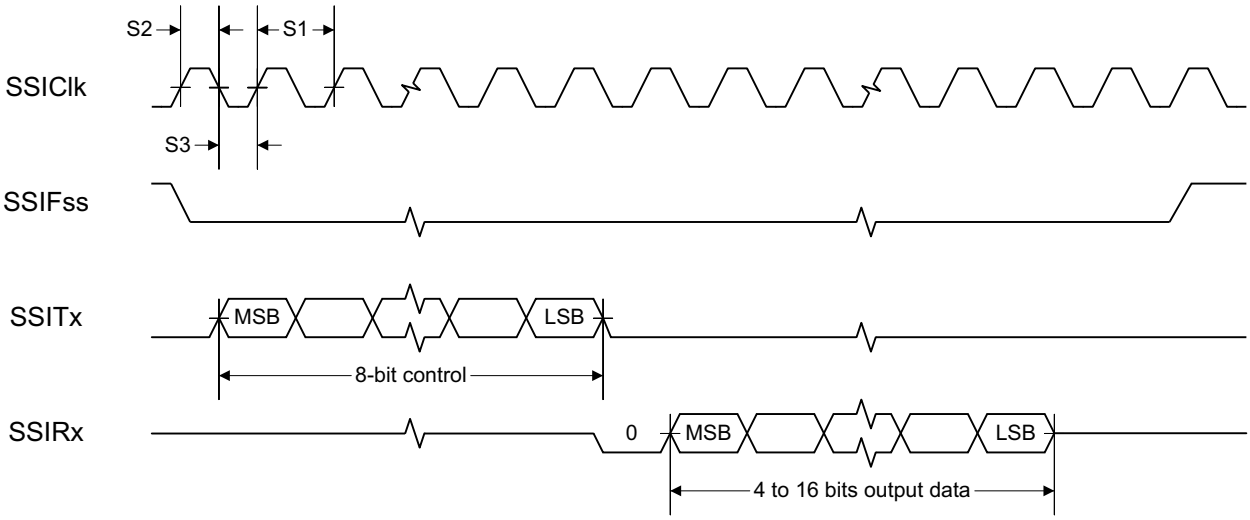


Figure 5-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

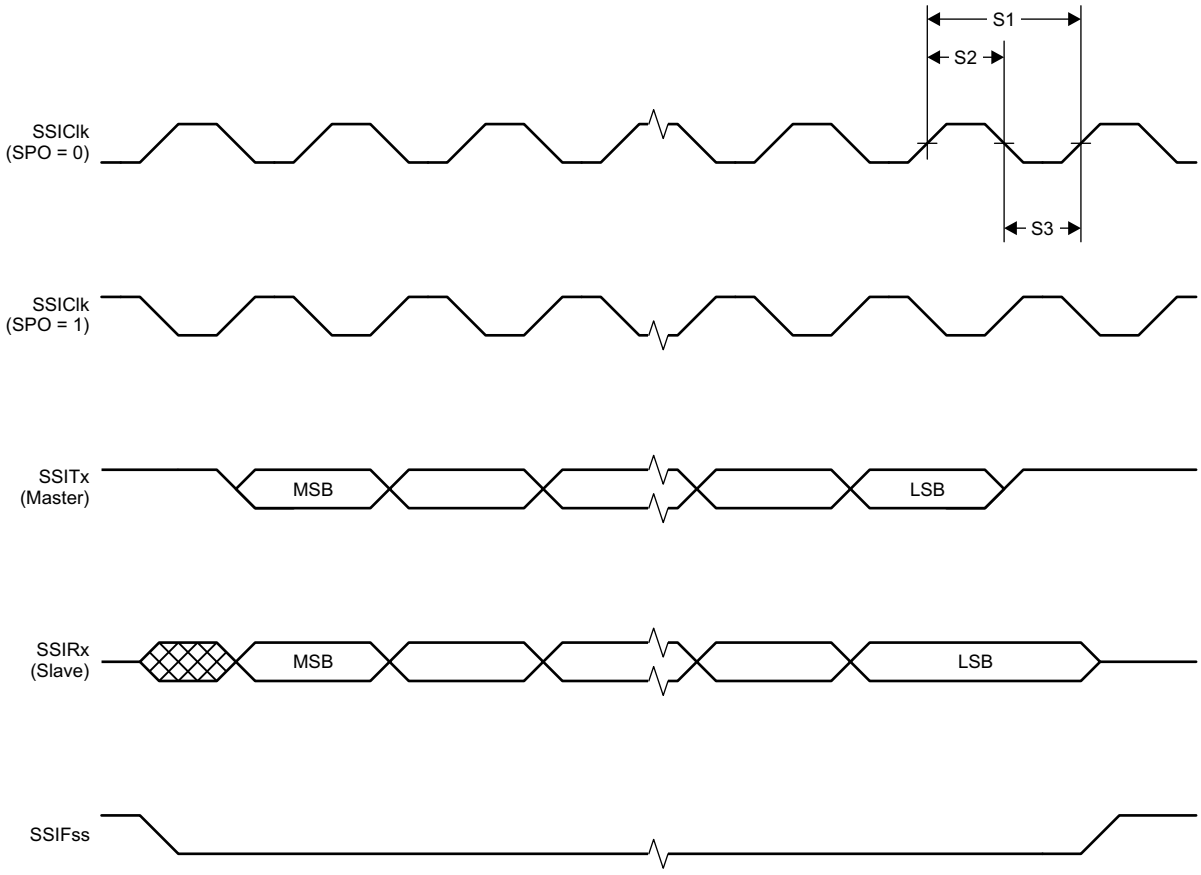


Figure 5-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.20 Typical Characteristics

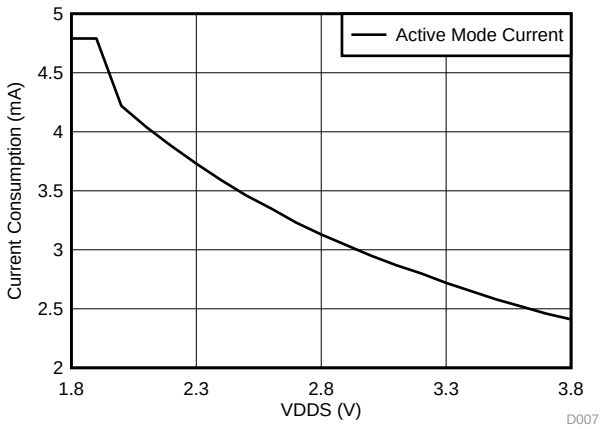


Figure 5-4. Active Mode (MCU) Current Consumption vs Supply Voltage (VDDS)

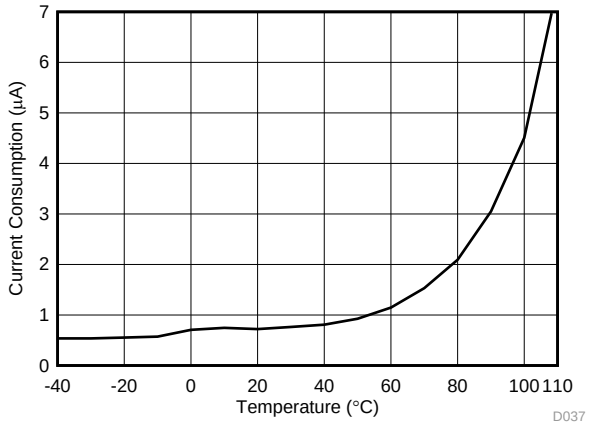


Figure 5-5. Standby MCU Current Consumption, 32-kHz Clock, RAM and MCU Retention

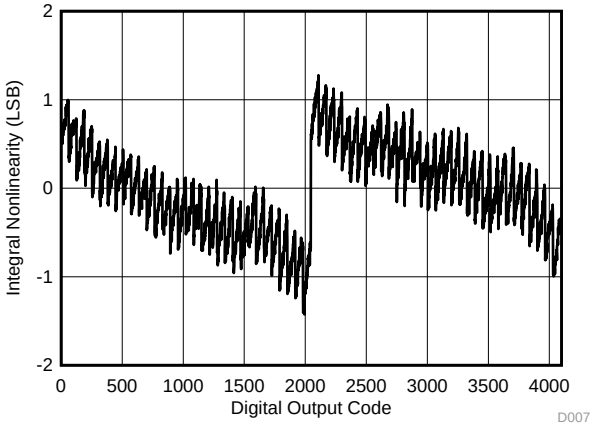


Figure 5-6. SoC ADC, Integral Nonlinearity vs Digital Output Code

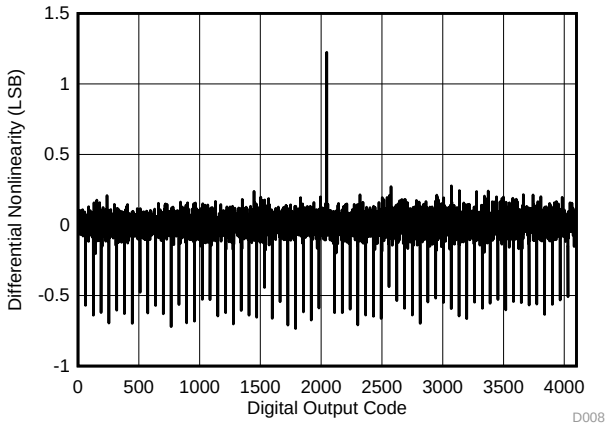


Figure 5-7. SoC ADC, Differential Nonlinearity vs Digital Output Code

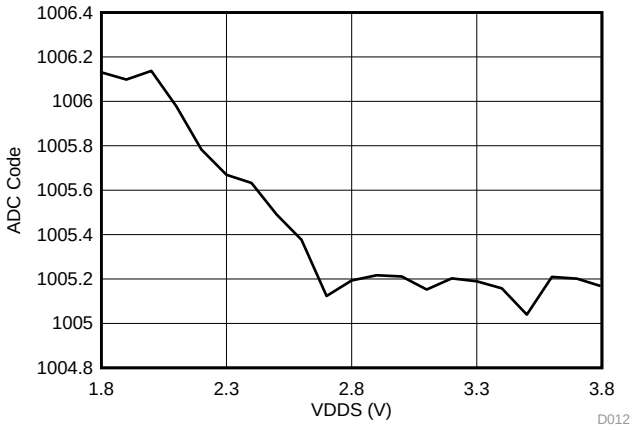


Figure 5-8. SoC ADC Output vs Supply Voltage (Fixed Input, Internal Reference, No Scaling)

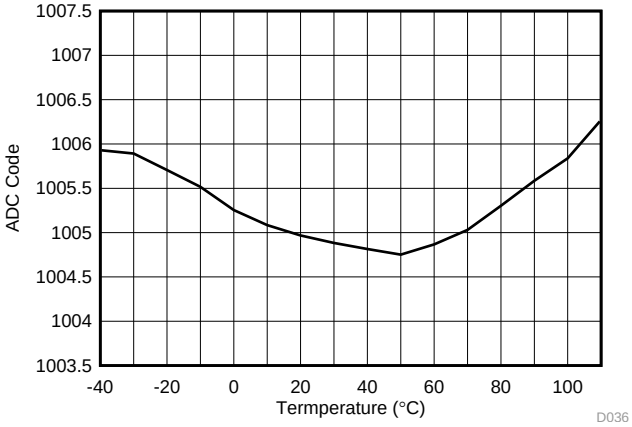


Figure 5-9. SoC ADC Output vs Temperature (Fixed Input, Internal Reference, No Scaling)

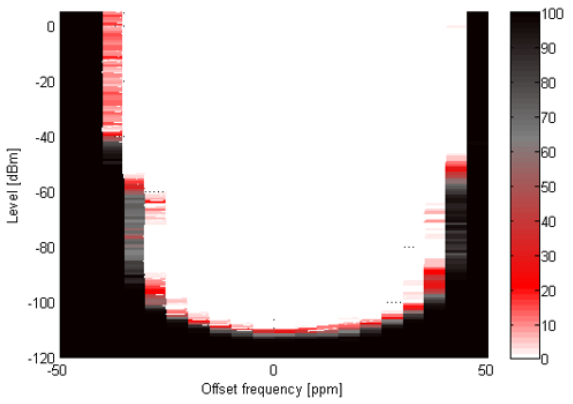


Figure 5-10. RX, (50-kbps) Packet Error Rate (PER) vs Input RF Level vs Frequency Offset, 868 MHz

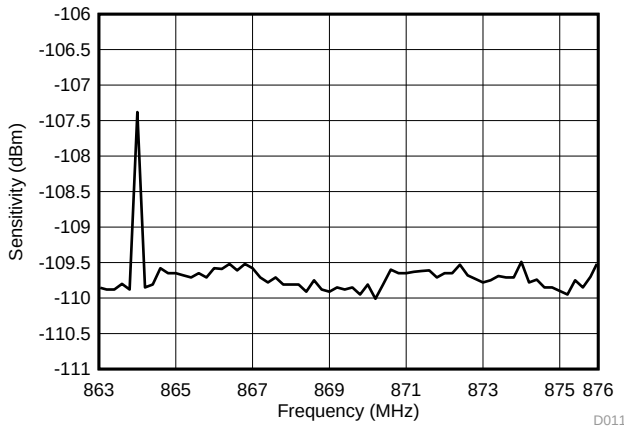


Figure 5-11. RX (50-kbps) Sensitivity vs Frequency

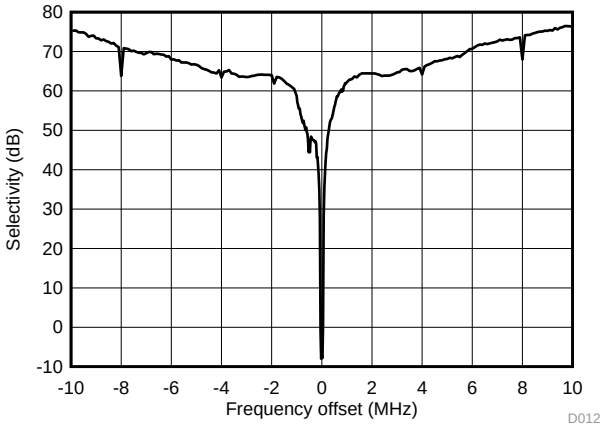


Figure 5-12. RX (50-kbps) Selectivity 868 MHz

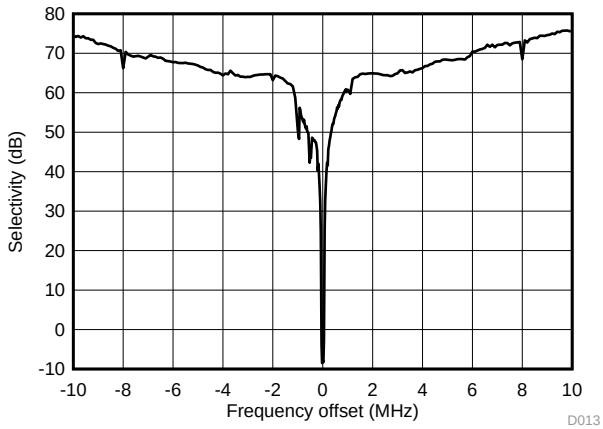


Figure 5-13. RX (50-kbps) Selectivity 915 MHz

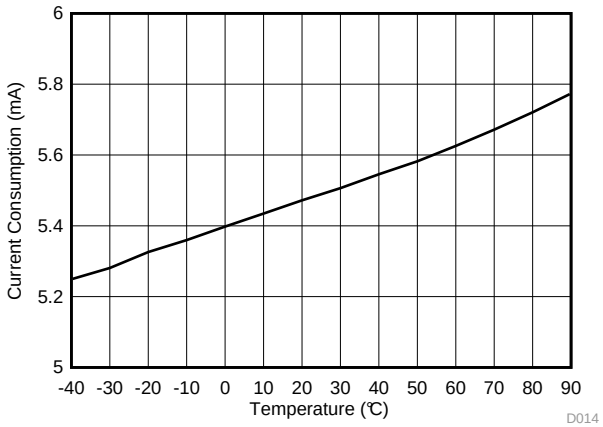


Figure 5-14. RX (50-kbps) Current Consumption vs Temperature 868 MHz

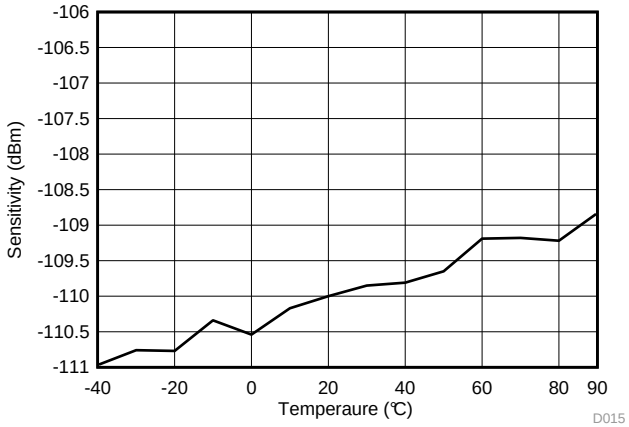


Figure 5-15. RX (50-kbps) Sensitivity vs Temperature 868 MHz

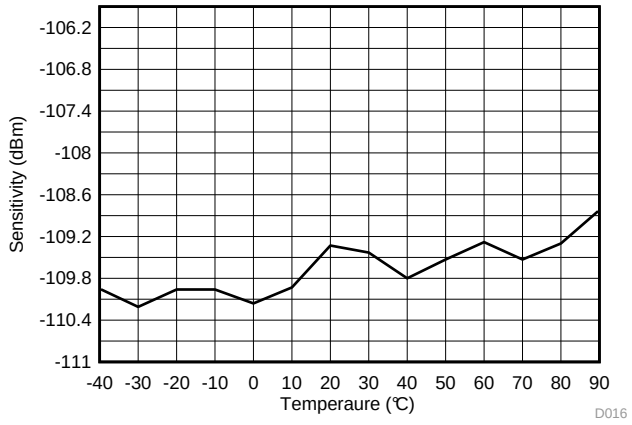


Figure 5-16. RX (50-kbps) Sensitivity vs Temperature 915 MHz

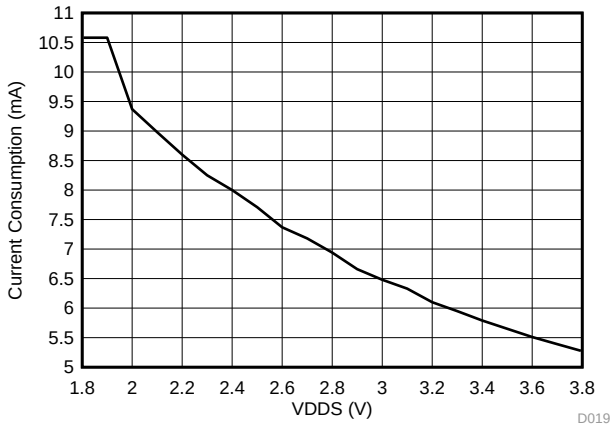


Figure 5-17. RX (50-kbps) Current Consumption vs Supply Voltage 915 MHz

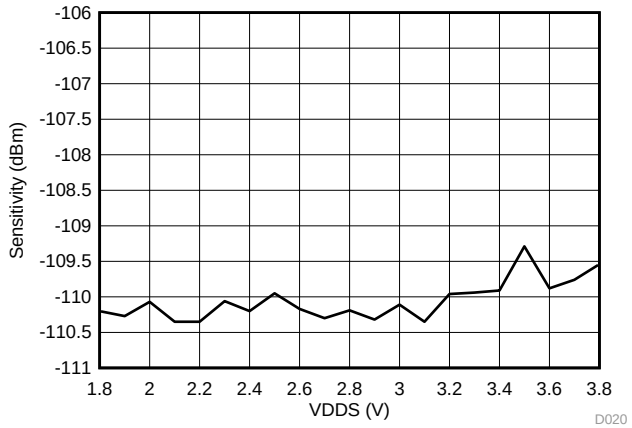
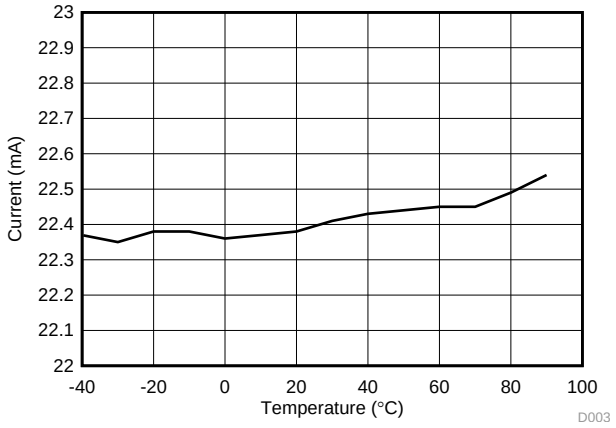


Figure 5-18. RX (50-kbps) Sensitivity vs Supply Voltage 868 MHz



DCDC On, 3.6 V

Figure 5-19. TX Current Consumption With Maximum Output Power vs Temperature 868 MHz

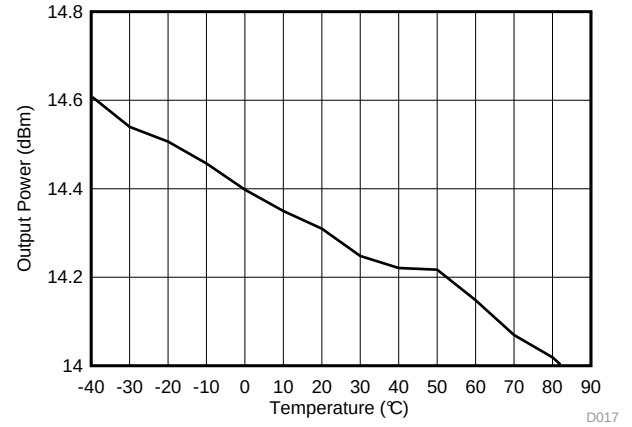


Figure 5-20. TX Maximum Output vs Temperature 868 MHz

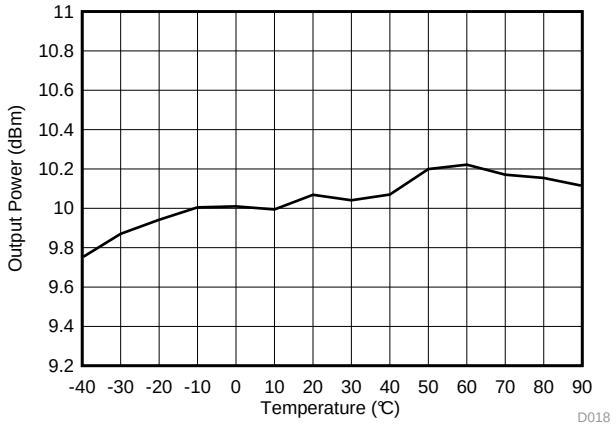


Figure 5-21. TX 10-dBm Output Power vs Temperature 868 MHz

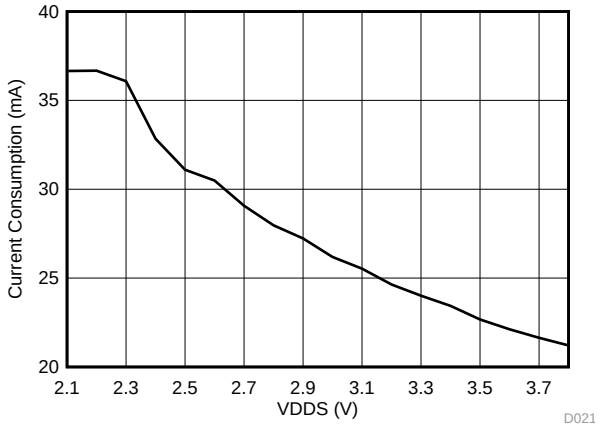


Figure 5-22. TX Current Consumption Maximum Output Power vs Supply Voltage 868 MHz

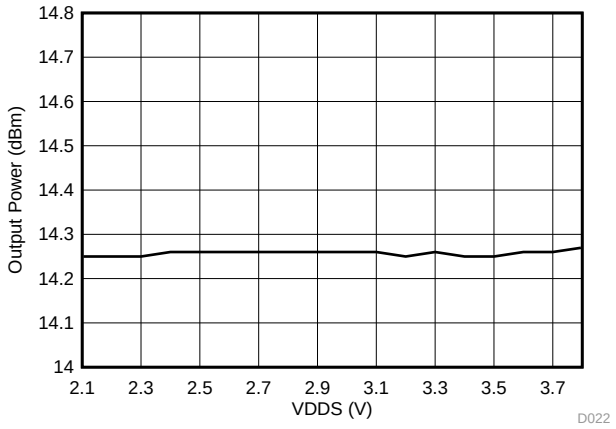


Figure 5-23. TX Maximum Output Power vs Supply Voltage 915 MHz

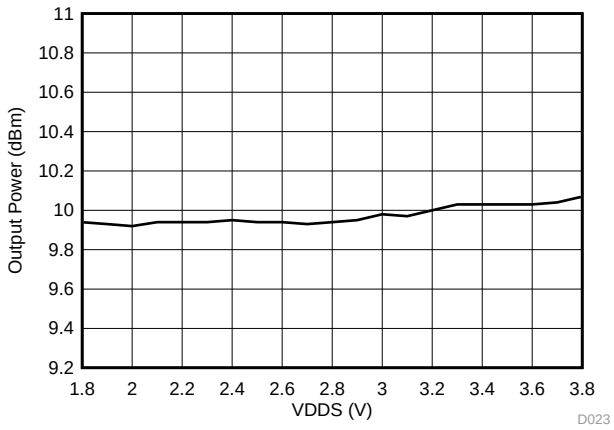


Figure 5-24. TX 10-dBm Output Power vs Supply Voltage 868 MHz

6 Detailed Description

6.1 Overview

节 1.4 shows a block diagram of the core modules of the CC13xx product family.

6.2 Main CPU

The CC1310 SimpleLink Wireless MCU contains an ARM Cortex-M3 (CM3) 32-bit CPU, which runs the application and the higher layers of the protocol stack.

The CM3 processor provides a high-performance, low-cost platform that meets the system requirements of minimal memory implementation and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

The CM3 features include the following:

- 32-bit ARM Cortex-M3 architecture optimized for small-footprint embedded applications
- Outstanding processing performance combined with fast interrupt handling
- ARM Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit ARM core in a compact memory size usually associated with 8- and 16-bit devices, typically in the range of a few kilobytes of memory for microcontroller-class applications:
  - Single-cycle multiply instruction and hardware divide
  - Atomic bit manipulation (bit-banding), delivering maximum memory use and streamlined peripheral control
  - Unaligned data access, enabling data to be efficiently packed into memory
- Fast code execution permits slower processor clock or increases sleep mode time
- Harvard architecture characterized by separate buses for instruction and data
- Efficient processor core, system, and memories
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Deterministic, high-performance interrupt handling for time-critical applications
- Enhanced system debug with extensive breakpoint and trace capabilities
- Serial wire trace reduces the number of pins required for debugging and tracing
- Migration from the ARM7™ processor family for better performance and power efficiency
- Optimized for single-cycle flash memory use
- Ultra-low power consumption with integrated sleep modes
- 1.25 DMIPS per MHz

6.3 RF Core

The RF core is a highly flexible and capable radio system that interfaces the analog RF and baseband circuits, handles data to and from the system side, and assembles the information bits in a given packet structure.

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU and leaving more resources for the user application. The RF core offers a high-level, command-based API to the main CPU.

The RF core supports a wide range of modulation formats, frequency bands, and accelerator features, which include the following (not all of the features have been characterized yet, see the *CC1310 SimpleLink Wireless MCU Silicon Errata* for more information):

- Wide range of data rates:
  - From 625 bps (offering long range and high robustness) to as high as 4 Mbps
- Wide range of modulation formats:
  - Multilevel (G) FSK and MSK
  - On-Off Keying (OOK) with optimized shaping to minimize adjacent channel leakage
  - Coding-gain support for long range
- Dedicated packet handling accelerators:
  - Forward error correction
  - Data whitening
  - 802.15.4g mode-switch support
  - Automatic CRC
- Automatic listen-before-talk (LBT) and clear channel assist (CCA)
- Digital RSSI
- Highly configurable channel filtering, supporting channel spacing schemes from 40 kHz to 4 MHz
- High degree of flexibility, offering a future-proof solution

The RF core interfaces a highly flexible radio, with a high-performance synthesizer that can support a wide range of frequency bands.

6.4 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in standby mode. The peripherals in this domain may be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the main CM3 CPU.

A PC-based development tool called *Sensor Controller Studio* is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Analog sensors using integrated ADC
- Digital sensors using GPIOs with bit-banged I^2C or SPI
- Capacitive sensing
- Waveform generation
- Pulse counting
- Key scan
- Quadrature decoder for polling rotational sensors

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active. A configurable internal reference can be used with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions.
- The ADC is a 12-bit, 200-ksamples/s ADC with 8 inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The analog modules can be connected to up to eight different GPIOs (see Table 6-1).

The peripherals in the Sensor Controller can also be controlled from the main application processor.

Table 6-1. GPIOs Connected to the Sensor Controller(1)

ANALOG CAPABLE	CC13x0		
	7 × 7 RGZ DIO NUMBER	5 × 5 RHB DIO NUMBER	4 × 4 RSM DIO NUMBER
Y	30	14	
Y	29	13	
Y	28	12	
Y	27	11	9
Y	26	9	8
Y	25	10	7
Y	24	8	6
Y	23	7	5
N	7	4	2
N	6	3	1
N	5	2	0
N	4	1	
N	3	0	
N	2		
N	1		
N	0		

(1) Depending on the package size, up to 15 pins can be connected to the Sensor Controller. Up to eight of these pins can be connected to analog modules.

6.5 Memory

The flash memory provides nonvolatile storage for code and data. The flash memory is in-system programmable.

The SRAM (static RAM) is split into two 4-KB blocks and two 6-KB blocks and can be used to store data and execute code. Retention of the RAM contents in standby mode can be enabled or disabled individually for each block to minimize power consumption. In addition, if flash cache is disabled, the 8-KB cache can be used as general-purpose RAM.

The ROM provides preprogrammed, embedded TI-RTOS kernel and Driverlib. The ROM also contains a bootloader that can be used to reprogram the device using SPI or UART.

6.6 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface.

6.7 Power Management

To minimize power consumption, the CC1310 device supports a number of power modes and power-management features (see Table 6-2).

Table 6-2. Power Modes

MODE	SOFTWARE-CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	On	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Current	1.2 mA + 25.5 µA/MHz	570 µA	0.6 µA	185 nA	0.1 µA
Wake-up Time to CPU Active(1)	–	14 µs	174 µs	1015 µs	1015 µs
Register Retention	Full	Full	Partial	No	No
SRAM Retention	Full	Full	Full	No	No
High-Speed Clock	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
Low-Speed Clock	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on Pin Edge	Available	Available	Available	Available	Off
Wake-up on Reset Pin	Available	Available	Available	Available	Available
Brown Out Detector (BOD)	Active	Active	Duty Cycled(2)	Off	N/A
Power On Reset (POR)	Active	Active	Active	Active	N/A

(1) Not including RTOS overhead
(2) The Brown Out Detector is disabled between recharge periods in STANDBY. Lowering the supply voltage below the BOD threshold between two recharge periods while in STANDBY may cause the BOD to lock the device upon wakeup until a Reset/POR releases it. To avoid this, it is recommended that STANDBY mode is avoided if there is a risk that the supply voltage (VDDS) may drop below the specified operating voltage range. For the same reason, it is also good practice to ensure that a power cycling operation, such as a battery replacement, triggers a Power-on-reset by ensuring that the VDDS decoupling network is fully depleted before applying supply voltage again (for example, inserting new batteries). This restriction does not apply to CC1310 die rev B or later.

In active mode, the application CM3 CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 6-2).

In idle mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event returns the processor to active mode.

In standby mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to return the device to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In shutdown mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or POR by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independent of the main CPU. This means that the main CPU does not have to wake up, for example to execute an ADC sample or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio lets the user configure the Sensor Controller and choose which peripherals are controlled and which conditions wake up the main CPU.

6.8 Clock Systems

The CC1310 device supports two external and two internal clock sources.

A 24-MHz external crystal is required as the frequency reference for the radio. This signal is doubled internally to create a 48-MHz clock.

The 32.768-kHz crystal is optional. The low-speed crystal oscillator is designed for use with a 32.768-kHz watch-type crystal.

The internal high-speed RC oscillator (48-MHz) can be used as a clock source for the CPU subsystem.

The internal low-speed RC oscillator (32-kHz) can be used as a reference if the low-power crystal oscillator is not used.

The 32-kHz clock source can be used as external clocking reference through GPIO.

6.9 General Peripherals and Modules

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to assign a set of peripherals to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in *Section 4*.

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz.

The UART implements a universal asynchronous receiver and transmitter function. The UART supports flexible baud-rate generation up to a maximum of 3 Mbps.

Timer 0 is a general-purpose timer module (GPTM) that provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers, or as a PWM module.

Timer 1, Timer 2, and Timer 3 are also GPTMs; each timer is functionally equivalent to Timer 0.

In addition to these four timers, a separate timer in the RF core handles timing for RF protocols; the RF timer can be synchronized to the RTC.

The I2S interface is used to handle digital audio (for more information, see the *CC13xx, CC26xx SimpleLink™ Wireless MCU Technical Reference Manual*).

The I^2C interface is used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100-kHz and 400-kHz operation, and can serve as both I^2C master and I^2C slave.

The TRNG module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.

The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected. The watchdog timer can generate an interrupt or a reset when a predefined time-out value is reached.

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the CM3 CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller follow (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits

The AON domain contains circuitry that is always enabled, except when in shutdown mode (where the digital supply is off). This circuitry includes the following:

- The RTC can be used to wake the device from any state where it is active. The RTC contains three compare registers and one capture register. With software support, the RTC can be used for clock and calendar operation. The RTC is clocked from the 32-kHz RC oscillator or crystal. The RTC can also be compensated to tick at the correct frequency even when the internal 32-kHz RC oscillator is used instead of a crystal.
- The battery monitor and temperature sensor are accessible by software and provide a battery status indication as well as a coarse temperature measure.

6.10 Voltage Supply Domains

The CC1310 device can interface to two or three different voltage domains depending on the package type. On-chip level converters ensure correct operation as long as the signal voltage on each input/output pin is set with respect to the corresponding supply pin (VDDS, VDDS2, or VDDS3). Table 6-3 lists the pin-to-VDDS mapping.

Table 6-3. Pin Function to VDDS Mapping Table

	Package		
	VQFN 7 × 7 (RGZ)	**VQFN 5 × 5 (RHB)**	**VQFN 4 × 4 (RSM)**
VDDS(1)	DIO 23–30 Reset_N	DIO 7–14 Reset_N	DIO 5–9 Reset_N
VDDS2	DIO 1–11	DIO 0–6 JTAG_TCKC JTAG_TMSC	DIO 0–4 JTAG_TCKC JTAG_TMSC
VDDS3	DIO 12–22 JTAG_TCKC JTAG_TMSC	NA	NA

(1) The VDDS_DCDC pin must always be connected to the same voltage as the VDDS pin.

6.11 System Architecture

Depending on the product configuration, the CC1310 device can function as a wireless network processor (WNP – a device running the wireless protocol stack, with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the ARM CM3 core inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Few external components are required for the operation of the CC1310 device. Figure 7-1 shows a typical application circuit.

The board layout greatly influences the RF performance of the CC1310 device.

On the Texas Instruments CC1310EM-7XD-7793 reference design, the optimal differential impedance seen from the RF pins into the balun and filter and antenna is 44 + j15.

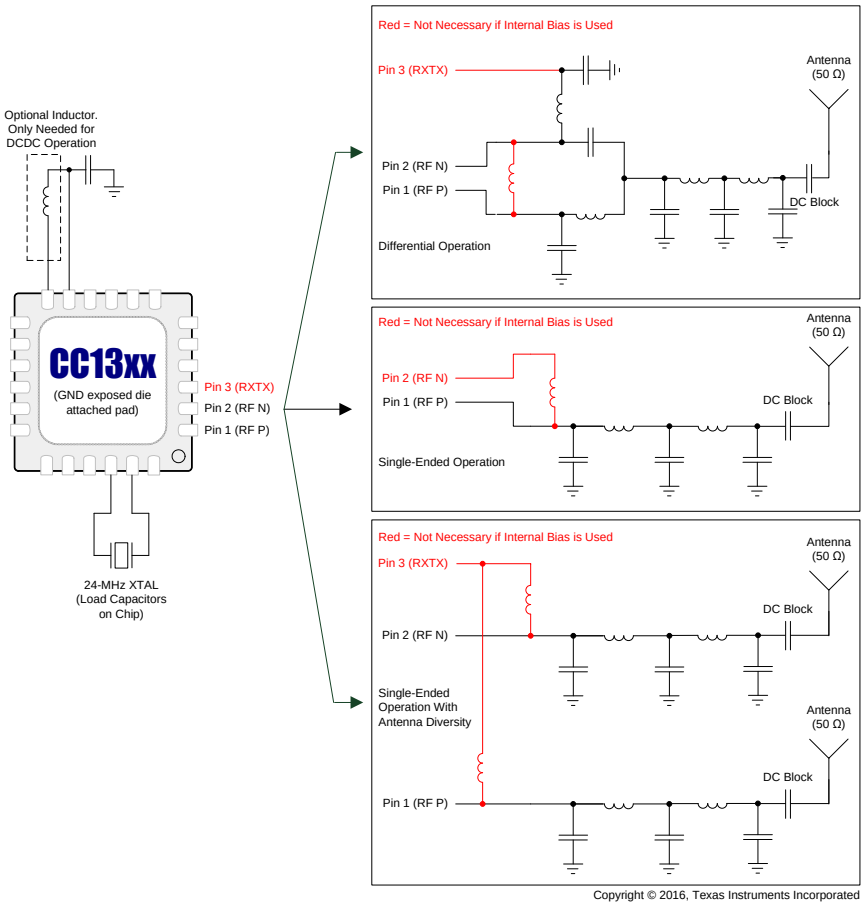


Figure 7-1 does not show decoupling capacitors for power pins. For a complete reference design, see the product folder on www.ti.com.

Figure 7-1. Differential Reference Design

7.1 TI Design

Humidity and Temp Sensor Node for Sub-1 GHz Star Networks Enabling 10+ Year Coin Cell Battery Life

This TI Design uses TI's nano-power system timer, boost converter, SimpleLink ultra-low-power Sub-1 GHz wireless MCU platform, and humidity-sensing technologies to demonstrate an ultra-low-power method to duty-cycle sensor end nodes leading to extremely long battery life. The TI Design includes techniques for system design, detailed test results, and information to get the design operating running quickly.

8 器件和文档支持

TI 提供大量的开发工具。下面介绍用于评估器件性能、生成代码以及开发解决方案的工具和软件。

8.1 器件命名规则

为了标明产品开发周期的各个产品阶段，TI 为所有部件号和/或日期代码添加了前缀。每个器件都具有以下三个前缀/标识中的一个：X、P 或无（无前缀）（例如 CC1310 正在批量生产，因此未分配前缀/标识）。

器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。只有合格的生产器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。这个后缀表示封装类型（例如 *RSM*）。

要获得 *CC1310* 器件（采用*RSM (4mm × 4mm)*、*RHB (5mm × 5mm)* 或 *RGZ (7mm × 7mm)* 封装类型）的订购部件号，请参见本文档的*封装选项附录*（TI 网站 www.ti.com），或者联系您的 TI 销售代表。

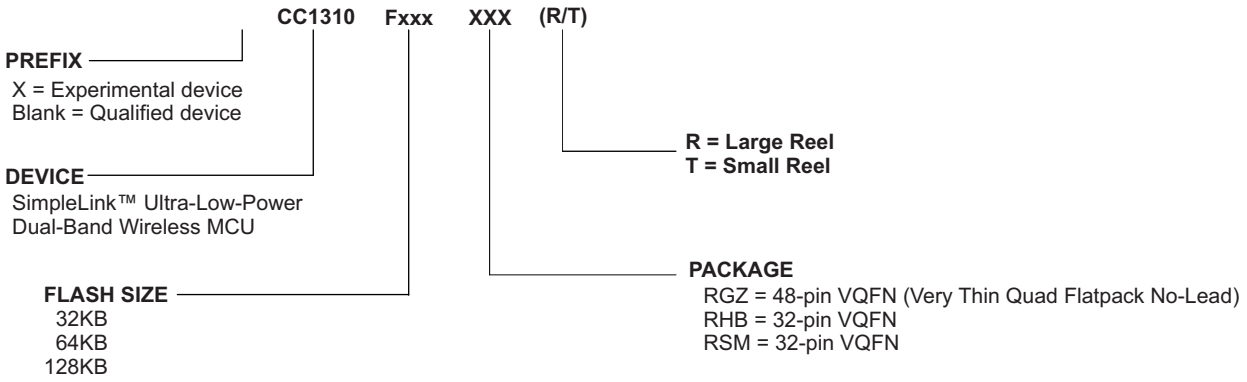


图 **8-1.** 器件命名规则

8.2 工具与软件

开发套件：

SimpleLink™ CC1310 低于 1GHz 的无线微控制器 (MCU) LaunchPad™ 开发套件

SimpleLink™ CC1310 低于 1GHz 的无线微控制器 (MCU) LaunchPad™ 开发套件是首款带有低于 1GHz 无线器件的 LaunchPad 套件，提供远程连接功能并与 32 位 ARM® Cortex®-M3 处理器相结合。

CC1310 器件是一款面向低功耗远距离 无线应用的无线 MCU。CC1310 无线 MCU 含有一个 32 位 ARM Cortex-M3 处理器（与主处理器工作频率同为 48MHz），并且具有丰富的外设功能集，其中包括一个独特的超低功耗传感器控制器。该传感器控制器非常适合连接外部传感器，还适合用于在系统其余部分处于睡眠模式的情况下自主收集模拟和数字数据。

软件工具：

SmartRF™ Studio 7

SmartRF Studio 是一款 PC 应用程序，可帮助无线电系统设计人员评估早期设计过程的 RF-IC。

- 测试无线数据包收发功能，连续波收发功能
- 将相关数据写入支持的评估板或调试器，评估定制板上的 RF 性能
- 可以不搭配任何硬件使用，但此时只能生成、编辑并导出无线配置设置
- 可与德州仪器 (TI) CC1310 系列 RF-IC 的多款开发套件搭配使用

Sensor Controller Studio

Sensor Controller Studio 为 CC1310 传感器控制器提供开发环境。此传感器控制器是 CC1310 中的一款专用功率优化型 CPU，可独立于系统 CPU 状态自主执行简单的后台任务。

- 允许使用 C 语言这类编程语言实现传感器控制器任务算法
- 输出传感器控制器接口驱动程序，其中整合了生成的传感器控制器机械代码和相关定义
- 通过使用集成传感器控制器任务测试和调试功能实现快速开发这有助于实现有效的传感器数据和算法验证可视化。

IDE 和编译器：

Code Composer Studio™

- 带有项目管理工具和编辑器的集成开发环境
- Code Composer Studio (CCS) 6.1 及更高版本内置支持 CC1310 系列器件的功能。
- 优先支持的 XDS 调试器：XDS100v3、XDS110 和 XDS200
- 与 TI-RTOS 高度集成，支持 TI-RTOS 对象视图

适用于 **ARM** 的 **IAR Embedded Workbench®**

- 带有项目管理工具和编辑器的集成开发环境
- IAR EWARM 7.30.3 及更高版本内置支持 CC1310 系列器件的功能。
- 广泛的调试器支持，支持 XDS100v3、XDS200、IAR I-Jet 和 Segger J-Link
- 带有项目管理工具和编辑器的集成开发环境
- 适用于 TI-RTOS 的 RTOS 插件

有关 CC1310 平台开发支持工具的完整列表，请访问德州仪器 (TI) 网站 www.ti.com。有关定价和购买信息，请联系最近的 TI 销售办事处或授权分销商。

8.3 文档支持

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹 (**CC1310**)。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

下面列出了介绍 CC2650CC1310CC2640R2F 器件、相关外设和其他技术材料的最新文档。

技术参考手册

*《**CC13xx、CC26xx SimpleLink™ 无线 MCU 技术参考手册**》*

参考指南

*《**CC26xx/CC13xx 电源管理软件开发者参考指南**》*

应用报告

*《将 **GCC/GDB 与 SimpleLink™ CC26xx/CC13xx 搭配使用**》*

*《**CC-天线-DK2 和天线测量结果汇总**》*

8.4 德州仪器 (TI) 低功耗射频网站

TI 的低功耗射频网站提供所有最新产品、应用和设计笔记、FAQ 部分、新闻资讯以及活动更新。请访问 www.ti.com/longrange。

8.5 低功耗射频电子新闻简报

通过低功耗射频电子新闻简报，您能够了解到最新的产品、新闻稿、开发者相关新闻以及关于德州仪器 (TI) 低功耗射频产品其它新闻和活动。低功耗射频电子新闻简报文章包含可获取更多在线信息的链接。

访问：www.ti.com.cn/lprfnewsletter 立即注册

8.6 其他信息

德州仪器 (TI) 为工业和消费类应用中所使用的专有应用和标准无线 应用 提供各种经济实用的低功耗射频 解决方案。其中包括适用于 1GHz 以下频段和 2.4GHz 频段的射频收发器、射频发送器、射频前端和片上系统以及各种软件解决方案。

此外，德州仪器 (TI) 还提供广泛的相关支持，例如开发工具、技术文档、参考设计、应用专业技术、客户支持、第三方服务以及大学计划。

低功耗射频 E2E 在线社区设有技术支持论坛并提供视频和博客，您有机会在此与全球同领域工程师交流互动。

凭借丰富的供选产品解决方案、可实现的最终应用以及广泛的技术支持，德州仪器 (TI) 能够为您提供最全面的低功耗射频产品组合。

8.7 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

TI E2E™ Online Community The TI engineer-ro-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI 嵌入式处理器维基网页 *德州仪器 (TI) 嵌入式处理器维基网站*。此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

低功耗射频在线社区 TI E2E 支持社区的无线连接部门

- 论坛、视频和博客
- 射频设计帮助
- E2E 交流互动

请点击此处加入我们。

低功耗射频开发者网络 德州仪器 (TI) 建立了一个大型低功耗射频开发合作伙伴网络，帮助客户加快应用开发。此网络中包括推荐的公司、射频顾问和独立设计工作室，他们可提供一系列硬件模块产品和设计服务，其中包括：

- 射频电路、低功耗射频和 ZigBee®设计服务
- 低功耗射频和 ZigBee 模块解决方案以及开发工具
- 射频认证服务和射频电路制造

如果需要有关模块、工程服务或开发工具的帮助：

请搜索低功耗射频开发者网络查找适合的合作伙伴。www.ti.com.cn/lprfnetwork

8.8 商标

SimpleLink, SmartRF, Code Composer Studio, 经济高效型超低功耗 2.4GHz 和低于 1GHz 的 RF 器件。, E2E are trademarks of Texas Instruments.
ARM7 is a trademark of ARM Limited (or its subsidiaries).
ARM, Cortex, Thumb are registered trademarks of ARM Limited (or its subsidiaries).
ULPBench is a trademark of Embedded Microprocessor Benchmark Consortium.
CoreMark is a registered trademark of Embedded Microprocessor Benchmark Consortium.
IAR Embedded Workbench is a registered trademark of IAR Systems AB.
IEEE Std 1241 is a trademark of Institute of Electrical and Electronics Engineers, Incorporated.
IEEE is a registered trademark of Institute of Electrical and Electronics Engineers, Incorporated.
Wi-SUN is a trademark of Wi-SUN Alliance, Inc.
ZigBee is a registered trademark of Zigbee Alliance.
All other trademarks are the property of their respective owners.

8.9 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.10 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过非披露义务的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

8.11 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

9.1 封装信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1310F128RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F128RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F128	Samples
CC1310F32RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F32RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F32	Samples
CC1310F64RGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples
CC1310F64RSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1310F64RSMT	ACTIVE	VQFN	RSM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	CC1310 F64	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

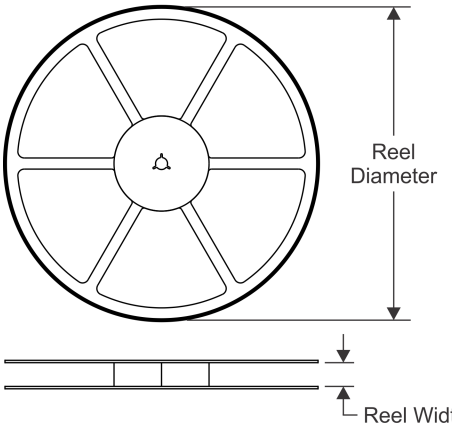
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

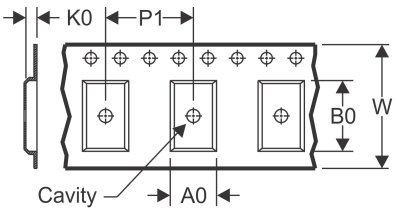
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

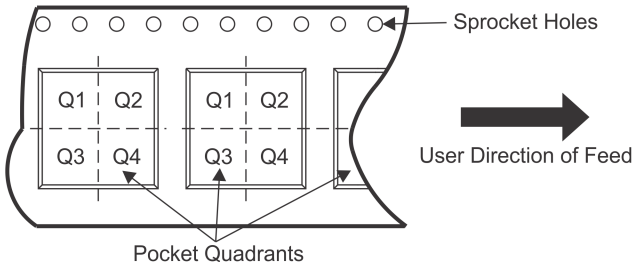


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

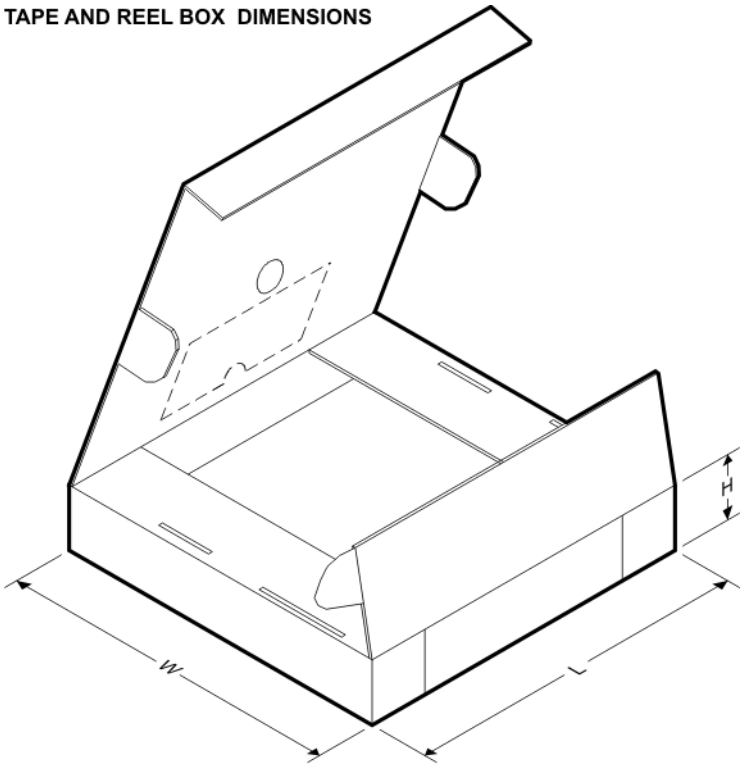
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC1310F128RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F128RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F128RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F128RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F128RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F128RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F32RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F32RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F32RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F32RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F32RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F64RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F64RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
CC1310F64RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F64RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
CC1310F64RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
CC1310F64RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

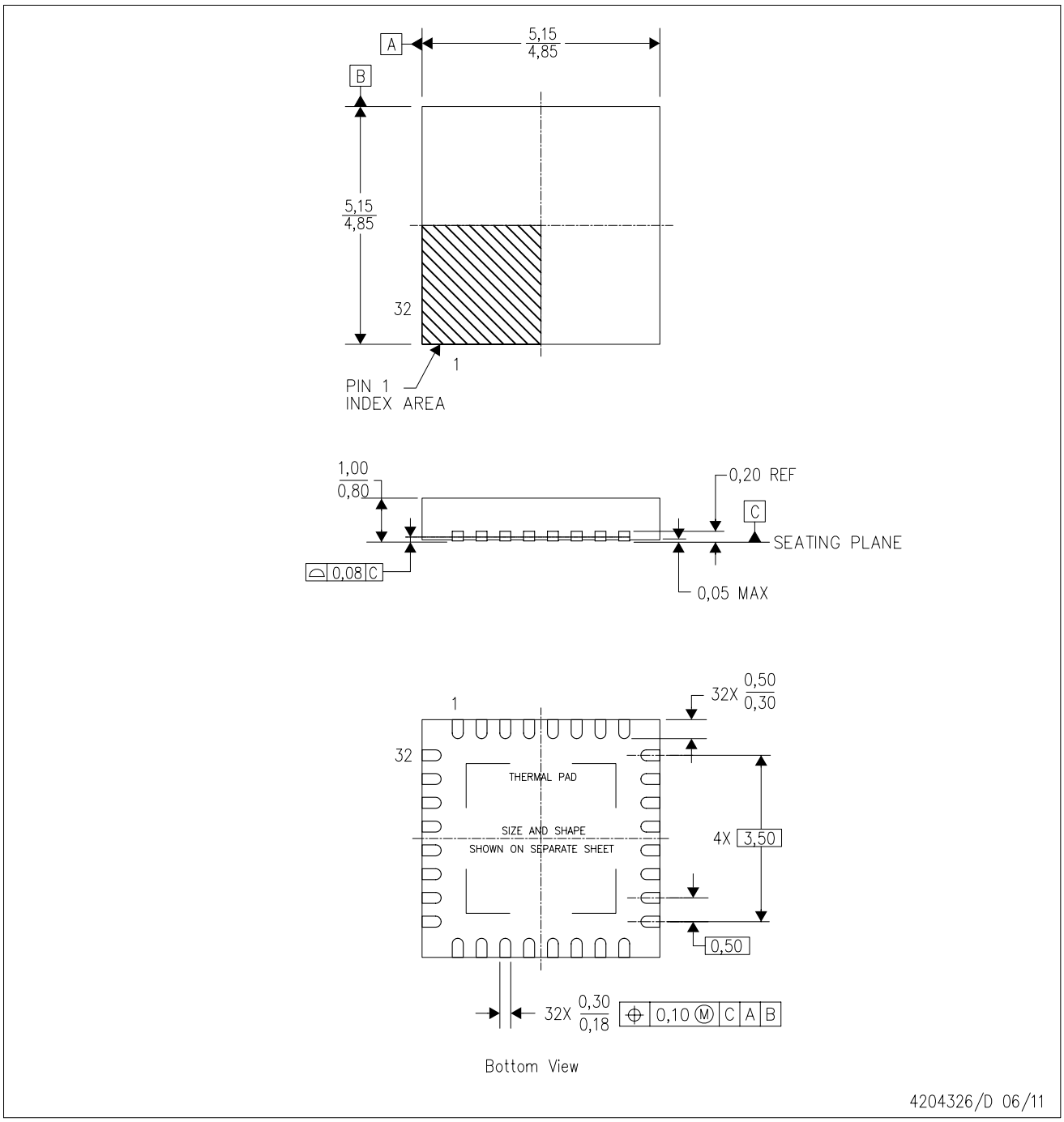
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC1310F128RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CC1310F128RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1310F128RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC1310F128RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC1310F128RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
CC1310F128RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
CC1310F32RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CC1310F32RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1310F32RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC1310F32RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC1310F32RSMT	VQFN	RSM	32	250	210.0	185.0	35.0
CC1310F64RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
CC1310F64RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
CC1310F64RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
CC1310F64RHBT	VQFN	RHB	32	250	210.0	185.0	35.0
CC1310F64RSMR	VQFN	RSM	32	3000	367.0	367.0	35.0
CC1310F64RSMT	VQFN	RSM	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

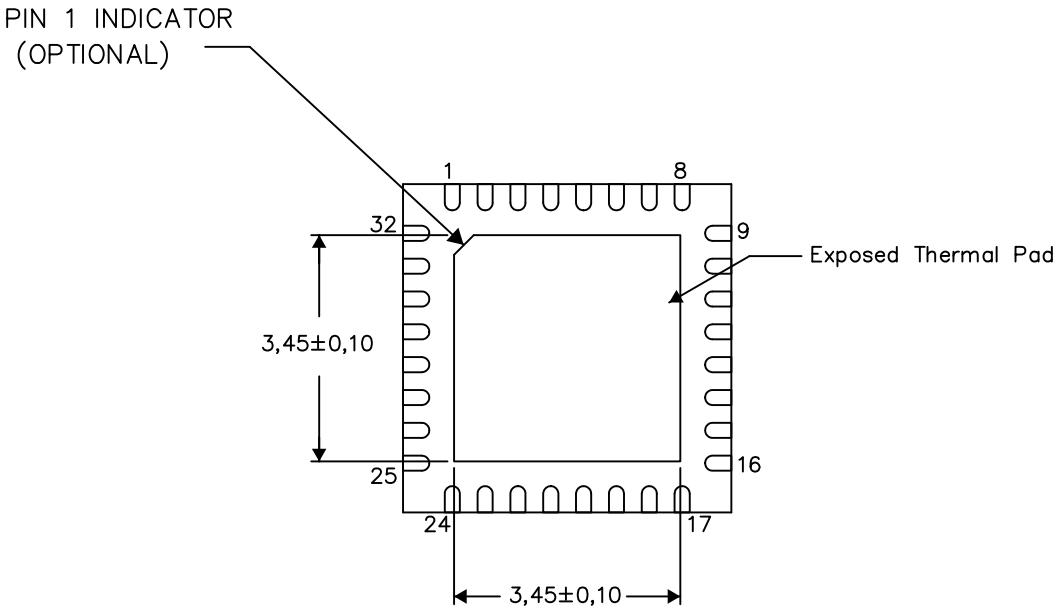
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



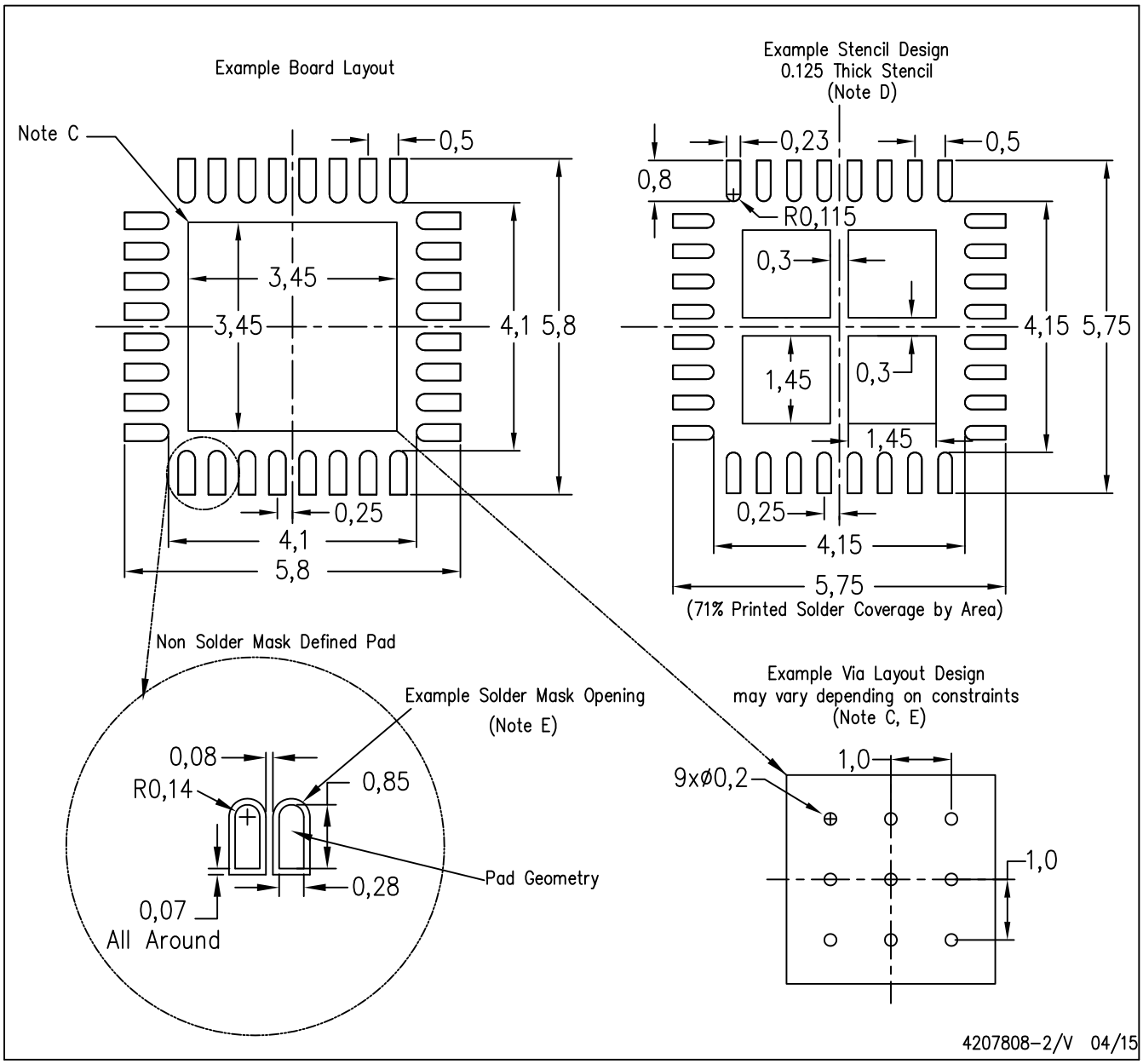
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

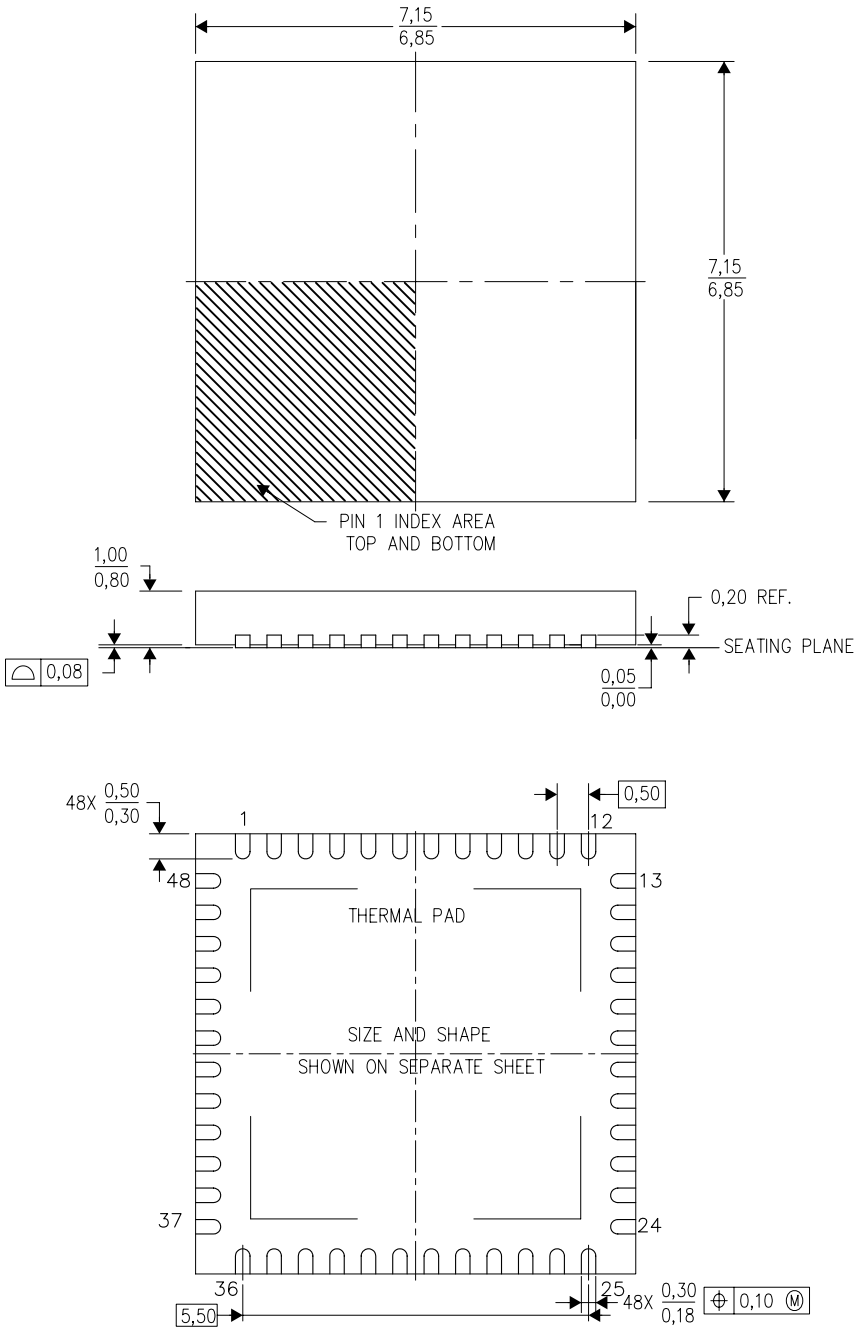
NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

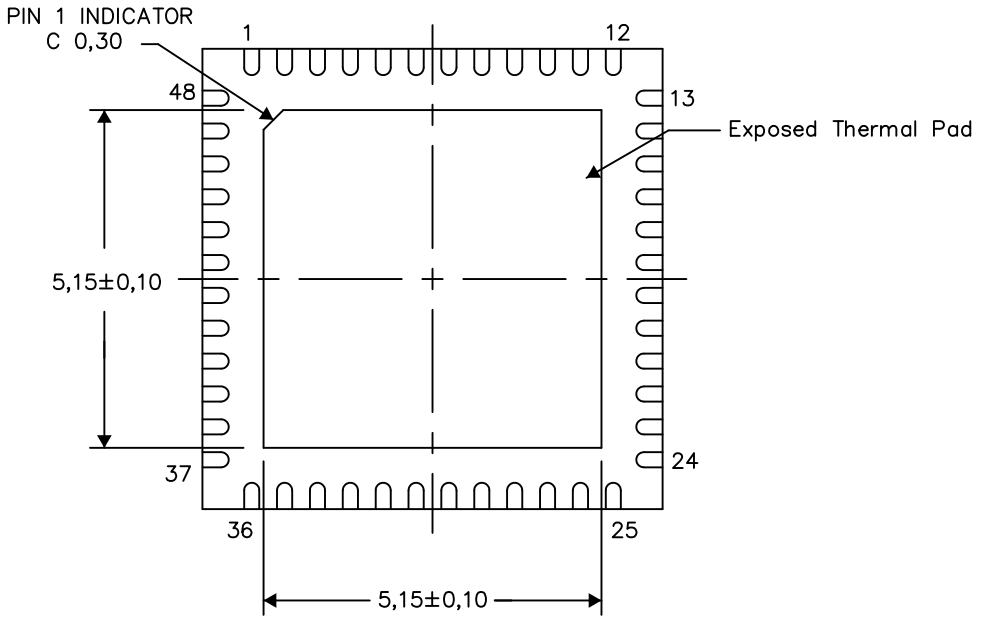
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



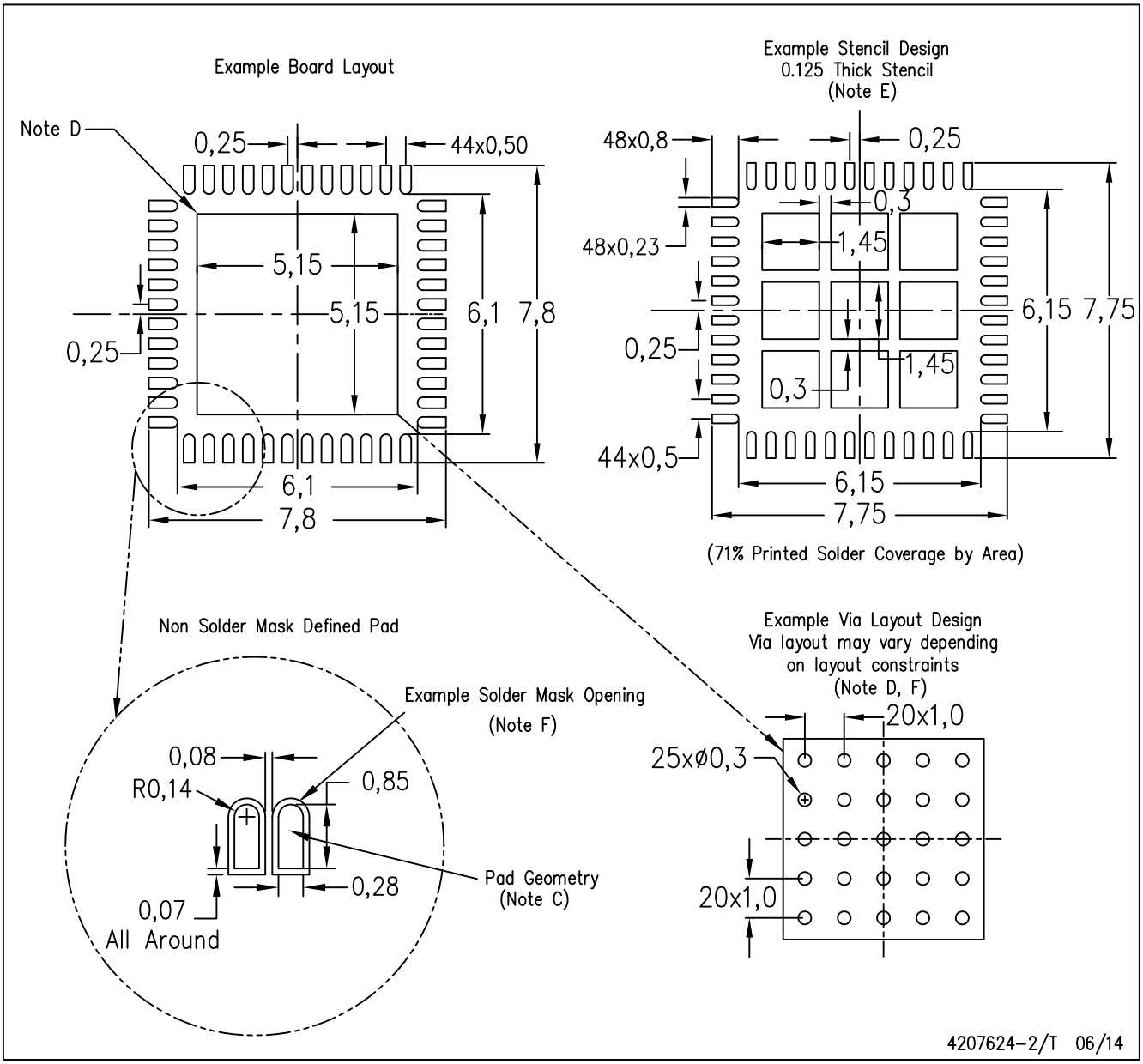
Bottom View

Exposed Thermal Pad Dimensions

4206354–2/Z 03/15

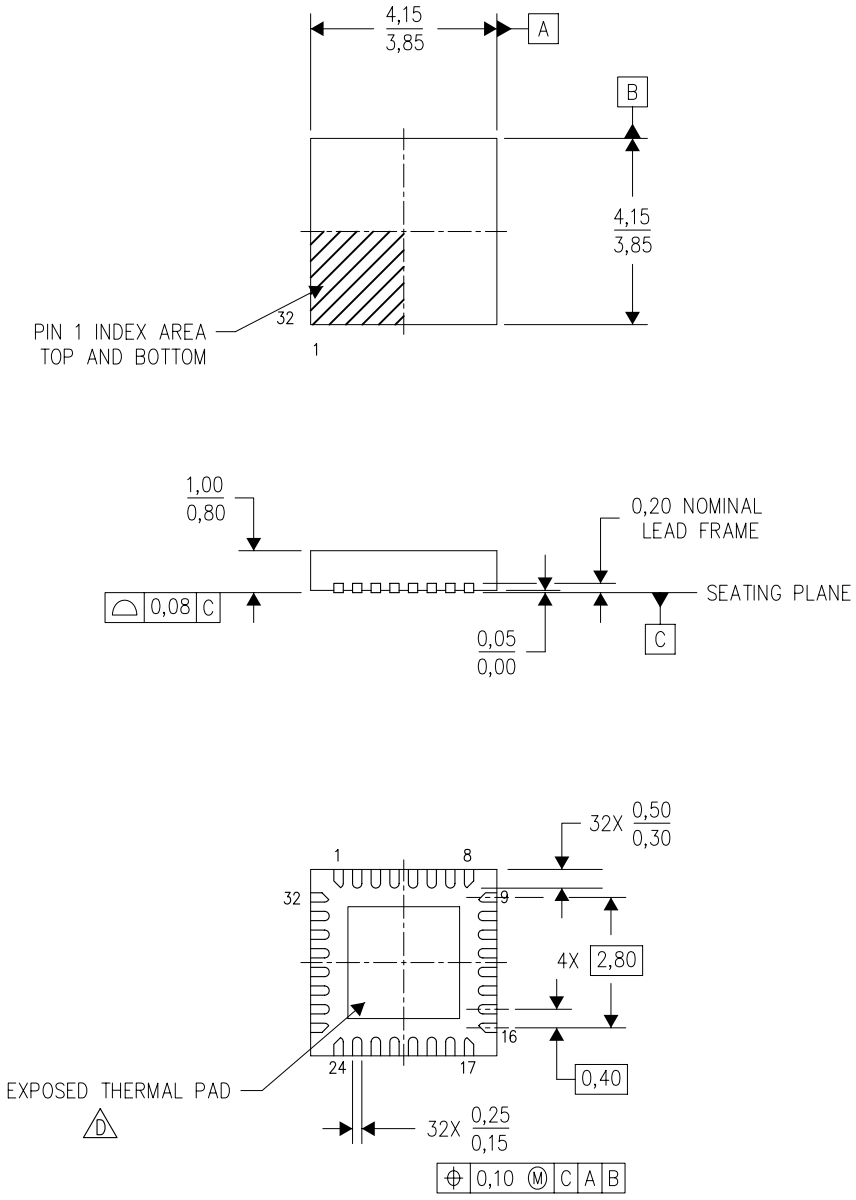
NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4207560/B 03/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

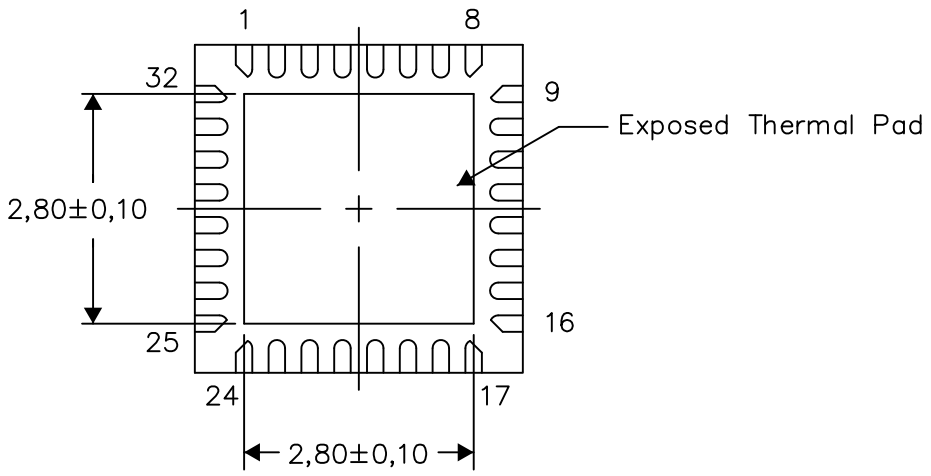
RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



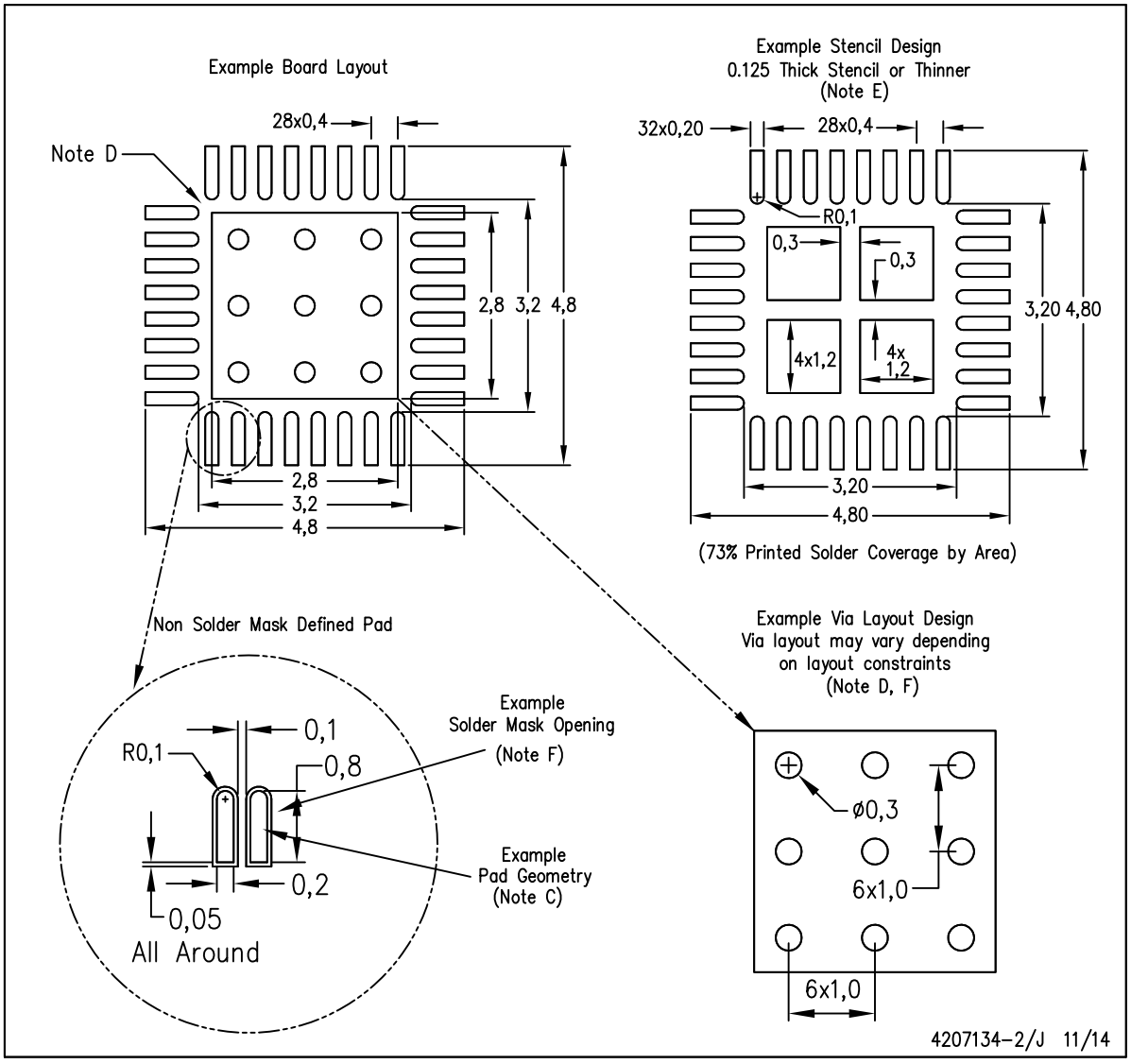
Bottom View

Exposed Thermal Pad Dimensions

4207868–2/I 07/14

NOTE: All linear dimensions are in millimeters

RSM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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