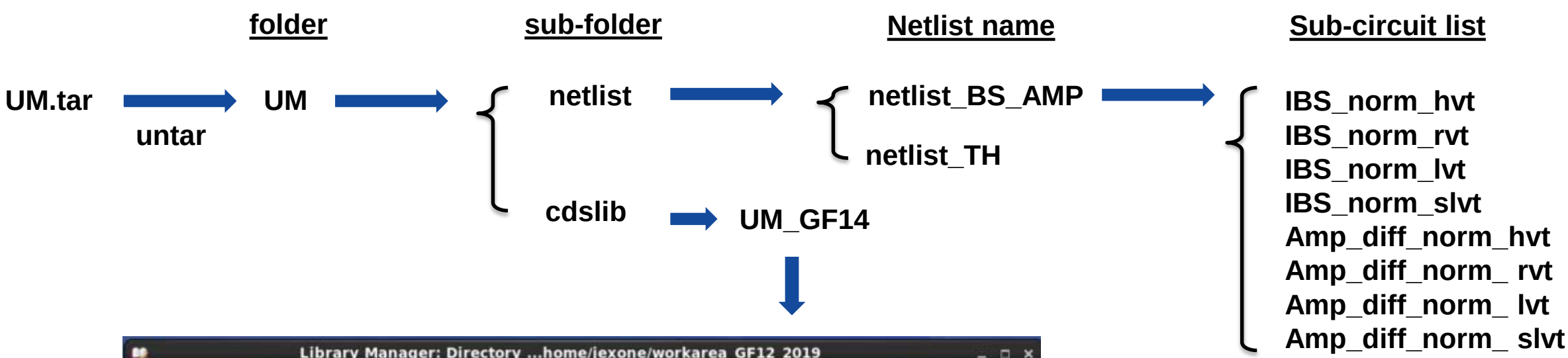
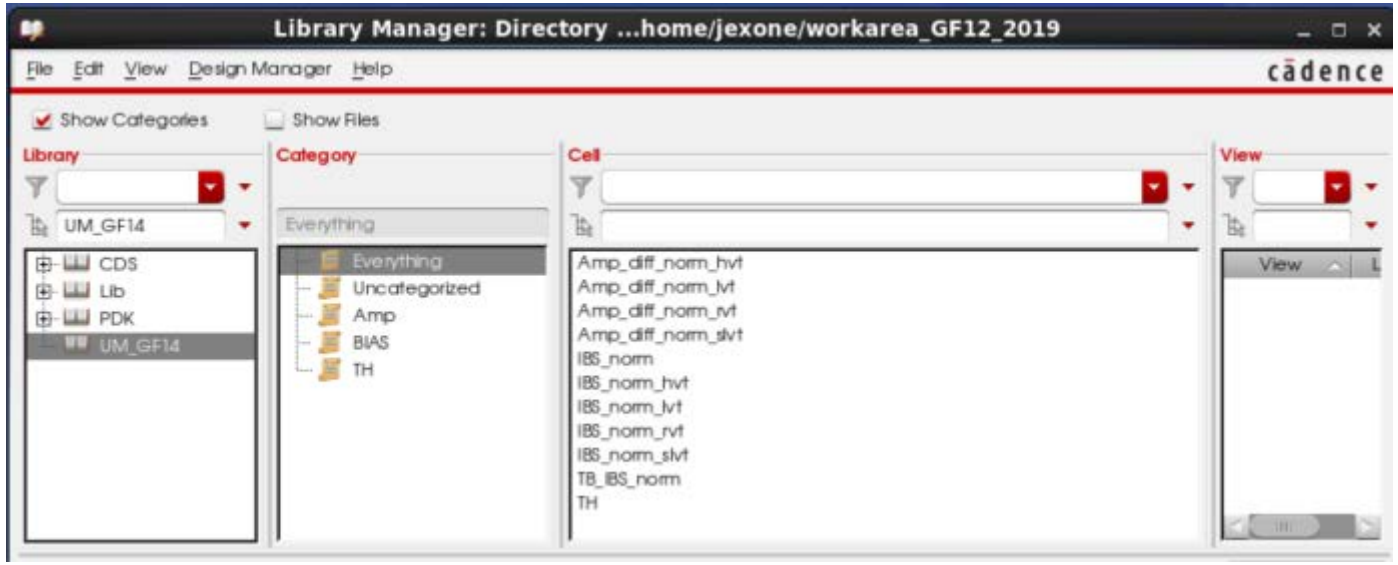
Automated AMS IP Generator for CMOS Technologies (collaboration with UMN)

University of Southern California

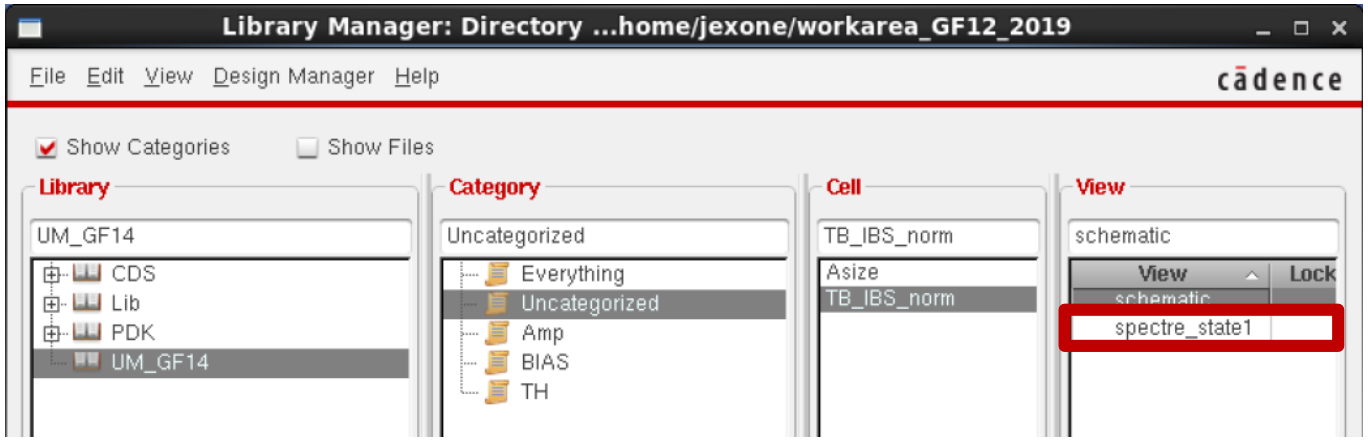
May. 2019

USC delivered File structure

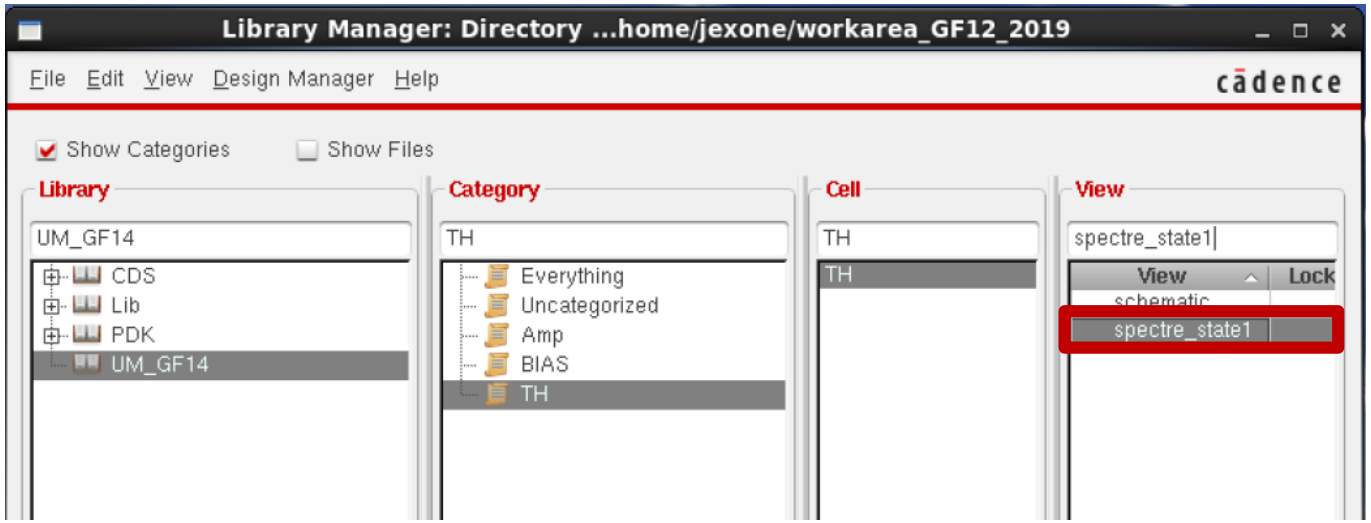




GF14 Design Testbench

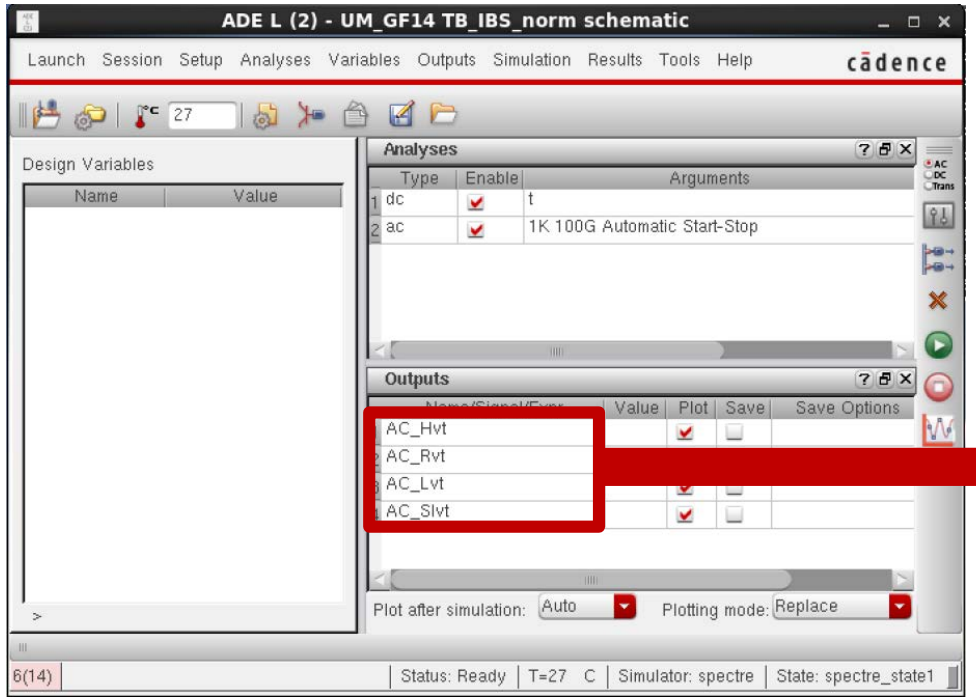


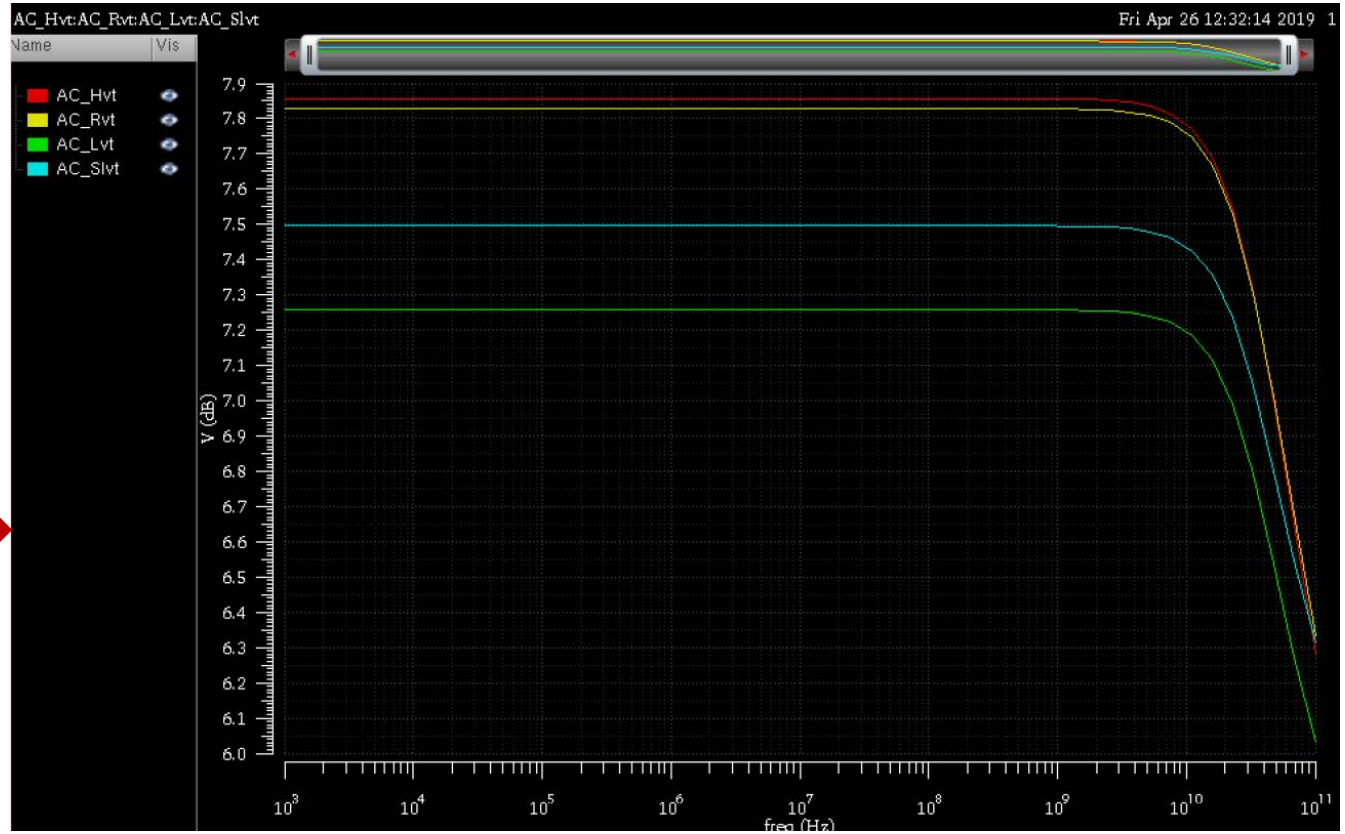
Amplifier's AC response Testbench



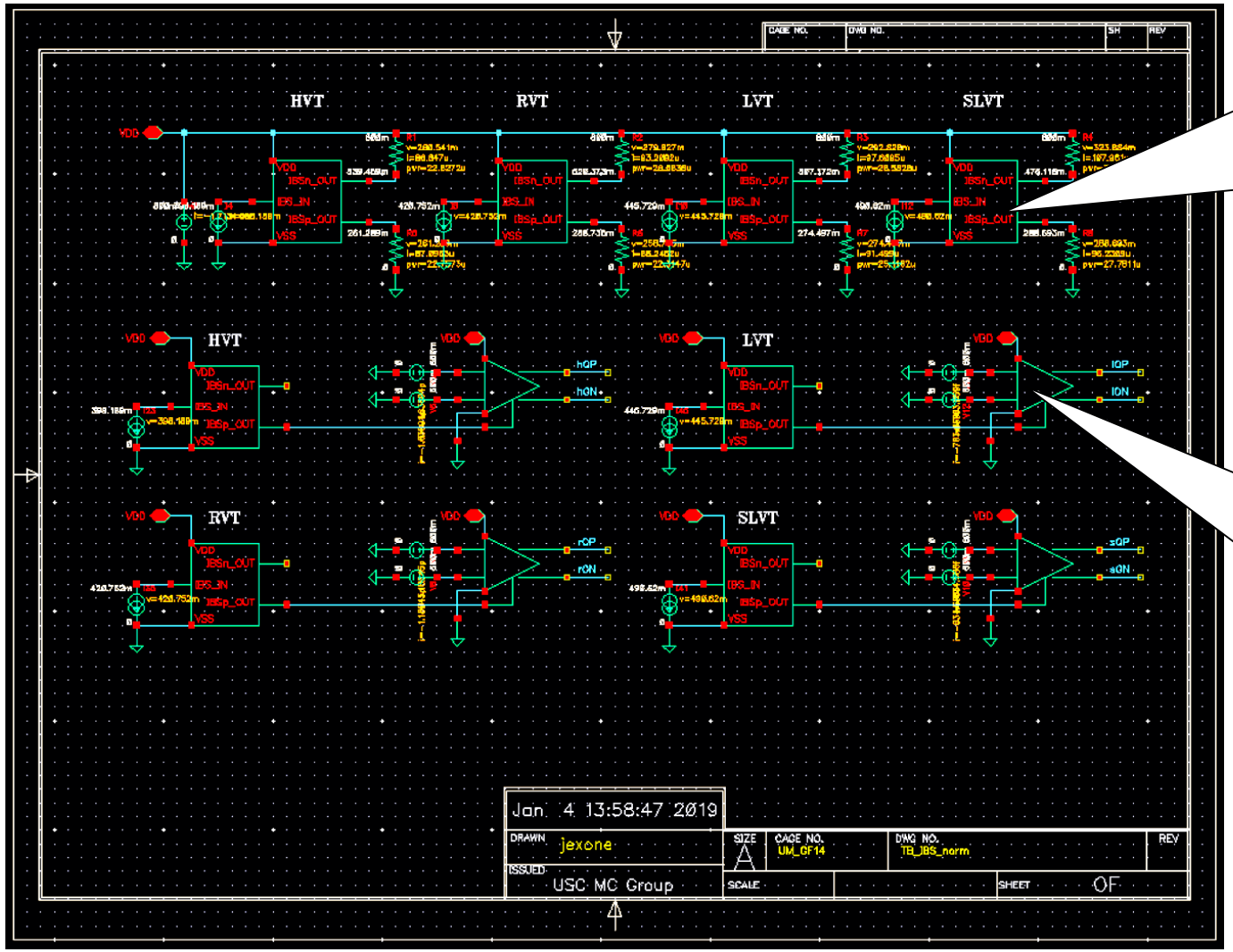
T/H's FFT evaluation Testbench

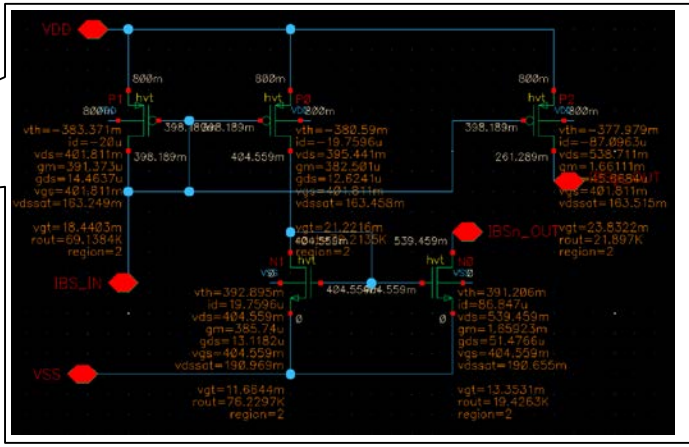
GF14 Design Test-Bench (Bias & Amp circuits)





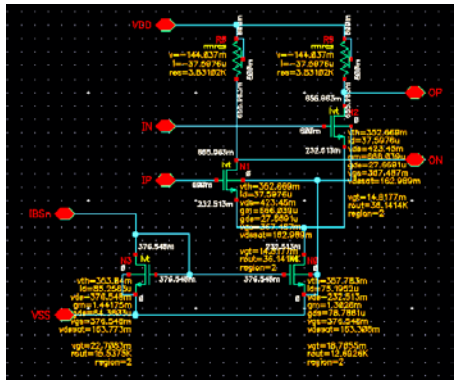
GF14 Design Example (Bias & Amp circuits)





Simple
Current mirror

NMOS/PMOS



Simple
Diff. Amp wit
Resistive Load

NMOS Input
600mV V_{CM}
800mV VDD

High V_{TH} CMOS
Normal V_{TH} CMOS
Low V_{TH} CMOS
Super-low V_{TH} CMOS

4 different type transistor Circuits are prepared.

GF14 Design Example (Switched Cap T/H)