# Hyperlinked Summary of Predictive Models

- Multiple fingers cannot be set for MOSFET when using the PTM model; multiplier can be used instead.
- Write *simulator lang = spice* at top of the .pm (model) file to simulate.

| Developer | Layout availability | Device type | Device flavors | Technology node (nm) | Latest Release Version |
|---|---|---|---|---|---|
| Nanoscale Integration & Modeling group @ ASU (PTM) | No | Bulk CMOS | - | 130, 90, 65 | 1.0 |
| | | | HP (High-Performance) | 45, 32, 22, 16 | 2.1 |
| | | | LP (Low-Power) | 45, 32, 22, 16 | 2.1 |
| | | Multi-gate transistors | HP (High-Performance) | NMOS: 20, 16, 14, 10, 7 | - |
| | | | | PMOS: 20, 16, 14, 10, 7 | |
| | | | LSTP (Low-Standby Power) | NMOS: 20, 16, 14, 10, 7 | - |
| | | | | PMOS: 20, 16, 14, 10, 7 | |
| ASU + ARM collaboration (ASAP)* | Yes | Multi-gate transistors | 4 threshold voltage, 3 corner | 7 | 1.6 |

* downloading requires registration with academic email.