

The Maze Game

Board Specifications

Fall 1976

TTL, DTL, MSI, + LSI Boards
and interfaces available for
the MIT 6.111/6.112 Digital
Design Labs in Fall 1976
used for the Maze project.

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Paper Tape Reader

The paper tape reader reads 8-channel (or less) paper tape in either the forward or backward direction. Reading speeds are from 0 to 30 characters per second from external pulse sources. The output of the tape reader is buffered by a set of flip-flops and available to the user by a cable. All electrical connections are compatible with RTL micrologic.

A representation of the control panel is given in Figure 1. The following list explains the function of each part.

1. Fuse
2. Fuse light - lights when fuse is blown
3. AC power switch
4. Power indicator light
5. Tape loaded light
6. Local clock switch - enables internally generated pulse train to drive the tape reader.
7. Local clock light - lights when local clock switch is up.
8. Forward-backward switch - determines the direction the tape will travel when driven by the local clock.
9. Forward and backward lights - indicate direction of tape travel.
10. Busy light
11. Reset push button - resets the busy flip-flop. The reset push button should be pushed if the reader does not respond to input pulses.
12. Data lights - indicate the state of the buffer flip-flops.
13. Output plug - external connections to the tape reader.

The following procedure should be used to load the tape (see Figure 2):

1. Insure that the star wheels are raised by turning the star wheel position knob counterclockwise.
2. Position the tape between the star wheels and the sprocket as indicated in Figure 2 so that channel 1 is the furthest from you. Note that the direction of forward travel is from right to left.
3. Lower the star wheels by turning the star wheel position

PAPER TAPE READER

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knob clockwise. If the AC power switch is on, the tape loaded light will be lit when the star wheels are down.

User connections to the tape reader may be made via the output plug. For the convenience of the user an adaptor cable is available which has a printed circuit card on one end so that connections may be made to an ordinary printed circuit connector. Details of these wiring connections are shown in Table I.

Both external drive pulses should be less than 10 MS long - preferably $.1\text{ MS}$; and no two pulses should occur within $3\frac{1}{4}\text{ ms}$ of each other. The busy level indicates the time at which external drive pulses will be ignored, and the completion pulse occurs after the line of tape has been stored in the output flip-flops.

Printed Circuit Card Pin No.	Output Plug Pin No.	RTL Loads	Signal
3	1	4	Tape channel 1
4	2	4	Tape channel 2
5	3	4	Tape channel 3
6	4	4	Tape channel 4
7	5	4	Tape channel 5
8	6	4	Tape channel 6
9	7	4	Tape channel 7
10	8	4	Tape channel 8
11	9	4	Local oscillator
12	10	2	External backward drive pulse
13	11	2	External forward drive pulse
14	12	4	Busy level
15	13	4	Completion pulse
16	14		GND
17	15		
18	16		

Table I

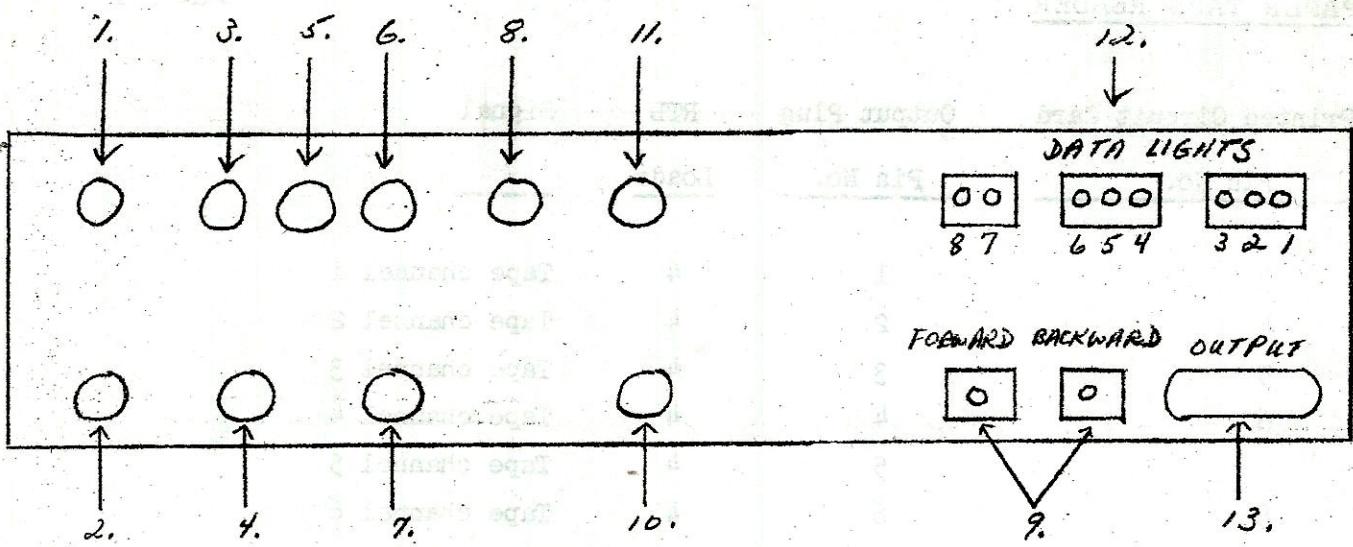


FIGURE 1. READER CONTROLS

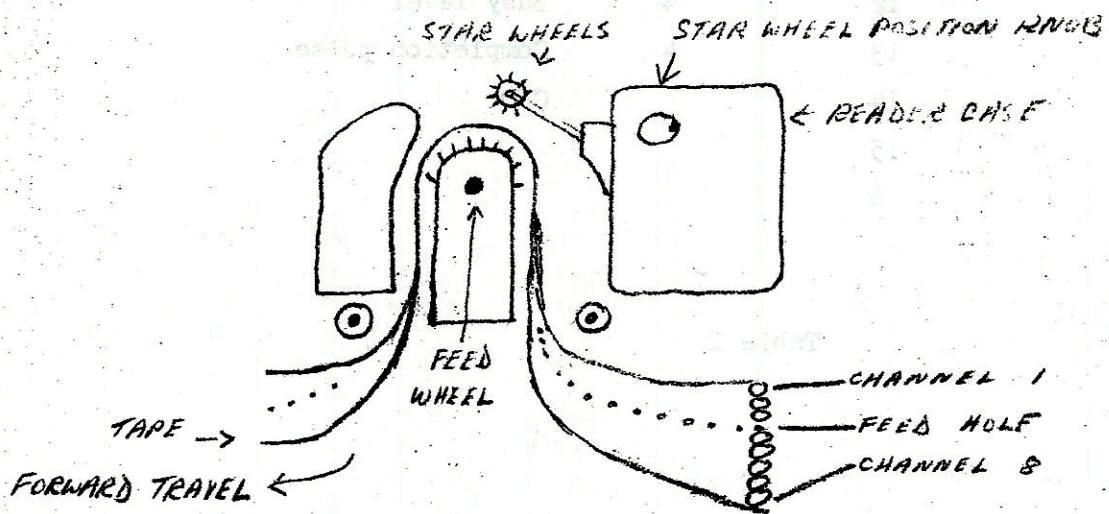
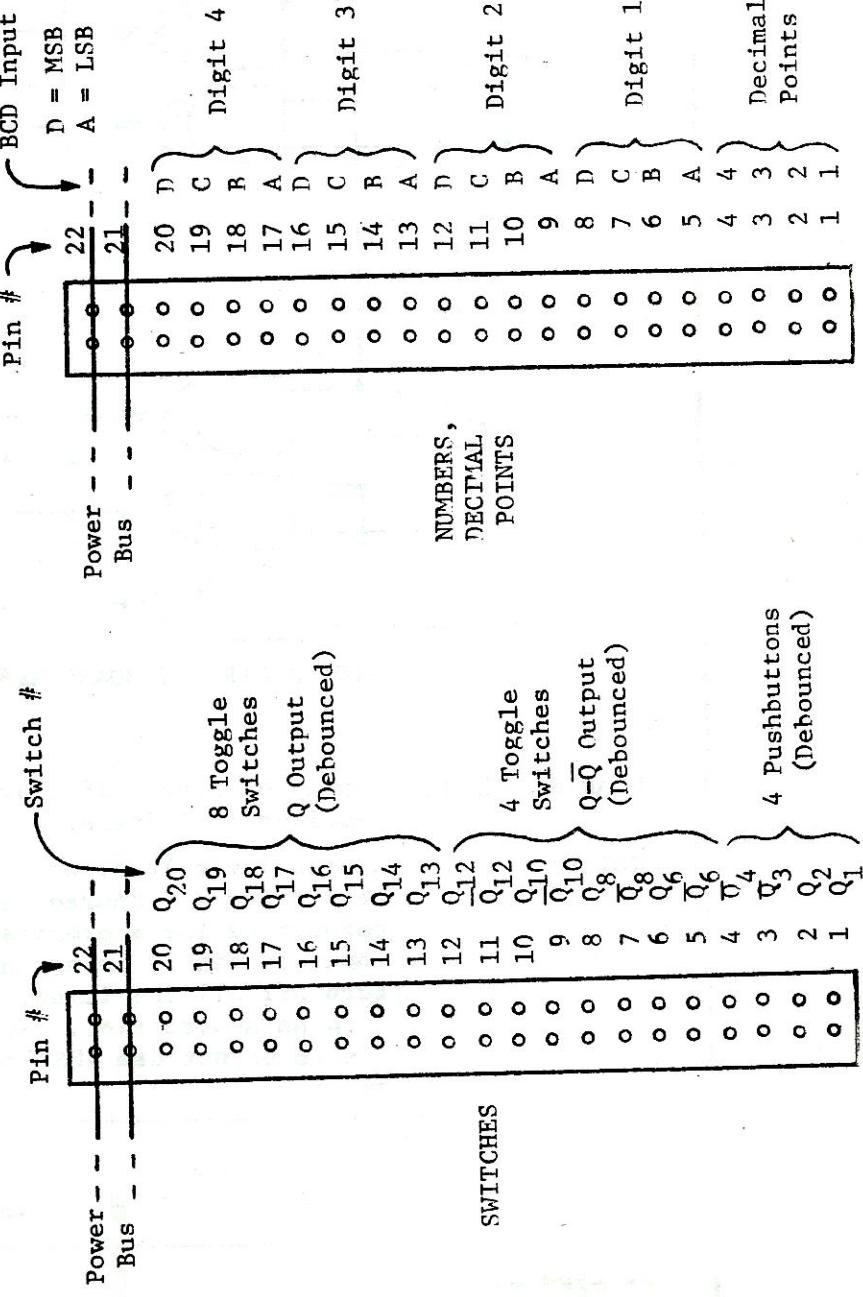
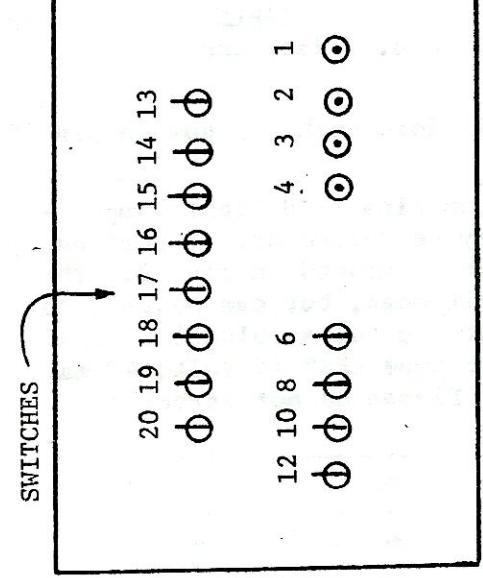


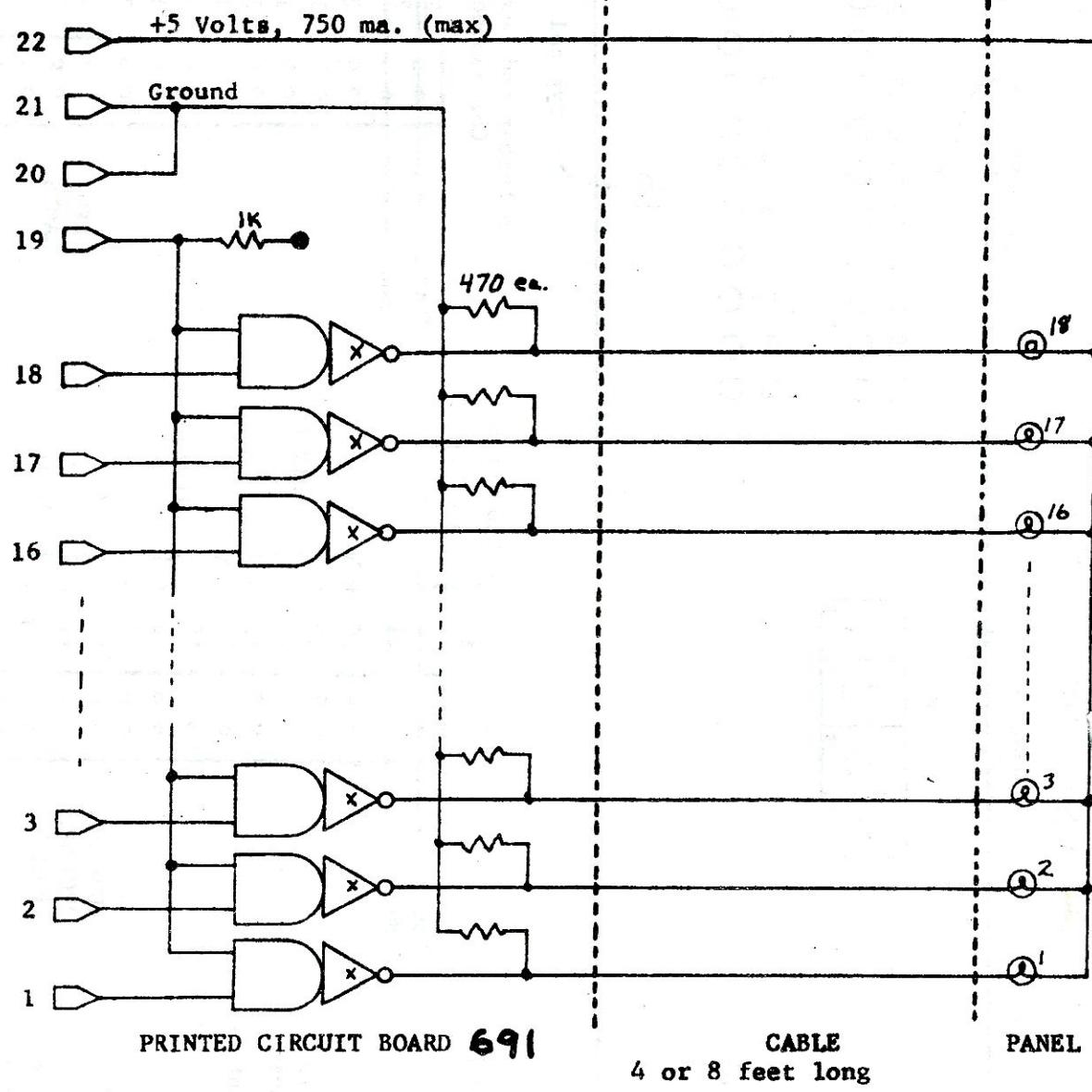
FIGURE 2. LOADING TAPE

LIGHT-SWITCH PANEL NUMERIC DISPLAY



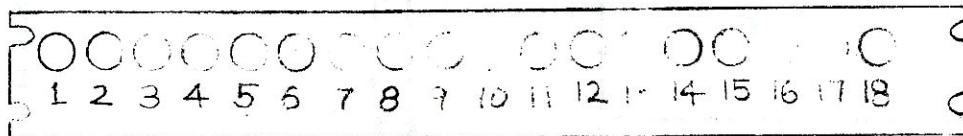
18 Lamp Indicator Assembly

PIN CONNECTIONS:

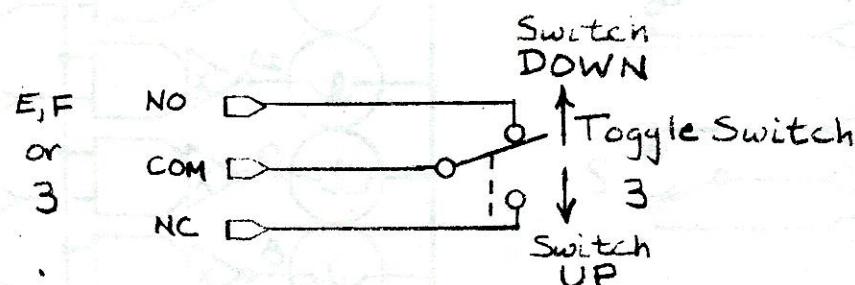
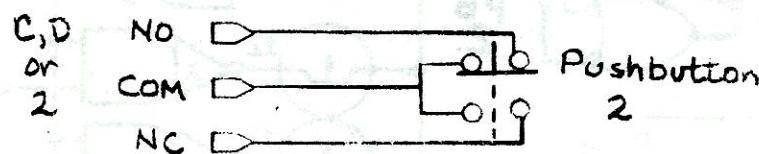
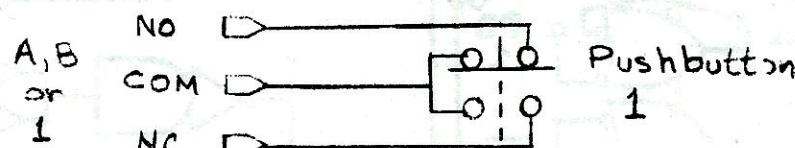


LOADING RULES: Inputs on pins 1-18 require (1) load each. Input on pin 19 requires (23) loads.

NOTES: A high logic level or an open on pins 1-18 light lamps 1-18 respectively. Unused lamps may be turned off if desired by connecting the appropriate pins to ground on pin 20. The input on pin 19 is normally left open, but can be used to turn off all the lamps. To test the bulbs, plug the card into an unused slot. Bulbs are type 6ESB [6 Volt, 40 ma.]. Please do not use 4ESB bulbs. Please do not stress the cable.



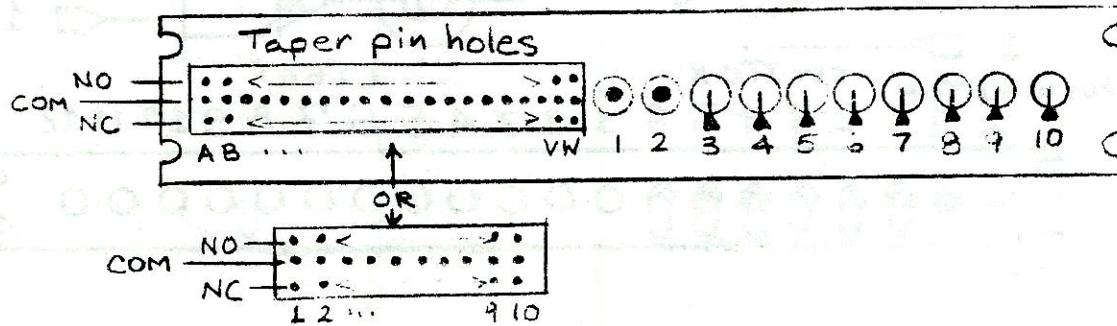
Switch Panel; 2 Pushbuttons, 8 Toggles SPDT



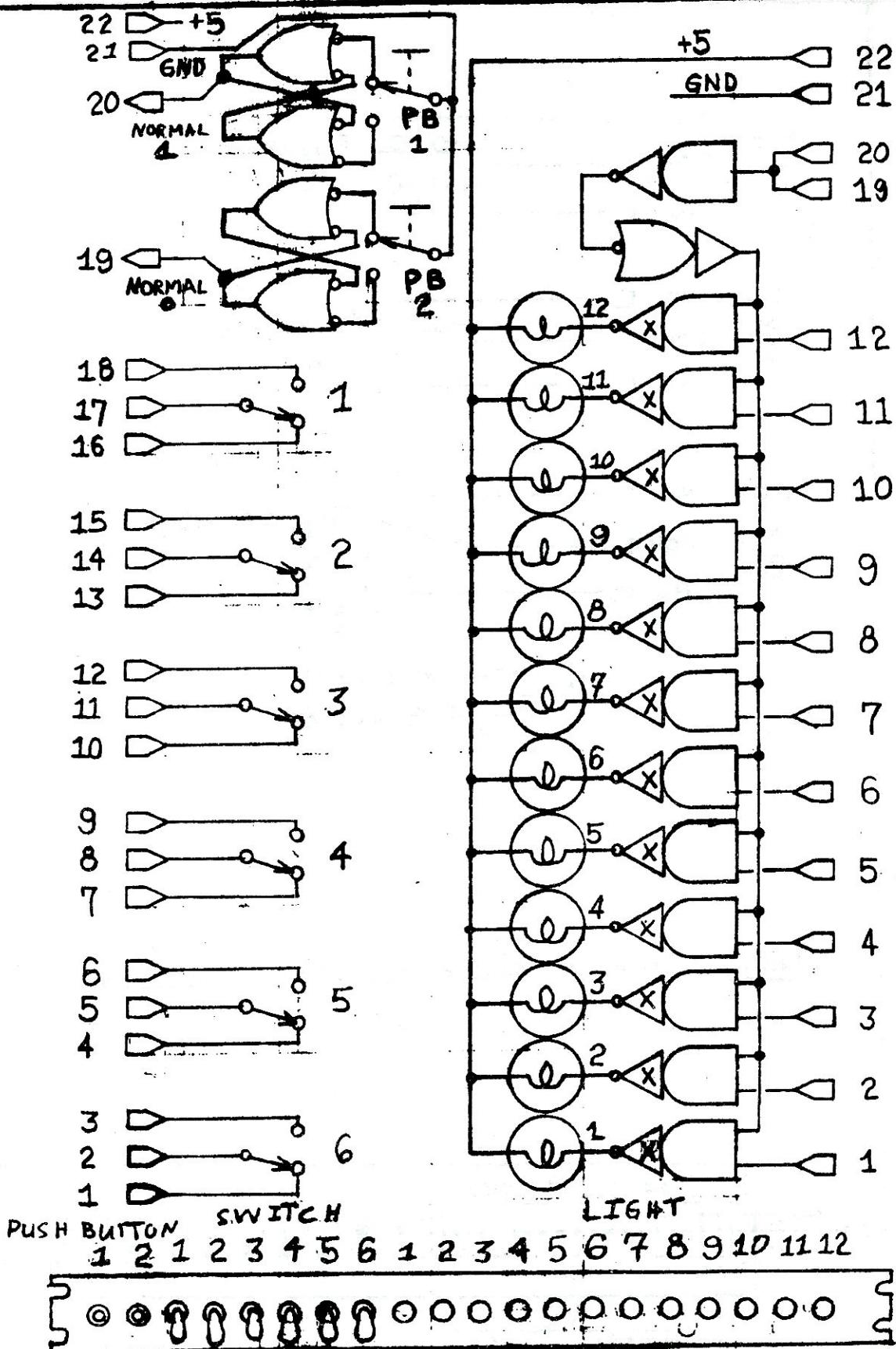
: Same for other
Toggle switches

V,W
or
10

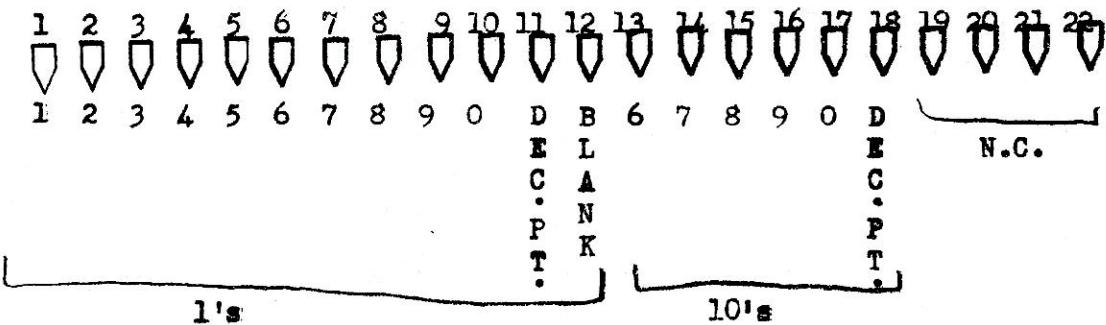
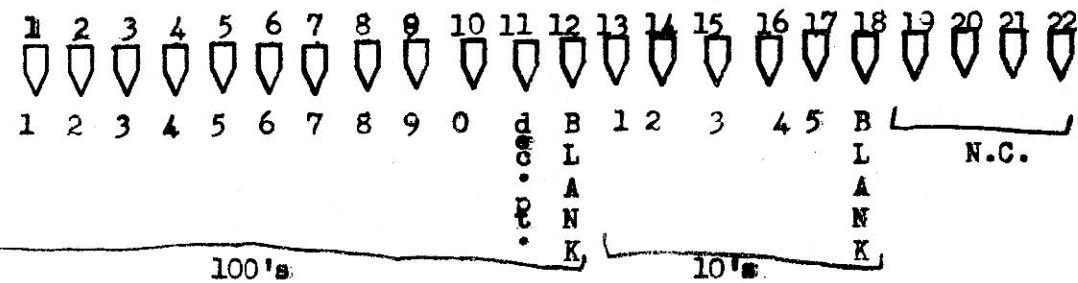
Note: None of these switches are debounced.



**COMBINATION
LIGHT & SWITCH PANEL**



PIN CONNECTIONS FOR THE NUMERIC READOUT PANEL



NOTES:

1. Terminals marked 'blank' must be grounded to turn digit on.
2. High logic level turns number or dec. pt. on.
3. When used with TTL board type 541 (BCD to Dec. conv.), inverters must be placed between the output of the 541 and the input to the lights.

STEAL TOOLS: DIAMOND AND PROTECTIVE KIT

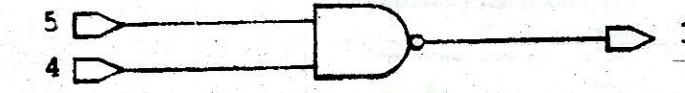
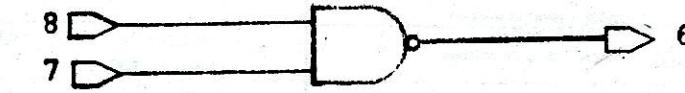
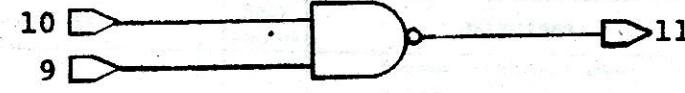
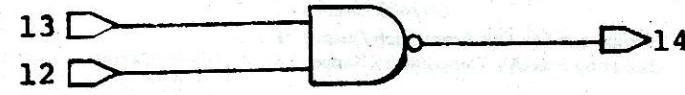
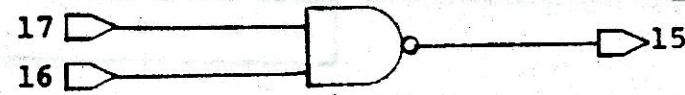
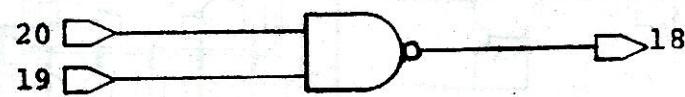


The diamond and protective kit have "stealth" button functions
and they used to reduce arrest level signals and
lower threshold values. The cost of installing and based off data base costs, it
is slightly less than half and has LID set to function and increase memory at

PIN CONNECTIONS:

22 — +5 Volts, 34 ma

21 — Ground

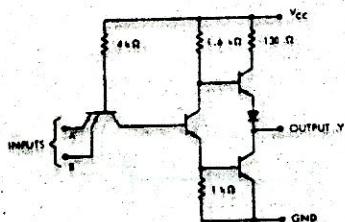


LOADING RULES: Inputs require 1.25 loads (1 if non-H series)
Outputs can drive 12.5 loads (10 if non-H series)

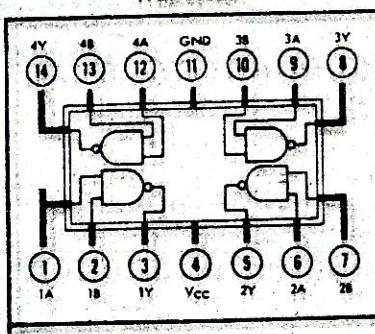
Propagation Delay is 6 ns (10nS if non-H series)

CIRCUIT TYPES SN5400, SN7400 QUADRUPLE 2-INPUT POSITIVE NAND GATES

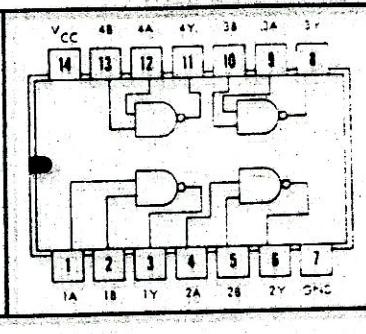
schematic (each gate)



W. FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NOTE: Component values shown are nominal.

positive logic: $Y = \bar{AB}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V _{CC} : SN5400 Circuits	4.5	5	5.5	V
SN7400 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T _A : SN5400 Circuits	-55	25	125	°C
SN7400 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V _{in(1)} Logical 1 input voltage required at both input terminals to ensure logical 0 level at output	1			2		V
V _{in(0)} Logical 0 input voltage required at either input terminal to ensure logical 1 level at output	2			0.8		V
V _{out(1)} Logical 1 output voltage	2	V _{CC} = MIN, V _{in} = 0.8 V, I _{load} = -400 μA	2.4	3.3		V
V _{out(0)} Logical 0 output voltage	1	V _{CC} = MIN, V _{in} = 2 V, I _{sink} = 16 mA	0.22	0.4		V
I _{in(0)} Logical 0 level input current (each input)	3	V _{CC} = MAX, V _{in} = 0.4 V			-1.6	mA
I _{in(1)} Logical 1 level input current (each input)	4	V _{CC} = MAX, V _{in} = 2.4 V V _{CC} = MAX, V _{in} = 5.5 V			40 μA 1 mA	
I _{OS} Short-circuit output current [§]	5	V _{CC} = MAX	SN5400	-20	-55	mA
I _{CC(0)} Logical 0 level supply current	6	V _{CC} = MAX, V _{in} = 5 V		-18	-55	mA
I _{CC(1)} Logical 1 level supply current	6	V _{CC} = MAX, V _{in} = 0		12	22	mA
			SN7400	4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pd0} Propagation delay time to logical 0 level	65	C _L = 15 pF, R _L = 400 Ω	7	15		ns
t _{pd1} Propagation delay time to logical 1 level	65	C _L = 15 pF, R _L = 400 Ω	11	22		ns

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

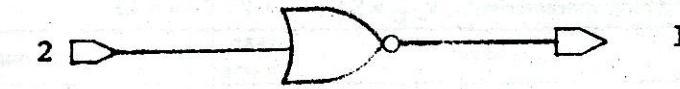
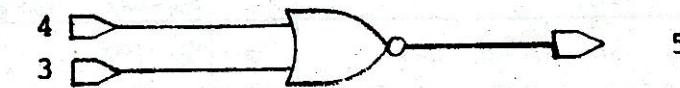
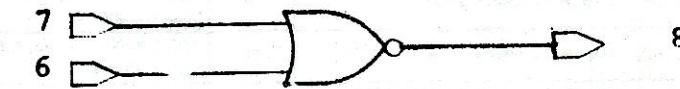
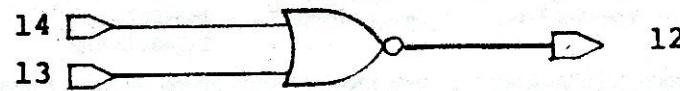
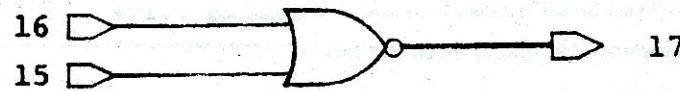
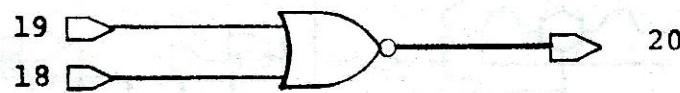
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time.

PIN CONNECTIONS:

22 + 5 Volts, 19 ma.

21 Ground



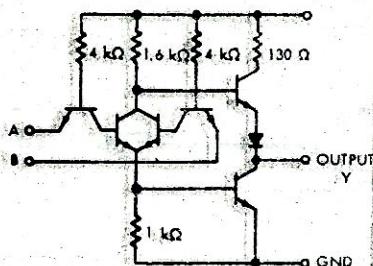
LOADING RULES: Inputs require 1 load
Outputs can drive 10 loads

Propagation delay is 10 ns

CIRCUIT TYPES SN5402, SN7402

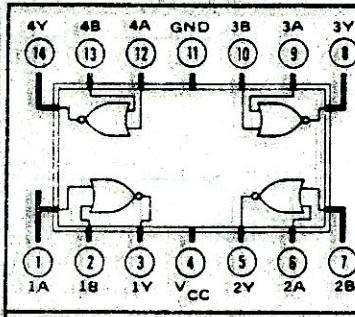
QUADRUPLE 2-INPUT POSITIVE NOR GATES

schematic (each gate)

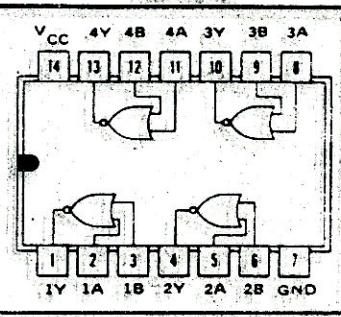


NOTE: Component values shown are nominal.

**W FLAT PACKAGE
(TOP VIEW)**



**J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)**



positive logic: $Y = \bar{A} + \bar{B}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V _{CC} : SN5402 Circuits	4.5	5	5.5	V
SN7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T _A : SN5402 Circuits	-55	26	125	°C
SN7402 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ^t	MIN	TYP [‡]	MAX	UNIT
V _{in(1)} Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	8			2		V
V _{in(0)} Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	9			0.8		V
V _{out(1)} Logical 1 output voltage	9	V _{CC} = MIN, V _{in} = 0.8 V, I _{load} = -400 μA	2.4	3.3		V
V _{out(0)} Logical 0 output voltage	10	V _{CC} = MIN, V _{in} = 2 V, I _{sink} = .16 mA	0.22	0.4		V
I _{in(0)} Logical 0 level input current (each input)	11	V _{CC} = MAX, V _{in} = 0.4 V		-1.6		mA
I _{in(1)} Logical 1 level input current (each input)	12	V _{CC} = MAX, V _{in} = 2.4 V V _{CC} = MAX, V _{in} = 5.5 V		40		μA
I _{OS} Short-circuit output current [§]	13	V _{CC} = MAX	SN5402	-20	-55	mA
			SN7402	-18	-55	
I _{CC(0)} Logical 0 level supply current	14	V _{CC} = MAX, V _{in} = 5 V		14	27	mA
I _{CC(1)} Logical 1 level supply current	14	V _{CC} = MAX, V _{in} = 0		8	16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pd0} Propagation delay time to logical 0 level	65	C _L = 15 pF, R _L = 400 Ω		8	15	ns
t _{pd1} Propagation delay time to logical 1 level	65	C _L = 15 pF, R _L = 400 Ω	12	22		ns

^t For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

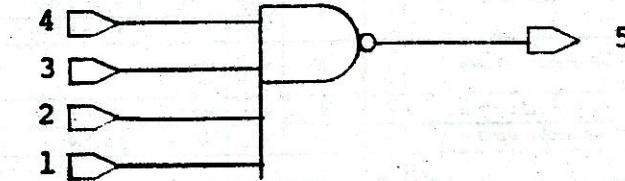
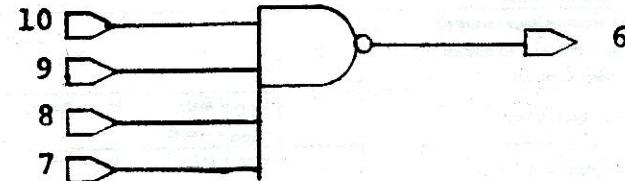
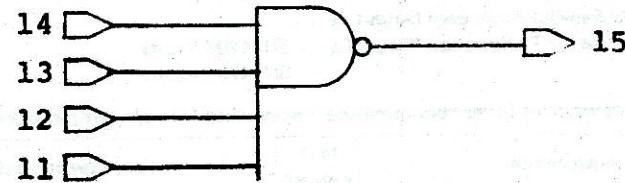
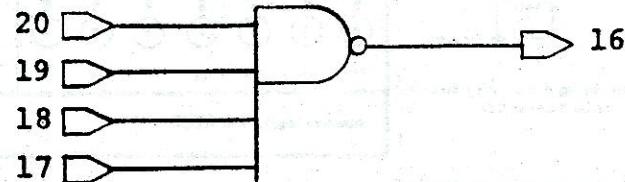
[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time.

PIN CONNECTIONS:

22 +5 Volts, 18 ma.

21 Ground

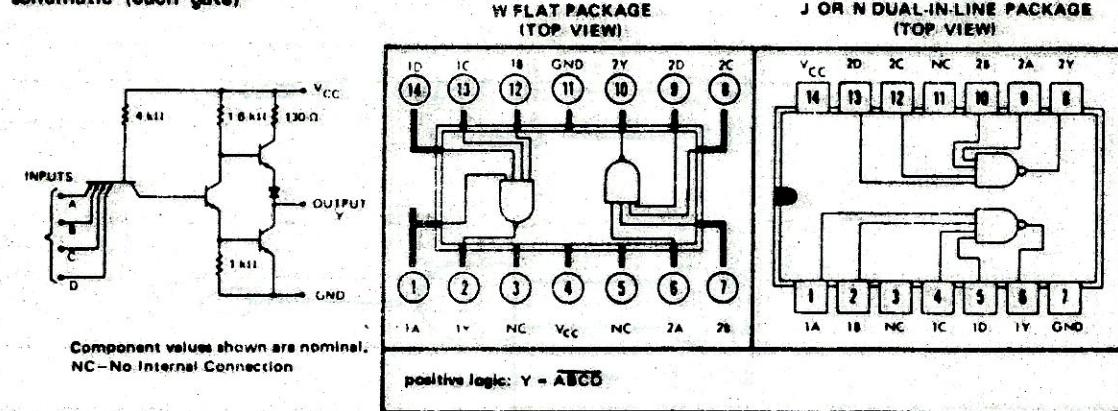


LOADING RULES: Inputs require 1.25 loads (1 if non-H series)
Outputs can drive 12.5 loads (10 if non-H series)

Propagation Delay is 6 ns (10ns if non-H series)

CIRCUIT TYPES SN5420, SN7420 DUAL 4-INPUT POSITIVE NAND GATES

schematic (each gate)



recommended operating conditions

Supply Voltage V_{CC}: SN5420 Circuits

SN7420 Circuits

Normalized Fan-Out From Each Output, N:

Operating Free-Air Temperature Range, T_A: SN5420 Circuits

SN7420 Circuits

	MIN	NOM	MAX	UNIT
	4.5	5	5.5	V
	4.75	5	5.25	V
			10	
	-55	25	125	°C
	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS ¹	MIN	TYP ²	MAX	UNIT
V _{in(1)} Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1			2		V
V _{in(0)} Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2			0.8		V
V _{out(1)} Logical 1 output voltage	2	V _{CC} = MIN, V _{in} = 0.8 V, I _{load} = -400 μA	2.4	3.3		V
V _{out(0)} Logical 0 output voltage	1	V _{CC} = MIN, V _{in} = 2 V, I _{sink} = 16 mA	0.22	0.4		V
I _{in(0)} Logical 0 level input current (each input)	3	V _{CC} = MAX, V _{in} = 0.4 V		-1.6		mA
I _{in(1)} Logical 1 level input current (each input)	4	V _{CC} = MAX, V _{in} = 2.4 V V _{CC} = MAX, V _{in} = 5.5 V		40	1	μA mA
I _{OS} Short-circuit output current ³	5	V _{CC} = MAX	SN5420 SN7420	-20 -18	-55 -55	mA
I _{CC(0)} Logical 0 level supply current	6	V _{CC} = MAX, V _{in} = 5 V		6	11	mA
I _{CC(1)} Logical 1 level supply current	6	V _{CC} = MAX, V _{in} = 0		2	4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pd0} Propagation delay time to logical 0 level	65	C _L = 15 pF, R _L = 400 Ω		8	15	ns
t _{pd1} Propagation delay time to logical 1 level	65	C _L = 15 pF, R _L = 400 Ω		12	22	ns

¹ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

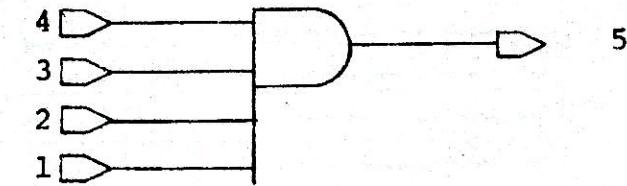
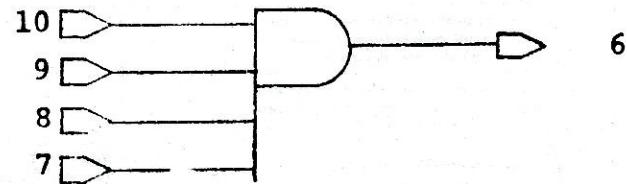
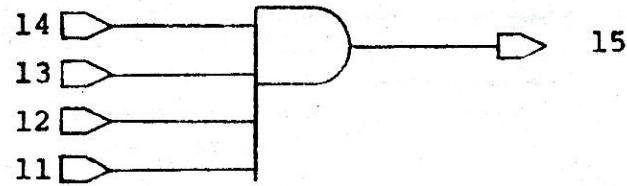
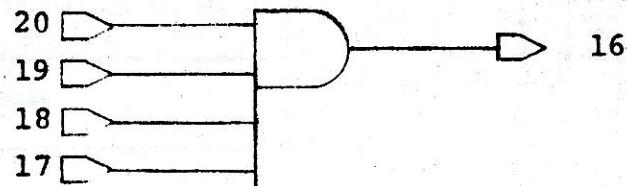
² All typical values are at V_{CC} = 5 V, T_A = 25°C.

³ Not more than one output should be shorted at a time.

PIN CONNECTIONS:

22 +5 Volts, 30 ma.

21 Ground

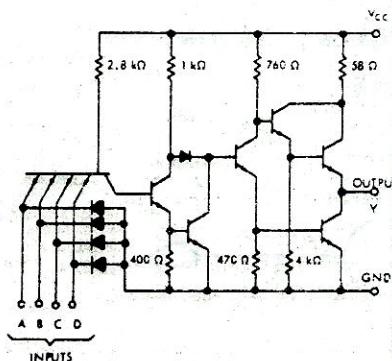


LOADING RULES: Inputs require 1.25 load (1 if non-H series)
Outputs can drive 12.5 loads (10 if non-H series)

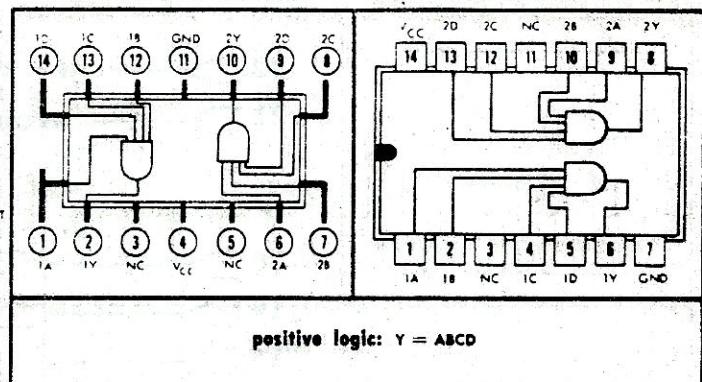
Propagation Delay is 8 ns (10 ns if non-H series)

CIRCUIT TYPES SN54H21, SN74H21 DUAL 4-INPUT POSITIVE AND GATES

schematic (each gate)



W
FLAT PACKAGE (TOP VIEW)



positive logic: $Y = ABCD$

- NOTES: 1. Component values shown are nominal
2. NC — No internal connection

recommended operating conditions

Supply Voltage V_{CC} : SN54H21 Circuits	4.5	5	5.5	V
SN74H21 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A : SN54H21 Circuits	-35	25	725	°C
SN74H21 Circuits	0	25	70	°C

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
		10	
-35	25	725	°C
0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{IO(H)}$ Logical 1 input voltage required at all input terminals to ensure logical 1 level at output	14			2		V
$V_{IO(L)}$ Logical 0 input voltage required at any input terminal to ensure logical 0 level at output	15			0.8		V
$V_{O(H)}$ Logical 1 output voltage	14	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $I_{load} = -500\text{ }\mu\text{A}$	2.4			V
$V_{O(L)}$ Logical 0 output voltage	15	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8\text{ V}$, $I_{load} = 20\text{ mA}$	0.4			V
I_{IH} Logical 0 level input current (each input)	16	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{ V}$	-2			mA
I_{IH} Logical 1 level input current (each input)	17	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{ V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{ V}$	50			mA
I_{OS} Short-circuit output current‡	18	$V_{CC} = \text{MAX}$, $V_{in} = 4.5\text{ V}$	-40		-100	mA
$I_{CC(0)}$ Logical 0 level supply current	19	$V_{CC} = \text{MAX}$, $V_{in} = 0$	20	32		mA
$I_{CC(1)}$ Logical 1 level supply current	19	$V_{CC} = \text{MAX}$, $V_{in} = 4.5\text{ V}$	12	20		mA

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD} Propagation delay time to logical 0 level	74	$C_L = 25\text{ pF}$, $R_L = 280\text{ }\Omega$	8.8	12		ns
t_{PD} Propagation delay time to logical 1 level	74	$C_L = 25\text{ pF}$, $R_L = 280\text{ }\Omega$	7.6	12		ns

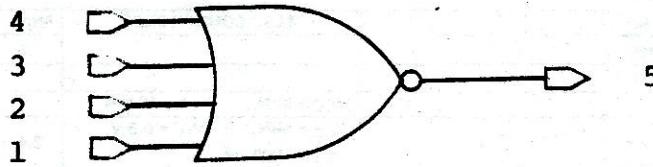
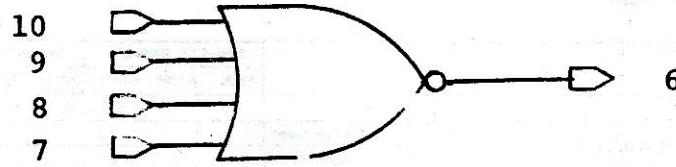
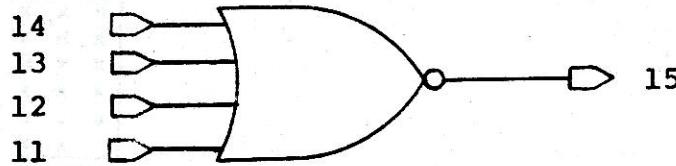
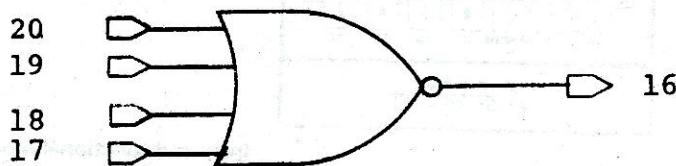
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.

§All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

22 + 5V @ 38 mA max.

21 Ground



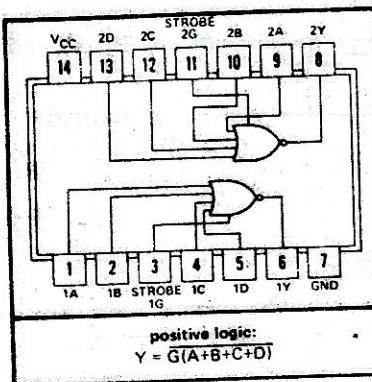
Inputs: 1 load each

Outputs: 10 loads each

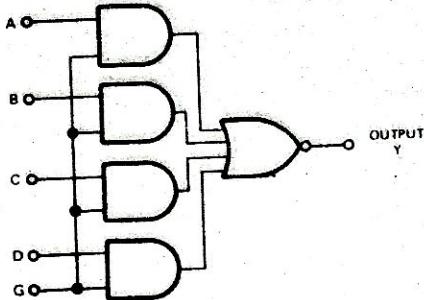
Typical averaged propagation delay: 10 ns (22 ns max.)

CIRCUIT TYPES SN5423, SN5425, SN7423, SN7425 DUAL 4-INPUT NOR GATES WITH STROBE

SN5425, SN7425
J OR N DUAL-IN-LINE OR
W FLAT PACKAGES (TOP VIEW)†



logic and functional block diagram (each gate)



TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	L	H	

Expander inputs are open.
 H = high level, L = low level, X = irrelevant

recommended operating conditions

	SN5423, SN5425			SN7423, SN7425			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20	20		
	Low logic level			10	10		
Operating free-air temperature range, T_A	-55	25	125	0	25	70	°C

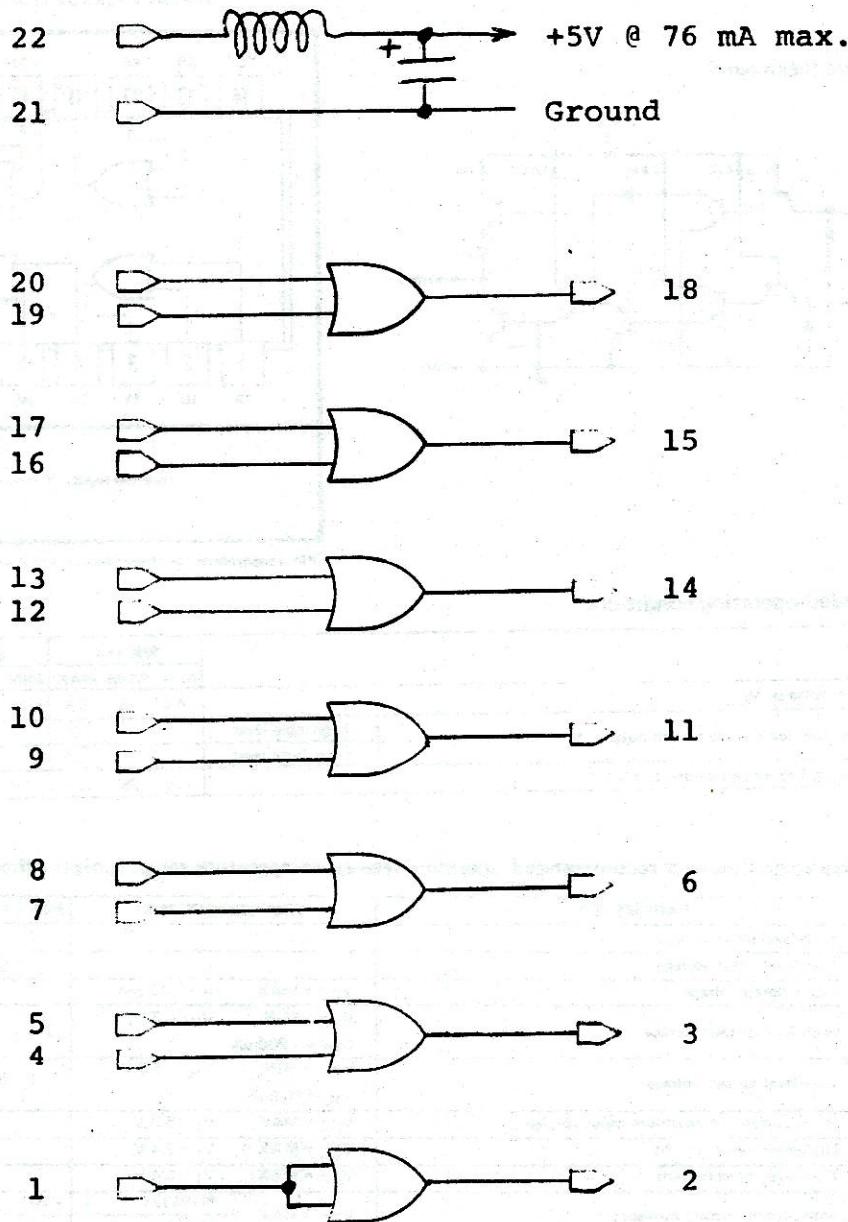
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage			2			V
V_{IL} Low-level input voltage				0.8		V
V_I Input clamp voltage	$V_{CC} = \text{MIN}$,	$I_I = -12 \text{ mA}$		-1.5		V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IL} = 0.8 \text{ V}$,	2.4	3.3		V
I_{OL} Low-level output voltage	$I_{OH} = -800 \mu\text{A}$					
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$,	$V_{IH} = 2 \text{ V}$,	0.22	0.4		V
I_I Input current at maximum input voltage	$I_{OL} = 16 \text{ mA}$			1		mA
I_{IH} High-level input current	data inputs			40		
	strobe inputs	$V_{CC} = \text{MAX}$,	$V_I = 2.4 \text{ V}$	160		μA
I_{IL} Low-level input current	data inputs			-1.6		
	strobe inputs	$V_{CC} = \text{MAX}$,	$V_I = 0.4 \text{ V}$	-6.4		mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$		-20	-55		mA
I_{CCH} Supply current, high-level output	$V_{CC} = \text{MAX}$,	All inputs at 0 V	8	16		mA
I_{CCL} Supply current, low-level output	$V_{CC} = \text{MAX}$,	All inputs at 5 V	10	19		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and \bar{X} are open.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.



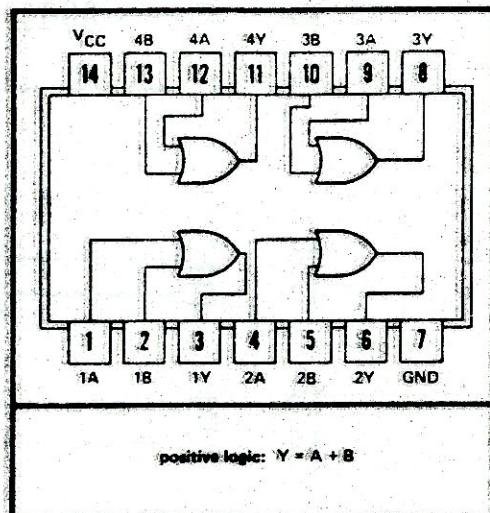
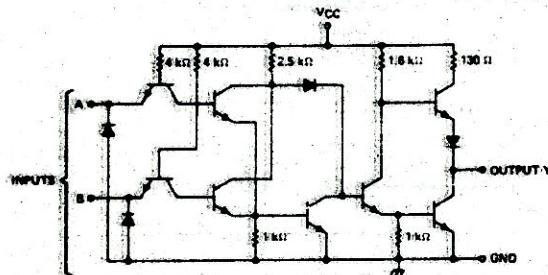
Inputs: 1 load each (except buffer: 2 loads)

Outputs: 10 loads each

Typical averaged propagation delay: 12 ns

CIRCUIT TYPES SNS432, SN7432 QUADRUPLE 2-INPUT POSITIVE-OR GATES

schematic (each gate)



[†]Pin assignments for these circuits are the same for all packages.

recommended operating conditions

	SN5432			SN7432			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N		High logic level		20		20	
		Low logic level		10		10	
Operating free-air temperature, T _A	-55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V _{IH} High-level input voltage		2			V
V _{IL} Low-level input voltage			0.8		V
V _I Input clamp voltage	V _{CC} = MAX, I _I = -12 mA			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, I _{OH} = -800 μA	2.4	3.3		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 16 mA	0.22	0.4		V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V	1			mA
I _{IIH} High-level input current	V _{CC} = MAX, V _I = 2.4 V		40		μA
I _{IIL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V		-1.6		mA
I _{OS} Short-circuit output current [§]	V _{CC} = MAX	-20	-55		mA
I _{ICCH} Supply current, high-level output	V _{CC} = MAX, See Note 2	15	22		mA
I _{ICCL} Supply current, low-level output	V _{CC} = MAX, See Note 3	23	38		mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time.

NOTES: 2. I_{ICCH} is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.

3. I_{ICCL} is measured with both inputs of all gates grounded, and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

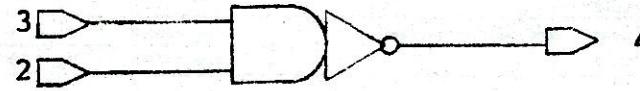
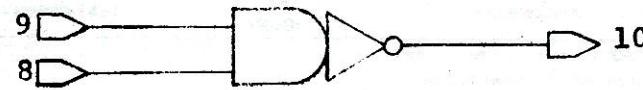
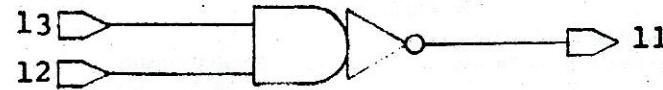
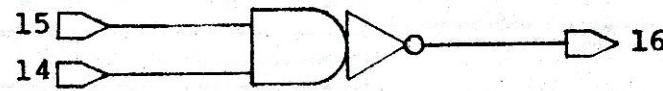
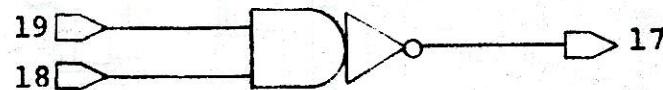
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL} Propagation delay time, high-to-low-level output	C _L = 15 pF, R _L = 400 Ω	14	22	ns	
t _{PLH} Propagation delay time, low-to-high-level output		10	15	ns	

PIN CONNECTIONS:

22 +5 Volts, 34 ma.

21 Ground

20

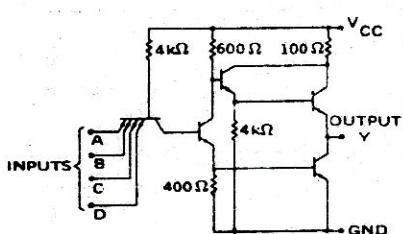
1000
1 +5 Volts

LOADING RULES: Each input requires 1.25 loads.
Each output can drive 37.5 loads.

Propagation Delay is 6 ns.

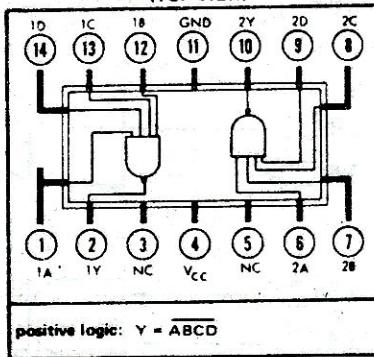
CIRCUIT TYPES SN5440, SN7440 DUAL 4-INPUT POSITIVE NAND BUFFERS

schematic (each gate)

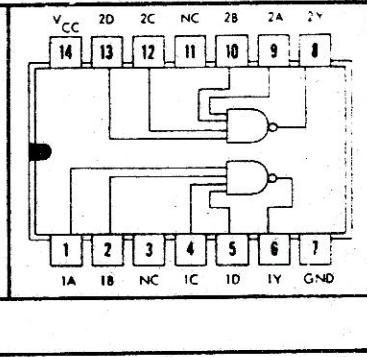


Component values shown are nominal.
NC—No Internal Connection

**W FLAT PACKAGE
(TOP VIEW)**



**J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)**



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : SN5440 Circuits	4.5	5	5.5	V
SN7440 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output, N			30	
Operating Free-Air Temperature Range, T_A : SN5440 Circuits	-55	25	125	°C
SN7440 Circuits	0	25	70	°C

electrical characteristics (over recommended free-air temperature range unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS [†]		MIN	TYP [‡]	MAX	UNIT
		V _{CC} = MIN,	V _{in} = 0.8 V,				
V _{in(1)} Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	I _{load} = -1.2 mA		2			V
V _{in(0)} Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2				0.8		V
V _{out(1)} Logical 1 output voltage	2	V _{CC} = MIN, V _{in} = 0.8 V, I _{load} = -1.2 mA		2.4	3.3		V
V _{out(0)} Logical 0 output voltage	1	V _{CC} = MIN, V _{in} = 2 V, I _{sink} = 48 mA			0.28	0.4	V
I _{in(0)} Logical 0 level input current (each input)	3	V _{CC} = MAX, V _{in} = 0.4 V			-1.6		mA
I _{in(1)} Logical 1 level input current (each input)	4	V _{CC} = MAX, V _{in} = 2.4 V V _{CC} = MAX, V _{in} = 5.5 V			40		μA
I _{OS} Short-circuit output current §	5	V _{CC} = MAX		SN5440	-20	-70	mA
I _{CC(0)} Logical 0 level supply current	6	V _{CC} = MAX, V _{in} = 5 V		SN7440	-18	-70	mA
I _{CC(1)} Logical 1 level supply current	6	V _{CC} = MAX, V _{in} = 0			17	27	mA
					4	8	mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, $N = 30$

PARAMETER	TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		C _L	R _L				
t _{pd0} Propagation delay time to logical 0 level	65	C _L = 15 pF,	R _L = 133 Ω	8	15		ns
t _{pd1} Propagation delay time to logical 1 level	65	C _L = 15 pF,	R _L = 133 Ω	13	22		ns

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

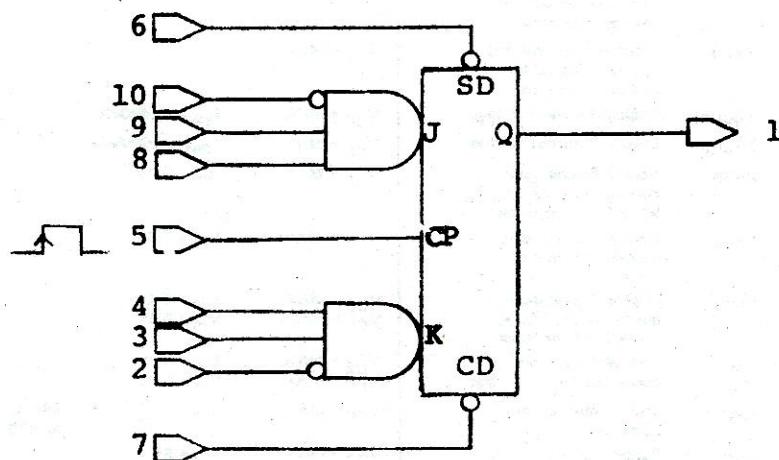
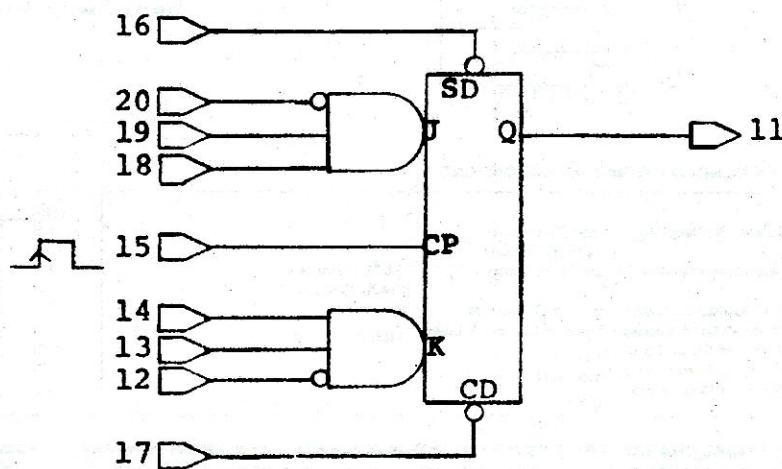
[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

PIN CONNECTIONS:

22 +5 Volts, 26 ma.

21 Ground



LOADING RULES: J, K, J, K, CP inputs require 1 load.
SD or CD require 2 loads.
Output can drive 10 loads.

Maximum Clock Frequency is 35 MHz.
Minimum Clock Pulse Width is 20 ns.
Propagation Delay is 22 ns.

Note: "CP" must be low when asserting "SD" or "CD"

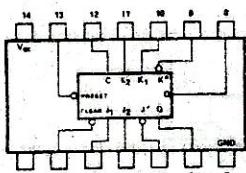
7470

DESCRIPTION

The S5470/N7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and \bar{Q} outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The S5470/N7470 flip-flop is ideally suited for medium- and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

A,F PACKAGE**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} :	S5470 Circuits	4.5	5	5.5	V
	N7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A :	S5470 Circuits	-65	25	125	°C
	N7470 Circuits	0	25	70	°C
Normalized Fanout from each Output, N		5		10	ns
Clock Pulse Transition Time to Logical 1 Level, t_1 (clock)		20		150	ns
Width of Clock Pulse, t_p (clock)		25		ns	ns
Width of Preset Pulse, t_p (preset)		25		ns	ns
Width of Clear Pulse, t_p (clear)		25		ns	ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	TEST CONDITIONS*			UNIT
		MIN	TYP**	MAX	
$V_{in(1)}$	$V_{CC} = \text{MIN}$		2		V
$V_{in(0)}$	$V_{CC} = \text{MIN}$		0.8		V
$V_{out(1)}$	$V_{CC} = \text{MIN}$, $I_{load} = -400\mu\text{A}$	2.4	3.5		V
$V_{out(0)}$	$V_{CC} = \text{MIN}$, $I_{sink} = 16\text{mA}$	0.22	0.4		V
$I_{in(0)}$	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$		-1.6		mA
$I_{in(0)}$	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$		-3.2		mA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$		40		mA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$		1		mA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$		80		mA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$		1		mA
I_{OS}	$V_{CC} = \text{MAX}$, $V_{in} = 0$	S5470 N7470	-20 -18	-75 -75	mA
I_{CC}	$V_{CC} = \text{MAX}$, $V_{in} = 5\text{V}$		13	26	mA

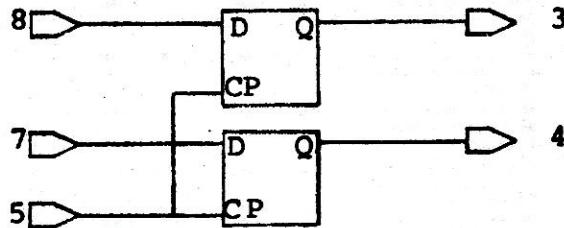
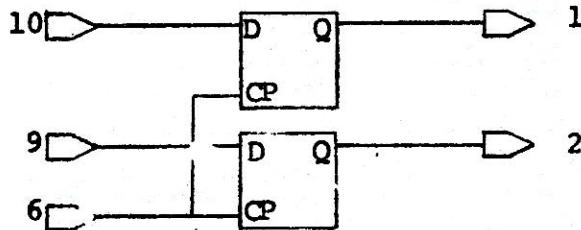
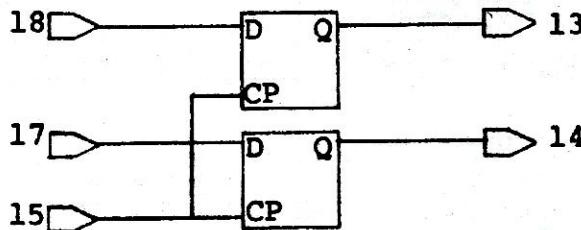
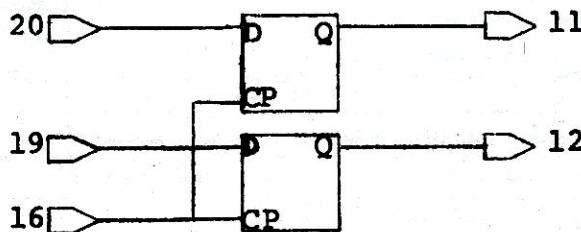
SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST CONDITIONS	TEST CONDITIONS			UNIT
		MIN	TYP	MAX	
f_{clock}	$C_L = 15\text{pF}$, $R_L = 400\Omega$		15	35	MHz
t_{setup}	$C_L = 15\text{pF}$, $R_L = 400\Omega$		10	20	ns
t_{hold}	$C_L = 15\text{pF}$, $R_L = 400\Omega$		0	5	ns
t_{pd1}	$C_L = 15\text{pF}$, $R_L = 400\Omega$			50	ns
t_{pd0}	$C_L = 15\text{pF}$, $R_L = 400\Omega$			50	ns
t_{pd1}	$C_L = 15\text{pF}$, $R_L = 400\Omega$		10	27	ns
t_{pd0}	$C_L = 15\text{pF}$, $R_L = 400\Omega$		10	18	ns

PIN CONNECTIONS:

22 +5 Volts, 64 ma.

21 Ground



LOADING RULES: D inputs require 2 loads.

CP inputs require 2 loads.

Note that pin 5 is connected to 2 CP inputs and thus requires 4 loads.

Q outputs can drive 10 loads.

Propagation Delay is 30 ns.

Note: These elements are not flip-flops. The "Q" output follows all changes in the "D" input while "CP" = 1 and retains (latches) the input value present when "CP" falls.

7475

DESCRIPTION

The SS475B/N7475B is a monolithic, quadruple, bistable latch with complementary Q and \bar{Q} outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is returned at the Q output until the clock is permitted to go high.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units.

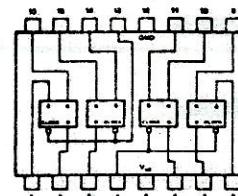
TRUTH TABLE

LOGIC (Each Latch)		
t_n	t_{n+1}	NOTES:
D	Q	1. t_n = bit time before clock pulse.
1	1	2. t_{n+1} = bit time after clock pulse
0	0	3. These voltages are with respect to network ground terminal.

- 1. t_n = bit time before clock pulse.
- 2. t_{n+1} = bit time after clock pulse
- 3. These voltages are with respect to network ground terminal.

PIN CONFIGURATIONS

B PACKAGE



RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): S5475 Circuits N7475 Circuits	4.5	5	5.5	V
Normalized Fan-Out from Outputs	4.75	5	6.25	V
Operating Free-Air Temperature Range, T_A : S5475 Circuits N7475 Circuits	-55	25	125	°C
	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	$V_{CC} = \text{MIN}$		2		V
$V_{in(0)}$	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	$V_{CC} = \text{MIN}$, $I_{load} = -400\mu A$		2.4		V
$V_{out(0)}$	$V_{CC} = \text{MIN}$, $I_{sink} = 16mA$			0.4	V

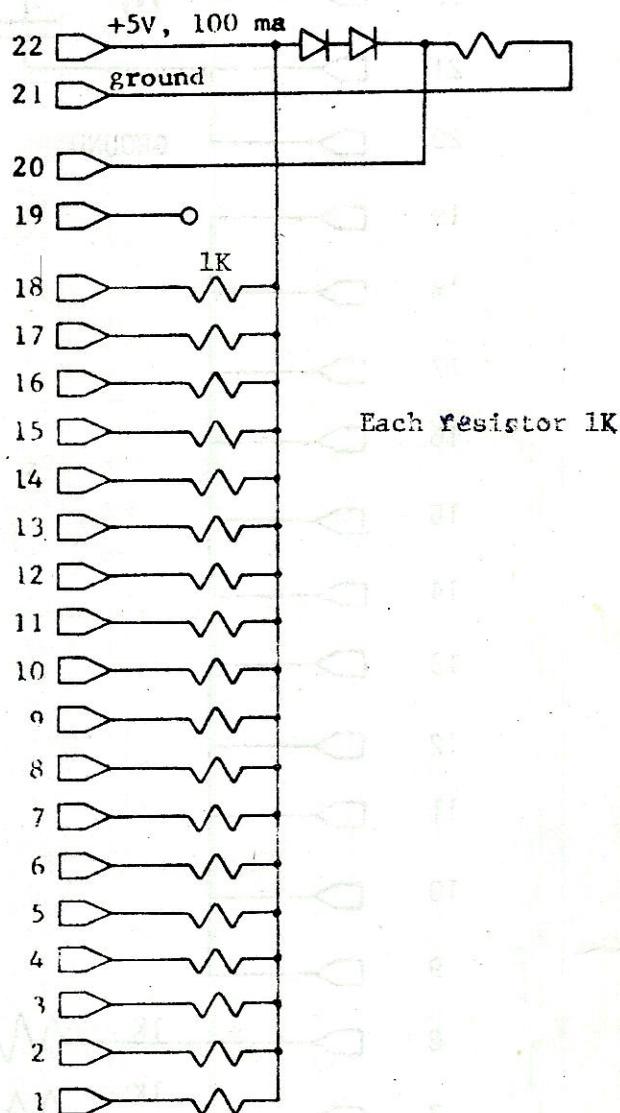
ELECTRICAL CHARACTERISTICS (Cont'd)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{in(0)}$	$V_{CC} = \text{MAX}$, $V_{in} = 0.4V$			-3.2	mA
$I_{in(0)}$	$V_{CC} = \text{MAX}$, $V_{in} = 0.4V$			-6.4	mA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 2.4V$			80	μA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 5.5V$		1		μA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 2.4V$		100		μA
$I_{in(1)}$	$V_{CC} = \text{MAX}$, $V_{in} = 5.5V$		1		μA
I_{OS}	$V_{CC} = \text{MAX}$, $V_{out} = 0$ S5475 N7475	-20	-75		mA
I_{OS}	$V_{CC} = \text{MAX}$, $V_{out} = 0$ N7475	-18	-75		mA
I_{CC}	$V_{CC} = \text{MAX}$, $N7475$	32	46		mA
I_{CC}	$V_{CC} = \text{MAX}$, $N7476$	32	53		mA

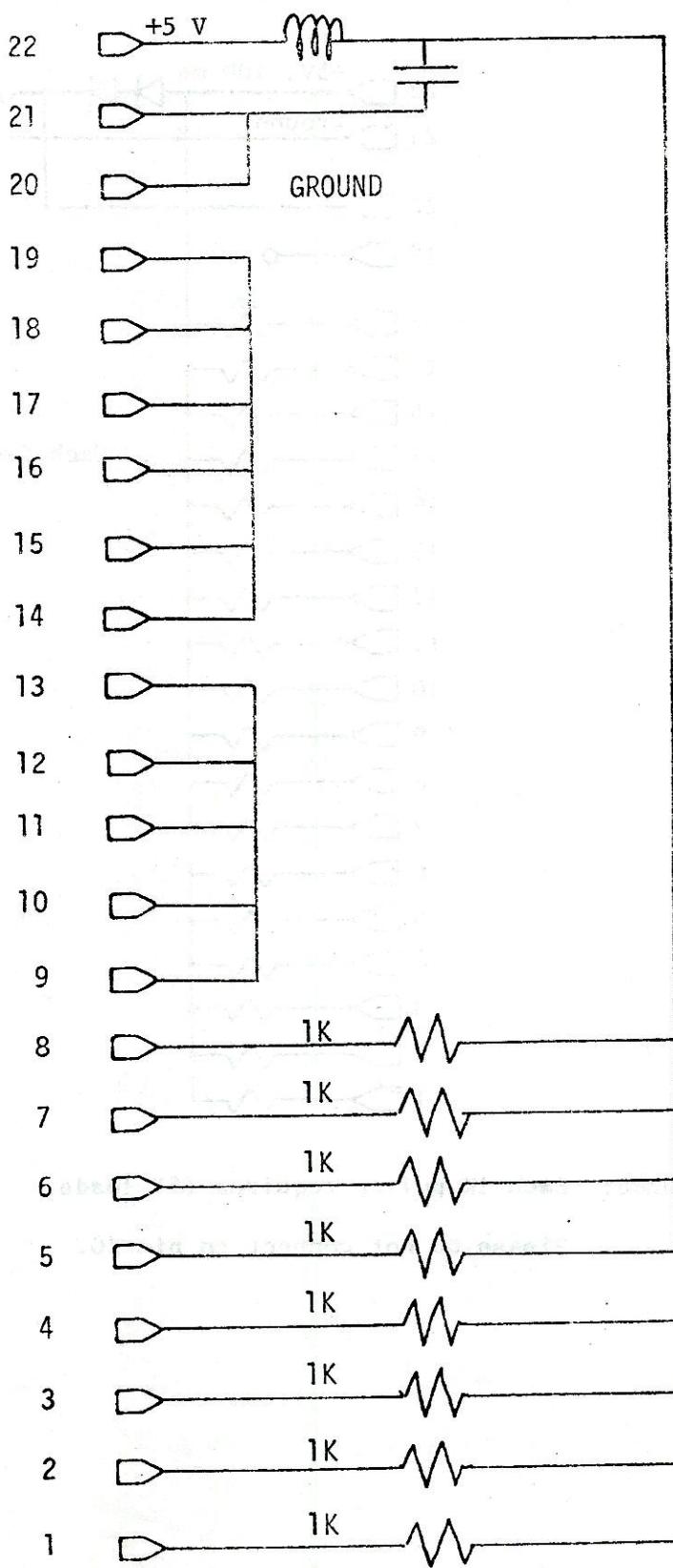
SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER	TEST CONDITIONS NOTE A	MIN	TYP	MAX	UNIT
t_{setup1}	$C_L = 15pF$, $R_L = 400\Omega$		7	20	ns
t_{setup0}	$C_L = 15pF$, $R_L = 400\Omega$		14	20	ns
t_{hold1}	$C_L = 15pF$, $R_L = 400\Omega$	0	15 ^b		ns
t_{hold0}	$C_L = 15pF$, $R_L = 400\Omega$	0	6 ^b		ns
$t_{pd1(D-Q)}$	$C_L = 15pF$, $R_L = 400\Omega$		16	30	ns
$t_{pd0(D-Q)}$	$C_L = 15pF$, $R_L = 400\Omega$		14	25	ns
$t_{pd1(D-\bar{Q})}$	$C_L = 15pF$, $R_L = 400\Omega$		24	40	ns
$t_{pd0(D-\bar{Q})}$	$C_L = 15pF$, $R_L = 400\Omega$		7	15	ns
$t_{pd1(C-Q)}$	$C_L = 15pF$, $R_L = 400\Omega$		16	30	ns
$t_{pd0(C-Q)}$	$C_L = 15pF$, $R_L = 400\Omega$		7	15	ns
$t_{pd1(C-\bar{Q})}$	$C_L = 15pF$, $R_L = 400\Omega$		16	30	ns
$t_{pd0(C-\bar{Q})}$	$C_L = 15pF$, $R_L = 400\Omega$		7	15	ns

18 1K pullup resistors

BOARD TYPE **600****PIN CONNECTIONS:****LOADING RULES:** Each 1K pullup requires (5) loads.**NOTE:** Please do not connect to pin 20.

PIN CONNECTIONS:

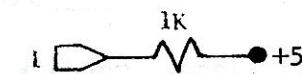
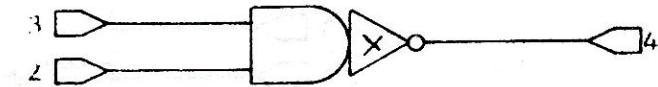
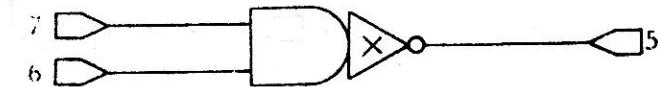
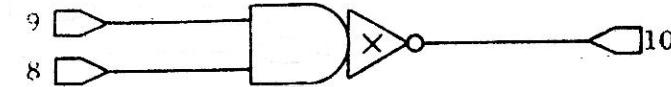
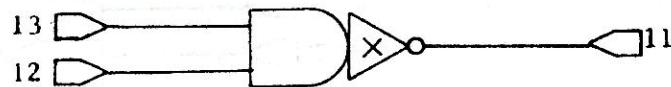
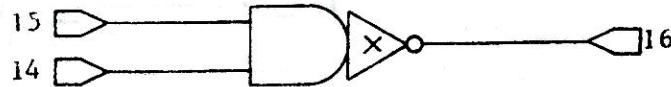
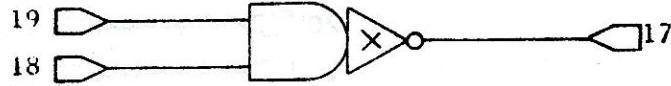


PIN CONNECTIONS:

22 +5 Volts, 24 ma.

21 Ground

20



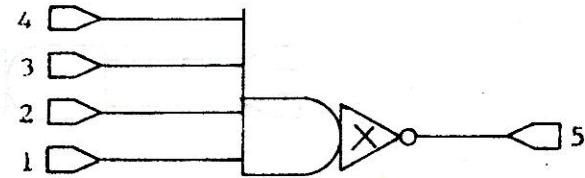
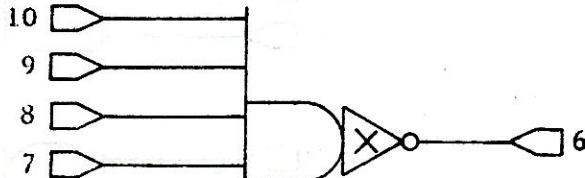
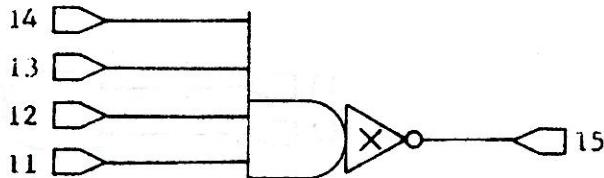
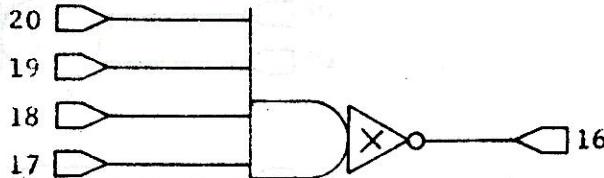
LOADING RULES: Inputs are (1) load. Outputs drive up to (25) loads, but at least (5) loads of external pullup is required. Wired logic is permitted up to about 100 outputs in parallel with no reduction in driving capability of (25).

USES: Very large buses. Output will sink about 100 ma. to ground, making the device useful for driving lamps, relays, etc. The load may be returned to voltages as high as +12. Inductive loads require a diode connected across the load with the cathode at the positive supply end.

PIN CONNECTIONS:

22 +5 Volts, 16 ma.

21 Ground



LOADING RULES: Inputs are (1) load. Outputs drive up to (25) loads, but at least (5) loads of external pullup is required. Wired logic is permitted up to about 100 outputs in parallel with no reduction in driving capability of (25).

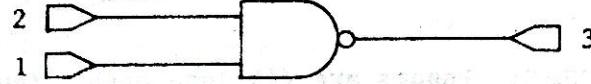
USES: Output will sink about 100 ma. to ground, making the device useful for driving lamps, relays, etc. The load may be returned to voltages as high as +12. Inductive loads require a diode connected across the load with the cathode at the positive supply end.

4 2-input and 4 1-input DTL NAND gates

PIN CONNECTIONS:

22 +5 Volts, 12.8 ma.

21 Ground

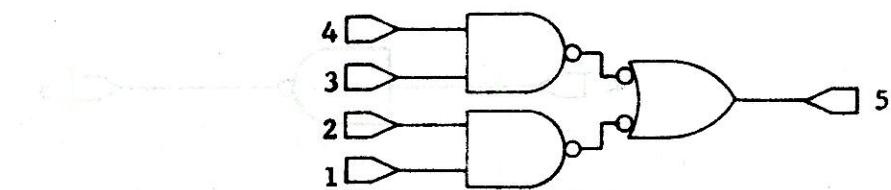
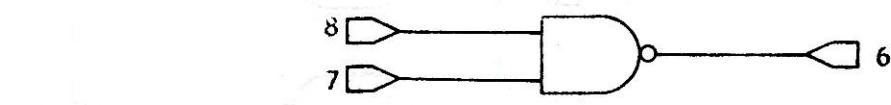
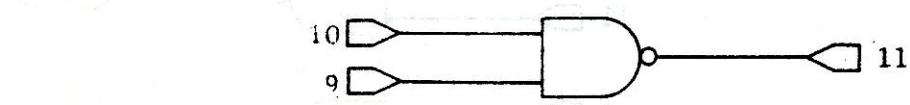
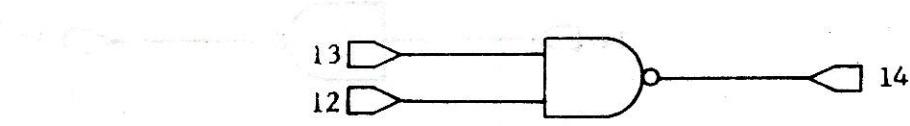
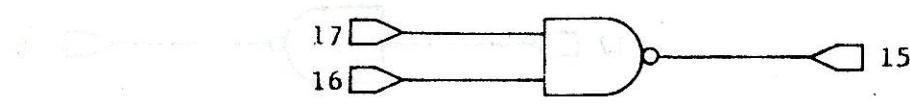


LOADING RULES: Inputs are (1) load, outputs are (8) loads. For each output in a wired logic connection subtract 5/6 load [Example: 7 outputs wired together can drive $8 - 6(5/6) = 3$ loads].

PIN CONNECTIONS:

22 +5 Volts, 12.8 ma.

21 Ground



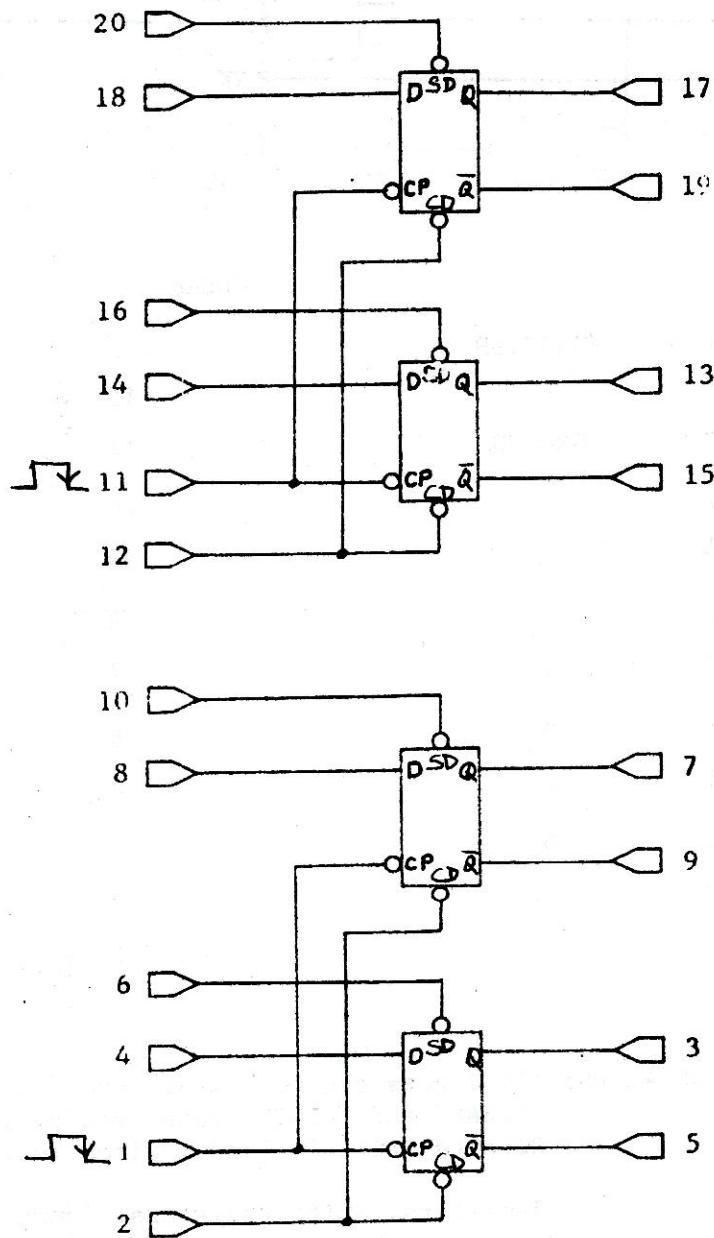
LOADING RULES: Inputs are (1) load each. Outputs will drive up to (8) loads. Wired logic is permitted; for each output in a wired logic connection after the first subtract (5/6) load from (8) loads.

USES: Combinational Networks.

PIN CONNECTIONS:

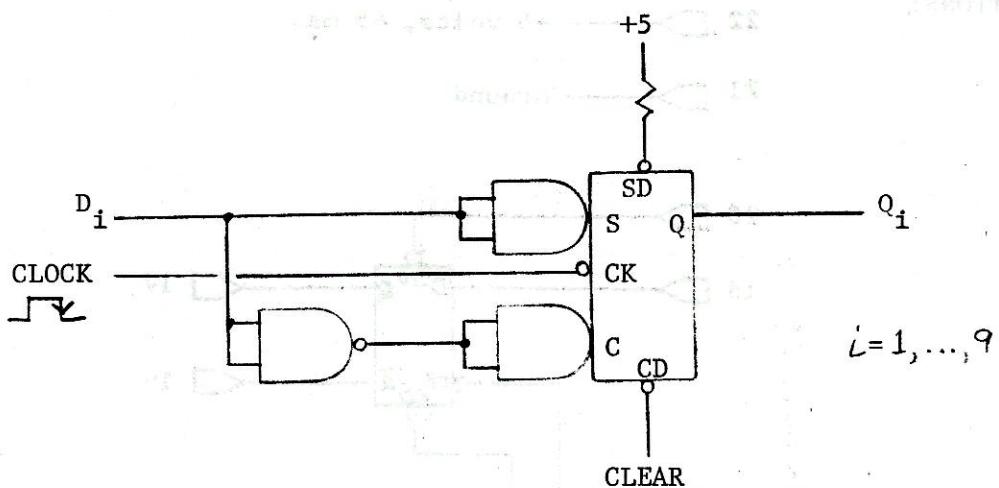
22 +5 Volts, 45 ma.

21 Ground



LOADING RULES: For each flip-flop, the D , CP , direct set and direct clear inputs are (2) loads each. Outputs can drive up to (10) loads and wired logic is not permitted.

USES: Buffer Registers, Shift registers, parallel-to-serial and serial-to-parallel converters, state variable storage.



PIN #	FUNCTION	PIN #	FUNCTION
22	+5	12	D ₅
21	GROUND	11	Q ₅
20	D ₁	10	D ₆
19	Q ₁	9	Q ₆
18	D ₂	8	D ₇
17	Q ₂	7	Q ₇
16	D ₃	6	D ₈
15	Q ₃	5	Q ₈
14	D ₄	4	D ₉
13	Q ₄	3	Q ₉
		2	CLEAR (all FFs)
		1	CLOCK (all FFs)

LOADING RULES: All inputs except "CLEAR" and "CLOCK" require 2 loads.
 "CLEAR" and "CLOCK" each require 18 loads.
 Outputs drive 10 loads; wired logic is not permitted.

USES: Registers, Shift registers, Counters

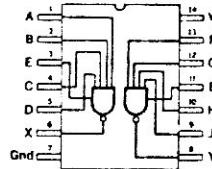
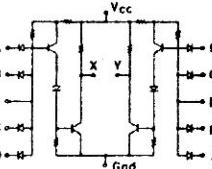
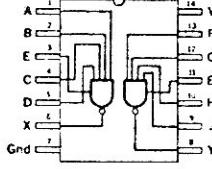
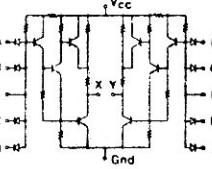
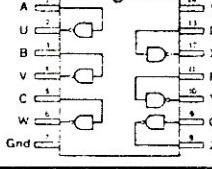
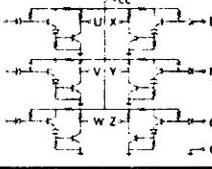
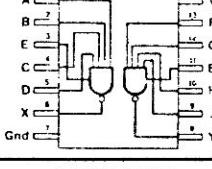
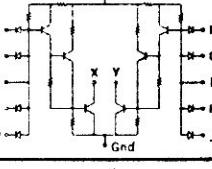
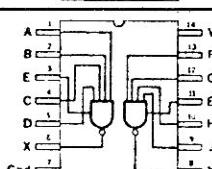
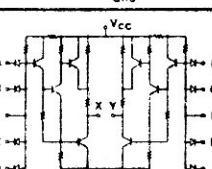
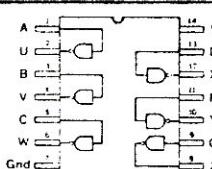
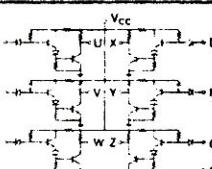
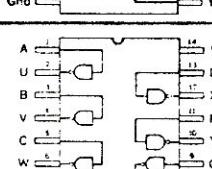
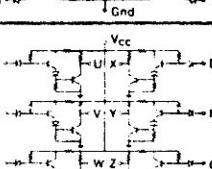
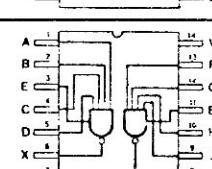
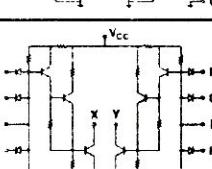
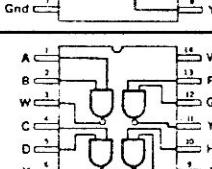
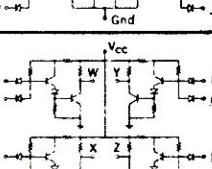
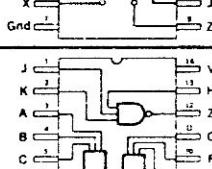
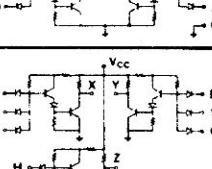
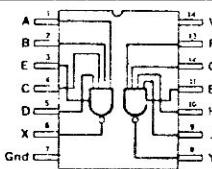
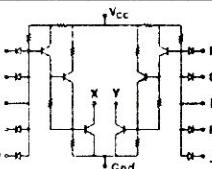
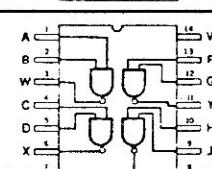
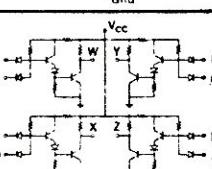
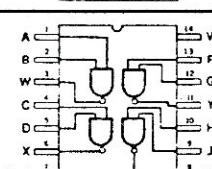
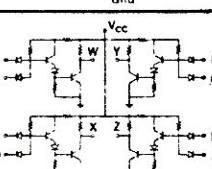
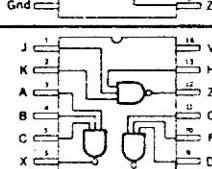
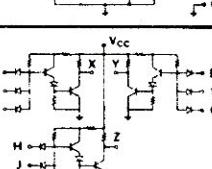
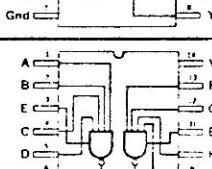
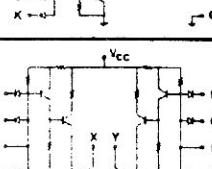
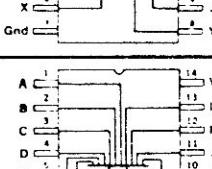
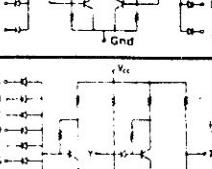
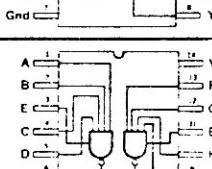
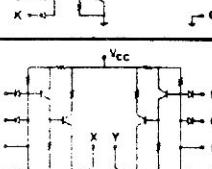
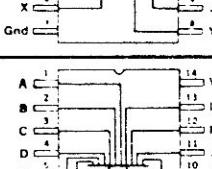
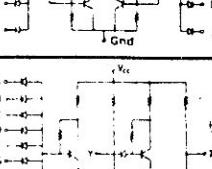
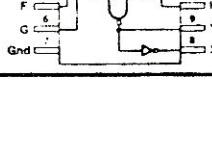
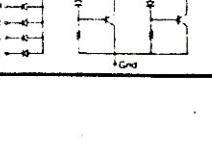
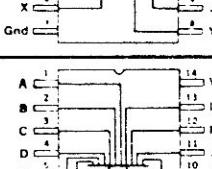
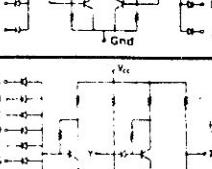
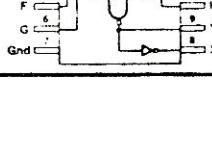
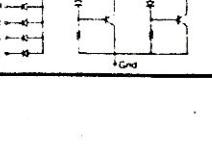
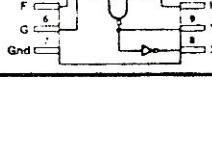
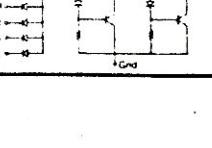
DTL (Diode-Transistor Logic) DIGITAL INTEGRATED CIRCUITS

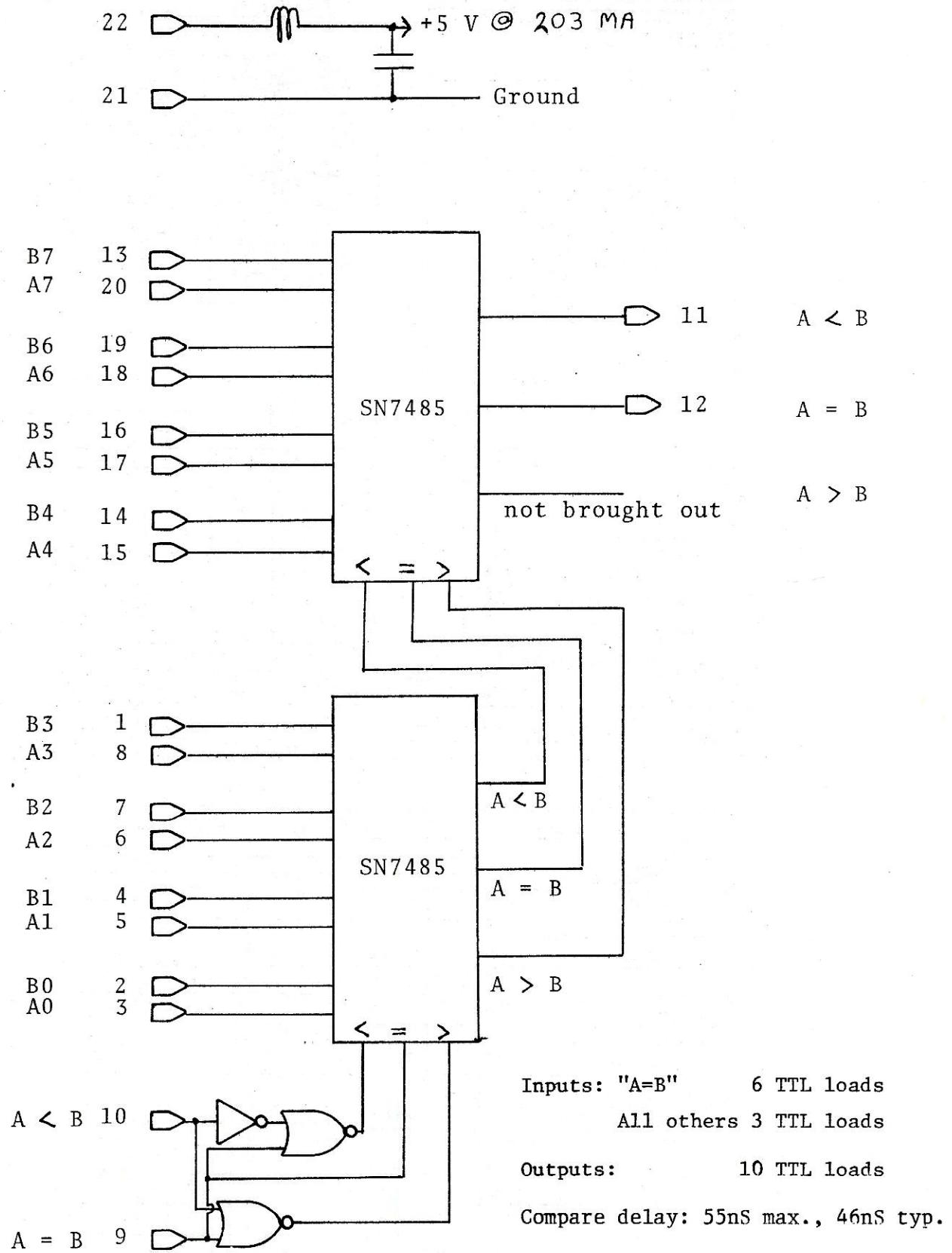
The Stewart-Warner DTL930 Series, available in 4 packages and two temperature ranges, is a highly efficient family of monolithic circuits designed to operate from a single power supply.

Design flexibility is enhanced by the broad selection of elements, choice of high speed or low power circuits, noise immunity/fan-out trade-off and the capability for performing collector logic.

MAXIMUM CIRCUIT RATINGS

Power Supply Voltage — Continuous	8.0 Vdc
Pulsed < 1 second	12.0 Vdc
Input Forward Current	10.0 mAdc
Input Reverse Current	1.0 mAdc
Output Current — Gates, Flip-Flop and One-Shots	30 mAdc
Buffer and Power Gate	100 mAdc
Operating Temperature — Military (1)	-55°C to +125°C
Industrial (2)	0°C to +75°C
Storage Temperature	-65°C to +150°C

FUNCTION	TYPE NO.	PROP. DELAY (ns)	PWR. CONSUMP- TION at 5V (mW)	RATED FAN-OUT	NOISE MARGIN (volts)	LOGIC AND PIN DIAGRAM	CIRCUIT SCHEMATIC
DUAL 4-INPUT NAND GATE	SW930-1	30	8	8	1.0		
	SW930-2	30	8	8	0.8		
	SW961-1	20	12	7	1.0		
	SW961-2	20	12	7	0.8		
DUAL 4-INPUT BUFFER	SW932-1	35	30	25	1.0		
	SW932-2	35	30	25	0.8		
HEX INVERTER	SW936-1	30	8	8	1.0		
	SW936-2	30	8	8	0.8		
	SW937-1	20	12	7	1.0		
	SW937-2	20	12	7	0.8		
DUAL 4-INPUT NAND POWER GATE	SW944-1	25	22	27	1.0		
	SW944-2	25	22	27	0.8		
QUADRUPLE 2-INPUT NAND GATE	SW946-1	30	8	8	1.0		
	SW946-2	30	8	8	0.8		
	SW949-1	20	12	7	1.0		
	SW949-2	20	12	7	0.8		
TRIPLE 3-INPUT NAND GATE	SW962-1	30	8	8	1.0		
	SW962-2	30	8	8	0.8		
	SW963-1	20	12	7	1.0		
	SW963-2	20	12	7	0.8		
DUAL 4-INPUT LAMP DRIVER	SW729-1	—	22	100 mA	1.0		
	SW729-2	—	22	100 mA	0.8		
10-INPUT COM- PLEMENTARY GATE	SW770-1	40	16	8	1.0		
	SW770-2	40	16	8	0.8		
	SW771-1	30	28	7	1.0		
	SW771-2	30	28	7	0.8		



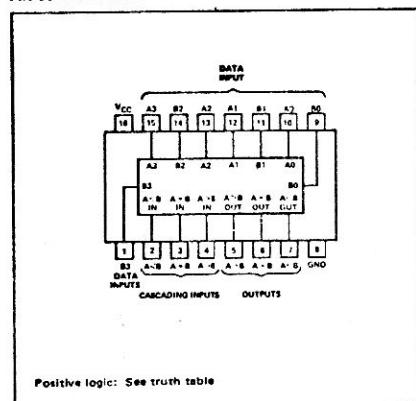
7485

DESCRIPTION

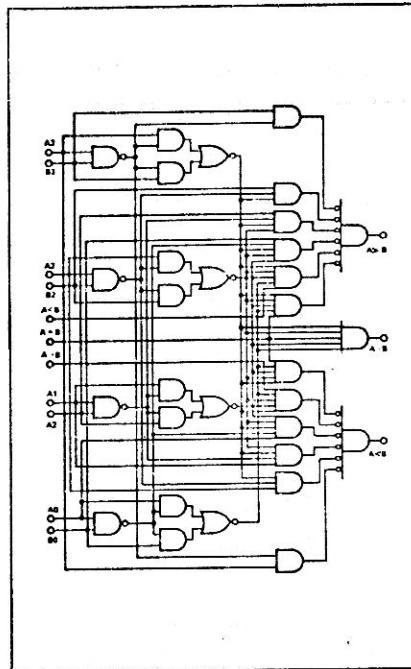
The 55485 and N7485 perform magnitude comparison of straight binary and straight BCD (B421) codes. Three fully decoded decisions about two 4 bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. When cascaded, the total time for comparison is the function of the word length; however, only a two-gate-level delay (12 ns) is added for each four-bit expansion.

These circuits are completely compatible with most TTL and DTL families. Typical average power dissipation is 2.5 milliwatts. The 55485 is characterized for operation over the full military temperature range of -55°C to 125°C; the N7485 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	F	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	H

RECOMMENDED OPERATING CONDITIONS

	55485			N7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N		10			10		
Operating free-air temperature, T _A	-55	125	0	0	70	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*		MIN	TYP**	MAX	UNIT
V _{IH} High-level input voltage			2			V
V _{IL} Low-level input voltage				0.8		V
V _I Input clamp voltage	V _{CC} = MIN, I _I = -12 mA			-1.5		V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA		2.4			V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA			0.4		V
I _I Input current at maximum	V _{CC} = MAX, V _I = 5.5 V			1		mA
I _{IH} High-level input current	A < B, A > B inputs all other inputs	V _{CC} = MAX, V _I = 2.4 V		40		μA
I _{IL} Low-level input current	A < B, A > B inputs all other inputs	V _{CC} = MAX, V _I = 0.4 V		120		mA
I _{OS} Short-circuit output current†	V _{CC} = MAX, V _O = 0	S5455 N7485	-20 -18	-55 -55		mA
I _{CC} Supply current	V _{CC} = MAX, See Note 1		55	88		mA

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any A or B data input	A > B, A < B	1	CL = 15 pF, R _L = 400 Ω, See Figure 1	7			ns
			2		12			
			3		17	26		
			4		23	35		
t _{PHL}	Any A or B data input	A < B, A > B	1		11			ns
			2		15			
			3		20	30		
			4		20	30		
t _{PLH}	A < B or A = B	A > B	1		7	11	ns	
t _{PLH}	A < B or A = B	A > B	1		11	17	ns	
t _{PLH}	A = B	A = B	2		13	20	ns	
t _{PLH}	A = B	A = B	2		11	17	ns	
t _{PLH}	A > B or A = B	A < B	1		7	11	ns	
t _{PLH}	A > B or A = B	A < B	1		11	17	ns	

22 $\rightarrow +5 \text{ V} @ 100 \text{ mA}$

21 \bullet Ground

19 20
18

16 17
15

14 12
13

11 9
10

7 8
6
5

4 1
3
2

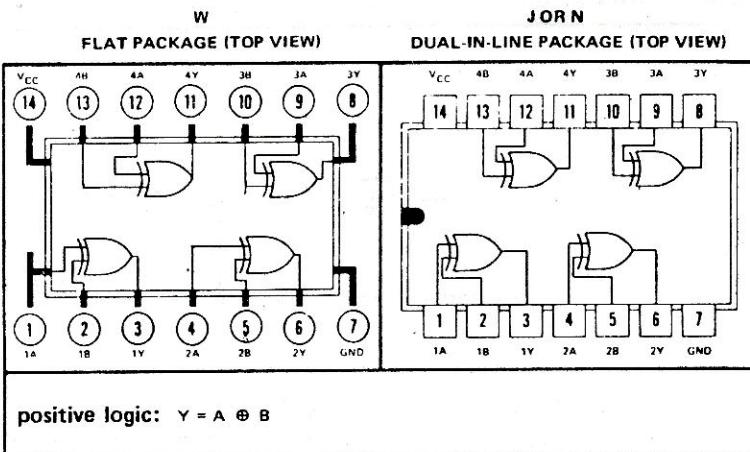
Inputs: 1 TTL load each

Outputs: 10 TTL loads each

- Input-Clamping Diodes Simplify System Design
- Fully Compatible with TTL, DTL, and Other MSI Circuits
- Typical Propagation Delay Times: 12 ns

logic

TRUTH TABLE		
INPUTS	OUTPUT	
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



description

Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\bar{B} + \bar{A}B$. When the input states are complementary, the output goes to a logical 1.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

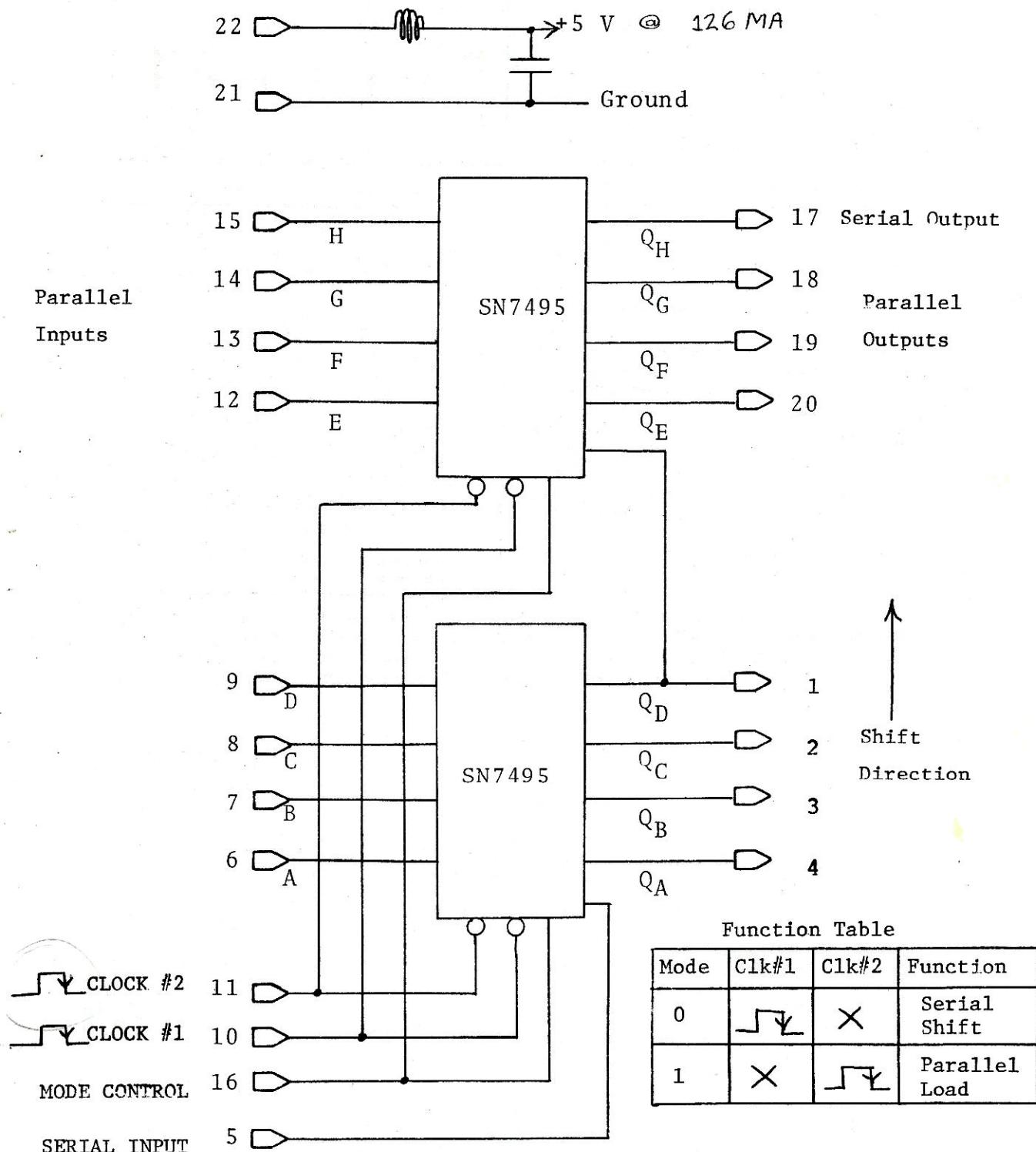
The SN5486 is characterized for operation over the full military temperature range of -55°C to 125°C and the SN7486 is characterized for operation from 0°C to 70°C .

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}	SN5486 Circuits	4.5	5	5.5	V
	SN7486 Circuits	4.75	5	5.25	V
Normalized Fan-out from each output,N:	Logical 0			10	
	Logical 1			20	

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0} Propagation delay time to logical 0 level (other input low)	7	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		11	17	ns
t_{pd1} Propagation delay time to logical 1 level (other input low)	7	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		15	23	ns
t_{pd0} Propagation delay time to logical 0 level (other input high)	7	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		13	22	ns
t_{pd1} Propagation delay time to logical 1 level (other input high)	7	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$		18	30	ns



Inputs: "CLOCK #1", "#2" 2 TTL loads
 "MODE CONTROL" 4 TTL loads
 All others 1 TTL load each

Outputs: Q_D 9 TTL loads; all others 10 TTL loads

Shift direction can be reversed by using Parallel Load mode and connecting each output to the preceding input.

description

This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverters-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

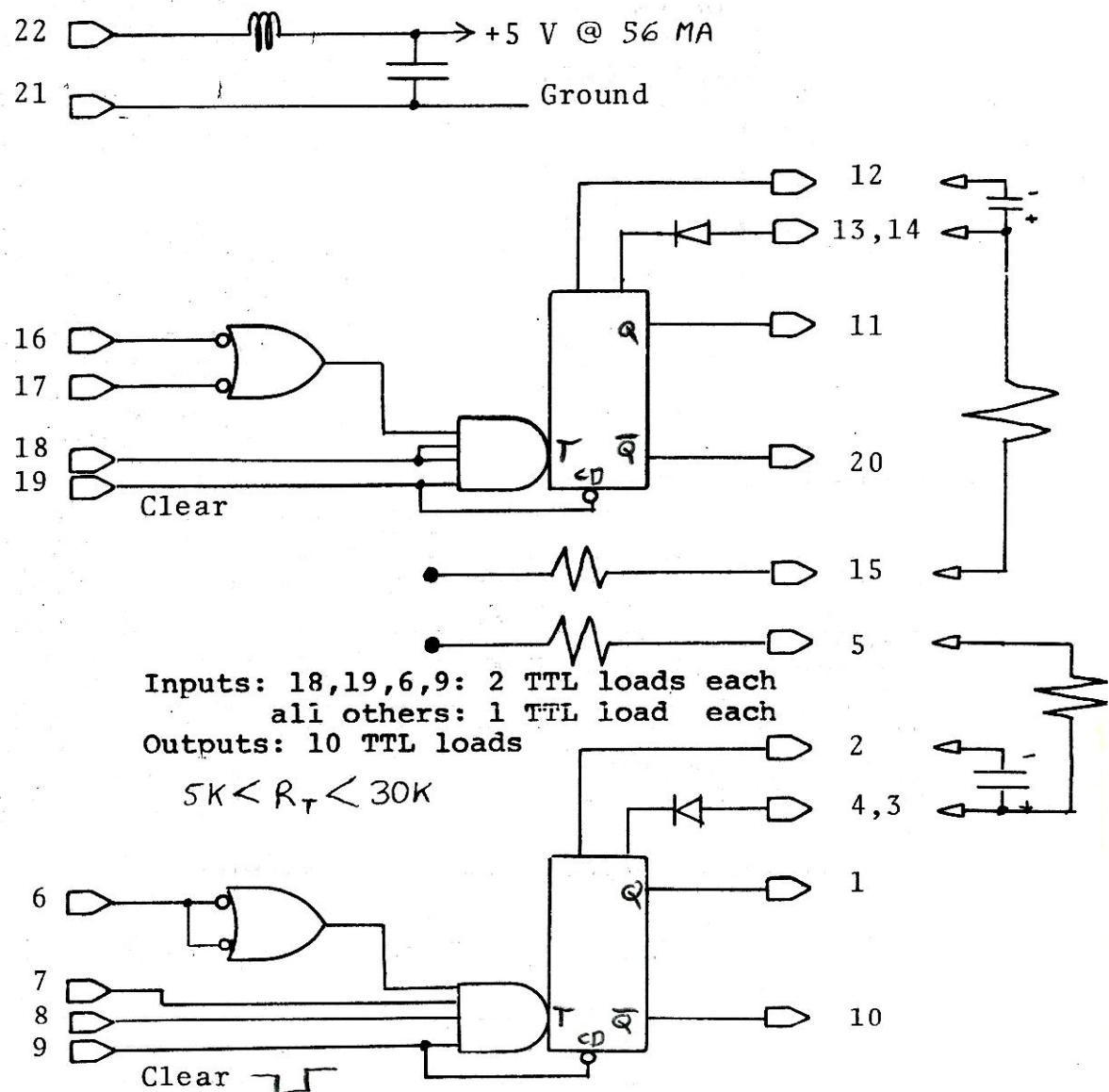
recommended operating conditions

Supply Voltage V_{CC} (See Note 1): SN5495A Circuits	
SN7495A Circuits	
Normalized Fan-Out From Each Output: High logic level	
Low logic level	
Width of Clock Pulse $t_p(\text{clock})$ (See Figure 9): SN5495A Circuits	
SN7495A Circuits	
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)	
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)	
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 input)	
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 input)	
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 input)	
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 input)	

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
		20	
		10	
20	10		ns
15	10		ns
10			ns
0			ns
15			ns
15			ns
5			ns
5			ns

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER	TEST FIGURE	TEST CONDITIONS ⁺		MIN	TYP	MAX	UNIT
		$C_L = 15 \text{ pF}$	$R_L = 400 \Omega$				
f_{max} Maximum shift frequency	9			25	36		MHz
Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	$C_L = 15 \text{ pF}$	$R_L = 400 \Omega$		18	27	ns
Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	$C_L = 15 \text{ pF}$	$R_L = 400 \Omega$		21	32	ns



description

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retriger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retrigerring, or to shorten by clearing. SN54122/SN74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with SN54121/SN74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000 \text{ pF}$, the output pulse width (t_w) is defined as:

$$t_w = 0.32 R_T C_{ext} \left(1 + \frac{0.7}{R_T} \right)$$

where

R_T is in $\text{k}\Omega$ (either internal or external timing resistor)

C_{ext} is in pF

t_w is in ns

- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Diode-Clamped Inputs
- D-C Triggered from High- or Low-Level Gated Logic Inputs
- Compatible for Use with TTL or DTL
- Typical Average Propagation Delay to Output Q . . . 21 ns

logic

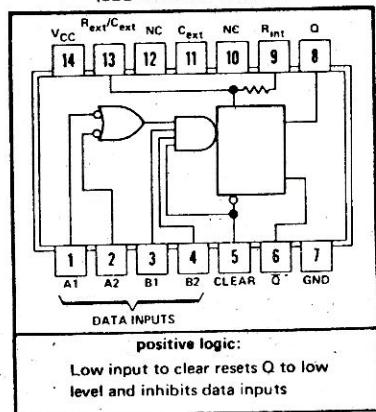
SN54122, SN74122

TRUTH TABLE

(See Note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	\bar{Q}
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	↑	↑
L	X	H	↑	↑	↑
X	L	H	H	L	H
X	L	↑	H	↑	↑
X	L	H	↑	↑	↑
H	↓	H	H	↑	↑
↓	↓	H	H	↑	↑
↓	H	H	H	↑	↑

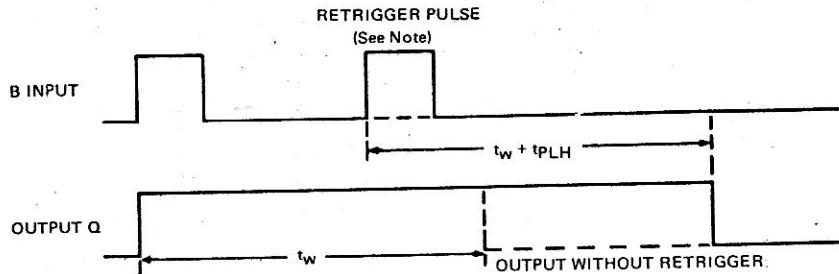
SN54122, SN74122
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)[†]
(SEE NOTES B THRU D)



recommended operating conditions

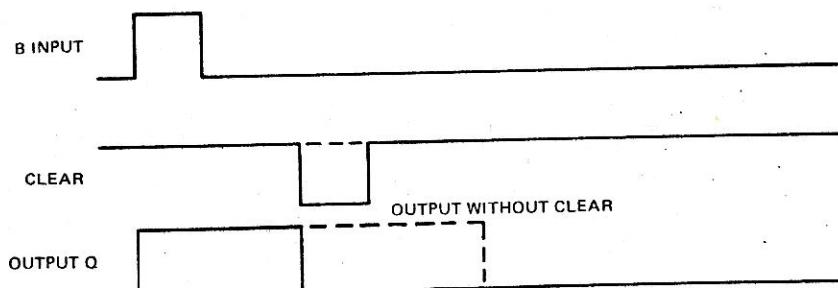
	SN54122, SN54123			SN74122, SN74123			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level		20	20		20	
	Low logic level		10	10		10	
Input data setup time, t _{setup} (see Note 3 and Figure 116)	40t			40t			ns
Input data hold time, t _{hold} (see Note 4 and Figure 116)	40t			40t			ns
Width of clear pulse, t _w (clear)	40t			40t			ns
External timing resistance	5		25	5		50	kΩ
External capacitance	No restriction			No restriction			
Wiring capacitance at R _{ext} /C _{ext} terminal	50			50			pF
Operating free-air temperature, T _A	-55	25	125	0	25	70	°C

Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.



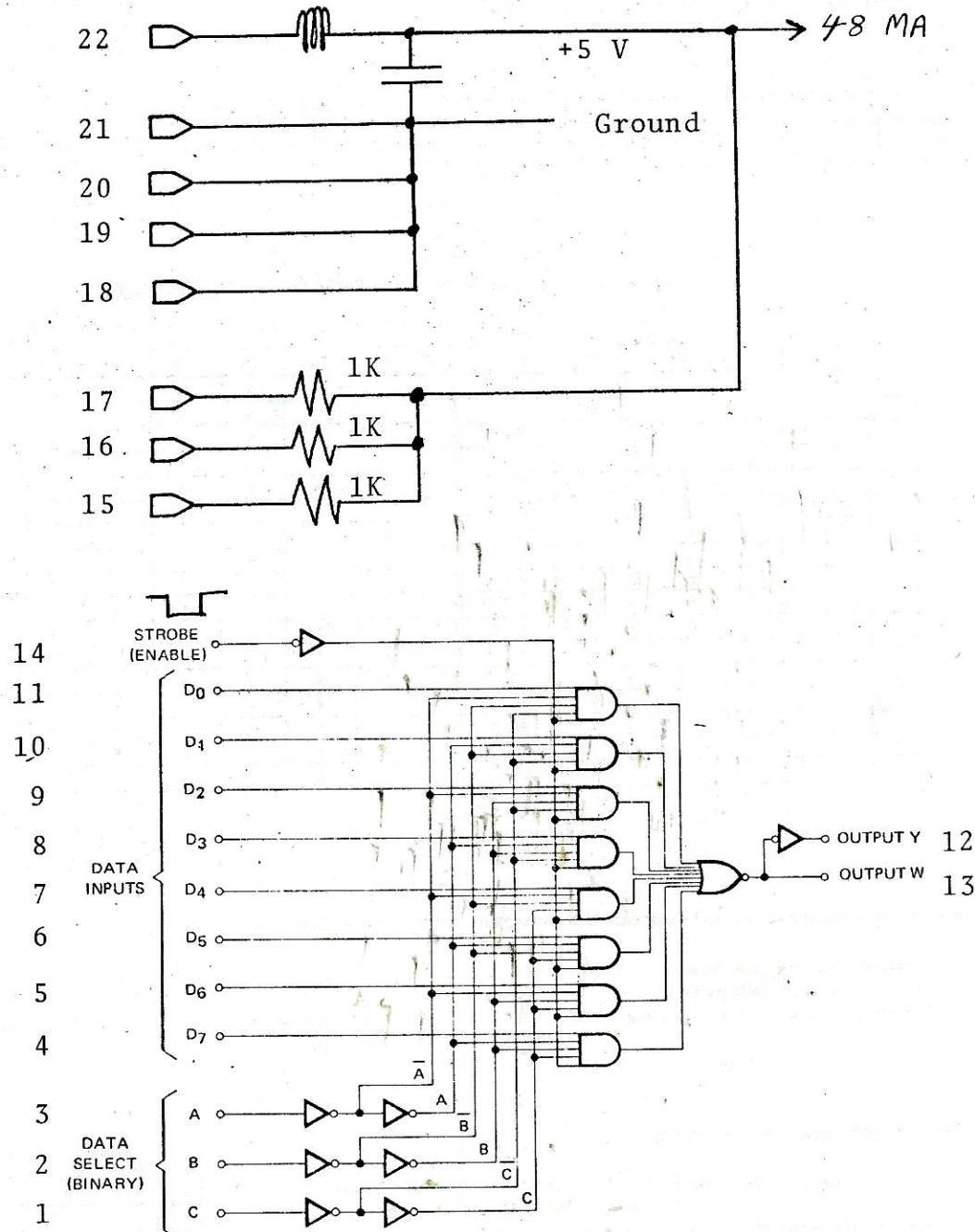
OUTPUT PULSE CONTROL USING RETRIGGER PULSE

NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.



OUTPUT PULSE CONTROL USING CLEAR INPUT

FIGURE A-TYPICAL INPUT/OUTPUT PULSES



Inputs: 1 TTL load each

Outputs: 10 TTL loads each

Note: Output glitches may occur if address bits are changed while enable is asserted.

74151

description

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. The SN54151/74151 features complementary outputs whereas the SN54150/SN74150 and SN54152/SN74152 have inverted outputs only. The SN54150/SN74150 and SN54151/SN74151 circuits are provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

These data selectors/multiplexers are fully compatible for use with other TTL or DTL circuits. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

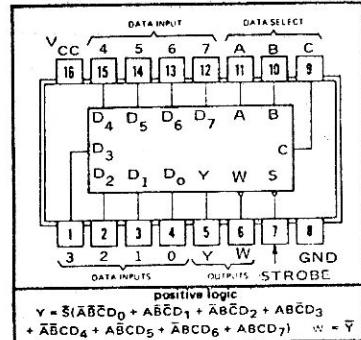
SN54150/SN74150 – 200 milliwatts

SN54151/SN74151 – 145 milliwatts

SN54152/SN74152 – 130 milliwatts

These data selectors feature Series 54H/74H circuitry for the OR function. This is done to minimize the capacitive effects of paralleling the phase-splitter transistors and thus reduce the propagation delay time. The SN54150, SN54151, and SN54152 are characterized for operation over the full military temperature range of -55°C to 125°C ; and the SN74150, SN74151 and SN74152 are characterized for operation from 0°C to 70°C .

SN54151, SN74151
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



TRUTH TABLE (SN54151/SN74151 AND SN54152/SN74152 ONLY)

INPUTS										OUTPUTS			
C	B	A	STROBE(1)	D₀	D₁	D₂	D₃	D₄	D₅	D₆	D₇	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	X	0	1
1	1	1	0	X	X	X	X	X	X	X	X	1	0

NOTES: 1. SN54151/SN74151 only.

2. When used to indicate an input, X = irrelevant.

absolute maximum ratings (over operating temperature range unless otherwise noted)

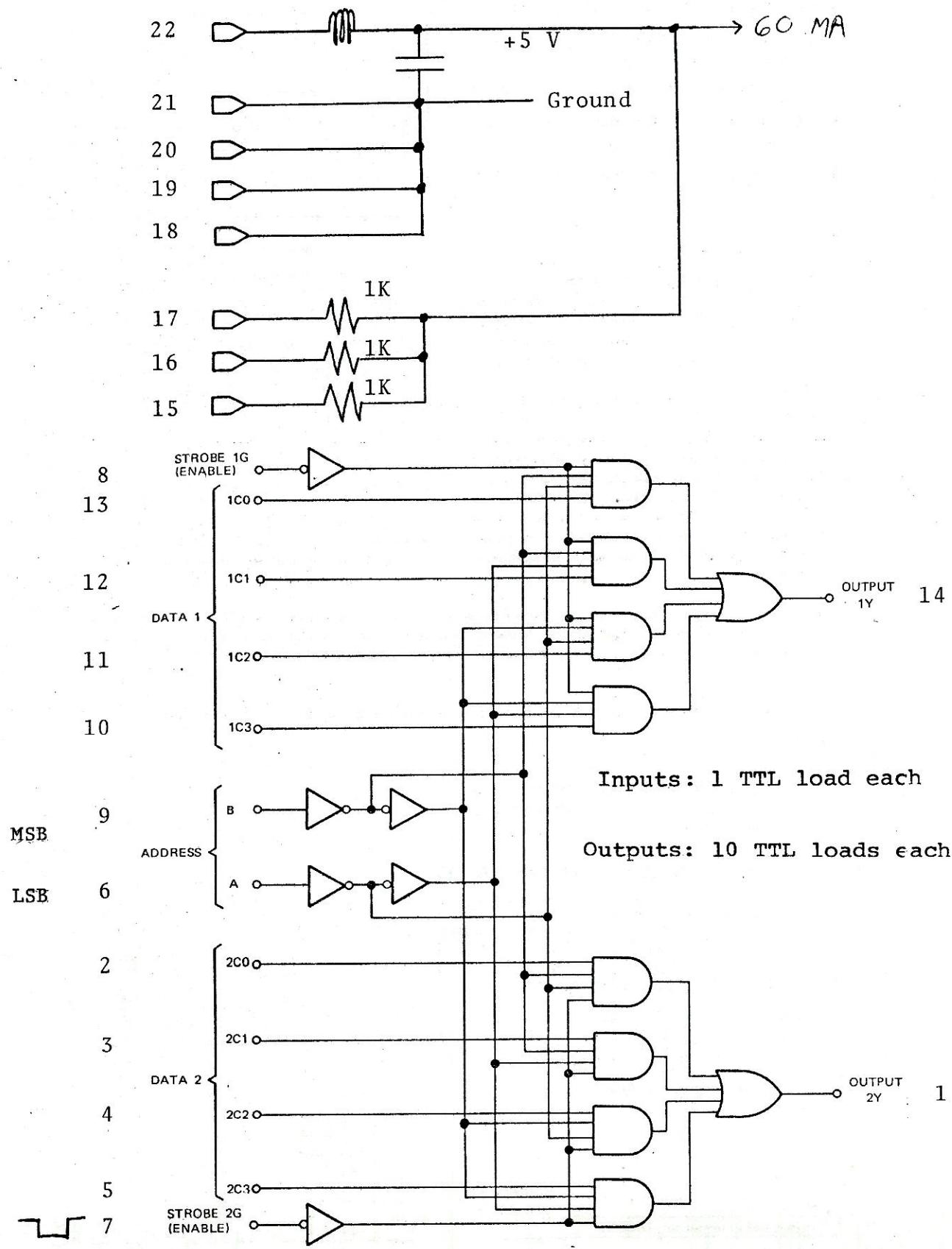
Supply Voltage V _{CC} (See Note 1)	7 V
Input Voltage, V _{in} (See Note 1)	5.5 V
Operating Free-Air Temperature Range: SN54150, SN54151, SN54152 Circuits	-55° C to 125° C
SN74150, SN74151, SN74152 Circuits	0° C to 70° C
Storage Temperature Range	-65° C to 150° C

recommended operating conditions

Supply Voltage V _{CC} (See Note 1): SN54150, SN54151, SN54152 Circuits	4.5	5	5.5	V
SN74150, SN74151, SN74152 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N): Logical 0			10	
Logical 1			20	

MIN	NOM	MAX	UNIT
4.5	5	5.5	V
4.75	5	5.25	V
		10	
		20	

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{pd0}	A,B,orC(4 levels)	Y			20	30	ns
t _{pd1}	A,B,orC(4 levels)	Y			35	52	ns
t _{pd0}	A,B,C,orD(3 levels)	W			22	33	ns
t _{pd1}	A,B,C,orD(3 levels)	W			23	35	ns
t _{pd0}	STROBE	Y			19	30	ns
t _{pd1}	STROBE	Y			35	52	ns
t _{pd0}	STROBE	W			21	30	ns
t _{pd1}	STROBE	W			15.5	24	ns
t _{pd0}	D ₀ thru D ₇	Y	C _L = 15pF, R _L = 400Ω		16	24	ns
t _{pd1}	D ₀ thru D ₇	Y			19	29	ns
t _{pd0}	E ₀ thru E ₁₅	W			8.5	14	ns
t _{pd1}	E ₀ thru E ₁₅	W			13	20	ns



- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- Typical Average Propagation Delay Times:

Data Input to Output	14 ns
Strobe Input to Output	17 ns
Select Input to Output	22 ns
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The SN54153 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74153 is characterized for operation from 0°C to 70°C .

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V _{CC}	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54153 Circuits	-55°C to 125°C
SN74153 Circuits	0°C to 70°C

Storage temperature range -65°C to 150°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER ^E	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
					CL = 30 pF, RL = 400 Ω	12	18	
t _{PLH}	Data	Y	6		15	23	ns	
t _{PHL}	Data	Y			22	34	ns	
t _{PLH}	Address	Y			22	34	ns	
t _{PHL}	Address	Y			19	30	ns	
t _{PLH}	Strobe	Y			15	23	ns	
t _{PHL}	Strobe	Y						

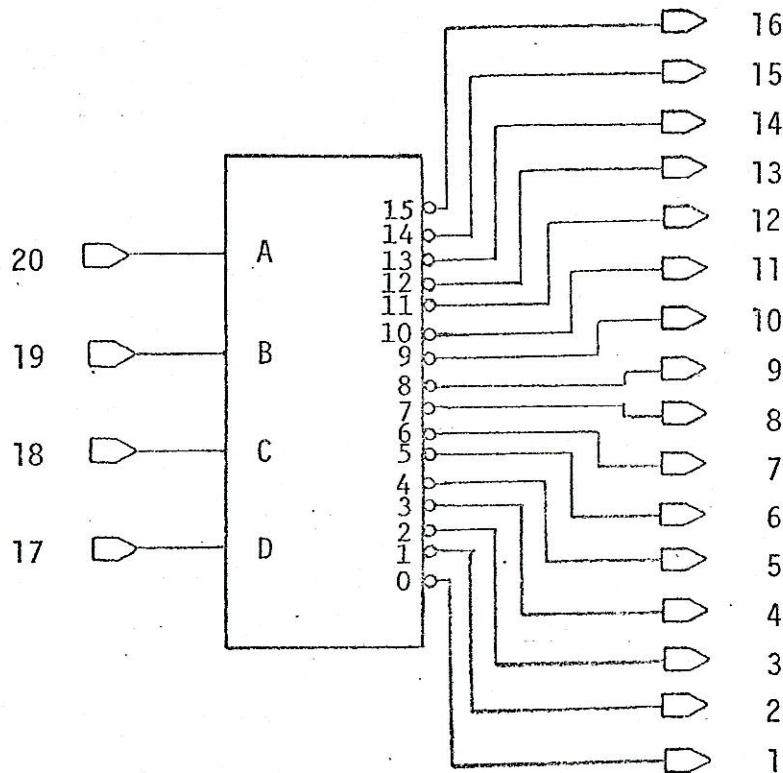
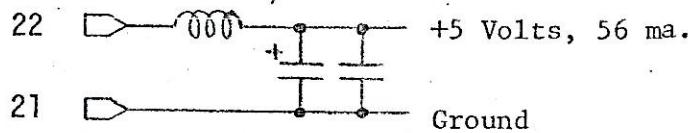
recommended operating conditions

			SN54153			SN74153			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V _{CC}			4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N		High logic level				20		20	
		Low logic level				10		10	
Operating free-air temperature range, T _A			-55	25	125	0	25	70	°C

Four To Sixteen Decoder/Demultiplexer

Board Type MSI 154

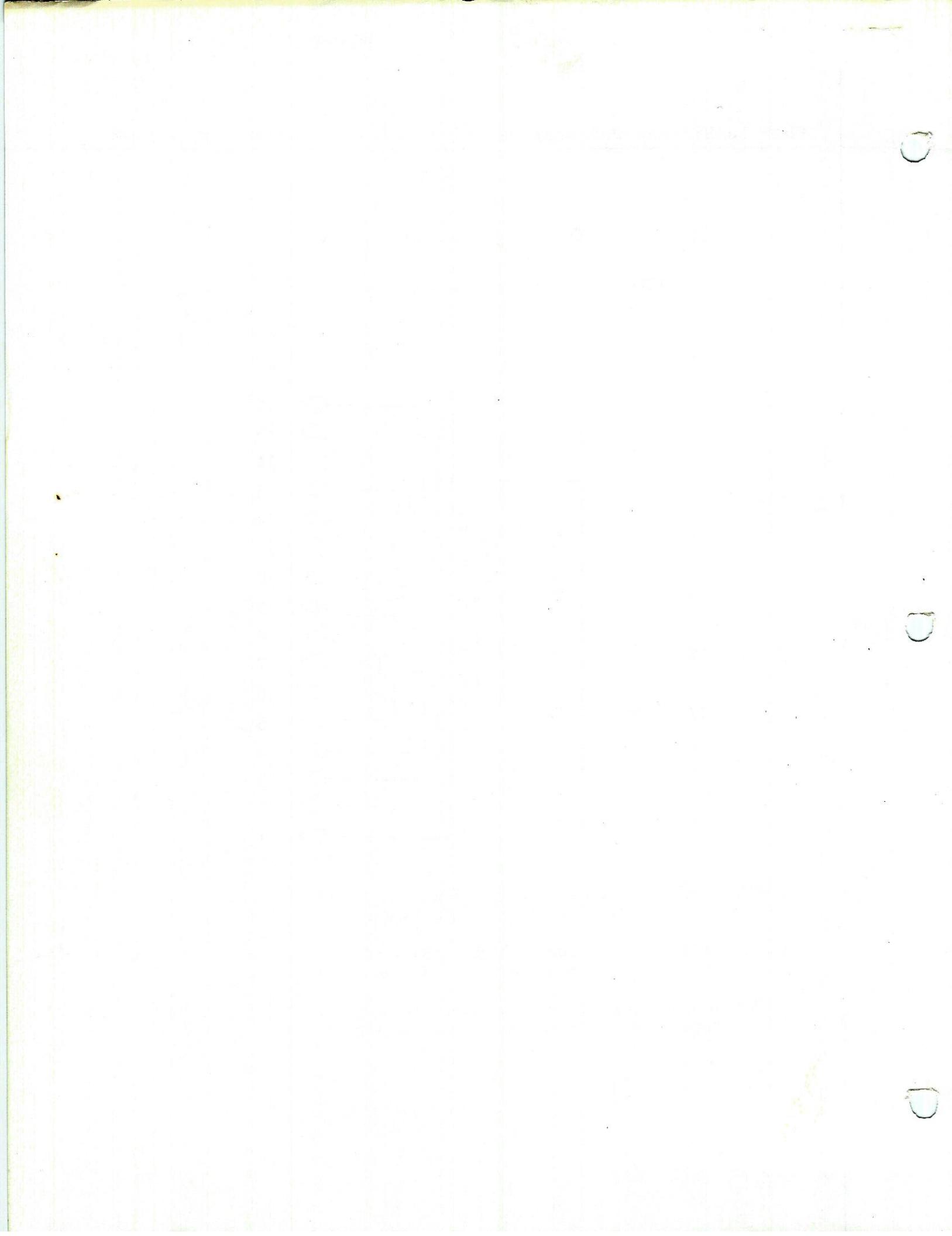
PIN CONNECTIONS:

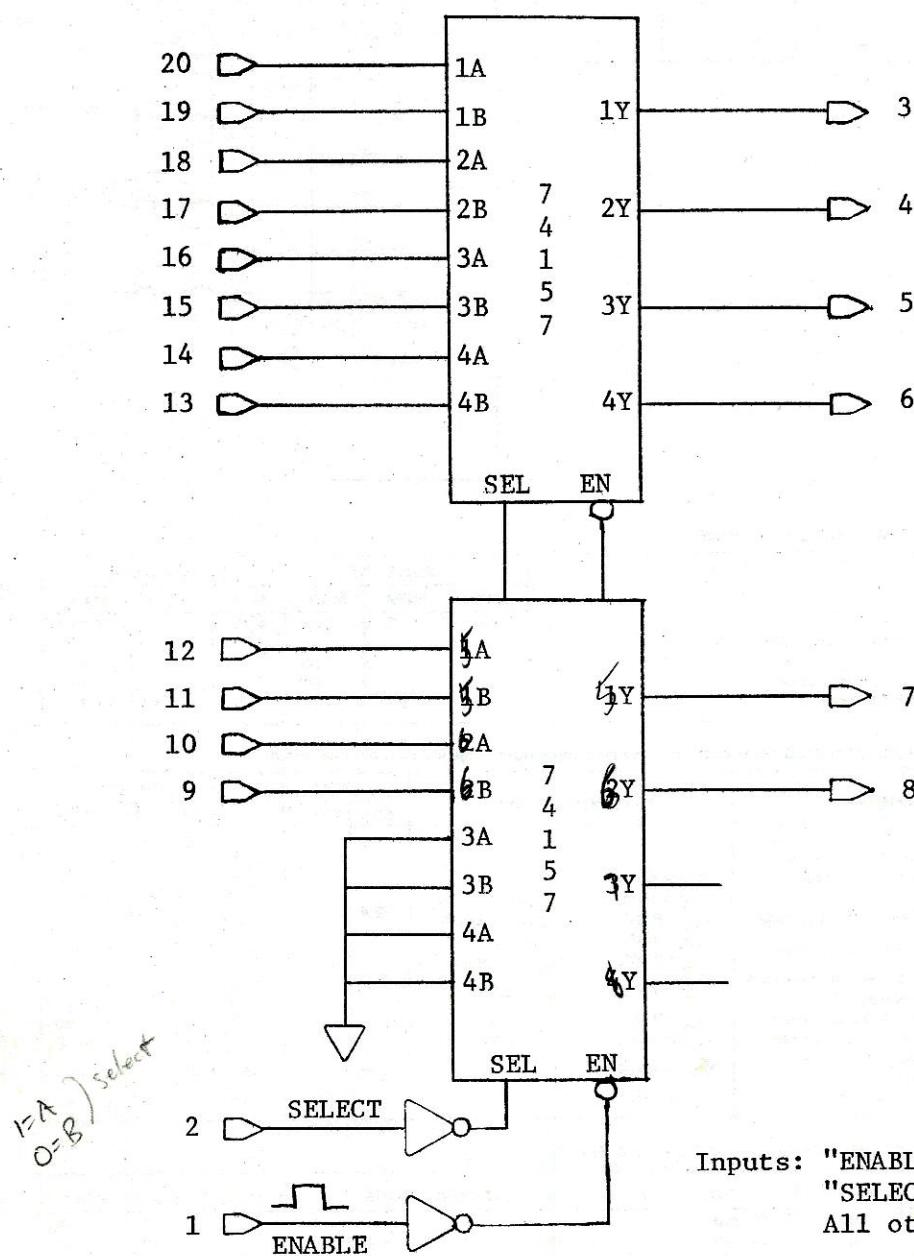
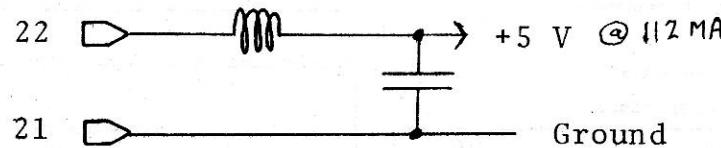


LOADING RULES: Inputs require 1 load.
Outputs can drive 10 loads.

PROPAGATION DELAY: Low-To-High <36nsec.
High-To-Low <33nsec.

NOTE: Outputs are asserted low (negative logic).
Inputs are asserted high (positive logic).

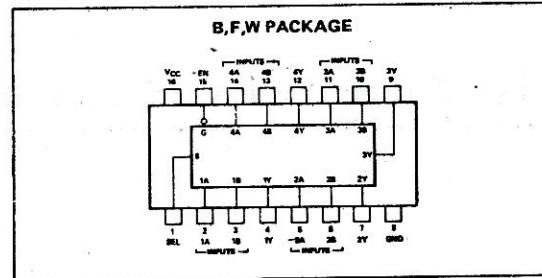




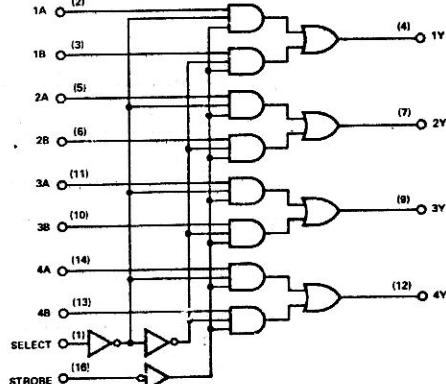
74157

DESCRIPTION

The S54157/N74157 and S54158/N74158 are identical with the exception of the S54158/N74158 being inverted. These devices are logical implementations of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The devices provide the ability, in one package, to select four bits of either data or control from two sources. By proper manipulation of the inputs, it can generate four functions of two variables with one variable common. Thus any number of random logic elements used to generate unusual truth tables can be replaced. All outputs are low when disabled (enable high). Both inputs and outputs are buffered.

PIN CONFIGURATION**S54/N74157****TRUTH TABLE**

INPUTS		OUTPUT	
STROBE	SELECT	A B	Y
H	X	X X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

**LOGIC DIAGRAM
S54/N74157****RECOMMENDED OPERATING CONDITIONS**

Supply Voltage V _{CC} Normalized Fan-Out from each Output, N High Logic Level Low Logic Level Operating Free-Air Temperature, T _A	S54157/58			N74157/58			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
4.5	5	5.5	4.75	5	5	5.25	V
-55	25	125	0	25	25	70	°C

ELECTRICAL CHARACTERISTICS (over operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS*	S54157/58			N74157/58			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
V _{IH} V _{IL} V _I	High-level input voltage Low-level input voltage Input clamp voltage	V _{CC} = MAX, V _{CC} = MIN, V _I = 0.8V, V _{CC} = MIN, V _I = 0.8V,	I _I = -12mA V _{IH} = 2V, I _{OH} = -800μA V _{IL} = 2V, I _{OL} = 16mA	2	0.8 -1.5	2	0.8 -1.5	V
V _{OH} V _{OL}	High-level output voltage Low-level output voltage	V _{CC} = MAX, V _{CC} = MIN, V _{IL} = 0.8V, V _{CC} = MAX,	V _{IH} = 2.4V V _{IL} = 0.4V	2.4	0.4	2.4	0.4	V
I _I I _{IH} I _{IL}	Input current at maximum input voltage High-level input current Low-level input current	V _{CC} = MAX, V _{CC} = MAX, V _{CC} = MAX,	V _I = 5.5V V _I = 2.4V V _I = 0.4V		1 40 -1.6		1 40 -1.6	mA μA mA
I _{OS} I _{CC}	Short-circuit output current† Supply current	V _{CC} = MAX V _{CC} = MAX		-20	-55 -18		-55 -18	mA
				30	48	30	48	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

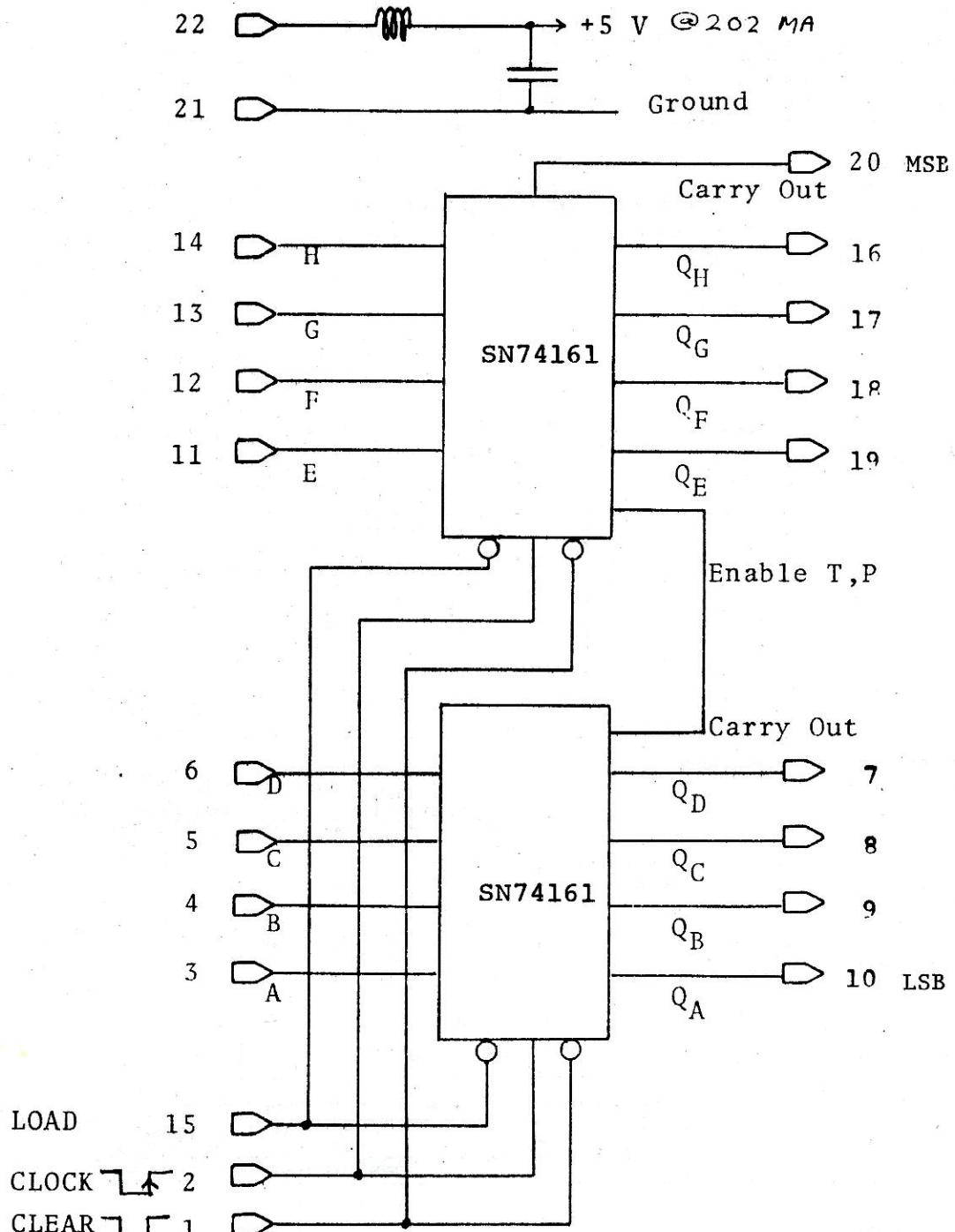
PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PHL} t _{PLH}	Data Data	Output Output	C _L = 15pF, R _L = 400		9 9	14 14	ns ns
t _{PHL} t _{PLH}	Enable Enable	Any Output Any Output		14 13	21 20		ns ns
t _{PHL} t _{PLH}	Select Select	Any Output Any Output			18 15	27 23	ns ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

(Asynchronous Clear; Master-Slave)



Note: a) Things happen at rising edge of CLOCK.
 b) CLEAR is Asynchronous; LOAD is synchronous

Inputs: "CLOCK": 4 TTL loads
 "CLEAR", "LOAD": 2 TTL loads each

All others: 1 TTL load each
 Outputs: 10 TTL loads each

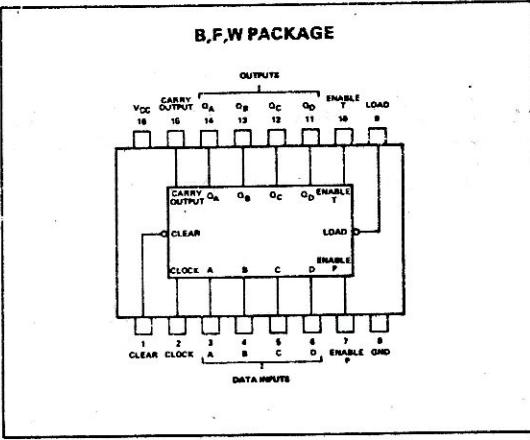
74161
74163

DESCRIPTION

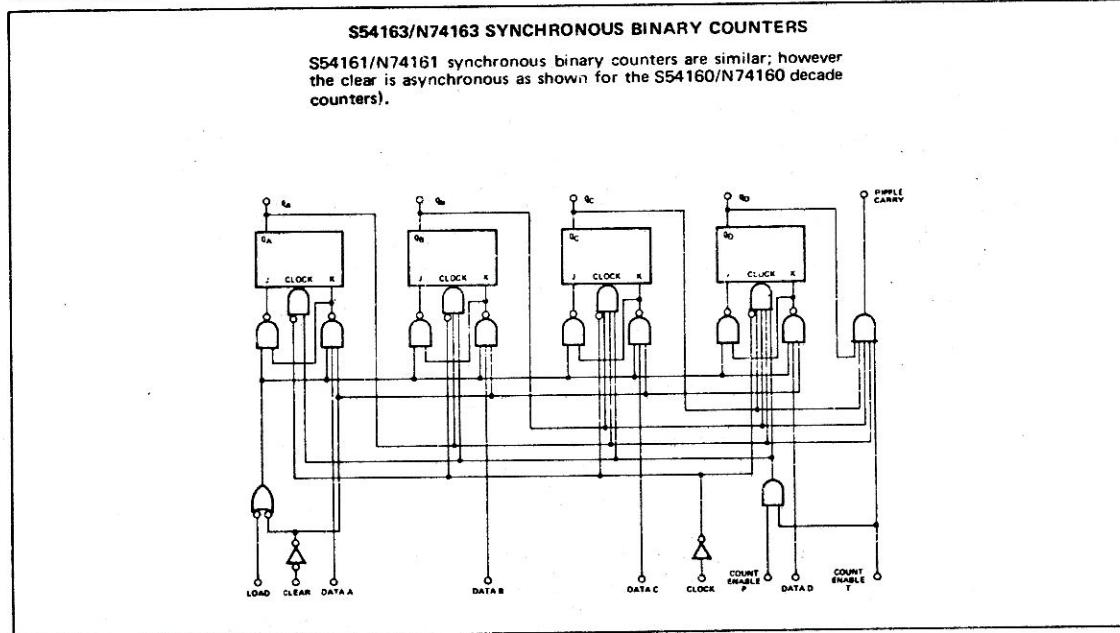
These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The S54160, S54162, N74160, and N74162 are decade counters and the S54161, S54163, N74161, and N74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs and power dissipation is typically 325 milliwatts.

PIN CONFIGURATION



LOGIC DIAGRAM



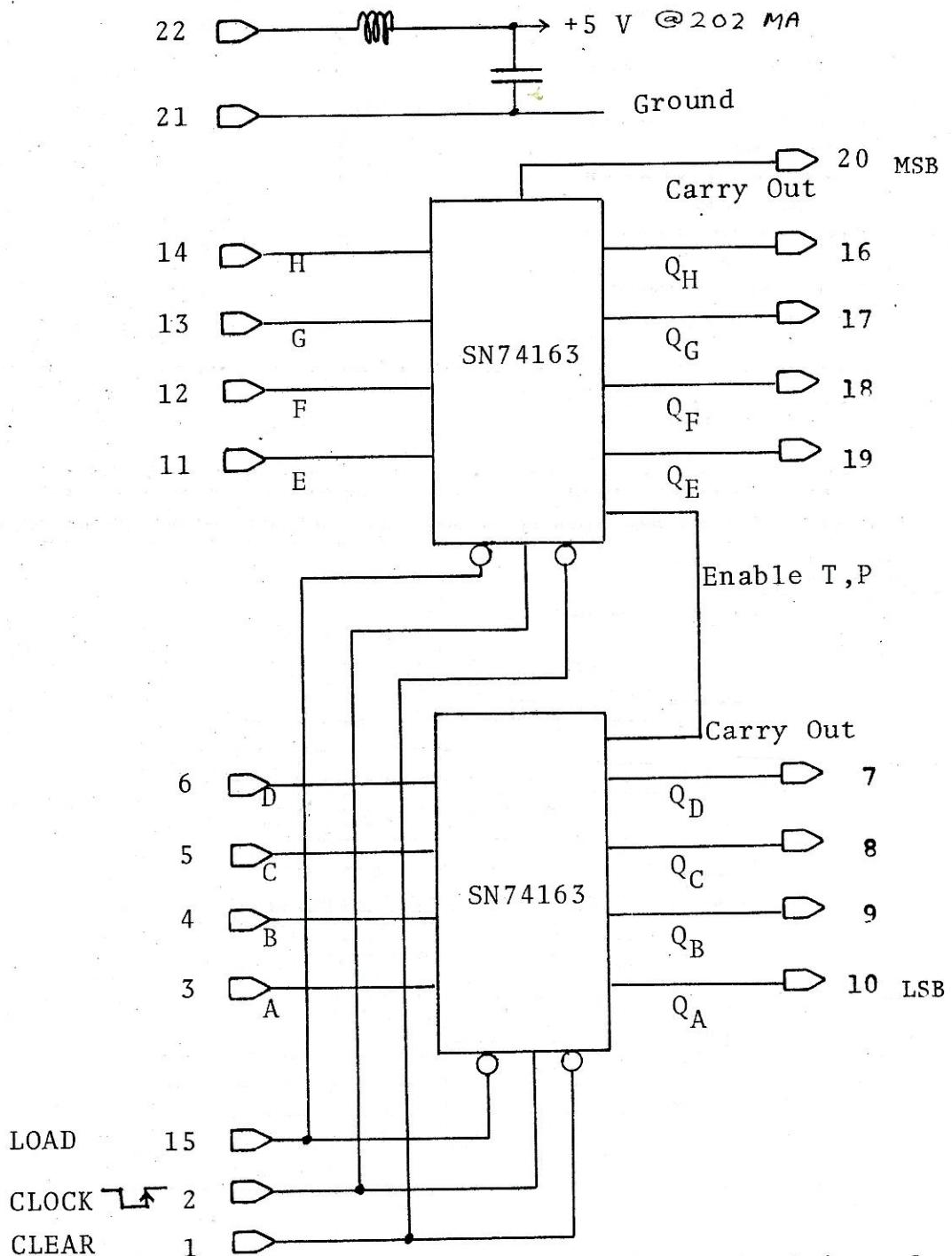
RECOMMENDED OPERATING CONDITIONS

	SS4160, SS4161 SS4162, SS4163			N74160, N74161 N74162, N74163			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N:							
High logic level	20		20			20	
Low logic level	10		10			10	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock Pulse, $t_w(clock)$	25			25		ns	
Width of Clear Pulse, $t_w(clear)$	20			20		ns	
Setup Time, t_{setup} :	Data Inputs, A,B,C,D	15		15			
Enable P	20			20			
Load	15			15			ns
Clear	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise specified)

PARAMETER	TEST CONDITIONS*	SS4160, SS4161 SS4162, SS4163			N74160, N74161 N74162, N74163			UNIT
		MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage	$V_{CC} = MAX$,			2			V
V_{IL}	Low-level input voltage	$V_{CC} = MAX$,			0.8			V
V_I	Input clamp voltage	$V_{CC} = MIN$,	$I_I = -12mA$		-1.5			V
V_{OH}	High-level output voltage	$V_{CC} = MIN$,	$V_{IH} = 2V$,		2.4			V
V_{OL}	Low-level output voltage	$V_{CC} = 0.8V$,	$I_{OH} = -800\mu A$		2.4			V
I_I	Input current at maximum input voltage	$V_{CC} = MIN$,	$V_{IH} = 2V$,		0.4			V
	High-level Clock or enable T	$V_{CC} = MAX$,	$I_{OL} = 16mA$		0.4			V
I_{IH}	input current Other inputs	$V_I = 5.5V$			1			mA
I_{IL}	Low-level Clock or enable T	$V_{CC} = MAX$,	$V_I = 2.4V$		80			μA
I_{IS}	input current Other inputs	$V_{CC} = MAX$,	$I_{IL} = 0.4V$		40			μA
I_{OS}	Short-circuit output current†	$V_{CC} = MAX$,			-3.2			mA
I_{CCCL}	Supply current, all outputs high	$V_{CC} = MAX$,	$I_{OS} = -57mA$		-1.6			mA
	Supply current, all outputs low	$V_{CC} = MAX$,	$I_{CCCL} = -57mA$		-57			mA
		See Note 3	59	85	59	94	101	mA
		See Note 4	63	91	63	101		mA

(Synchronous Clear; Master-Slave)



Note: a) Things happen at rising edge of CLOCK.
 b) CLEAR and LOAD are synchronous
 c) CLEAR wins out over LOAD.

Inputs: "CLOCK": 4 TTL loads
 "CLEAR", "LOAD": 2 TTL loads each
 All others: 1 TTL load each
 Outputs: 10 TTL loads each

74161
74163

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25^\circ C$, $N = 10$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency		25	32	MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock		23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock		23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock	$C_L = 15\text{pF}, R_L = 400\Omega$	15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T		8	13	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T		10	15	ns
t_{PLH}	Propagation delay time, high-to-low-level Q output from clear		20	30	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.

† Not more than one output should be shorted at a time.

NOTES:

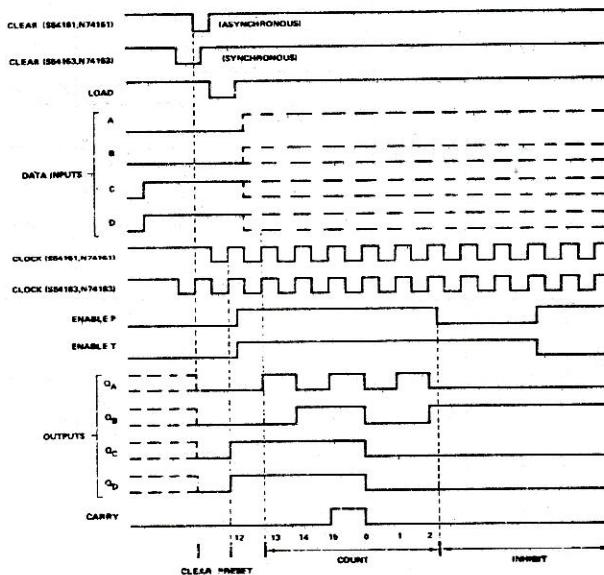
3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.

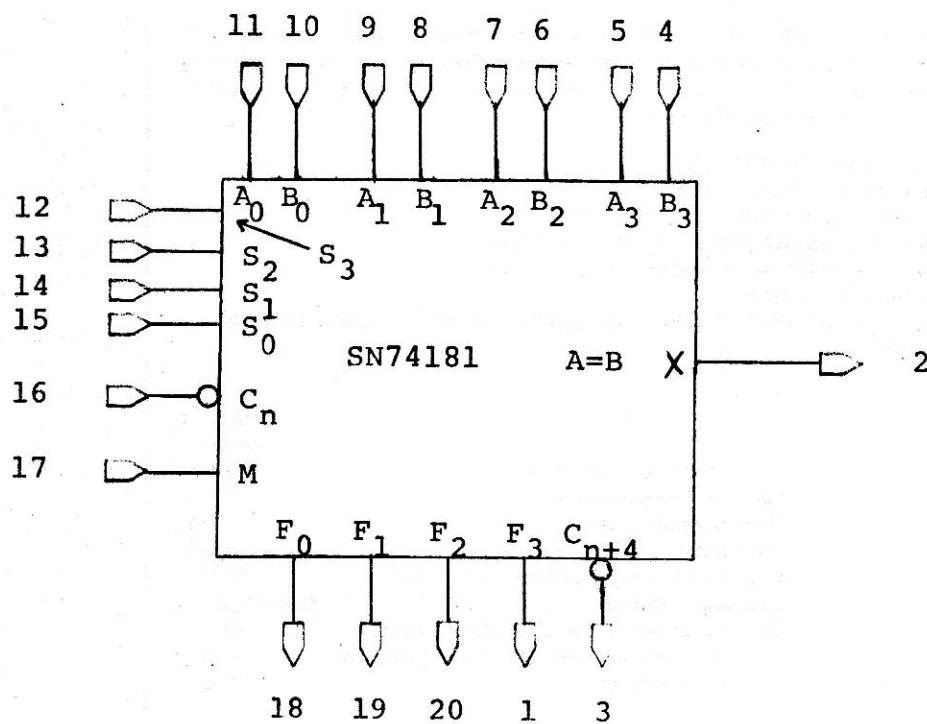
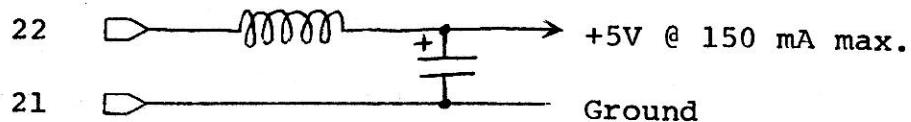
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES FOR 54161, 74161, 54163, 74163 SYNCHRONOUS BINARY COUNTERS

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.





Inputs - Any A or B : 3 loads each
 Any S : 4 loads each
 "M" : 1 load
 " C_n " : 5 loads

Outputs - Any, except "A=B" : 10 loads each
 "A=B" output is open-collector - requires
 an external pull-up:
 Maximum sinking capability at low-level
 output - 16 mA
 Maximum current stolen at high-level
 output - 1/4 mA
 Maximum allowable voltage at output - 5V

TTL/MSI 9341/54181, 74181

4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION — The TTL/MSI 9341/54181, 74181 is a 4-bit high speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The ALU is fully compatible with all members of the Fairchild TTL family.

- PROVIDES 16 ARITHMETIC OPERATIONS
ADD, SUBTRACT, COMPARE, DOUBLE,
PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES
EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR, PLUS
TEN OTHER LOGIC OPERATIONS
- FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS
- INPUT CLAMP DIODES
- TTL COMPATIBLE

PIN NAMES

\bar{A}_0 to \bar{A}_3 , \bar{B}_0 to \bar{B}_3

S_0, S_1, S_2, S_3

M

C_n

$F_0, \bar{F}_1, F_2, \bar{F}_3$

$A = B$

G

P

$C_n + 4$

NOTES:

a. 1 Unit Load (U.L.) = $40\mu A$ HIGH/1.6 mA LOW.

b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

Operand (Active LOW) Inputs

Function - Select Inputs

Mode Control Input

Carry Input

Function (Active LOW) Outputs (Note b)

Comparator Output

Carry Generate (Active LOW) Output (Note b)

Carry Propagate (Active LOW) Output (Note b)

Carry Output (Note b)

LOADING (Note a)

3 U.L.

4 U.L.

1 U.L.

5 U.L.

10 U.L.

Open Collector

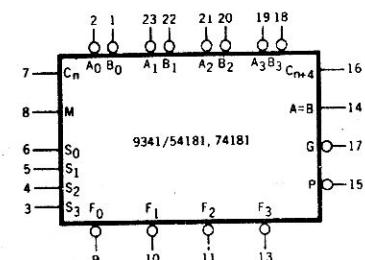
10 U.L.

10 U.L.

10 U.L.

10 U.L.

LOGIC SYMBOL

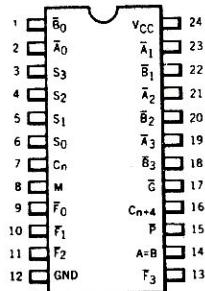


V_{CC} = Pin 24

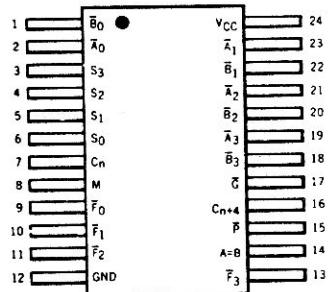
GND = Pin 12

CONNECTION DIAGRAMS

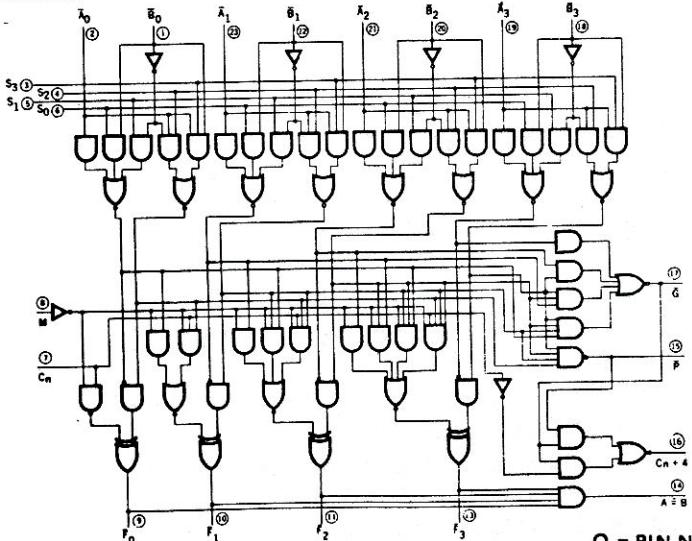
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



O = PIN NUMBERS

FUNCTIONAL DESCRIPTION — The TTL/MSI 9341/54181, 74181 is a 4-bit, high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \dots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs Logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs Arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals P (carry propagate) and G (carry generate). P and G are not affected by carry in. When speed requirements are not stringent, the 9341/54181, 74181 can be used in a simple ripple carry mode by connecting the carry out (C_{n+4}) signal to the carry input (C_n) of the next unit. For high speed operation the 9341/54181, 74181 is used in conjunction with the 9342/54182, 74182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 9341/54181, 74181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the 9341/54181, 74181 goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A = B output is open collector and can be wire ANDed with other A = B outputs to give a comparison for more than 4-bits. The A = B signal can also be used with the carry out signal to indicate $A > B$ and $A < B$.

The Function Table lists the Arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus Select Code LHHL generates A minus B minus 1 (2's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1's complement), a CARRY OUT means BORROW; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

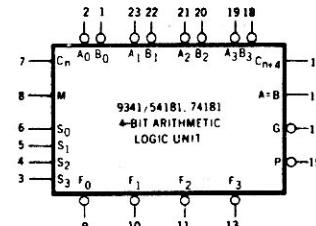
As indicated the 9341/54181, 74181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

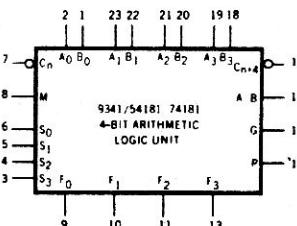
MODE SELECT INPUTS $S_3 S_2 S_1 S_0$	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
	LOGIC (M = H)	ARITHMETIC** (M = L) ($C_n = L$)	LOGIC (M = H)	ARITHMETIC** (M = L) ($C_n = H$)
L L L L	\bar{A}	A minus 1	\bar{A}	A
L L L H	\bar{AB}	AB minus 1	$\bar{A} + B$	$A + B$
L L H L	$A + \bar{B}$	\bar{AB} minus 1	\bar{AB}	$A + B$
L L H H	Logical 1 minus 1		Logical 0 minus 1	
L H L L	$A + B$	$A + (A + \bar{B})$	\bar{AB}	$A + \bar{B}$
L H L H	\bar{B}	AB plus $(A + \bar{B})$	B	$(A + B)$ plus \bar{AB}
L H M L	$A \oplus B$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H M H	$A + \bar{B}$	$A + \bar{B}$	\bar{AB}	\bar{AB} minus 1
H L L L	\bar{AB}	A plus $(A + B)$	$\bar{A} + B$	A plus AB
H L L H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H L H L	B	AB plus $(A + B)$	B	$(A + B)$ plus AB
H L H H	$A + B$	$A + B$	AB	AB minus 1
H H L L	Logical 0 plus A^*		Logical 1 plus A^*	
H H L H	\bar{AB}	AB plus A	$\bar{A} + \bar{B}$	$(A + B)$ plus A
H H M L	AB	AB plus A	$A + B$	$(A + B)$ plus A
H H M H	A	A	A	A minus 1

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS

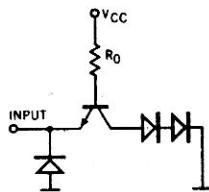


V_{CC} = Pin 24
GND = Pin 12

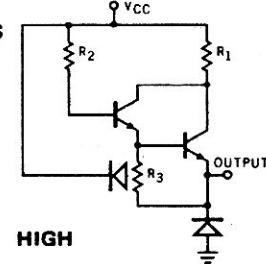
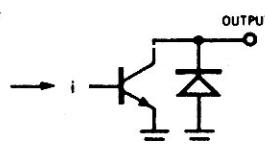
H = High Voltage Level
L = Low Voltage Level
*Each bit is shifted to the next more significant position
**Arithmetic operations expressed in 2's complement notation

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUITS



INPUT CURRENT VERSUS INPUT VOLTAGE

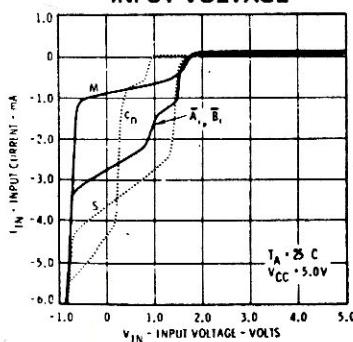


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

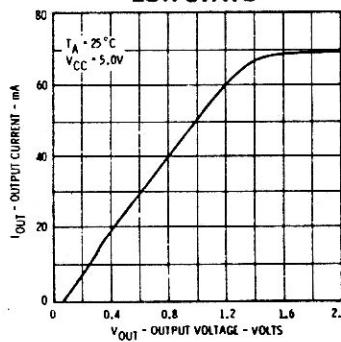


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE

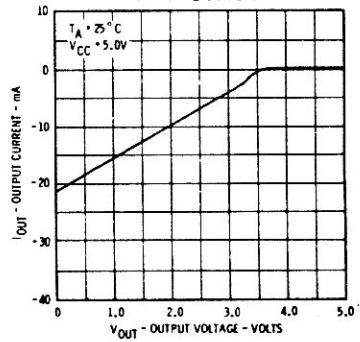


Fig. 3

SWITCHING CHARACTERISTICS ($T_A = 25^\circ C$, $V_{CC} = 5.0 V$, Pin 12 = GND)

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		Typ.	Max.		
t_{PLH}	(C_n to C_{n+4})	12 13	16 17	ns	$M = OV$, (Sum or Diff Mode) See Fig. 4 and Tables I & II
t_{PHL}	(C_n to \bar{F} outputs)	13 14	16 17	ns	$M = OV$, (Sum Mode) See Fig. 4 and Table I
t_{PLH}	(\bar{A} or \bar{B} inputs to \bar{G} output)	16 9	19 12	ns	$M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V$ (Sum Mode) See Fig. 4 and Table I
t_{PHL}	(\bar{A} or \bar{B} inputs to \bar{G} output)	18 13	22 17	ns	$M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V$ (Diff Mode) See Fig. 5 and Table II
t_{PLH}	(\bar{A} or \bar{B} inputs to \bar{P} output)	16 11	19 15	ns	$M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V$ (Sum Mode) See Fig. 4 and Table I
t_{PHL}	(\bar{A} or \bar{B} inputs to \bar{P} output)	17 14	21 19	ns	$M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V$ (Diff Mode) See Fig. 5 and Table II
t_{PLH}	(\bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs)	19 24	26 32	ns	$M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V$ (Sum Mode) See Fig. 4 and Table I
t_{PHL}	(\bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs)	20 28	26 34	ns	$M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V$ (Diff Mode) See Fig. 5 and Table II
t_{PLH}	(\bar{A}_i or \bar{B}_i inputs to \bar{F}_{i+1} outputs)	23 19	29 25	ns	$M = OV, S_0 = S_3 = 4.5 V, S_1 = S_2 = OV$ (Sum Mode) See Fig. 4 and Table I
t_{PHL}	(\bar{A}_i or \bar{B}_i inputs to \bar{F}_{i+1} outputs)	23 24	29 30	ns	$M = OV, S_0 = S_3 = OV, S_1 = S_2 = 4.5 V$ (Diff Mode) See Fig. 5 and Table II
t_{PLH}	(\bar{A} or \bar{B} inputs to \bar{F} outputs)	18 21	22 26	ns	$M = 4.5 V$ (Logic Mode) See Fig. 4 and Table III
t_{PHL}	(\bar{A} or \bar{B} inputs to C_{n+4} output)	16 26	21 30	ns	$M = OV, S_0 = S_3 = 4.5 V, S_1 = S_2 = OV$ (Sum Mode) See Fig. 6 and Table I
t_{PLH}	(\bar{A} or \bar{B} inputs to C_{n+4} output)	19 26	25 30	ns	$M = OV, S_0 = S_3 = OV, S_1 = S_2 = 4.5 V$ (Diff Mode)
t_{PLH}	(\bar{A} or \bar{B} inputs to $A = B$ output)	33 30	44 37	ns	$M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V,$ $R_O = 400 \Omega$ to $5.0 V$ (Diff Mode) See Fig. 5 and Table II
t_{PHL}					

NOTES:

- (1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
- (2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
- (3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
- (4) Note more than one output should be shorted at a time.

SWITCHING TIME WAVEFORMS

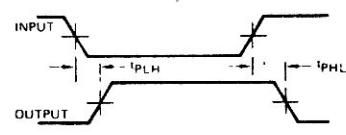
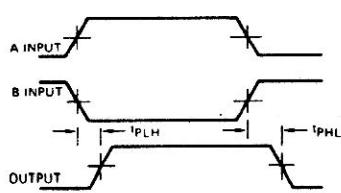
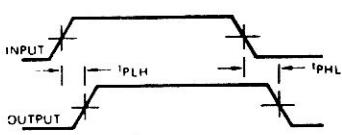
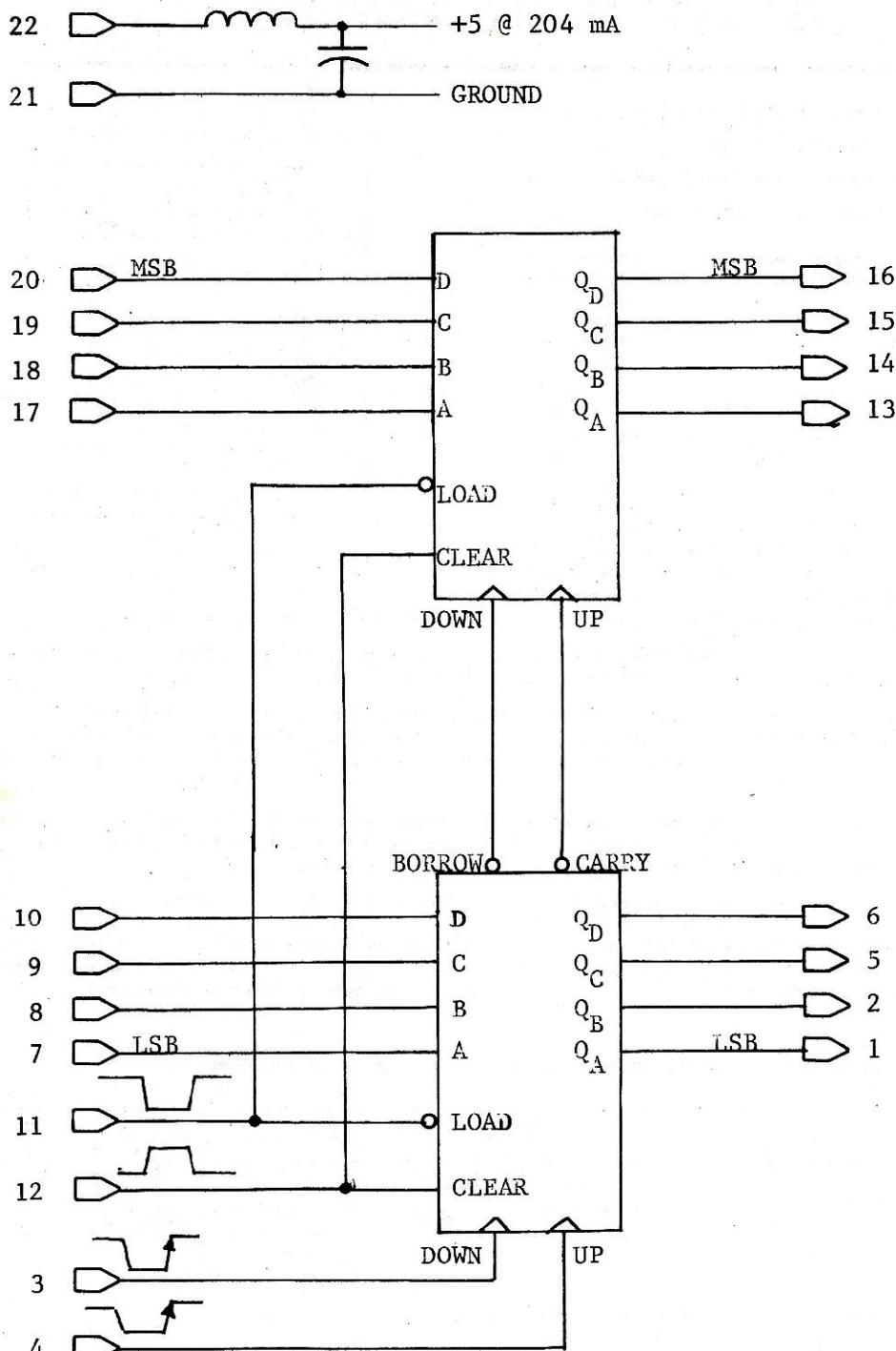


Fig. 4

Fig. 5

Fig. 6



NOTE:

1. TO COUNT IN EITHER DIRECTION, OPPOSITE CLOCK LINE MUST BE HIGH.
2. ASYNCHRONOUS CLEAR AND LOAD.
3. ALL OUTPUTS WILL DRIVE 10 LOADS; LOAD & CLEAR 2 LOADS, OTHERS 1 LOAD.

**TYPES SN54192, SN54193, SN54L192, SN54L193, SN54LS192, SN54LS193
SN74192, SN74193, SN74L192, SN74L193, SN74LS192, SN74LS193**
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

BULLETIN NO. DL-S 7211828, DECEMBER 1972

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'L192, 'L193	7 MHz	43 mW
'LS192, 'LS193	32 MHz	85 mW

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, 'L192, and 'LS192 circuits are BCD counters and the '193, 'L193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

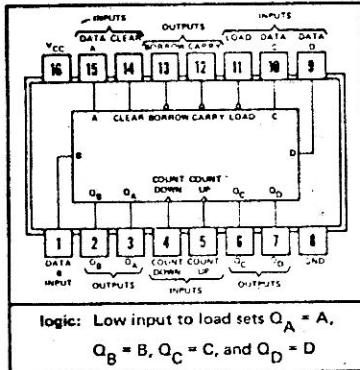
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

'192, '193 . . . J, N, OR W PACKAGE
'L192, 'L193 . . . J OR N PACKAGE
'LS192, 'LS193 . . . J, N, OR W PACKAGE
(TOP VIEW)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54L'	SN54LS'	SN74'	SN74L'	SN74LS'	UNIT
Supply voltage, V _{CC} (see Note 1)	7	8	7	7	8	7	V
Input voltage	5.5	5.5	7	5.5	5.5	7	V
Operating free-air temperature range	-55 to 125			0 to 70			°C
Storage temperature range	-65 to 150			-65 to 150			°C

NOTE 1: Voltage values are with respect to network ground terminal.

PIN CONNECTIONS:

22 — +5 Volts

21 — Ground

20 — -15 Volts

19 — +15 Volts

18 — DAC Output: -2.5V to +2.5V

17 — MSB

16

15

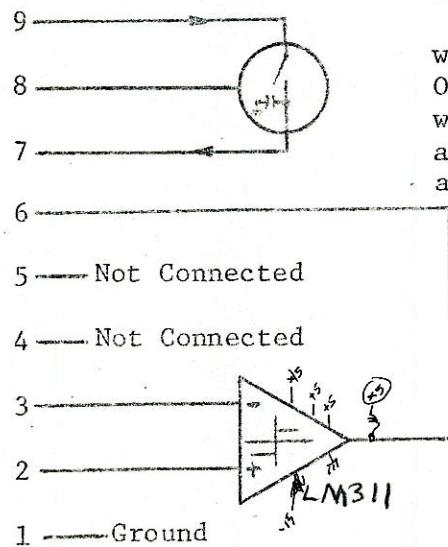
14

13

12

11

10 — LSB



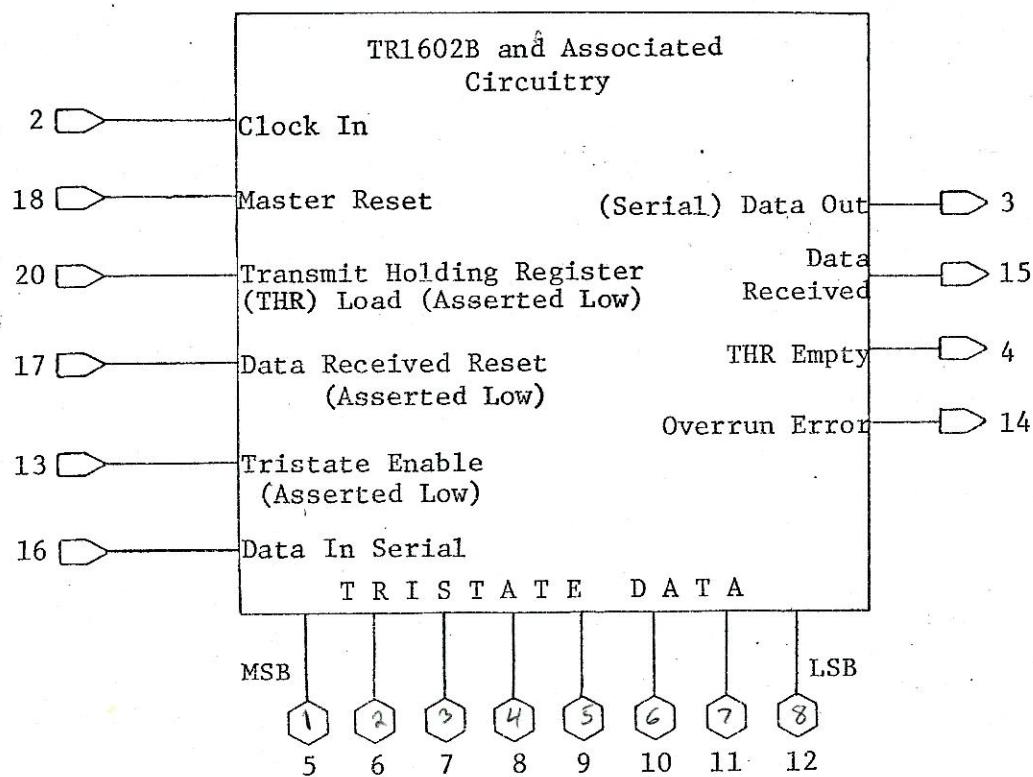
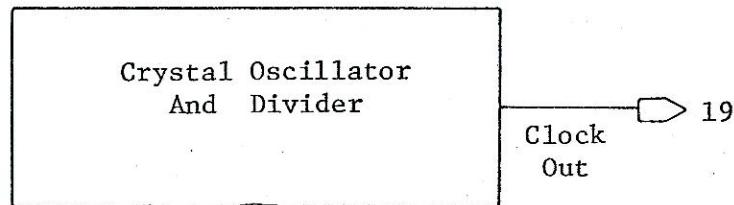
SAMPLE & HOLD:

Output (Pin 7) tracks input (Pin 9) while control (Pin 8) is a digital high. Output will remember the analog input when control is pulled low, for as long as control is pulled low, limited to about 50msec. Input and output are analog, for inputs to pin 9 between -5 volts and +5 volts only.

ANALOG COMPARATOR:

Output (Pin 6) is digital high if the voltage on the + input is greater than the voltage on the - input of the comparator. Output is TTL/DTL. Inputs are analog voltages.

This board contains an 8 bit DAC, an analog comparator, and a sample and hold circuit. The board requires that +15 and -15 be connected to the appropriate pins in addition to the normal rack +5 supply. The second supply should also be grounded to pin 21. The output of the DAC is -2.5 volts for 00000000 in, and +2.5 volts for 11111111 in. If desired, the DAC, Comparator, and Sample/Hold can be wired together to form a high speed Analog to Digital Converter system. The comparator can be used to detect a specific analog level or difference, and is good for inputs between -10 and +10 volts. Negative feedback on the comparator is not advised.



Normally, a crystal is inserted into the crystal oscillator socket that is appropriate for the baud rate being used, and 'Clock Out' (Pin 19) is connected to 'Clock In' (Pin 2).

For definitions of signal names, see attached information.

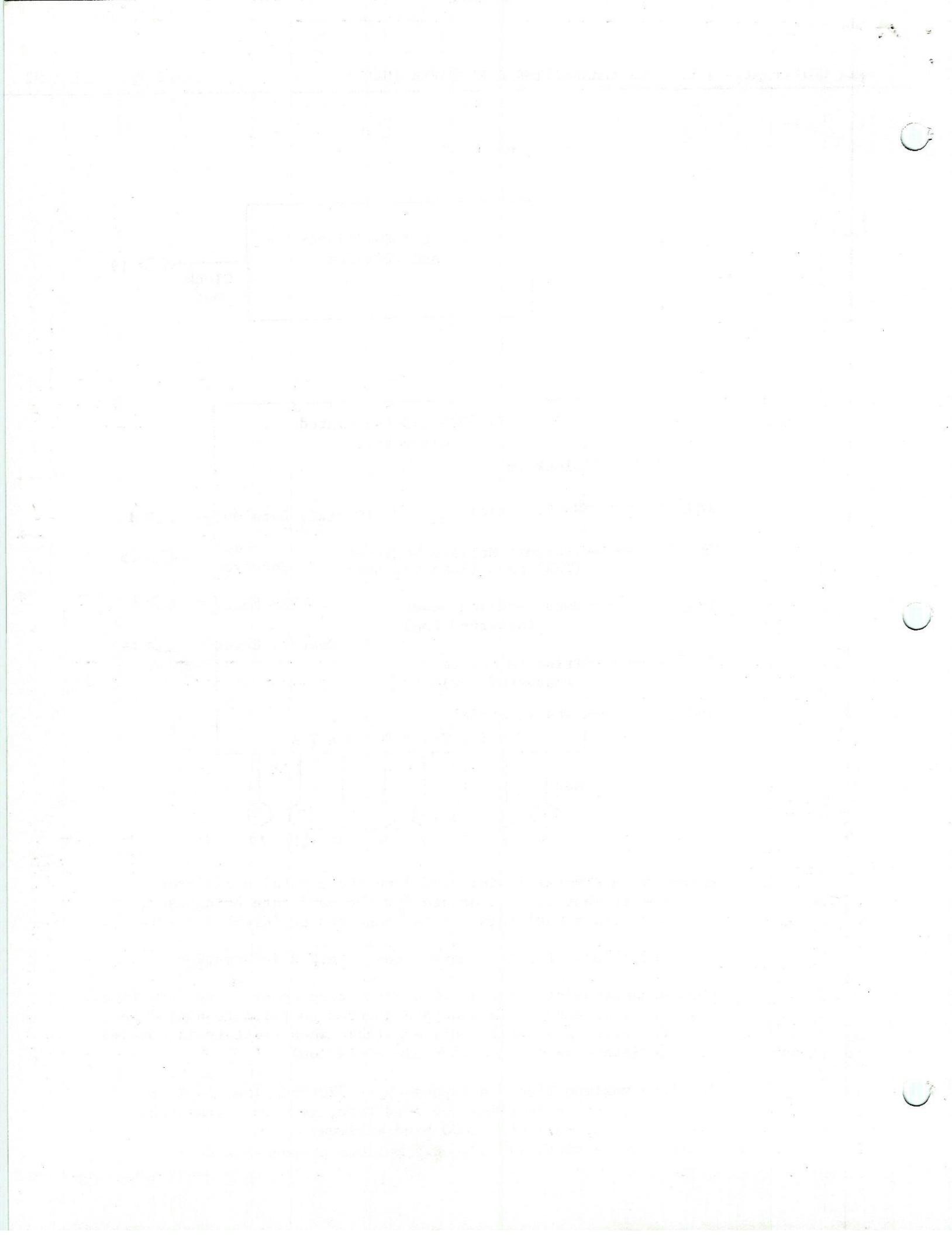
Observe appropriate caution when connecting to tristate data lines.

Parallel data in is always connected to tristate data lines.

Parallel data out is only available when tristate is enabled (tristate is enabled when pin 13 is low).

Absolute maximum clock in frequency is 320KHz. The clock in frequency is 16 times the baud rate, so this corresponds to a baud rate of 20,000 Baud maximum.

Minimum pulse width is 500nsec. Maximum propagation delay is 500nsec.



FEATURES

- SILICON GATE TECHNOLOGY – LOW THRESHOLD CIRCUITRY
Directly TTL and DTL Compatible – External Resistors Eliminated
- D.C. STABLE (STATIC) CIRCUITRY
- FULL DUPLEX OR HALF DUPLEX OPERATION
Transmits And Receives Serial Data Simultaneously Or Alternately
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- FULLY PROGRAMMABLE – EXTERNALLY SELECTABLE
Word Length
Baud Rate
Even/Odd Parity (Receiver/Verification – Transmitter/Generation)
Parity Inhibit – Verification/Generation
One, One and One-Half, or Two Stop Bit Generation
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
Transmission Complete
Buffer Register Transfer Complete
Received Data Available
Parity Error
Framing Error
Overrun Error
- THREE-STATE OUTPUTS
Receiver Register Outputs
Status Flags
- AVAILABLE IN CERAMIC OR HERMETIC PLASTIC CAVITY PACKAGES

APPLICATIONS

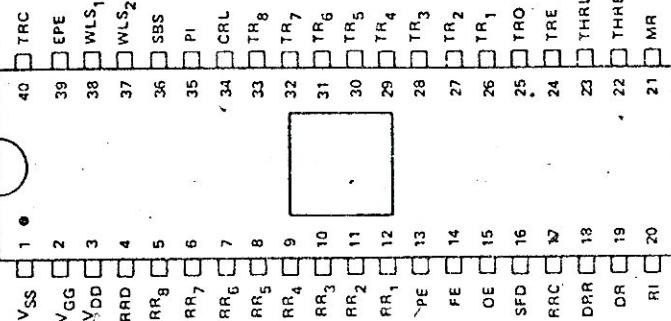
- | | |
|----------------------------------|-----------------------------------|
| • PERIPHERALS | • CARD AND TAPE READERS |
| • TERMINALS | • PRINTERS |
| • MINI COMPUTERS | • DATA SETS |
| • FACSIMILE TRANSMISSION | • CONTROLLERS |
| • MODEMS | • KEYBOARD ENCODERS |
| • CONCENTRATORS | • REMOTE DATA ACQUISITION SYSTEMS |
| • ASYNCHRONOUS DATA MULTIPLEXERS | • ASYNCHRONOUS DATA CASSETTES |

GENERAL DESCRIPTION

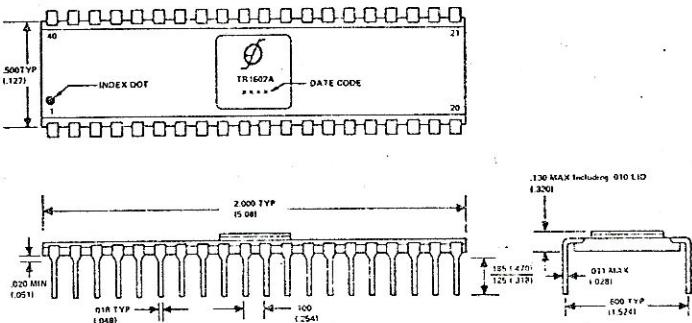
The TR1602A & the TR1602B are ASYNCHRONOUS RECEIVER/TRANSMITTER sub-systems using silicon gate process technology. The use of this low threshold process provides direct compatibility with all forms of current sinking logic. Interfacing restraints, such as external resistors, drivers and level shifting circuitry, are eliminated. All output lines have been designed to drive TTL directly.

The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one half when transmitting a 5 bit code. Note: See TR1402A Data Sheet for operation with 5 level code-2 stop bits.

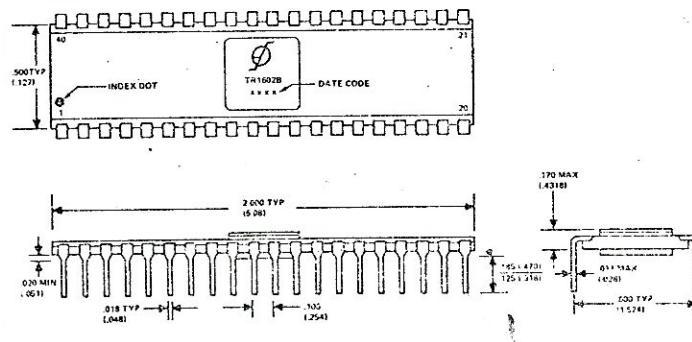
PIN CONNECTIONS

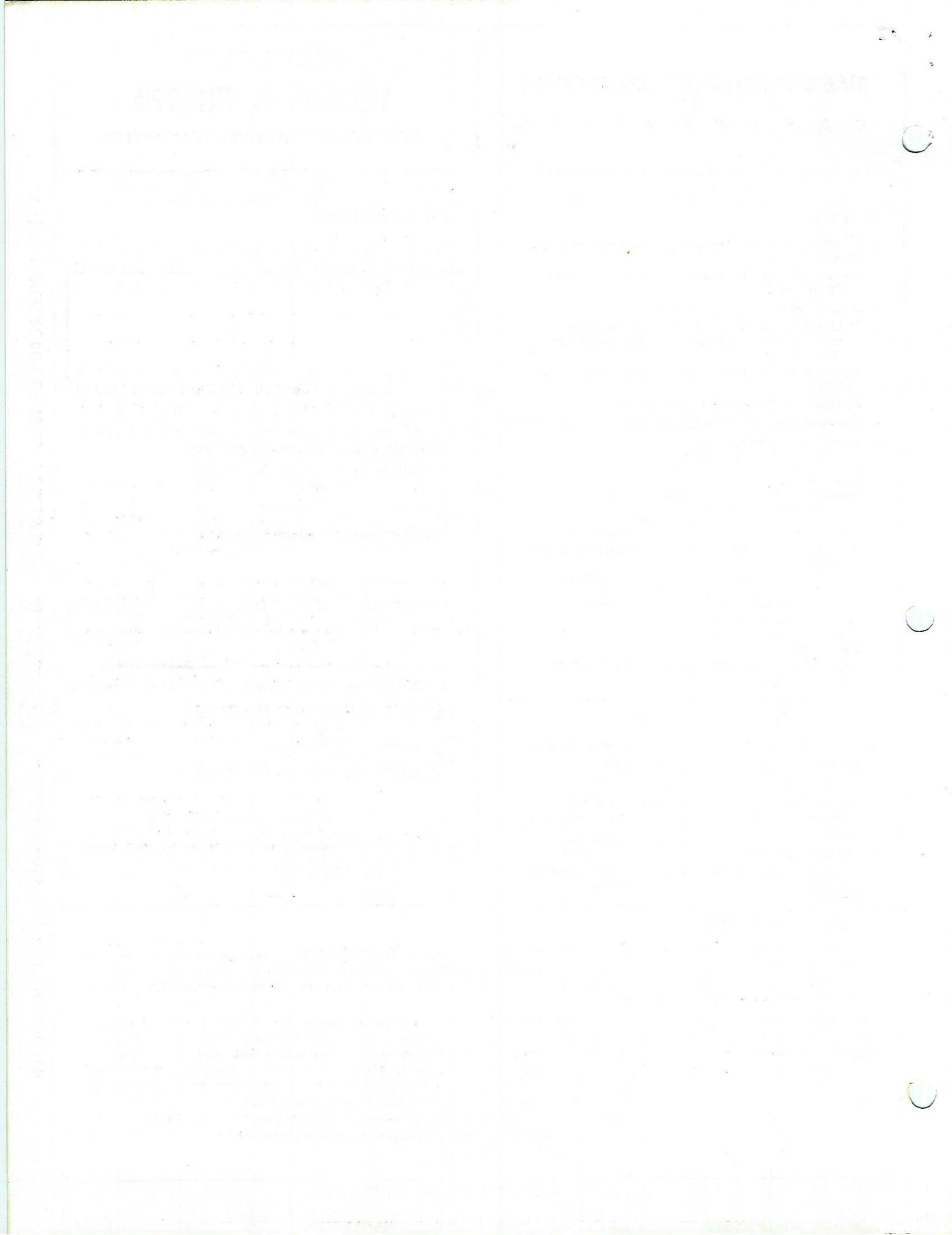


TR1602A CERAMIC PACKAGE OUTLINE



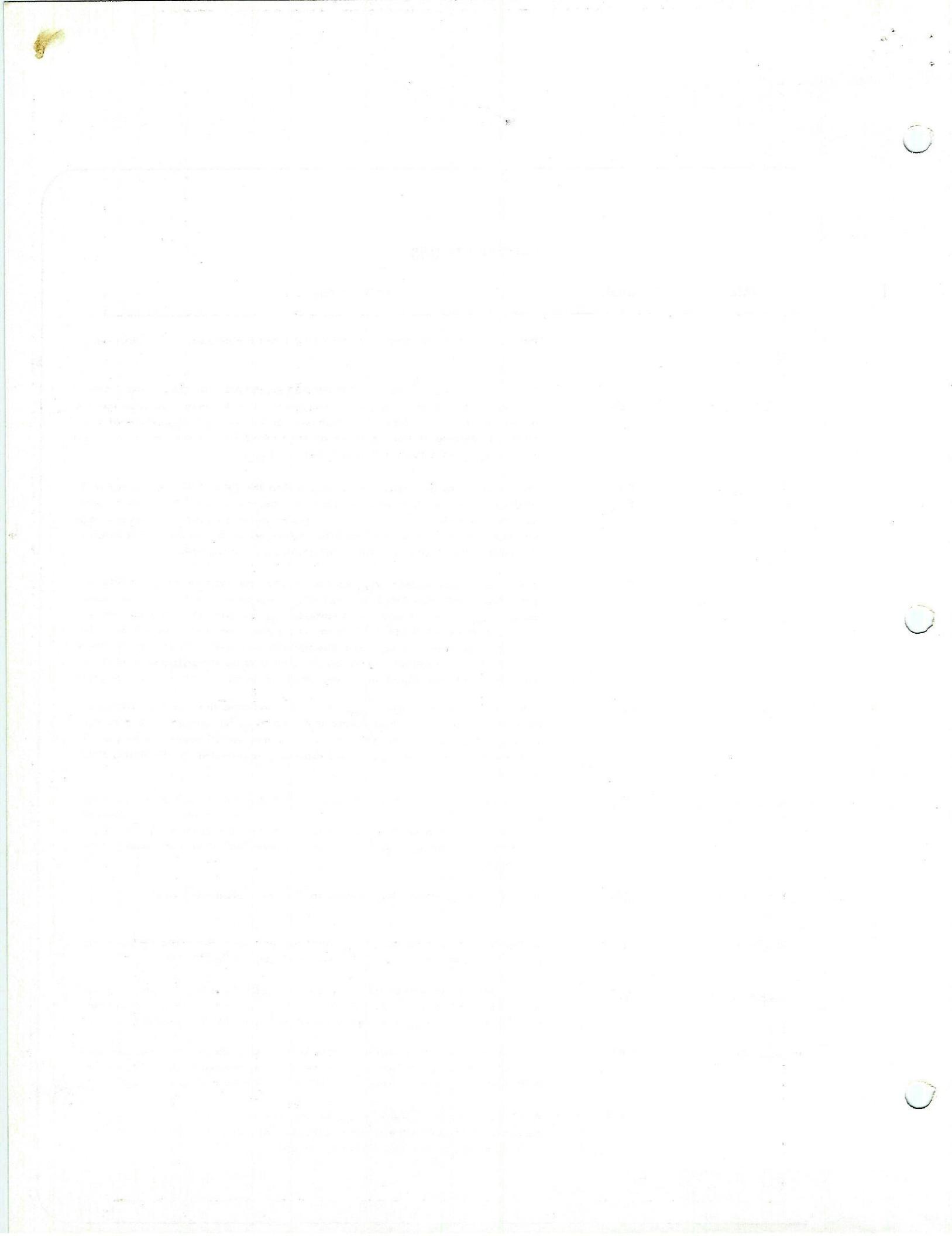
TR1602B HERMETIC PLASTIC CAVITY PACKAGE OUTLINE

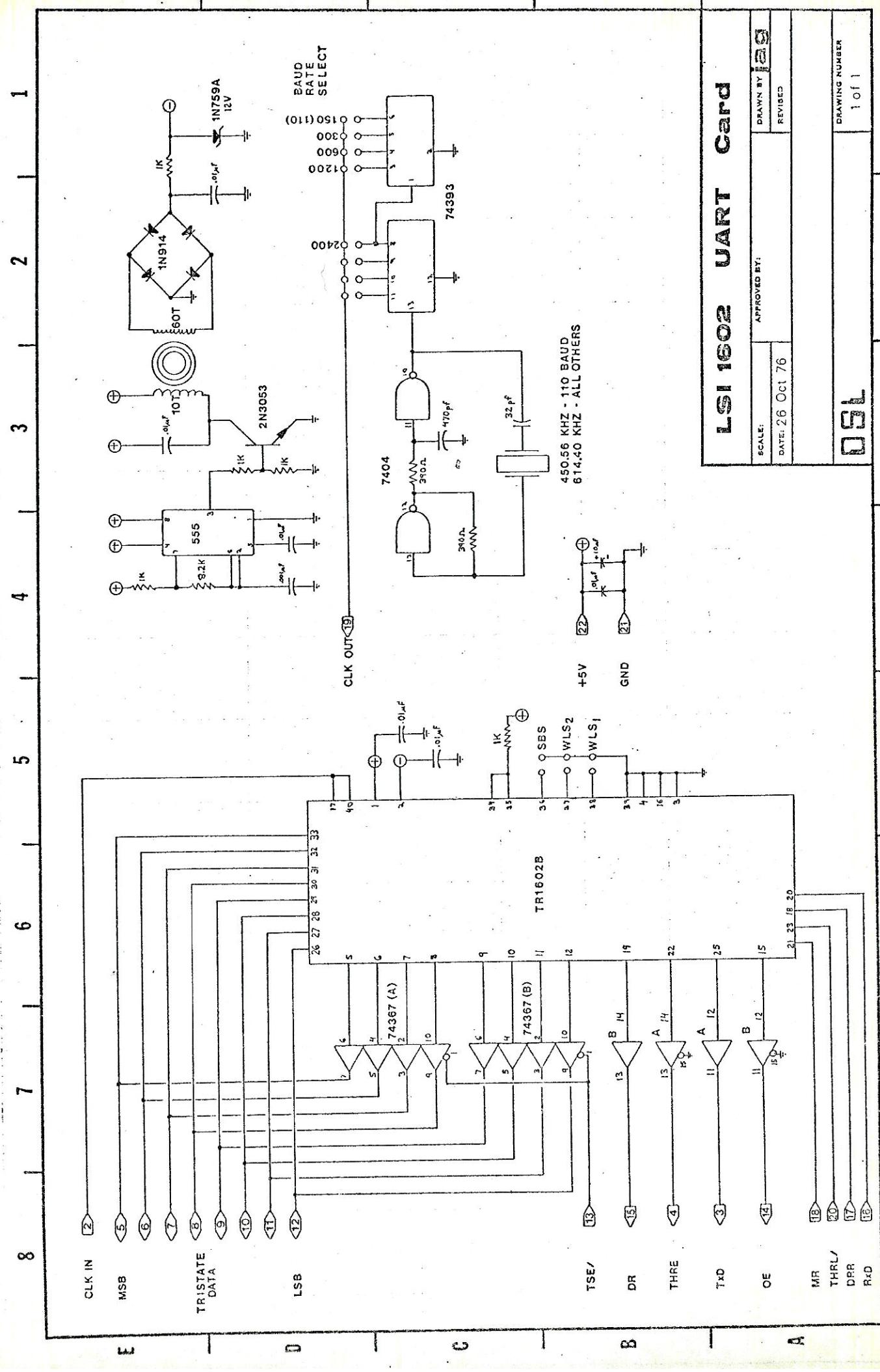


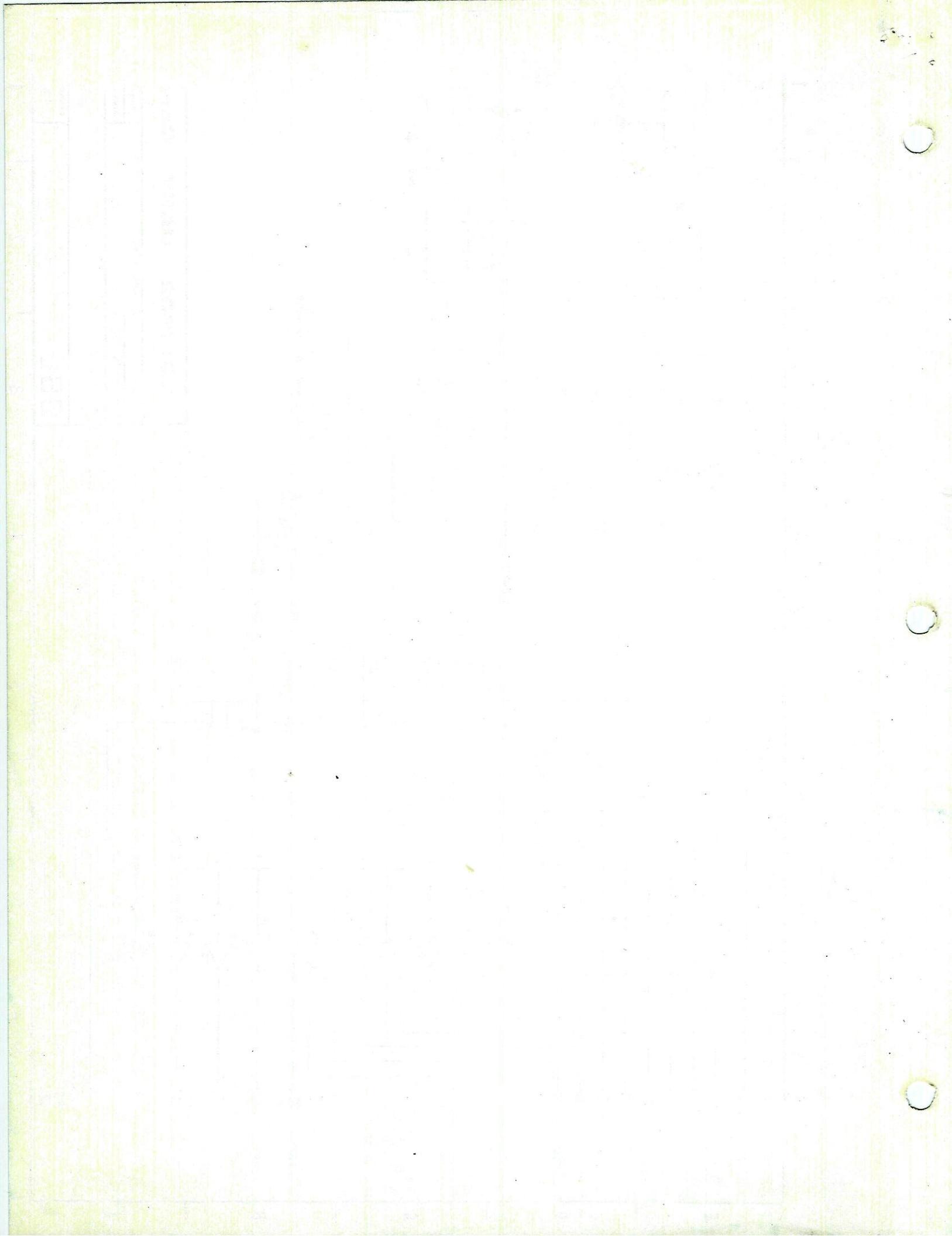


PIN DEFINITIONS

NAME	SYMBOL	FUNCTION
Clock	C	The clock frequency is sixteen (16) times the desired shift rate.
Data Out	DO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH} . Start of transmission is defined as the transition of the START bit from a high-level output voltage, V_{OH} , to a low-level output voltage, V_{OL} .
Transmitter Register Data Inputs	TR ₁ - TR ₈	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected the character is right justified to the least significant bit, RR ₁ , and the excess bits are disregarded. A high-level input voltage, V_{IH} , will cause a high-level output voltage, V_{OH} , to be transmitted.
Transmitter Holding Register Load	THRL	A low-level input voltage, V_{IL} , applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL} , to a high-level input voltage, V_{IH} , transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
Overrun Error	OE	A high-level output voltage, V_{OH} , on this line indicates that the Data REceived Flag (pin 19) was not reset before the next character was transferred to the REceiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
Receiver Holding Register Data	RR ₈ - RR ₁	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines. For character formats of fewer than eight bits received characters are right-justified with RR ₁ (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL} .
Data Received Reset	DRR	A low-level input voltage, V_{IL} , applied to this line resets the DR line.
Data Received	DR	A high-level output voltage, V_{OH} , indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
Data In	DI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH} , must be present when data is not being received.
Master Reset	MR	This line is strobed to a high-level input voltage, V_{IH} , to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH} .
Transmitter Holding Register Empty	THRE	A high-level output Voltage, V_{OH} , on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.

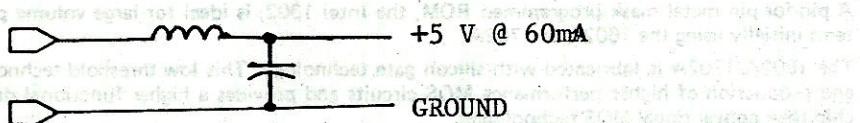




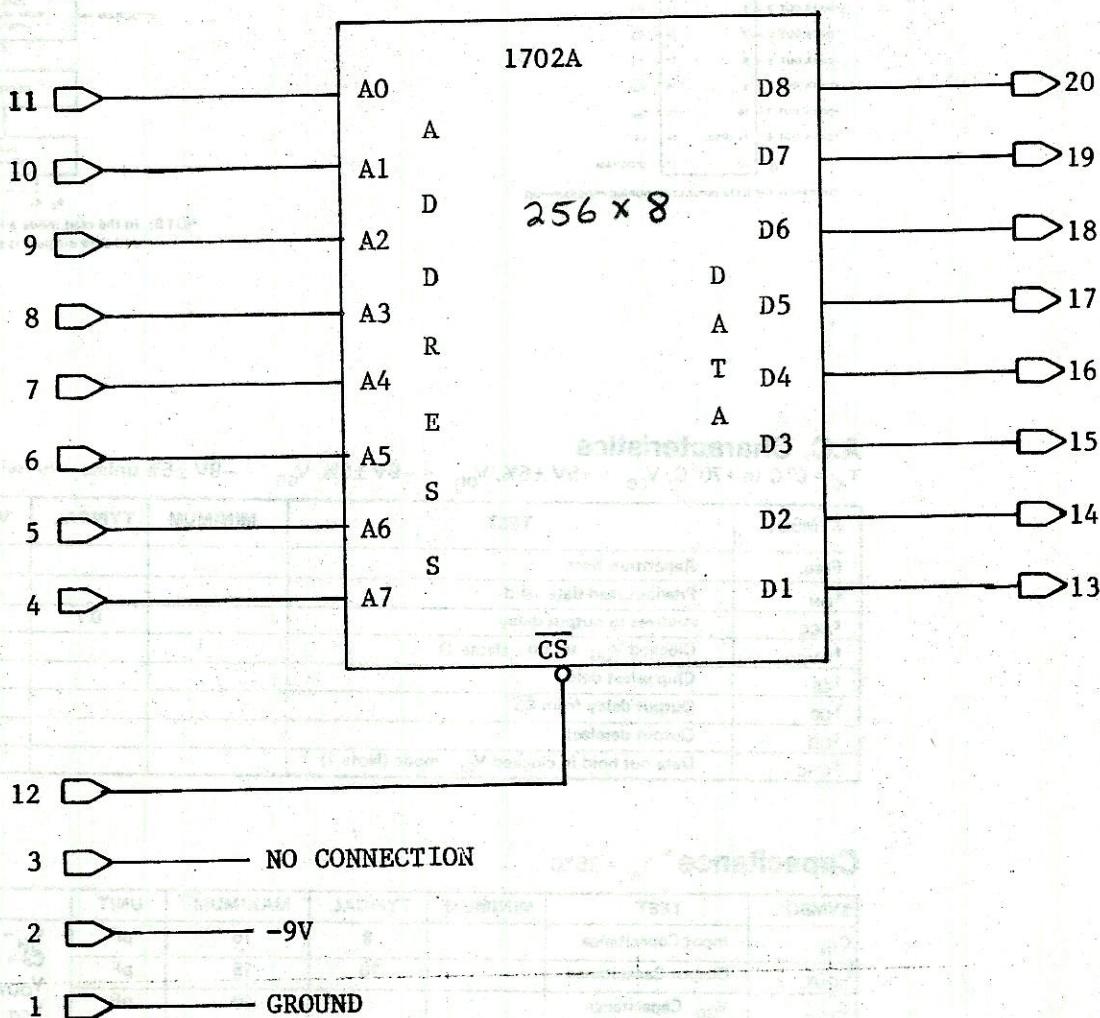


PROGRAMMABLE READ ONLY MEMORY

This document describes the 1702A programmable read only memory chip. It contains 256 words by 8 bits of memory. The chip is programmed via a serial port on pin 11. Addressing is done via pins A0-A7. The outputs are tristate and enable via CS.



1702A Pinout Diagram

**NOTE:**

1. EACH ADDRESS LINE = 1 LOAD
2. OUTPUTS ARE TRISTATE, ENABLED WHEN CS LOW. EACH OUTPUT CAN DRIVE ONLY 1 TTL LOAD.

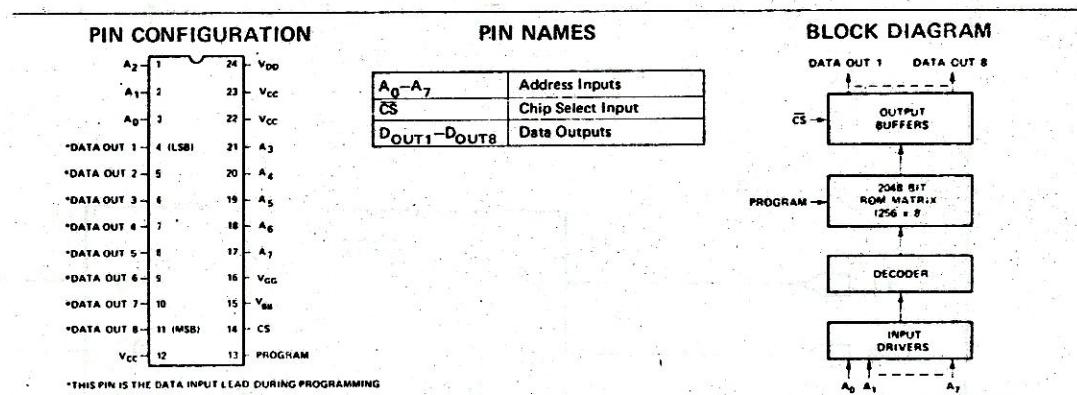
The 1602A and 1702A are 256 word by 8-bit electrically programmable ROMs ideally suited for uses where fast turn-around and pattern experimentation are important. The 1602A and 1702A undergo complete programming and functional testing on each bit position prior to shipment, thus insuring 100% programmability.

The 1602A and 1702A use identical chips. The 1702A is packaged in a 24 pin dual in-line package with a transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device. The 1602A is packaged in a 24 pin dual in-line package with a metal lid and is not erasable.

The circuitry of the 1602A/1702A is entirely static; no clocks are required.

A pin-for-pin metal mask programmed ROM, the Intel 1302, is ideal for large volume production runs of systems initially using the 1602A or 1702A.

The 1602A/1702A is fabricated with silicon gate technology. This low threshold technology allows the design and production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.



U.S. Patent No. 3660819

A.C. Characteristics

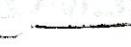
$T_A = 0^\circ C$ to $+70^\circ C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, $V_{GG} = -9V \pm 5\%$ unless otherwise noted

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT
Freq.	Repetition Rate			1	MHz
t_{OH}	Previous read data valid			100	ns
t_{ACC}	Address to output delay		0.7	1	μs
t_{DVGG}	Clocked V_{GG} set up (Note 1)	1			μs
t_{CS}	Chip select delay			100	ns
t_{CO}	Output delay from CS			900	ns
t_{OD}	Output deselect			300	ns
t_{OHC}	Data out hold in clocked V_{GG} mode (Note 1)			5	μs

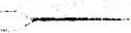
Capacitance * $T_A = 25^\circ C$

SYMBOL	TEST	MINIMUM	TYPICAL	MAXIMUM	UNIT	CONDITIONS
C_{IN}	Input Capacitance		8	15	pF	$V_{IN} = V_{CC}$ $CS = V_{CC}$ $V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$
C_{OUT}	Output Capacitance		10	15	pF	All unused pins are at A.C. ground
C_{VGG}	V_{GG} Capacitance (Note 1)			30	pF	

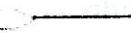
*This parameter is periodically sampled and is not 100% tested.

22  +  → +5V @ 433 mA max.

21   Ground

19 

18 

17 

12 

6  Read / WRITE

11  A₉

10  A₈

9  A₇

8  A₆

7  A₅

5  A₄

4  A₃

3  A₂

2  A₁

1  A₀

20  OUTPUT ENABLE

Data Outputs

D₃ D₂ D₁ D₀

13

14

15

16

Inputs: 1 TTL load each

Outputs: Open-Collector type - external pull-up required
 Maximum sinking capability at low-level output - 48 mA
 Maximum current stolen at high-level output - 1/4 mA
 Maximum allowable voltage at output - 5V

Reading: Access time - 1 us (1000 ns) max.

Old data valid after changing address - 50 ns min.

Writing: Address setup time before asserting "WRITE" - 200 ns min
 "WRITE" pulse width - 750 ns min.

Address hold time after removing "WRITE" - 75 ns min.

Data setup time before "WRITE" can fall - 800 ns min.

Data hold time after removing "WRITE" - 125 ns min.

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

- Single +5 Volts Supply Voltage
- Directly TTL Compatible — All Inputs and Output
- Static MOS — No Clocks or Refreshing Required
- Low Power — Typically 150 mW
- Access Time — Typically 500 nsec
- Three-State Output — OR-Tie Capability

- Simple Memory Expansion — Chip Enable Input
- Fully Decoded — On Chip Address Decode
- Inputs Protected — All Inputs Have Protection Against Static Charge
- Low Cost Packaging — 16 Pin Plastic Dual-In-Line Configuration

The Intel 2102 is a 1024 word by one bit static random access memory element using normally off N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

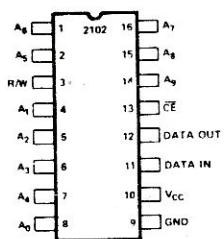
The 2102 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, output, and a single +5 volt supply. A separate chip enable (CE) lead allows easy selection of an individual package when outputs are OR-tied.

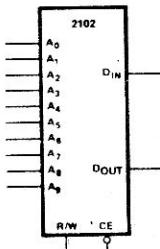
The Intel 2102 is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance easy to use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost silicone packaging.

PIN CONFIGURATION



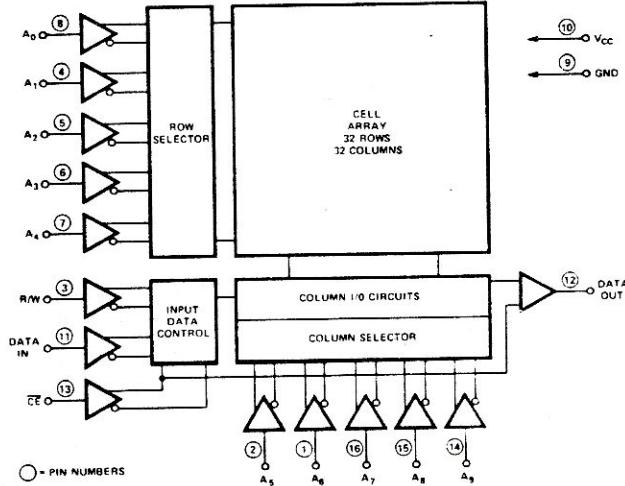
LOGIC SYMBOL



PIN NAMES

D _{IN}	DATA INPUT	CE	CHIP ENABLE
A ₀ - A ₉	ADDRESS INPUTS	D _{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V _{CC}	POWER (+5V)

BLOCK DIAGRAM



○ = PIN NUMBERS

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage On Any Pin With Respect To Ground	-0.5V to +7V
Power Dissipation	1 Watt

***COMMENT:**

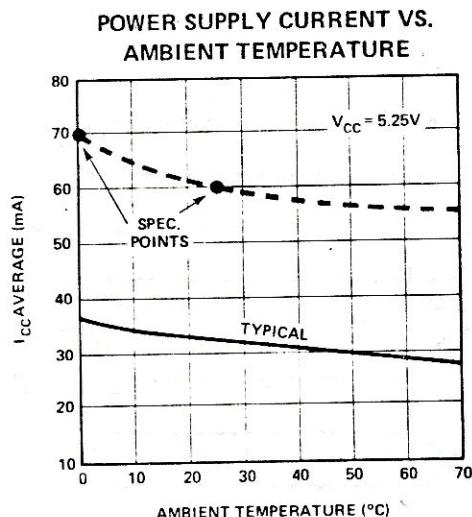
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. and Operating Characteristics

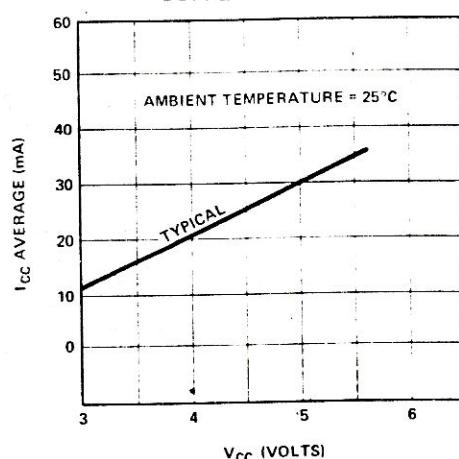
$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP. ⁽¹⁾	MAX.		
I_{LI}	INPUT LOAD CURRENT (ALL INPUT PINS)			10	μA	$V_{IN} = 0$ to 5.25V
I_{LOH}	OUTPUT LEAKAGE CURRENT			10	μA	$\overline{CE} = 2.2\text{V}$, $V_{OUT} = 4.0\text{V}$
I_{LOL}	OUTPUT LEAKAGE CURRENT			-100	μA	$\overline{CE} = 2.2\text{V}$, $V_{OUT} = 0.45\text{V}$
I_{CC1}	POWER SUPPLY CURRENT		30	60	mA	ALL INPUTS = 5.25V DATA OUT OPEN $T_A = 25^\circ\text{C}$
I_{CC2}	POWER SUPPLY CURRENT			70	mA	ALL INPUTS = 5.25V DATA OUT OPEN $T_A = 0^\circ\text{C}$
V_{IL}	INPUT "LOW" VOLTAGE	-0.5		+0.65	V	
V_{IH}	INPUT "HIGH" VOLTAGE	2.2		V_{CC}	V	
V_{OL}	OUTPUT "LOW" VOLTAGE			+0.45	V	$I_{OL} = 1.9\text{mA}$
V_{OH}	OUTPUT "HIGH" VOLTAGE	2.2			V	$I_{OH} = -100\mu\text{A}$

(1) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

Typical D.C. Characteristics

POWER SUPPLY CURRENT VS.
SUPPLY VOLTAGE



A. C. Characteristics $T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5\text{V} \pm 5\%$ unless otherwise specified

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN.	TYP. ⁽¹⁾	MAX.	
READ CYCLE					
t_{RC}	READ CYCLE	1000			ns
t_A	ACCESS TIME		500	1000	ns
t_{CO}	CHIP ENABLE TO OUTPUT TIME			500	ns
t_{OH1}	PREVIOUS READ DATA VALID WITH RESPECT TO ADDRESS	50			ns
t_{OH2}	PREVIOUS READ DATA VALID WITH RESPECT TO CHIP ENABLE	0			ns
WRITE CYCLE					
t_{WC}	WRITE CYCLE	1000			ns
t_{AW}	ADDRESS TO WRITE SETUP TIME	200			ns
t_{WP}	WRITE PULSE WIDTH	750			ns
t_{WR}	WRITE RECOVERY TIME	50			ns
t_{DW}	DATA SETUP TIME	800			ns
t_{DH}	DATA HOLD TIME	100			ns
t_{CW}	CHIP ENABLE TO WRITE SETUP TIME	900			ns

(1) Typical values are for $T_A=25^\circ\text{C}$ and nominal supply voltage.
Capacitance $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$
A.C. CONDITIONS OF TEST

Input Pulse Levels: +0.65 Volt to 2.2 Volt

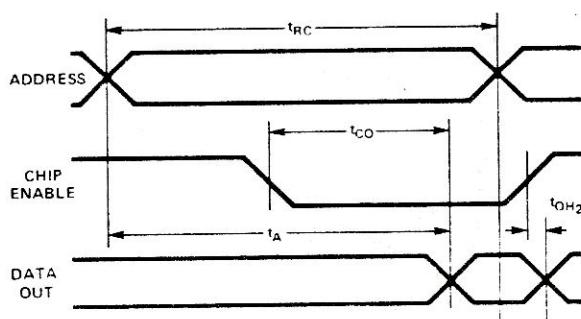
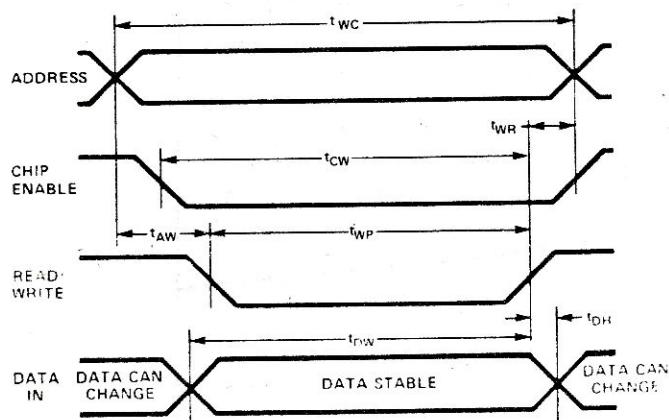
Input Pulse Rise and Fall Times: 20nsec

Timing Measurement Reference Level: 1.5 Volt

Output Load: 1 TTL Gate and $C_L = 100\text{ pF}$

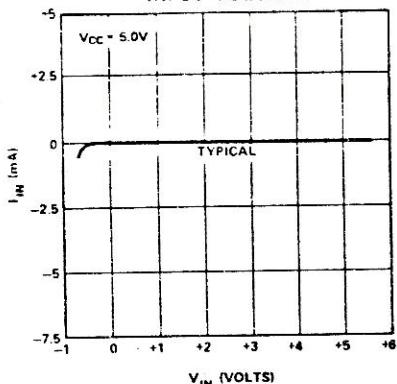
SYMBOL	TEST	LIMITS (pF)	
		TYP.	MAX.
C_{IN}	INPUT CAPACITANCE (ALL INPUT PINS) $V_{IN} = 0\text{V}$	3	5
C_{OUT}	OUTPUT CAPACITANCE $V_{OUT} = 0\text{V}$	7	10

Waveforms

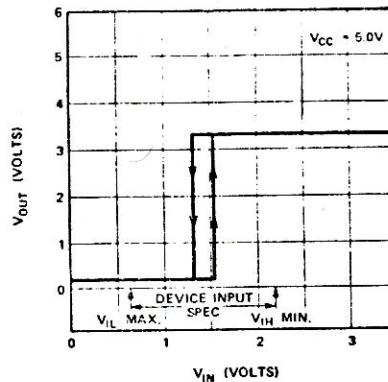
READ CYCLE

WRITE CYCLE


Typical D. C. Characteristics

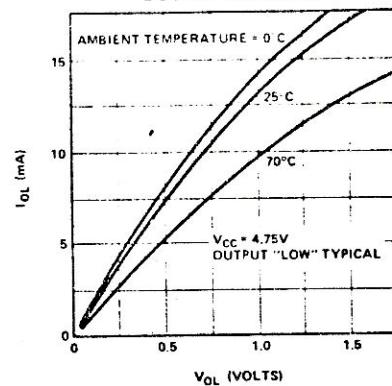
INPUT CURRENT VS.
INPUT VOLTAGE



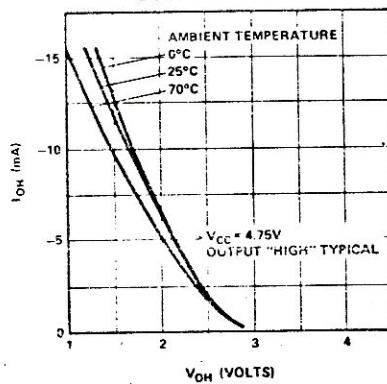
EFFECTIVE INPUT
CHARACTERISTIC



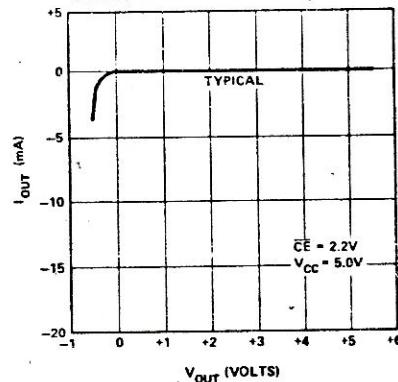
OUTPUT SINK CURRENT VS.
OUTPUT VOLTAGE



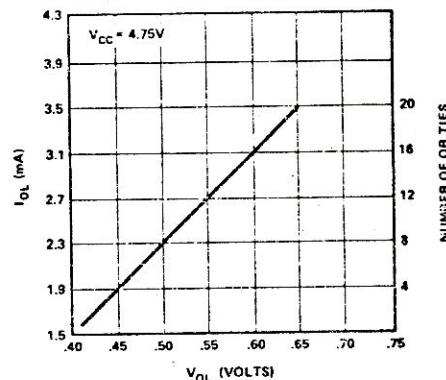
OUTPUT SOURCE CURRENT VS.
OUTPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT
VOLTAGE WITH CHIP DISABLED

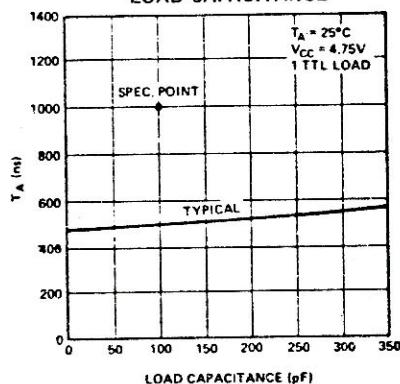


RELATIONSHIP BETWEEN OUTPUT
SINK CURRENT, NUMBER OF OR-TIES,
AND OUTPUT VOLTAGE



Typical A. C. Characteristics

ACCESS TIME VS.
LOAD CAPACITANCE



ACCESS TIME VS.
AMBIENT TEMPERATURE

