MC74HC589A

8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

High−Performance Silicon−Gate CMOS

The MC74HC589A device consists of an 8−bit storage latch which feeds parallel data to an 8−bit shift register. Data can also be loaded serially (see the Function Table). The shift register output, Q_H, is a 3−state output, allowing this device to be used in bus−oriented systems.

The HC589A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.
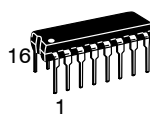
Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates
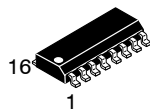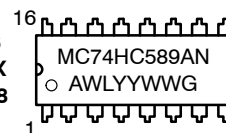- These Devices are Pb−Free, Halogen Free and are RoHS Compliant
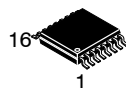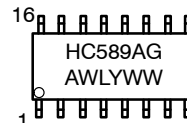
ON Semiconductor®

MARKING DIAGRAMS

PDIP−16
N SUFFIX
CASE 648

MC74HC589AN
AWLYYWWG

SOIC−16
D SUFFIX
CASE 751B

HC589AG
AWLYWW

TSSOP−16
DT SUFFIX
CASE 948F

HC
589A
ALYW▪
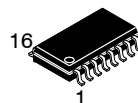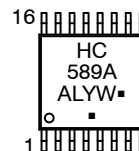
SOEIAJ−16
F SUFFIX
CASE 966

74HC589A
ALYWG
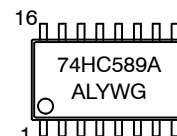
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb−Free Package
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC74HC589A
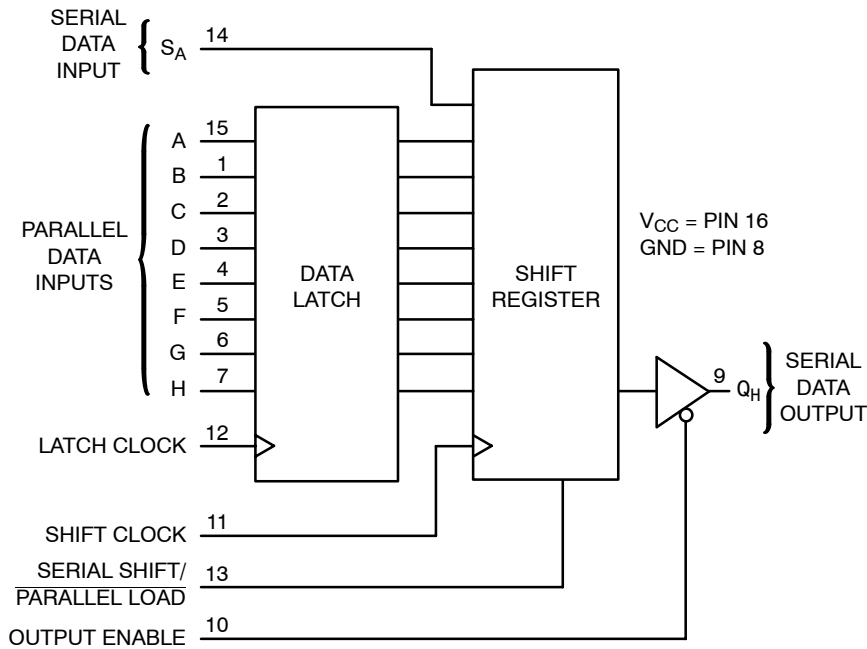
Figure 1. Logic Diagram

V_{CC} = PIN 16
GND = PIN 8
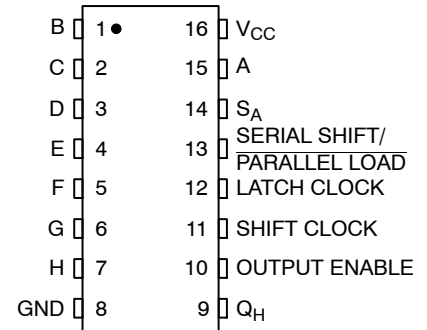
Figure 2. Pin Assignment

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74HC589ANG	PDIP−16 (Pb−Free)	25 Units / Rail
MC74HC589ADG	SOIC−16 (Pb−Free)	48 Units / Rail
MC74HC589ADR2G	SOIC−16 (Pb−Free)	2500 Tape & Reel
MC74HC589ADTR2G	TSSOP−16*	2500 Tape & Reel
MC74HC589AFELG	SOEIAJ−16 (Pb−Free)	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	-0.5 to $+7.0$	V
V_{in}	DC Input Voltage	(Referenced to GND)	$-0.5 \leq V_{CC} + 0.5$	V
V_{out}	DC Output Voltage	(Referenced to GND)	$-0.5 \leq V_{CC} + 0.5$	V
I_{in}	DC Input Current, per Pin		± 20	mA
I_{out}	DC Output Current, per Pin		± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		± 75	mA
I_{GND}	DC Ground Current per Ground Pin		± 75	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		$+150$	°C
θ_{JA}	Thermal Resistance	PDIP SOIC TSSOP	78 112 148	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL 94 V–0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>4000 >200 >1000	V
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND at 85°C (Note 4)	± 300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage	(Referenced to GND)	2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage	(Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	$V_{CC} = 2.0$ V $V_{CC} = 3.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	0 0 0	1000 800 500 400	ns

5. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND, Note NO TAG)

Symbol	Parameter	Test Conditions		V_{CC} V	Guaranteed Limit			Unit
					−55°C to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\lvert I_{out} \rvert \leq$ 20 μA		2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\lvert I_{out} \rvert \leq$ 20 μA		2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\lvert I_{out} \rvert \leq$ 20 μA		2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL}	$\lvert I_{out} \rvert \leq$ 2.4 mA $\lvert I_{out} \rvert \leq$ 6.0 mA $\lvert I_{out} \rvert \leq$ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} $\lvert I_{out} \rvert \leq$ 20 μA		2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL}	$\lvert I_{out} \rvert \leq$ 2.4 mA $\lvert I_{out} \rvert \leq$ 6.0 mA $\lvert I_{out} \rvert \leq$ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND		6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND		6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA		6.0	4	40	160	μA

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns, Notes NO TAG and NO TAG)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$-55°C$ to $25°C$	$\leq 85°C$	$\leq 125°C$	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 4 and 10)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to Q_H (Figures 3 and 10)	2.0 3.0 4.5 6.0	175 100 40 30	225 110 50 40	275 125 60 50	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to Q_H (Figures 4 and 10)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Serial Shift/Parallel Load to Q_H (Figures 6 and 10)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q_H (Figures 5 and 11)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q_H (Figures 5 and 11)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 10)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)	–	15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Package)*	50	pF

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}{}^2 f + I_{CC} V_{CC}$.

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TIMING REQUIREMENTS (Input $t_r = t_f = 6$ ns, Note NO TAG)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55°C to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, A–H to Latch Clock (Figure 7)	2.0 3.0 4.5 6.0	100 40 20 17	125 50 25 21	150 60 30 26	ns
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 8)	2.0 3.0 4.5 6.0	100 40 20 17	125 50 25 21	150 60 30 26	ns
t_{su}	Minimum Setup Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Shift Clock (Figure 9)	2.0 3.0 4.5 6.0	100 40 20 17	125 50 25 21	150 60 30 26	ns
t_h	Minimum Hold Time, Latch Clock to A–H (Figure 7)	2.0 3.0 4.5 6.0	25 10 5 5	30 12 6 6	40 15 8 7	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 8)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 4)	2.0 3.0 4.5 6.0	75 40 15 13	95 50 19 16	110 60 23 19	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 3)	2.0 3.0 4.5 6.0	80 40 16 14	100 50 20 17	120 60 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 6)	2.0 3.0 4.5 6.0	80 40 16 14	100 50 20 17	120 60 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

FUNCTION TABLE

	Inputs						Resulting Function		
Operation	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A–H	Data Latch Contents	Shift Register Contents	Output Q_H
Force Output into High Impedance State	H	X	X	X	X	X	X	X	Z
Load Parallel Data into Data Latch	L	H	⌐	L, H, ⌐	X	a–h	a–h	U	U
Transfer Latch Contents to Shift Register	L	L	L, H, ⌐	X	X	X	U	$LR_N \rightarrow SR_N$	LR_H
Contents of Input Latch and Shift Register are Unchanged	L	H	L, H, ⌐	L, H, ⌐	X	X	U	U	U
Load Parallel Data into Data Latch and Shift Register	L	L	⌐	X	X	a–h	a–h	a–h	h
Shift Serial Data into Shift Register	L	H	X	⌐	D	X	*	$SR_A = D$, $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$
Load Parallel Data in Data Latch and Shift Serial Data into Shift Register	L	H	⌐	⌐	D	a–h	a–h	$SR_A = D$, $SR_N \rightarrow SR_{N+1}$	$SR_G \rightarrow SR_H$

LR = latch register contents
SR = shift register contents
a–h = data at parallel data inputs A–H
D = data (L, H) at serial data input S_A

U = remains unchanged
X = don't care
Z = high impedance
* = depends on Latch Clock input

Switching Waveforms
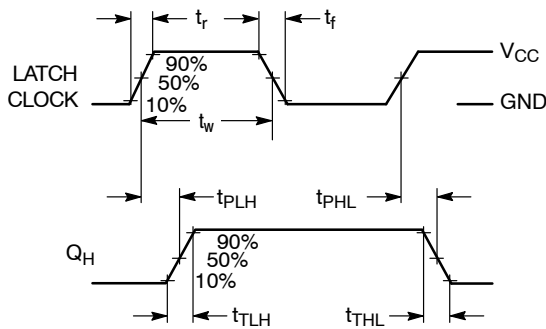
Figure 3. (Serial Shift/Parallel Load = L)
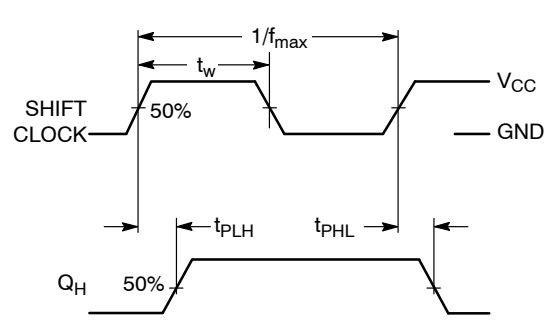
Figure 4. (Serial Shift/Parallel Load = H)
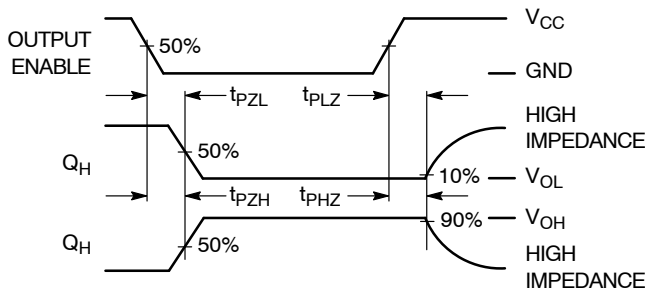
Figure 5.
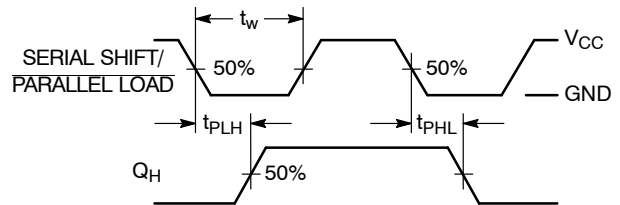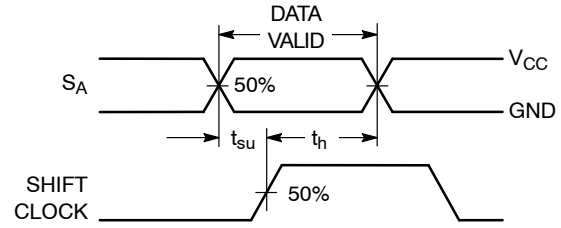

Figure 6.

Switching Waveforms
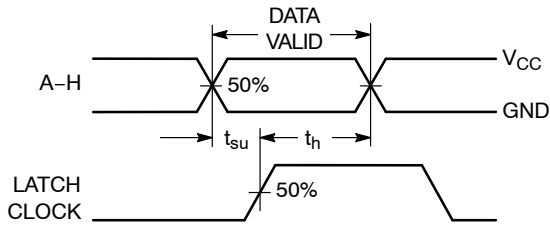
Figure 7.

Figure 8.
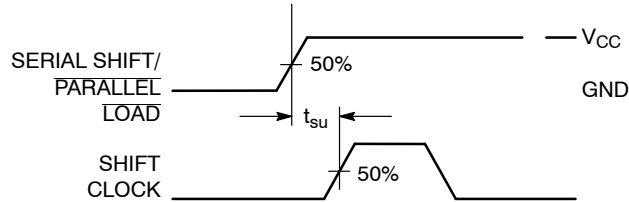
Figure 9.
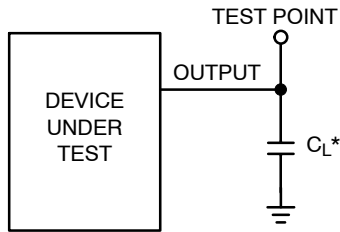
*Includes all probe and jig capacitance.

Figure 10. Test Circuit

CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}.
CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.
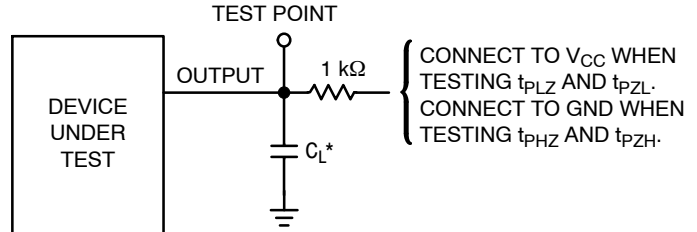
*Includes all probe and jig capacitance.

Figure 11. Test Circuit

Pin Descriptions

Data Inputs

A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

S_A (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/$\overline{\text{Parallel Load}}$ is high. Data on this input is ignored when Serial Shift/$\overline{\text{Parallel Load}}$ is low.

Control Inputs

Serial Shift/$\overline{\text{Parallel Load}}$ (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

Shift Clock (Pin 11)

Serial shift clock. A low−to−high transition on this input shifts data on the serial data input into the shift register and

data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Data latch clock. A low−to−high transition on this input loads the parallel data on inputs A−H into the data latch.

Output Enable (Pin 10)

Active−low output enable A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

Output

Q_H (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register. This is a 3−state output.
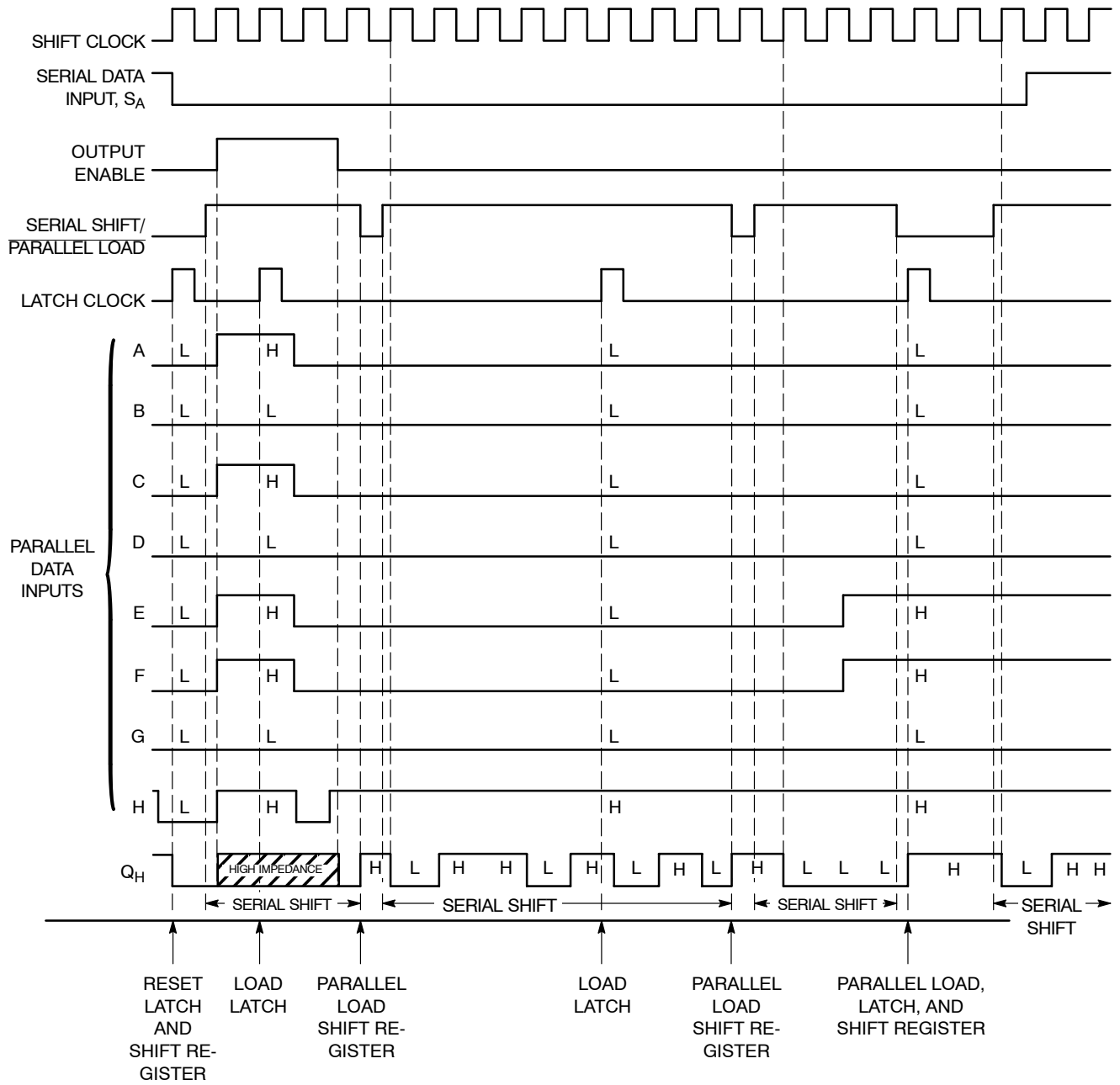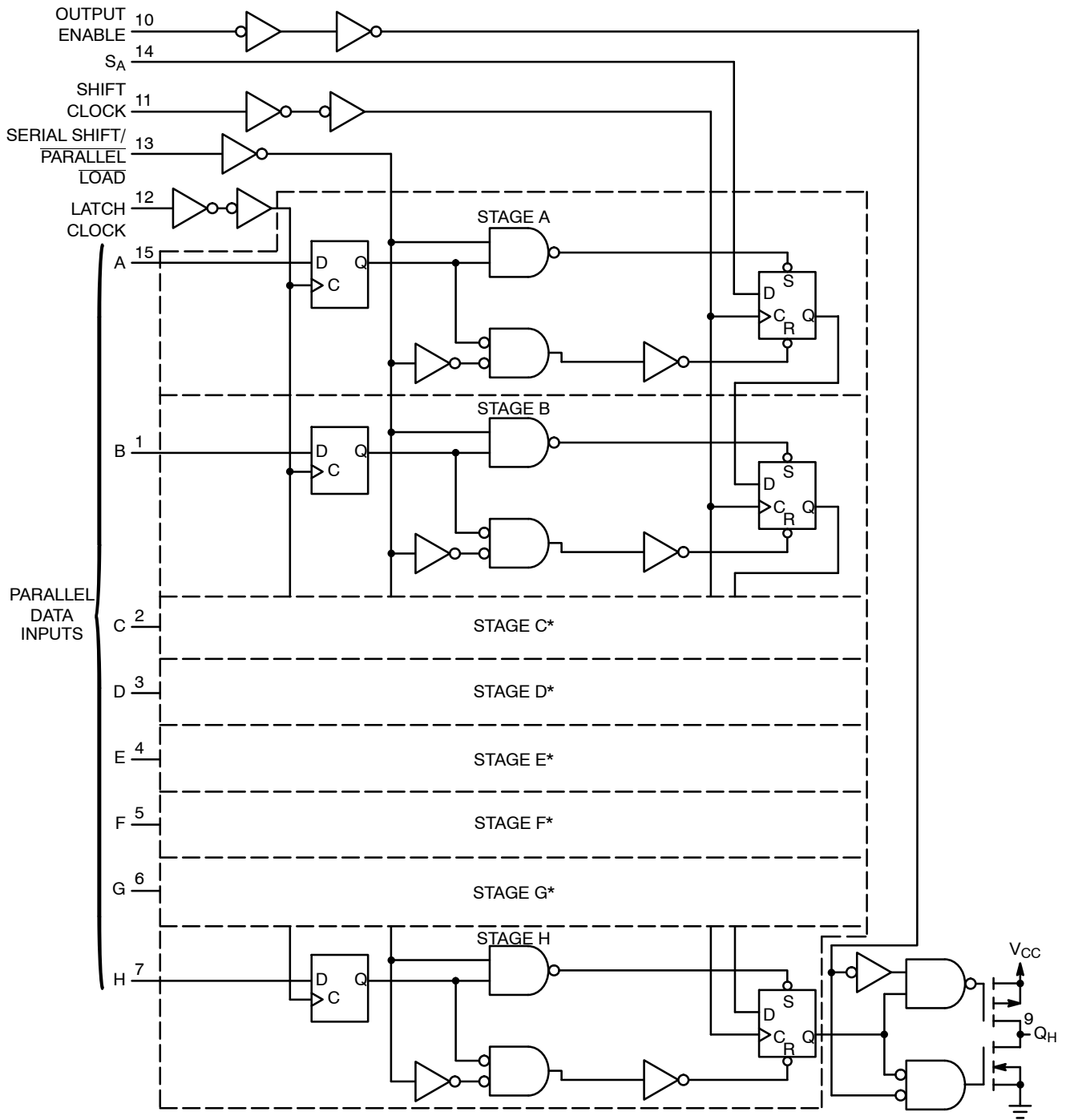
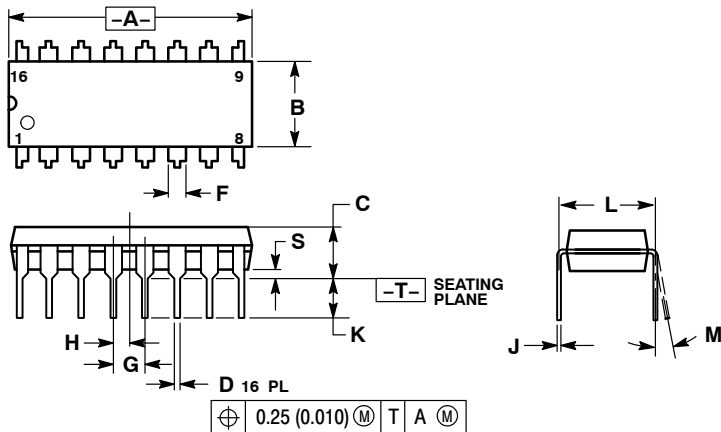# MC74HC589A

Figure 12. Timing Diagram

MC74HC589A

*Stages C thru G (not shown in detail) are identical to stages A and B above.

Figure 13. Logic Detail

MC74HC589A

PACKAGE DIMENSIONS

PDIP−16
CASE 648−08
ISSUE T

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

MC74HC589A
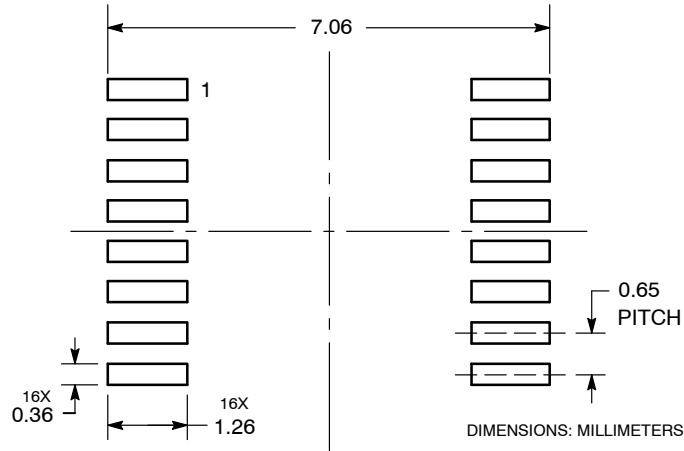
PACKAGE DIMENSIONS

SOIC−16
CASE 751B−05
ISSUE K
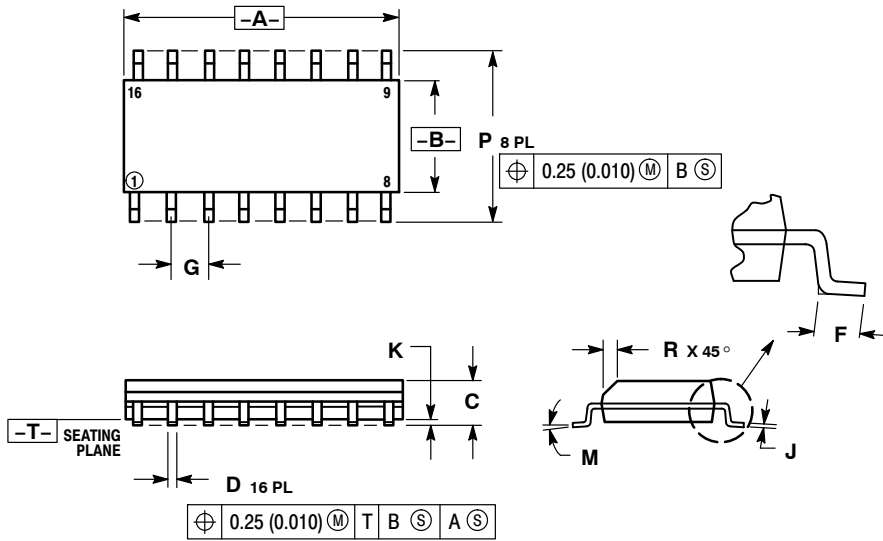
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT

DIMENSIONS: MILLIMETERS
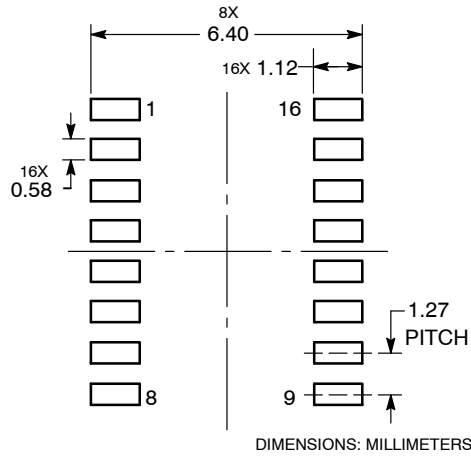
MC74HC589A

PACKAGE DIMENSIONS

TSSOP−16
CASE 948F−01
ISSUE B
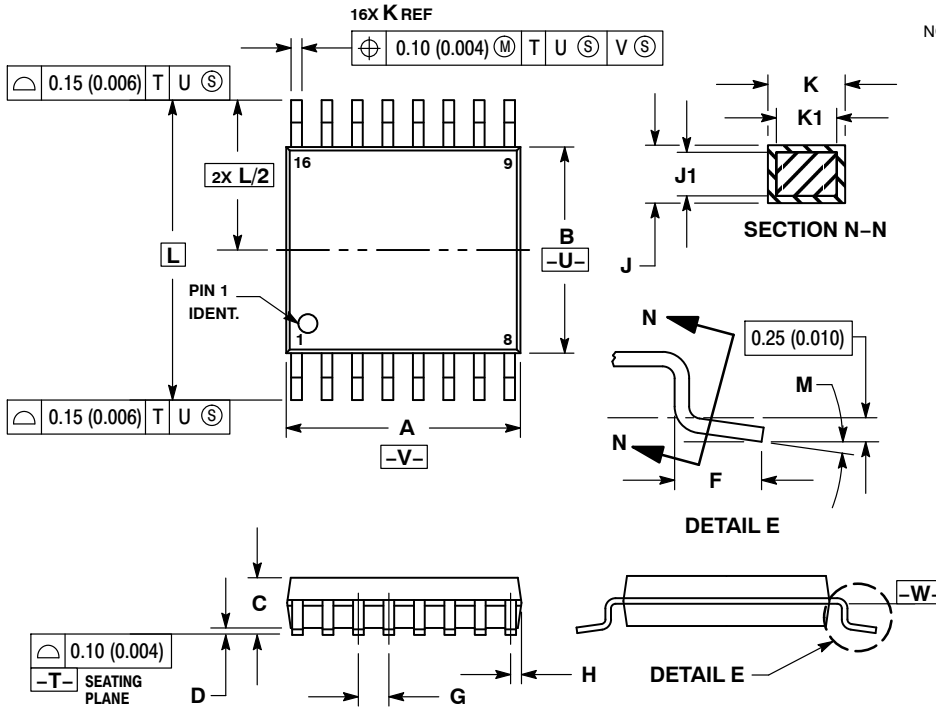
16X **K** REF

⊕ | 0.10 (0.004) Ⓜ | T | U Ⓢ | V Ⓢ

△ | 0.15 (0.006) | T | U Ⓢ

2X **L/2**

L

PIN 1
IDENT.

16

9

B
−U−

1

8

△ | 0.15 (0.006) | T | U Ⓢ

A
−V−

C

△ | 0.10 (0.004)
−T− SEATING
PLANE

D

G

H

K

K1

J1

J

SECTION N−N

N

0.25 (0.010)

M

N

F

DETAIL E

−W−

DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

MC74HC589A

PACKAGE DIMENSIONS

SOEIAJ–16
CASE 966–01
ISSUE A
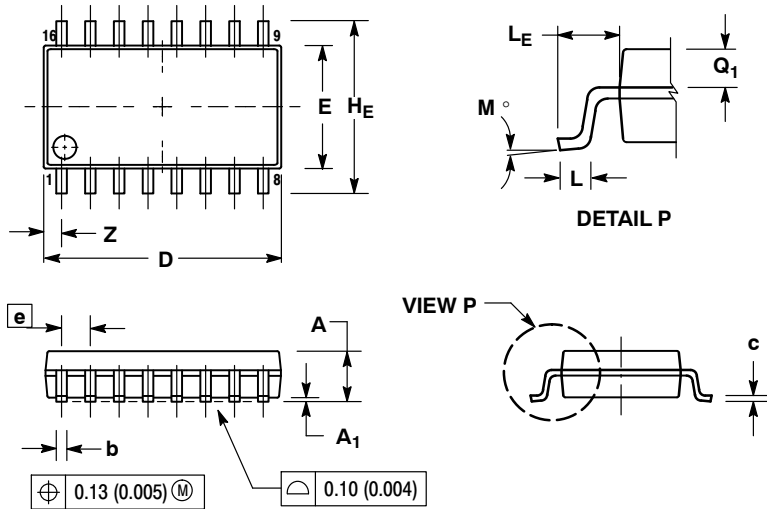
DETAIL P

VIEW P

⊕ 0.13 (0.005) Ⓜ   ◁ 0.10 (0.004)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A$_1$	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H$_E$	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L$_E$	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q$_1$	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

MC74HC589A/D