IT6563

Single Chip 4 Lane DisplayPort1.2 to HDMI2.0 Converter with Embedded MCU

Preliminary Datasheet

Specification V0.92

ITE TECH. INC.

1. General Description

The IT6563FN is a high-performance single-chip DisplayPort to HDMI converter. Combined with DisplayPort receiver and HDMI transmitter, the IT6563FN support DisplayPort input and HDMI output by conversion function.

The build-in DisplayPort receiver is fully compatible with DisplayPort 1.2a and HDCP 1.3/2.2 specifications. With 4-lane HBR2 (High-Bit-Rate 2) configuration, the DP receiver can support VESA resolution up to WUXGA (1920x1200 @120Hz) or WQXGA (2560X1600 RB @120Hz) or support CEA resolution up to 1080P@120Hz or 4Kx2K@60Hz. This DisplayPort receiver also supports MCCS over AUX channel.

The build-in HDMI transmitter is a high-performance HDMI 2.0 transmitter, fully compliant with HDMI 2.0, HDCP 1.4/2.2 and backward compatible to DVI 1.0 specifications. This HDMI transmitter can support color depth up to 36bits (12bits/color) and ensures robust transmission of high-quality uncompressed video content. Aside from the various video output formats supported, this HDMI transmitter also support 8 channels digital audio, with sampling rate up to 192kHz and sample size up to 24 bits, and HBR audio.

With embedded MCU and Flash, IT6563FN is easy to program through the ISP interface or DP AUX channel. Customers need no external Flash and MCU, can save the BOM cost and board size.

Each IT6563FN comes preprogrammed with an unique HDCP key, in compliance with the 1.3/2.2 --Amendment for DisplayPort, rev1.0 and HDCP 1.4/2.2--HDMI compliance standard so as to provide secure transmission of high-definition content. Users of the IT6563FN need not purchase any HDCP keys or ROMs.

2. Features

2.1 DisplayPort Receiver

- Compliance with DisplayPort Specification **V1.2a** at **1.62/2.7/5.4 Gbps** data rate (Low bit rate/High bit rate/High bit rate 2)
- Support flexible **1/2/4** lanes configurations; Full **21.6Gbps** data rate support (4 lanes at 5.4Gbps)
- Support DPCD **Rev.1.2**
- Support metadata transport for static High Dynamic Range (HDR) for 4K60 422/420 mode.
- Support HDCP **1.3**/**2.2** with HDCP key embedded
- Support MCCS over AUX
- Support 3D display left/right field/frame
- Support Spread Spectrum Clocking up to **0.5%** down-spread to reduce EMI
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.
- Support 8-channel, uncompressed LPCM I2S audio with sample rates of 32~192 kHz and sample sizes of 16~24 bits, and HBR audio.
- Automatic loss of signal detection for Link management
- Intelligent, programmable power management
- Embedded two blocks EDID RAM to saving BOM cost
- Compliance with “DP only” or “DP++” source device

2.2 HDMI Transmitter

- Single channel HDMI transmitter
- Compliant with HDMI 2.0b, HDCP 1.4/2.2 and DVI 1.0 specifications
- Supporting link speeds of up to 6.0Gbps (link clock rate of 600MHz)
- Support 8-channel, uncompressed LPCM I2S audio with sample rates of 32~192 kHz and

sample sizes of 16~24 bits, and HBR.

- Support Gamut Metadata packet for High Dynamic Range (HDR) for 4K60 422/420 mode.
- Software programmable, auto-calibrated TMDS source terminations provide for optimal source signal quality
- Software programmable HDMI output current, enabling user to optimize the performance for fixed-cable systems or those with pre-defined cable length
- Integrated pre-programmed HDCP keys
- Purely hardware HDCP engine increasing the robustness and security of HDCP operation
- Monitor detection through Hot Plug Detection and Receiver Termination Detection
- Embedded full-function pattern generator
- Intelligent, programmable power management

2.3 Common Features

- Support up to **WUXGA (1920x1200 @120Hz), WQXGA (2560X1600 RB @120Hz)** VESA display format
- Support up to **1080P@240Hz**, **4Kx2K@60Hz** CEA display format.
- Support DP input color depth 6/8/10/12 bits
- Support HDMI output color depth 8/10/12 bits
- Digital audio output interface supporting
    - ♦ One I2S interface supporting 2-channel audio with sample rates of 32~192kHz and sample sizes of 16~24 bits
    - ♦ S/PDIF interface supporting PCM digital audio at up to 192kHz frame rate
    - ♦ HBR audio up to 768KHz.
- Embedded MCU and Flash
- Automatic Audio Error detection with soft mute function, preventing annoying harsh output

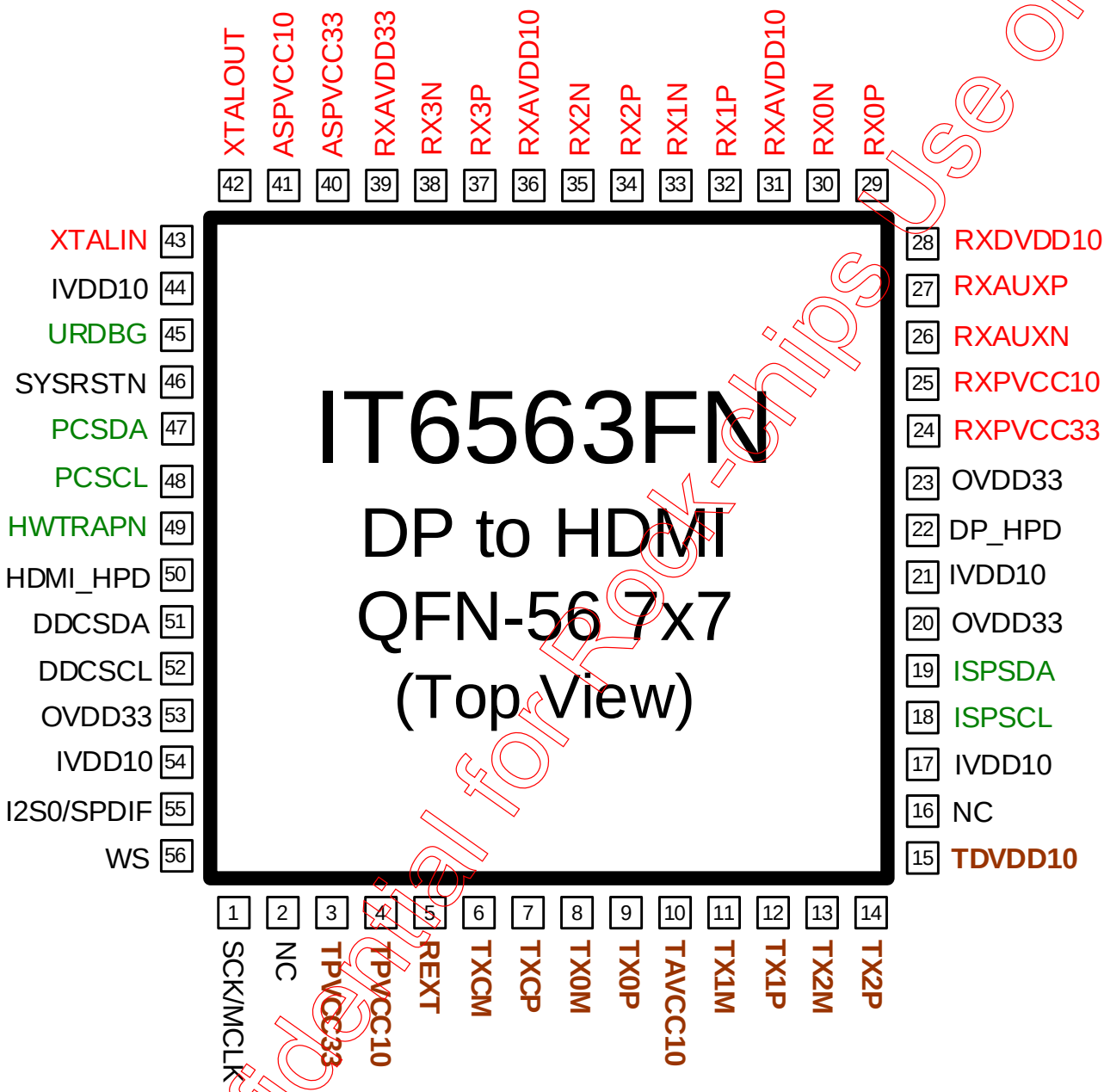
sound due to audio error or hot-unplug

- 56-pin QFN (7mm x 7mm) package
- RoHS Compliant (100% Green available)

3. Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6563FN	-20~70	56-pin QFN	Green

Pin Diagram



Red: DP RX AFE pin
Brown: HDMI TX AFE pin
Green: MCU pin
Others: TTL pin

Figure 1. IT6563 Pin Diagram

Pin Description

DP Analog Front-end Interface Pins

Pin Name	Direction	Description	Type	Pin No.
RX0P	Analog	DP Lane 0 positive input	DP	29
RX0N	Analog	DP Lane 0 negative input	DP	30
RX1P	Analog	DP Lane 1 positive input	DP	32
RX1N	Analog	DP Lane 1 negative input	DP	33
RX2P	Analog	DP Lane 2 positive input	DP	34
RX2N	Analog	DP Lane 2 negative input	DP	35
RX3P	Analog	DP Lane 3 positive input	DP	37
RX3N	Analog	DP Lane 3 negative input	DP	38
RXAUXP	Analog	DP AUX channel positive input	DP	27
RXAUXN	Analog	DP AUX channel negative input	DP	26
XTALIN	Input	Crystal clock input	Analog	43
XTALOUT	Output	Crystal clock output	Analog	42

TMDS Analog Front-end Interface Pins

Pin Name	Direction	Description	Type	Pin No.
TX2P	Analog	HDMI Channel 2 positive output	TMDS	14
TX2M	Analog	HDMI Channel 2 negative output	TMDS	13
TX1P	Analog	HDMI Channel 1 positive output	TMDS	12
TX1M	Analog	HDMI Channel 1 negative output	TMDS	11
TX0P	Analog	HDMI Channel 0 positive output	TMDS	9
TX0M	Analog	HDMI Channel 0 negative output	TMDS	8
TXCP	Analog	HDMI Clock Channel positive output	TMDS	7
TXCM	Analog	HDMI Clock Channel negative output	TMDS	6
REXT	Analog	External resistor for setting TMDS output level. Default tied to AGND via a 11K-Ohm SMD resistor.	Analog	5

HDMI Interface Pins

Pin Name	Direction	Description	Type	Pin No.
DDCSCL	I/O	I^2C Clock for HDMI DDC (5V-tolerant)	LVTTL	52
DDCSDA	I/O	I^2C Data for HDMI DDC (5V-tolerant)	LVTTL	51
HDMI_HPD	I/O	Hot Plug Detection for HDMI (5V-tolerant)	Schmitt	50

Audio Interface Pins

Pin Name	Direction	Description	Type	Pin No.
I2S0/SPDIF	I/O	I2S serial data output, doubles as S/PDIF audio output	LVTTL	55
WS	I/O	I2S word select output	LVTTL	56
SCK/MCLK	I/O	I2S serial clock output, doubles as Audio master clock	LVTTL	1

System Control/Programming Pins

Pin Name	Direction	Description	Type	Pin No.
SYSRSTN	Input	Hardware reset pin. Active LOW.	Schmitt	46
DP_HPD	Output	DisplayPort HPD/IRQ pin	LVTTL	22
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	LVTTL	48
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	LVTTL	47
URDBG	I/O	UR interface for S/W debugging	LVTTL	45
HWTRAPN	I/O	I^2C access path selection.	Schmitt	49
ISPSCL	Input	ISP programming data pin	LVTTL	18
ISPSDA	I/O	ISP programming clock pin	LVTTL	19

Power/Ground Pins

Pin Name	Description	Type	Pin No.
TPVCC10	HDMI PLL power (1.0V)	Power	4
TPVCC33	HDMI PLL power (3.3V)	Power	3
TAVCC10	HDMI analog frontend power (1.0V)	Power	10
TDVDD10	HDMI digital frontend power (1.0V)	Power	15
IVDD10	Digital logic power (1.0V)	Power	17, 21, 44, 54
OVDD33	I/O Pin power (3.3V)	Power	20, 23, 53
ASPVCC33	Power for oscillator and PLL (3.3V)	Power	40
RXDVDD10	DP digital frontend power (1.0V)	Power	28
RXAVDD10	DP analog frontend power (1.0V)	Power	31, 36
ASPVCC10	Power for oscillator and PLL (1.0V)	Power	41
RXAVDD33	DP analog frontend power (3.3V)	Power	39
RXPVCC10	DP PLL power (1.0V)	Power	25
RXPVCC33	DP PLL power (3.3V)	Power	24
NC	No Connection		2,16

Block Diagram

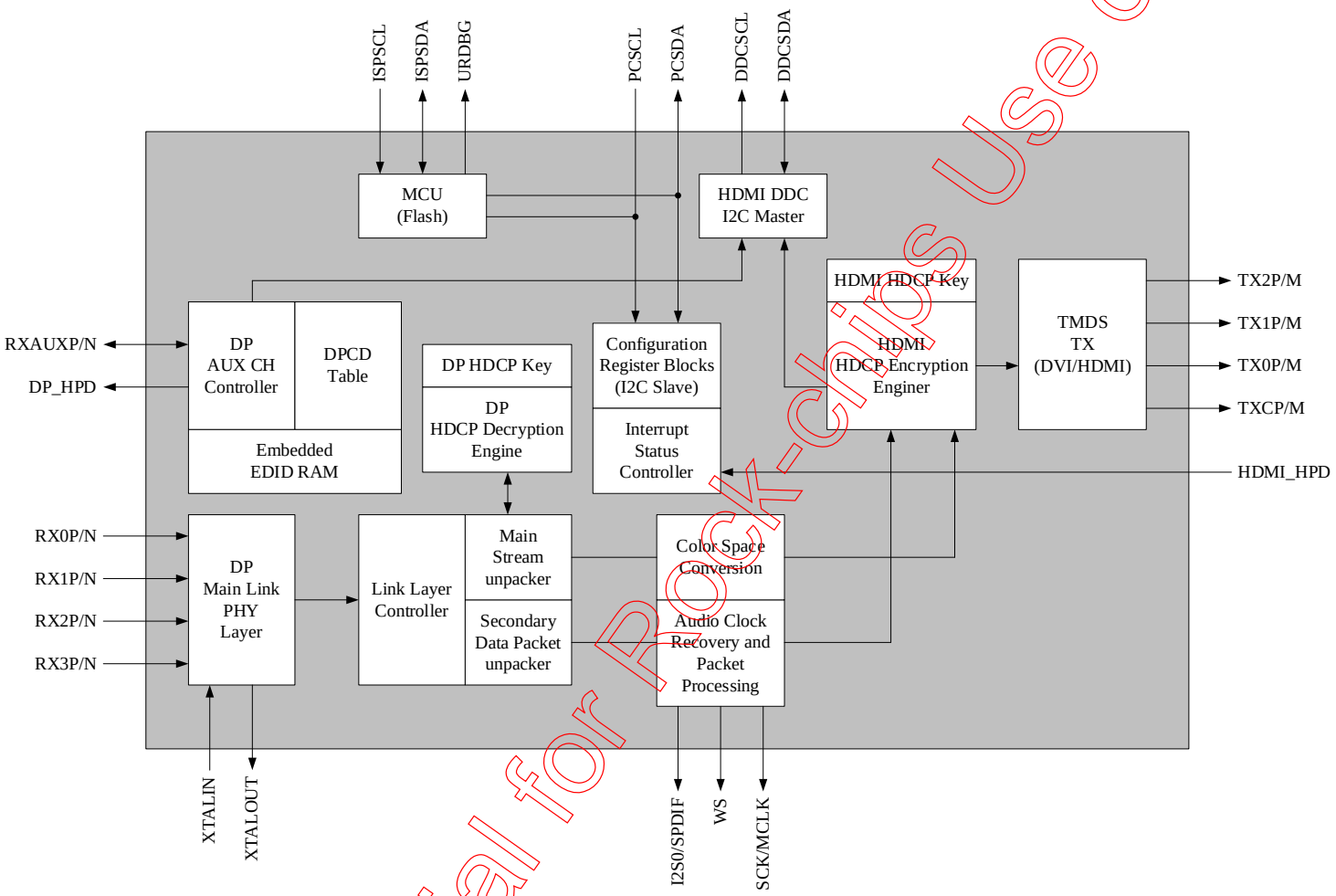


Figure 2. The IT6563 Block Diagram

Functional Description

Overview

The IT6563FN is a DisplayPort to HDMI converter. With a 4 lanes DisplayPort 1.2a compliant Receiver and HDMI 2.0 Transmitter integrated, the IT6563FN can support multimedia stream transport with video resolution up to 1920x1200@120Hz, 2560x1600RB@120Hz, 1920x1080P@240Hz or 4Kx2K@60Hz and with audio of up to 8 channel LPCM formant and up to 192kHz sample rate and up to 24-bit sample size.

DisplayPort Receiver

The DisplayPort receiver of IT6563FN provides complete solutions for DisplayPort 1.2a Sink systems, supporting reception and processing of Deep Color video and digital audio. Advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion. The integrated receiver analog frontend macro is capable of receiving and decoding data at up to 5.4Gbps. Adaptive equalization is employed to support long cables.

HDMI Transmitter

The HDMI transmitter of IT6563FN is a low-power version of HDMI 2.0 transmitter. This HDMI transmitter support processing and transmission of Deep Color video and up to 8 channel LPCM digital audio. This HDMI transmitter supports color depths of 10bits and 12bits up to 4K@30Hz.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
TPVCC10	HDMI PLL supply voltage	-0.5		1.5	V
TPVCC33	HDMI PLL supply voltage	-0.3		4.0	V
TAVCC10	HDMI analog frontend supply voltage	-0.5		1.5	V
TDVDD10	HDMI digital frontend supply voltage	-0.5		1.5	V
IVDD10	Digital logic supply voltage	-0.5		1.5	V
OVDD33	I/O pins supply voltage	-0.3		4.0	V
ASPVCC33	DP oscillator and PLL supply voltage	-0.3		4.0	V
RXDVDD10	DP digital frontend supply voltage	-0.5		1.5	V
RXAVDD10	DP analog frontend supply voltage	-0.5		1.5	V
ASPVCC10	DP oscillator and PLL supply voltage	-0.5		1.5	V
RXAVDD33	DP analog frontend supply voltage	-0.3		4.0	V
RXPVCC10	DP PLL supply voltage	-0.5		1.5	
RXPVCC33	DP PLL supply voltage	-0.3		4.0	
V_I	Input voltage	-0.3		OVDD33+0.3	V
V_O	Output voltage	-0.3		OVDD33+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
TPVCC10	HDMI PLL supply voltage	0.95	1.0	1.05	V
TPVCC33	HDMI PLL supply voltage	3.0	3.3	3.6	V
TAVCC10	HDMI analog frontend supply voltage	0.95	1.0	1.05	V
TDVDD10	HDMI digital frontend supply voltage	0.95	1.0	1.05	V
IVDD10	Digital logic supply voltage	0.95	1.0	1.05	V
OVDD33	I/O pins supply voltage	3.0	3.3	3.6	V
ASPVCC33	DP oscillator and PLL supply voltage	3.0	3.3	3.6	V
RXDVDD10	DP digital frontend supply voltage	0.95	1.0	1.05	V
RXAVDD10	DP analog frontend supply voltage	0.95	1.0	1.05	V

ASPVCC10	DP oscillator and PLL supply voltage	0.95	1.0	1.05	V
RXAVDD33	DP analog frontend supply voltage	3.0	3.3	3.6	V
RXPVCC10	DP PLL supply voltage	0.95	1.0	1.05	V
RXPVCC33	DP PLL supply voltage	3.0	3.3	3.6	
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	-20	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance		29		°C/W

Notes:
1. TPVCC10, TPVCC33, TAVCC10, ASPVCC33, RXAVDD10 and ASPVCC10 should be regulated.
2. See System Design Consideration for supply decoupling and regulation.

Operation Power Specification

Normal Active Mode, DP to HDMI (DP/HDMI HDCP2.2 on)

Symbol	VideoTiming	MHz	HBR2/4	HBR/4	HBR/2	LBR/4	LBR/2	LBR/1	Unit
3V3 total current	480P60	27	●	●	●	●	●	27.27	mA
	720P60	74.25	●	●	●	●	31.9	X	mA
	1080P60	148.5	●	●	31.82	29.23	X	X	mA
	1080P120	297	●	33.03	X	X	X	X	mA
	4K2KP30	297	●	33.99	X	X	X	X	mA
	4K2KP60	594	41.23	X	X	X	X	X	mA
1V0 total current	480P60	27	●	●	●	●	●	193.9	mA
	720P60	74.25	●	●	●	●	219.2	X	mA
	1080P60	148.5	●	●	300.38	258.7	X	X	mA
	1080P120	297	●	379.19	X	X	X	X	mA
	4K2KP30	297	●	376.57	X	X	X	X	mA
	4K2KP60	594	591.62	X	X	X	X	X	mA
Total Power	480P60	25	●	●	●	●	●	283.9	mW
	720P60	74.25	●	●	●	●	324.4	X	mW
	1080P60	148.5	●	●	405.39	355.1	X	X	mW
	1080P120	297	●	488.19	X	X	X	X	mW
	4K2KP30	297	●	488.74	X	X	X	X	mW
	4K2KP60	594	727.68	X	X	X	X	X	mW

Notes:
1. HBR2/4 means HBR2 mode(5.4Ghz) with 4 lanes.

Standby Mode

Symbol	Standby	Unit
I_{VDD33}	2.529	mA
I_{VDD10}	12.888	mA
Total Power	21.24	mW

Notes:
1. Standby definition: HDMI Monitor un-plug, the IT6563 de-assert DP HPD, and still continue Polling HDMI Plug-in status!
2. IVDD33 : Total current of 3.3V power pins. IVDD10: Total current of 1.0V power pins.

DC Electrical Specification

Under functional operation conditions

			OVDD33=3.3V			Unit
Symbol	Parameter	Pin Type	Min	Typ	Max	
V_{IL}	Input low voltage[1]	5V-TOL	GND		0.8	V
V_{IH}	Input high voltage[1]	5V-TOL	2.5		5.5	V

Symbol	Parameter	Pin Type	Min	Typ	Max	Unit
V_{IH}	Input high voltage[1]	LVTTL	2.0		3.6	V
V_{IL}	Input low voltage[1]	LVTTL	GND		0.8	V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt	0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt		1.6	2.0	V
V_{OL}	Output low voltage[1]	LVTTL			0.4	V
V_{OH}	Output high voltage[1]	LVTTL	2.4			V
I_{IN}	Input leakage current[1]	all	-10		+10	μA
I_{OZ}	Output leakage current[1]	all	-10		+10	μA
C_{IN}	Input Capacitance[1]	LVTTL		2.1		pF
I_{OL}	Serial programming output sink current[2]	Schmitt	4		16	mA
V_{AUX_diff}	DP AUX Channel differential swing[3]	Differential	0.27		1.36	V
V_{Rx_diff}	DP Main Link differential swing[3]	Differential	40			mV
V_{swing}	TMDS bit-rate <= 3.4Gbps output data/clock channel single-ended swing[4]	TMDS	400		600	mV
	TMDS bit-rate > 3.4Gbps output data channel single-ended swing[4]	TMDS	400		600	mV
	TMDS bit-rate > 3.4Gps output clock channel single-ended swing[4]	TMDS	200		600	mV

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real I^2C environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of the IT6563FN are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6563FN Programming Guide for proper register setting.
3. Limits defined by Displyport 1.2a standard.
4. Limits defined by HDMI 1.4/2.0 standard.

Audio AC Timing Specification

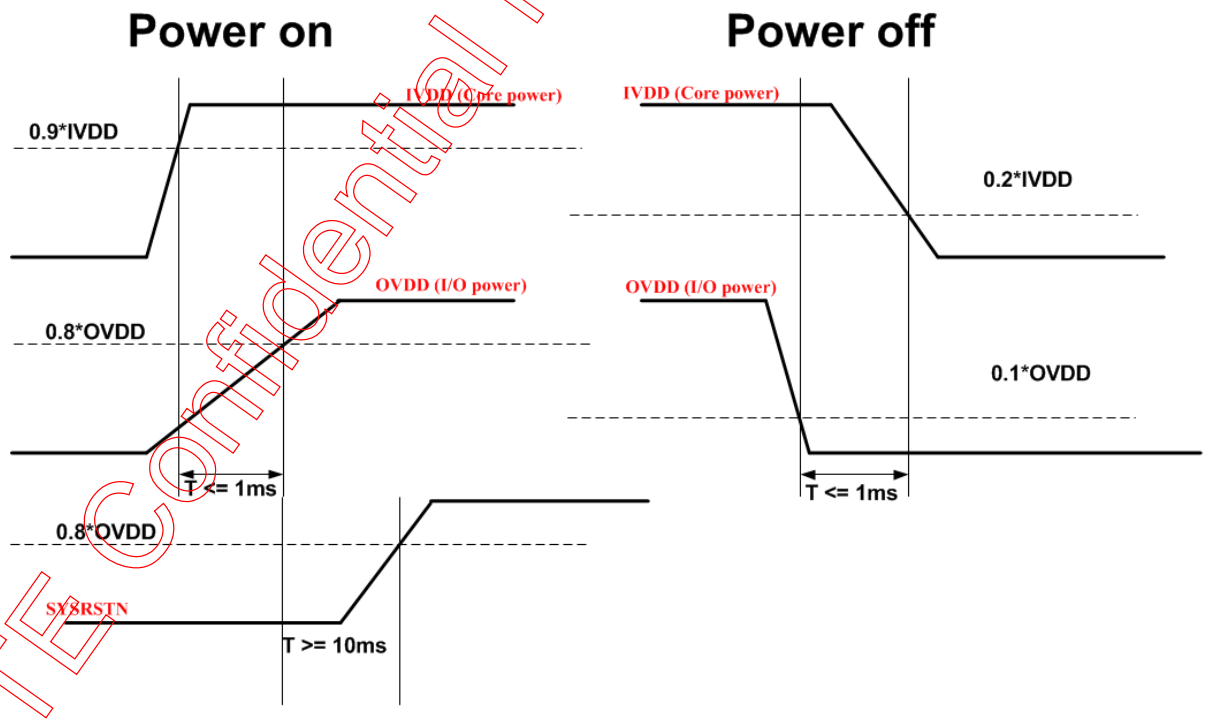
Under functional operation conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{S_I2S}	I^2S sample rate	Up to 2 channels	32		192	KHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		192	KHz
F_{XTAL}	External audio crystal frequency	± 50ppm accuracy		27		MHz

Notes:

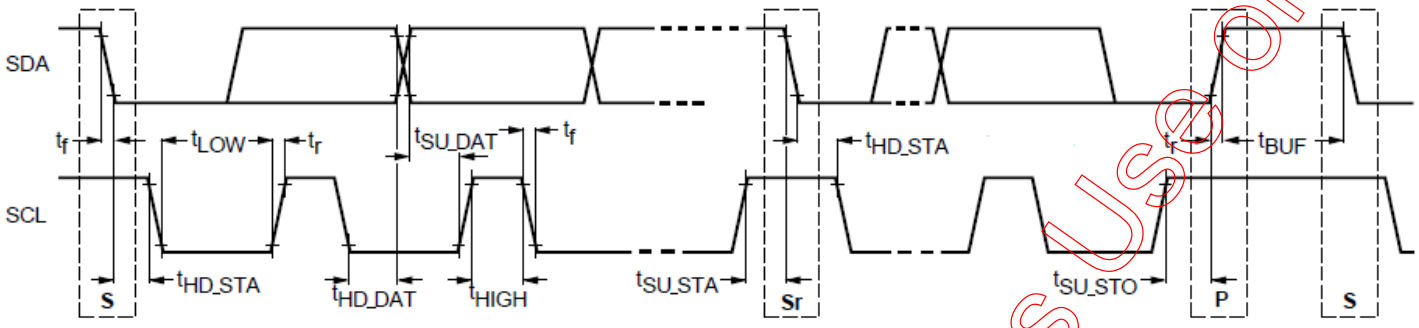
1. The IT6563FN is designed to work in default with a 27MHz crystal for audio functions.

Power and System Reset Sequence



When power on, please keep IVDD go 0.9*IVDD before OVDD go 0.8*OVDD (IVDD must supply earlier than or equal to OVDD).
And please keep the time interval between IVDD and OVDD shorter than 1ms when power on or power off.

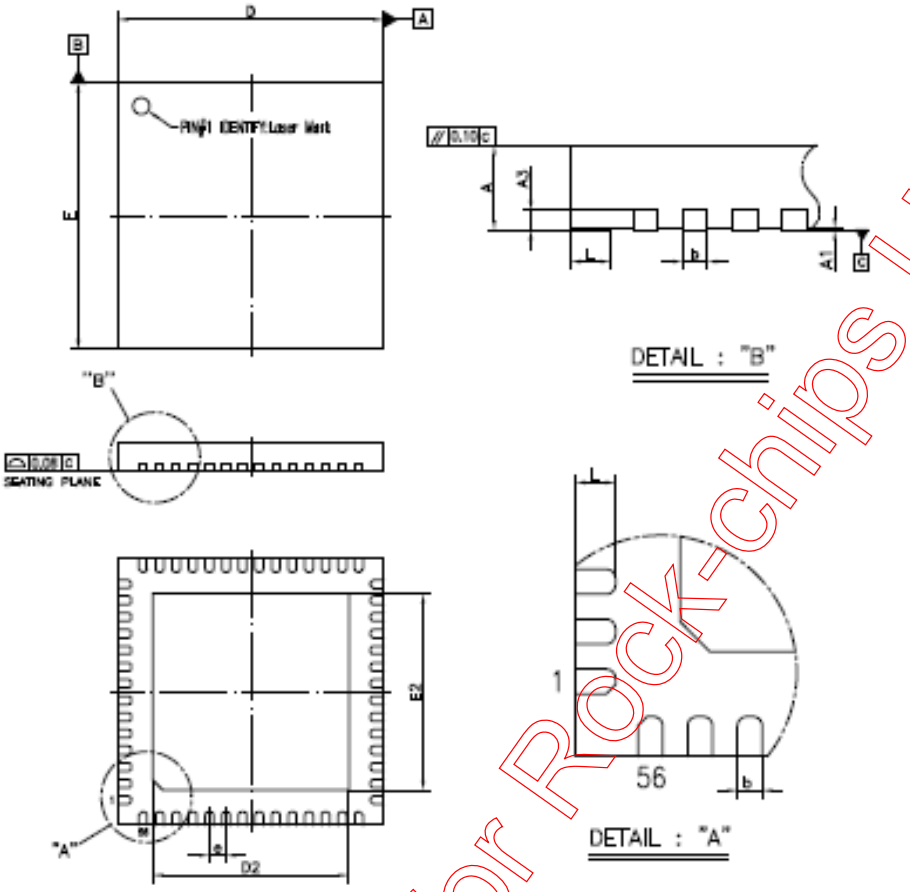
Characteristics of the PCSDA (PIN47) and PCSCL(PIN48) for F/S-mode I²C-bus



Symbol	Parameter	Standard mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{HD_STA}	Hold time for (repeated) START condition	4.0	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	us
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	us
t_{HD_DAT}	Data hold time	0	3.45	0	0.9	us
t_{SU_DAT}	Data set-up time	250	-	100	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	$20+0.1C_b$(1)	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	$20+0.1C_b$(1)	300	ns
t_{SU_STO}	Set-up time for STOP condition	4.0	-	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	us
C_b	Capacitive load for each bus line	-	400	-	200	pF
V_{nL}	Noise Margin at the LOW level	0.1*OVDD33	-	0.1*OVDD33	-	V
V_{nH}	Noise Margin at the HIGH level	0.1*OVDD33	-	0.1*OVDD33	-	V

Notes:
1. C_b = total capacitance of one bus line in pF.

Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	---	0.002	0.00	---	0.05
A3	0.008 REF			0.20 REF		
b	0.006	0.008	0.010	0.15	0.20	0.25
D / E	0.276 BSC			7.00 BSC		
D2 / E2	0.201	0.205	0.209	5.10	5.20	5.30
e	0.016 BSC			0.40 BSC		
L	0.014	0.016	0.018	0.35	0.40	0.45

Notes:

1. Controlling dimension : Millimeter
2. Reference document : JEDEC MO-220.
3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

Figure 3. 56-pin QFN Package Dimensions