Embedded LPDDR5 SDRAM

MT62F512M32D2, MT62F1G32D4

Features

- **Architecture**
  - 12.8 GB/s maximum bandwidth per channel
  - Frequency range: 800–5 MHz (data rate range per pin: 6400–40 Mb/s with WCK:CK = 4:1)
  - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5 data interface**
  - Single x16 channel/die
  - Double-data-rate command/address entry
  - Differential command clocks (CK_t/CK_c) for high-speed operation
  - Differential data clocks (WCK_t/WCK_c)
  - Optional differential read strobe (RDQS_t/RDQS_c)
  - 16*n*-bit or 32*n*-bit prefetch architecture
  - 4KB page size with 8-bank (8B mode), 2KB page size with bank group (BG mode), or 16-bank (16B mode) operation
  - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
  - Background ZQ calibration/command-based ZQ calibration
  - Optional link protection (link ECC)
  - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
  - V_{DD1} = 1.70–1.95V; 1.8V NOM
  - V_{DD2H} = 1.01–1.12V; 1.05V NOM
  - V_{DD2L} = V_{DD2H} or 0.87–0.97V; 0.9V NOM
  - V_{DDQ} = 0.5V NOM or 0.3V NOM (ODT off)
- **I/O characteristics**
  - Interface-LVSTL 0.5/0.3
  - I/O type: Low-swing single-ended, V_{SS} terminated
  - V_{OH}-compensated output drive
  - Programmable V_{SS} on-die termination (ODT)
  - Non target ODT support
  - DVFSQ support
- **Low power features**
  - DVFSC: Dynamic voltage frequency scaling core
  - Single-ended CK, single-ended WCK and single-ended RDQS
  - Data copy
  - Write X

Options	Marking
• V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ} (ODT on)/(ODT off): 1.8V/1.05V/0.9V/0.5V/0.3V	F
• Array configuration	
– 512 Meg x 32 (2 channels x16 I/O)	512M32
– 1 Gig x 32 (2 channels x16 I/O)	1G32
• Device configuration	
– 2 die in package	D2
– 4 die in package	D4
• FBGA "green" package	
– 315-ball TFBGA (12.4mm × 15.0mm, seated height: 1.1mm MAX, Ø0.48 SMD)	DS
• Speed grade, cycle time (^{t}WCK)	
– 6400 Mb/s	-031
• Operating temperature:	
– –25°C to +85°C	WT
• Revision	:B

‡Products and specifications discussed herein are for evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications.

Part Number Ordering Information

Figure 1: Part Number Chart

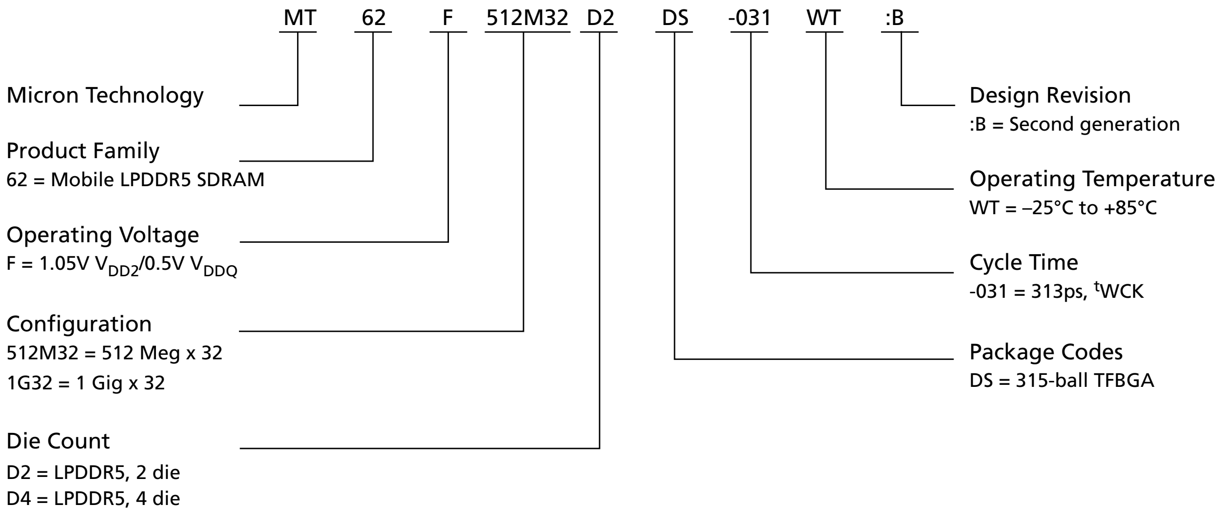

MT
62
F
512M32
D2
DS
-031
WT
:B
Micron Technology
Product Family
62 = Mobile LPDDR5 SDRAM
Operating Voltage
F = 1.05V V_{DD2}/0.5V V_{DDQ}
Configuration
512M32 = 512 Meg x 32
1G32 = 1 Gig x 32
Die Count
D2 = LPDDR5, 2 die
D4 = LPDDR5, 4 die
Design Revision
:B = Second generation
Operating Temperature
WT = –25°C to +85°C
Cycle Time
-031 = 313ps, ^{t}WCK
Package Codes
DS = 315-ball TFBGA

Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F512M32D2DS-031 WT:B	2GB (16Gb)	6400 Mb/s
MT62F1G32D4DS-031 WT:B	4GB (32Gb)	6400 Mb/s

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

LPDDR5 Data Sheet List

This data sheet only describes the product specifications that are unique to the Micron devices listed in Table 1.

For general LPDDR5 specifications, please refer to the data sheets below.

- General LPDDR5 Specifications 1: Mode Registers
- General LPDDR5 Specifications 2: AC/DC and Interface Specifications
- General LPDDR5 Specifications 3: Features and Functionalities

Important Notes and Warnings

Micron Technology, Inc. ("Micron") reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions. This document supersedes and replaces all information supplied prior to the publication hereof. You may not rely on any information set forth in this document if you obtain the product described herein from any unauthorized distributor or other source not authorized by Micron.

Automotive Applications. Products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets. Distributor and customer/distributor shall assume the sole risk and liability for and shall indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting directly or indirectly from any use of non-automotive-grade products in automotive applications. Customer/distributor shall ensure that the terms and conditions of sale between customer/distributor and any customer of distributor/customer (1) state that Micron products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets and (2) require such customer of distributor/customer to indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting from any use of non-automotive-grade products in automotive applications.

Critical Applications. Products are not authorized for use in applications in which failure of the Micron component could result, directly or indirectly in death, personal injury, or severe property or environmental damage ("Critical Applications"). Customer must protect against death, personal injury, and severe property and environmental damage by incorporating safety design measures into customer's applications to ensure that failure of the Micron component will not result in such harms. Should customer or distributor purchase, use, or sell any Micron component for any critical application, customer and distributor shall indemnify and hold harmless Micron and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such critical application, whether or not Micron or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Micron product.

Customer Responsibility. Customers are responsible for the design, manufacture, and operation of their systems, applications, and products using Micron products. ALL SEMICONDUCTOR PRODUCTS HAVE INHERENT FAILURE RATES AND LIMITED USEFUL LIVES. IT IS THE CUSTOMER'S SOLE RESPONSIBILITY TO DETERMINE WHETHER THE MICRON PRODUCT IS SUITABLE AND FIT FOR THE CUSTOMER'S SYSTEM, APPLICATION, OR PRODUCT. Customers must ensure that adequate design, manufacturing, and operating safeguards are included in customer's applications and products to eliminate the risk that personal injury, death, or severe property or environmental damages will result from failure of any semiconductor component.

Limited Warranty. In no event shall Micron be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by Micron's duly authorized representative.

General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.

Device Configuration

Table 2: Die Organization in the Package

Die Organization	512M32 (16Gb/package)	1G32 (32Gb/package)
Channel A, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel B, rank 0	x16 mode × 1 die	x16 mode × 1 die
Channel A, rank 1	–	x16 mode × 1 die
Channel B, rank 1	–	x16 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Addressing

Description	512M32 (16Gb/package), 1G32 (32Gb/package)		
Density per die	8Gb		
Bits	8,589,934,592		
Bank mode	BG mode	16B mode	8B mode
Configuration	32Mb × 16 DQ × 4 Banks × 4BG	32Mb × 16 DQ × 16 Banks	64Mb × 16 DQ × 8 Banks
Number of banks	4	16	8
Number of bank groups	4	1	1
Array prefetch bits	256	256	512
Rows per bank	32,768		
Columns	64		
Page size (bytes)	2048	2048	4096
Native burst length	16	16	32
Number of I/Os	16		
Bank address	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–
Row address	R[14:0]		
Column address	C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit		

Notes:
1. Refer to the SDRAM Addressing section in General LPDDR5 Specification 3.
2. Refer to the Speed Grades and Effective Burst Length in General LPDDR5 Specifications 3.

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

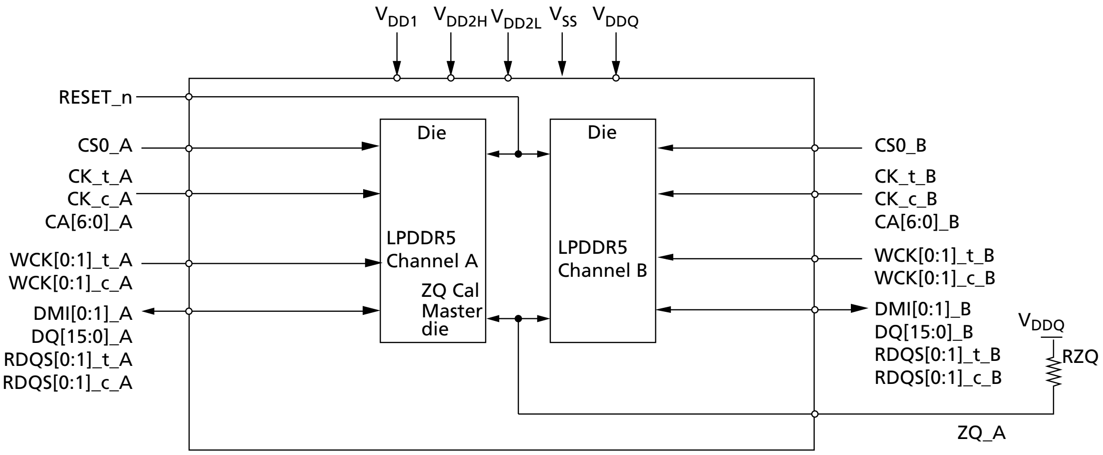
Parameter	Symbol	8Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	^{t}RFCab	210	210	ns
REFRESH cycle time (per bank)	^{t}RFCpb	120	120	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	^{t}PBR2ACT	7.5	10	ns

Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5 Specifications 3 for all refresh parameters.

Package Block Diagrams

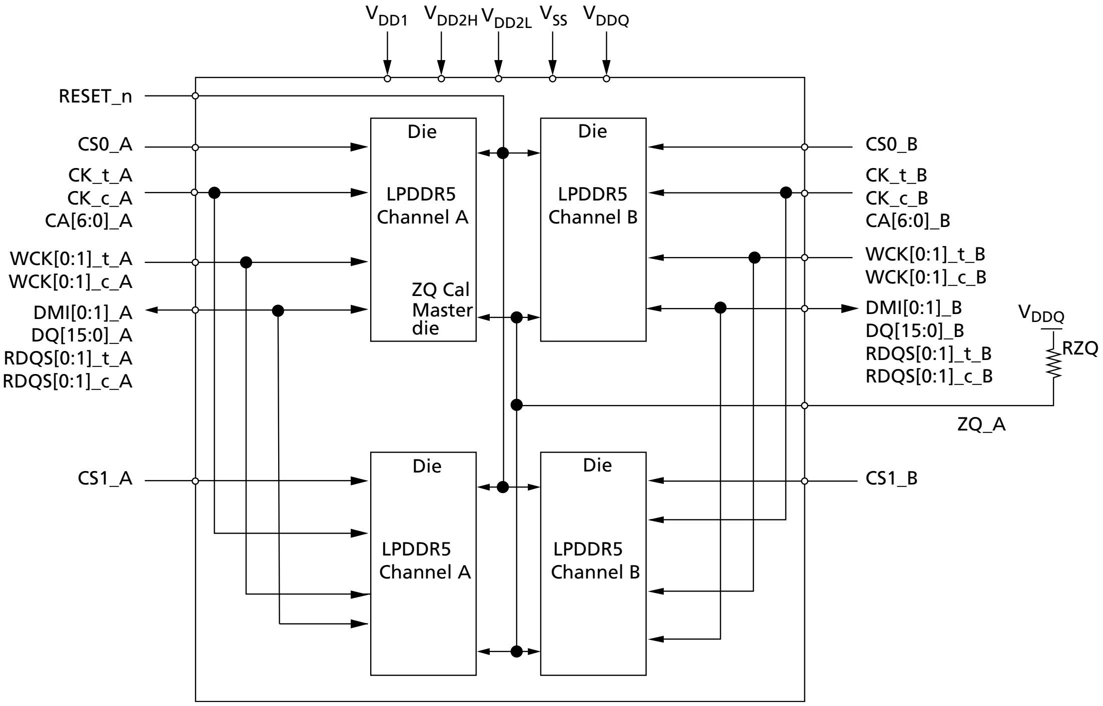
Dual Die, Dual Channel

Figure 2: Dual-Die, Dual-Channel Package Block Diagram


V_{DD1}
V_{DD2H}
V_{DD2L}
V_{SS}
V_{DDQ}
RESET_n
CS0_A
CK_t_A
CK_c_A
CA[6:0]_A
WCK[0:1]_t_A
WCK[0:1]_c_A
DMI[0:1]_A
DQ[15:0]_A
RDQS[0:1]_t_A
RDQS[0:1]_c_A
Die
LPDDR5
Channel A
ZQ Cal
Master
die
Die
LPDDR5
Channel B
CS0_B
CK_t_B
CK_c_B
CA[6:0]_B
WCK[0:1]_t_B
WCK[0:1]_c_B
DMI[0:1]_B
DQ[15:0]_B
RDQS[0:1]_t_B
RDQS[0:1]_c_B
V_{DDQ}
RZQ
ZQ_A

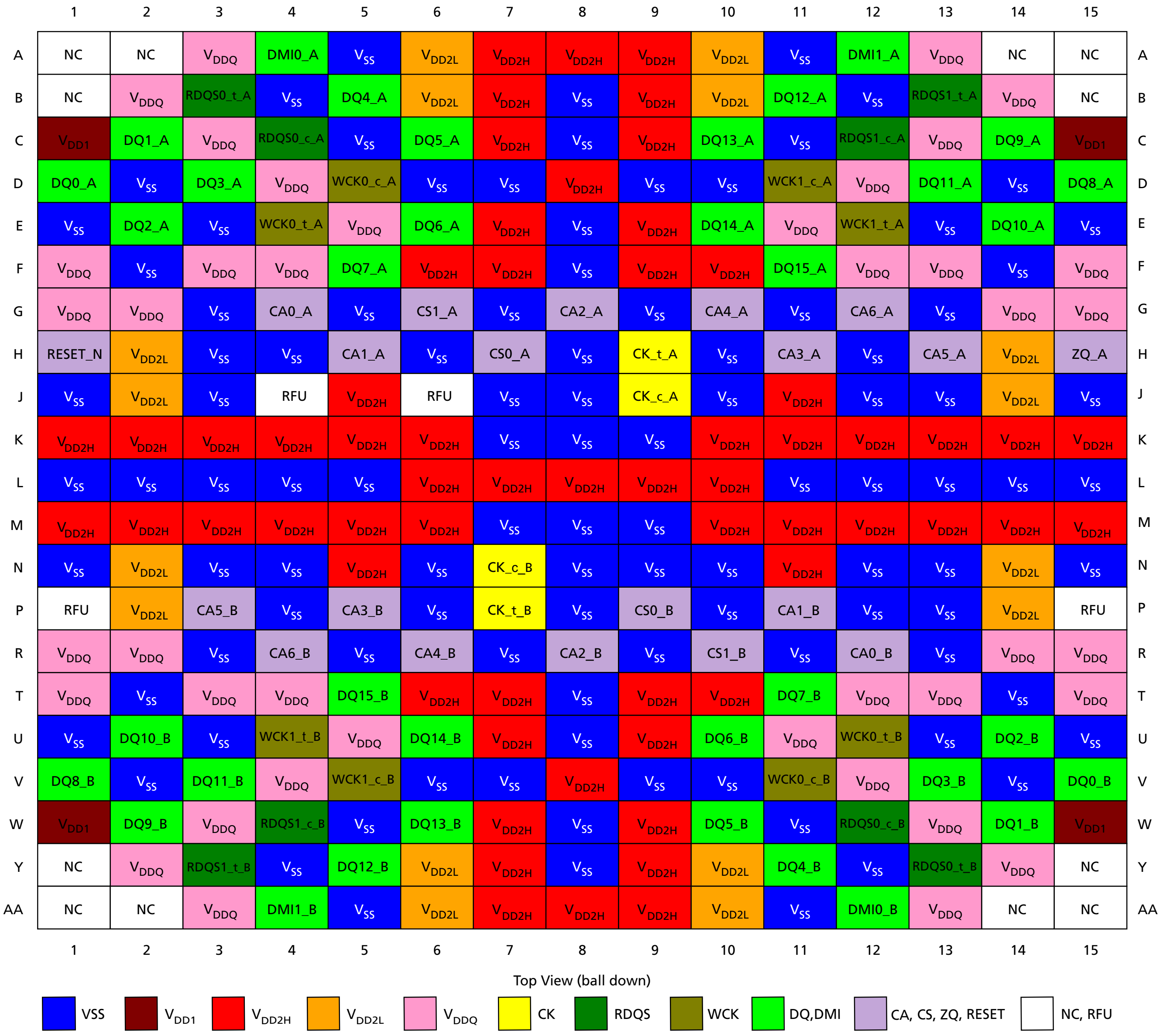
Quad Die, Dual Channel

Figure 3: Quad-Die, Dual-Channel Package Block Diagram


V_{DD1}
V_{DD2H}
V_{DD2L}
V_{SS}
V_{DDQ}
RESET_n
CS0_A
CK_t_A
CK_c_A
CA[6:0]_A
WCK[0:1]_t_A
WCK[0:1]_c_A
DMI[0:1]_A
DQ[15:0]_A
RDQS[0:1]_t_A
RDQS[0:1]_c_A
Die
LPDDR5
Channel A
ZQ Cal
Master
die
Die
LPDDR5
Channel B
CS0_B
CK_t_B
CK_c_B
CA[6:0]_B
WCK[0:1]_t_B
WCK[0:1]_c_B
DMI[0:1]_B
DQ[15:0]_B
RDQS[0:1]_t_B
RDQS[0:1]_c_B
V_{DDQ}
RZQ
ZQ_A
CS1_A
Die
LPDDR5
Channel A
Die
LPDDR5
Channel B
CS1_B

Ball Assignments and Descriptions

Figure 4: 315-Ball Dual-Channel Discrete FBGA



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	NC	NC	V_{DDQ}	DMI0_A	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI1_A	V_{DDQ}	NC	NC	A
B	NC	V_{DDQ}	RDQS0_t_A	V_{SS}	DQ4_A	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ12_A	V_{SS}	RDQS1_t_A	V_{DDQ}	NC	B
C	V_{DD1}	DQ1_A	V_{DDQ}	RDQS0_c_A	V_{SS}	DQ5_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ13_A	V_{SS}	RDQS1_c_A	V_{DDQ}	DQ9_A	V_{DD1}	C
D	DQ0_A	V_{SS}	DQ3_A	V_{DDQ}	WCK0_c_A	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK1_c_A	V_{DDQ}	DQ11_A	V_{SS}	DQ8_A	D
E	V_{SS}	DQ2_A	V_{SS}	WCK0_t_A	V_{DDQ}	DQ6_A	V_{DD2H}	V_{SS}	V_{DD2H}	DQ14_A	V_{DDQ}	WCK1_t_A	V_{SS}	DQ10_A	V_{SS}	E
F	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ7_A	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ15_A	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	F
G	V_{DDQ}	V_{DDQ}	V_{SS}	CA0_A	V_{SS}	CS1_A	V_{SS}	CA2_A	V_{SS}	CA4_A	V_{SS}	CA6_A	V_{SS}	V_{DDQ}	V_{DDQ}	G
H	RESET_N	V_{DD2L}	V_{SS}	V_{SS}	CA1_A	V_{SS}	CS0_A	V_{SS}	CK_t_A	V_{SS}	CA3_A	V_{SS}	CA5_A	V_{DD2L}	ZQ_A	H
J	V_{SS}	V_{DD2L}	V_{SS}	RFU	V_{DD2H}	RFU	V_{SS}	V_{SS}	CK_c_A	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	J
K	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	K
L	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	L
M	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2H}	M
N	V_{SS}	V_{DD2L}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	CK_c_B	V_{SS}	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	V_{DD2L}	V_{SS}	N
P	RFU	V_{DD2L}	CA5_B	V_{SS}	CA3_B	V_{SS}	CK_t_B	V_{SS}	CS0_B	V_{SS}	CA1_B	V_{SS}	V_{SS}	V_{DD2L}	RFU	P
R	V_{DDQ}	V_{DDQ}	V_{SS}	CA6_B	V_{SS}	CA4_B	V_{SS}	CA2_B	V_{SS}	CS1_B	V_{SS}	CA0_B	V_{SS}	V_{DDQ}	V_{DDQ}	R
T	V_{DDQ}	V_{SS}	V_{DDQ}	V_{DDQ}	DQ15_B	V_{DD2H}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2H}	DQ7_B	V_{DDQ}	V_{DDQ}	V_{SS}	V_{DDQ}	T
U	V_{SS}	DQ10_B	V_{SS}	WCK1_t_B	V_{DDQ}	DQ14_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ6_B	V_{DDQ}	WCK0_t_B	V_{SS}	DQ2_B	V_{SS}	U
V	DQ8_B	V_{SS}	DQ11_B	V_{DDQ}	WCK1_c_B	V_{SS}	V_{SS}	V_{DD2H}	V_{SS}	V_{SS}	WCK0_c_B	V_{DDQ}	DQ3_B	V_{SS}	DQ0_B	V
W	V_{DD1}	DQ9_B	V_{DDQ}	RDQS1_c_B	V_{SS}	DQ13_B	V_{DD2H}	V_{SS}	V_{DD2H}	DQ5_B	V_{SS}	RDQS0_c_B	V_{DDQ}	DQ1_B	V_{DD1}	W
Y	NC	V_{DDQ}	RDQS1_t_B	V_{SS}	DQ12_B	V_{DD2L}	V_{DD2H}	V_{SS}	V_{DD2H}	V_{DD2L}	DQ4_B	V_{SS}	RDQS0_t_B	V_{DDQ}	NC	Y
AA	NC	NC	V_{DDQ}	DMI1_B	V_{SS}	V_{DD2L}	V_{DD2H}	V_{DD2H}	V_{DD2H}	V_{DD2L}	V_{SS}	DMI0_B	V_{DDQ}	NC	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

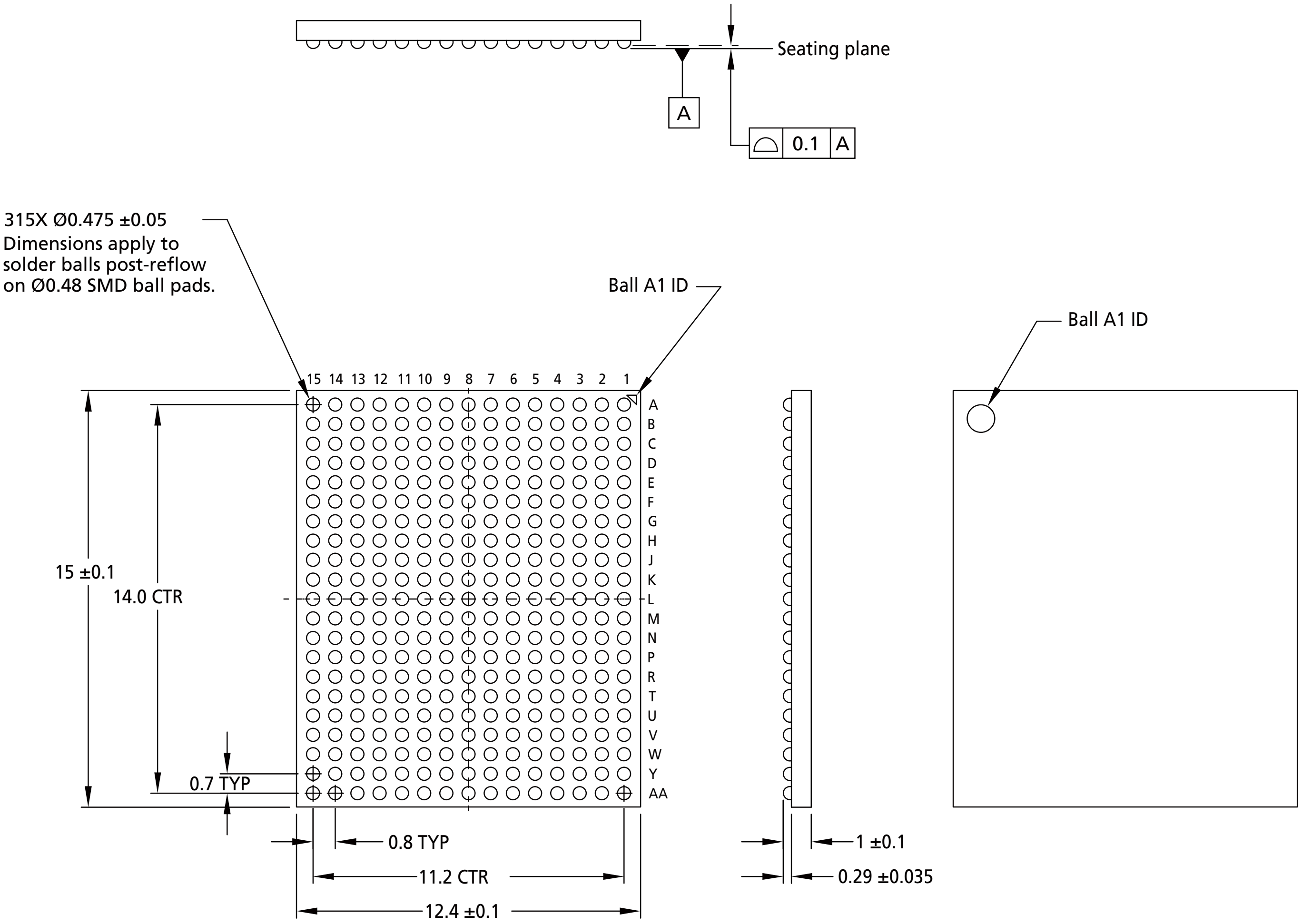
Table 5: Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B] CK_c_[A:B]	Input	**Clock:** CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	**Chip select:** CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B] WCK[1:0]_c_[A:B]	Input	**Data clock:** WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	**Data input/output:** Bidirectional data bus.
RDQS[1:0]_t_[A:B] RDQS[1:0]_c_[A:B]	I/O Output	**Read data strobe:** RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	**Data mask inversion:** DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V_{DDQ} through a 240Ω ±1% resistor.
V_{DDQ}, V_{DD1}, V_{DD2H}, V_{DD2L}	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
V_{SS}	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**Reset:** When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	**No connect:** Not internally connected.

Package Dimensions

315-Ball Package (Package Code: DS)

Figure 5: 315-Ball TFBGA – 12.4mm × 15mm (Package Code: DS)


Seating plane
A
0.1
A
315X Ø0.475 ±0.05
Dimensions apply to
solder balls post-reflow
on Ø0.48 SMD ball pads.
Ball A1 ID
Ball A1 ID
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N P R T U V W Y AA
15 ±0.1
14.0 CTR
0.7 TYP
0.8 TYP
11.2 CTR
12.4 ±0.1
1 ±0.1
0.29 ±0.035

Notes:
1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni).

Product-Specific Mode Register Definition

Table 6: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			**Unified NT ODT behavior mode**	**DMI output behavior mode**	**Optimized refresh mode**	**Enhanced WCK always-on mode**	**Latency mode**	**NT ODT timing mode**
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
MR5	**Manufacturer ID**							
	1111 1111b : Micron							
MR6	**Revision ID1**							
	0000 0110b							
MR8	**I/O width**		**Density**					
	OP[7:6] = 00b: x16		OP[5:2] = 0100b: 8Gb					
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			**WCK2DQ OSC FM**					
	OP[5] = 1b: WCK2DQ OSC FM supported							
MR21	**WXS**				**ODTD-CSFS**	**WXFS**	**RDCFS**	**WDCFS**
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	**RECC**		**WECC**					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 3)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 3)							
MR24	**DFES**							
	OP[7] = 1b: DFE is supported							
MR26		**RDQSTFS**						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							

Table 6: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR27								**RFM**
	OP[0] = 0b: RFM not required							
MR43		**SBEC Rule**						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							

Notes:
1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5 Specification 1 for mode registers not described here.
3. Write link ECC and read link ECC are supported.

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5 Specifications 2 for detailed conditions.

Table 7: I_{DD} Parameters – Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C

Notes 1 and 2 apply to entire table.

Symbol	Supply	Speed Grade	Unit	Note
		6400 Mb/s		
I_{DD01}	V_{DD1}	2.80	mA	
I_{DD02H}	V_{DD2H}	32.00		
I_{DD02L}	V_{DD2L}	0.25		
I_{DD0Q}	V_{DDQ}	0.75		
I_{DD2P1}	V_{DD1}	1.20	mA	
I_{DD2P2H}	V_{DD2H}	1.80		
I_{DD2P2L}	V_{DD2L}	0.25		
I_{DD2PQ}	V_{DDQ}	0.75		
I_{DD2PS1}	V_{DD1}	1.20	mA	
$I_{DD2PS2H}$	V_{DD2H}	1.80		
$I_{DD2PS2L}$	V_{DD2L}	0.25		
I_{DD2PSQ}	V_{DDQ}	0.75		
I_{DD2N1}	V_{DD1}	1.20	mA	
I_{DD2N2H}	V_{DD2H}	16.00		
I_{DD2N2L}	V_{DD2L}	0.25		
I_{DD2NQ}	V_{DDQ}	0.75		
I_{DD2NS1}	V_{DD1}	1.20	mA	
$I_{DD2NS2H}$	V_{DD2H}	16.00		
$I_{DD2NS2L}$	V_{DD2L}	0.25		
I_{DD2NSQ}	V_{DDQ}	0.75		
I_{DD3P1}	V_{DD1}	1.30	mA	
I_{DD3P2H}	V_{DD2H}	4.80		
I_{DD3P2L}	V_{DD2L}	0.25		
I_{DD3PQ}	V_{DDQ}	0.75		
I_{DD3PS1}	V_{DD1}	1.30	mA	
$I_{DD3PS2H}$	V_{DD2H}	4.80		
$I_{DD3PS2L}$	V_{DD2L}	0.25		
I_{DD3PSQ}	V_{DDQ}	0.75		
I_{DD3N1}	V_{DD1}	1.60	mA	
I_{DD3N2H}	V_{DD2H}	23.00		
I_{DD3N2L}	V_{DD2L}	0.25		
I_{DD3NQ}	V_{DDQ}	0.75		

Table 7: I_{DD} Parameters – Single Die (Continued)

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C

Notes 1 and 2 apply to entire table.

Symbol	Supply	Speed Grade	Unit	Note
		6400 Mb/s		
I_{DD3NS1}	V_{DD1}	1.60	mA	
$I_{DD3NS2H}$	V_{DD2H}	23.00		
$I_{DD3NS2L}$	V_{DD2L}	0.25		
I_{DD3NSQ}	V_{DDQ}	0.75		
I_{DD4R1}	V_{DD1}	7.10	mA	3, 4
I_{DD4R2H}	V_{DD2H}	360.00		
I_{DD4R2L}	V_{DD2L}	0.25		
I_{DD4RQ}	V_{DDQ}	105.78		
I_{DD4W1}	V_{DD1}	6.10	mA	3
I_{DD4W2H}	V_{DD2H}	280.00		
I_{DD4W2L}	V_{DD2L}	0.25		
I_{DD4WQ}	V_{DDQ}	0.75		
I_{DD51}	V_{DD1}	20.00	mA	
I_{DD52H}	V_{DD2H}	160.00		
I_{DD52L}	V_{DD2L}	0.25		
I_{DD5Q}	V_{DDQ}	0.75		
I_{DD5AB1}	V_{DD1}	2.20	mA	
$I_{DD5AB2H}$	V_{DD2H}	24.00		
$I_{DD5AB2L}$	V_{DD2L}	0.25		
I_{DD5ABQ}	V_{DDQ}	0.75		
I_{DD5PB1}	V_{DD1}	2.20	mA	
$I_{DD5PB2H}$	V_{DD2H}	24.00		
$I_{DD5PB2L}$	V_{DD2L}	0.25		
I_{DD5PBQ}	V_{DDQ}	0.75		

Notes:
1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BG mode. DVFSC and DVFSQ disabled.
3. BL = 16, DBI disabled.
4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF, R_{ON} = 40 ohm, T_C = 25°C.

Table 8: Full-Array Power-Down Self Refresh Current – Single Die

V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V; T_C = –25°C to +85°C

Temperature	Symbol	Supply	Value	Unit
25°C	I_{DD61}	V_{DD1}	0.25	mA
	I_{DD62H}	V_{DD2H}	0.60	
	I_{DD62L}	V_{DD2L}	0.01	
	I_{DD6Q}	V_{DDQ}	0.01	
85°C	I_{DD61}	V_{DD1}	2.00	
	I_{DD62H}	V_{DD2H}	5.30	
	I_{DD62L}	V_{DD2L}	0.25	
	I_{DD6Q}	V_{DDQ}	0.75	

Notes:
1. I_{DD6}25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6}85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
2. DVFSC and DVFSQ disabled.

Revision History

Rev. B – 10/2020

- Updated 315b package Coplanarity from 0.08mm to 0.1mm

Rev. A – 9/2020

- Initial release , CCM005-1974498342-68 y31m_embedded_lpddr5.pdf – Rev. A 4/2020 EN

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992
Micron and the Micron logo are trademarks of Micron Technology, Inc.
All other trademarks are the property of their respective owners.
This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.