Reference Schematics For RK3588

RK3588_AIOT_REF_SCH_V10

Main Functions Introduction

1) PMIC: 1xRK806-1+DiscretePower
2) RAM: 2xLPDDR4/4X_32bit or 2xLPDDR5_32bit
3) ROM: eMMC5.1(Default) or SPI Flash
4) Support: 1xSDMMC3.0 Card
5) Support: 1 x TYPEC3.0(With DP TX)+1 x USB3.0 HOST+ 1 x USB20 HOST or USB3.0/2.0 HUB
6) Support: 3 x SATA3.0 Connector (7pin) or SATA PM
7) Support: 1 x 4Lane PCIe3.0 Connector (Dual Mode)
8) Support: 2 x 4Lanes MIPI DPHY RX Camera
9) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
10) Support: 1 x HDMI2.0 RX
11) Support: 2 x HDMI2.1 TX or 2 x eDP1.3 TX
12) Support: 2 x 4Lanes MIPI D/CHY-TX
13) Support: 1xVGA Connector(DP to VGA)
14) Support: 1x4Lanes DP Port
15) Support: a/b/g/n/ac/ax 2T2R WIFI 6/5(PCIE/SDIO) +BT5.0
16) Support: 1x 10/100/1000 RJ45 Port(RGMII)
17) Support: 1x 10/100/1000 RJ45 Port(PCIE)
18) Support: 4G Module
19) Support: PCIE M.2
20) Support: 1xHeadphone+2xSPK+1xAnalog MIC

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Project:	RK3588_AIOT_SCH				
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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	01.Index and Notes				
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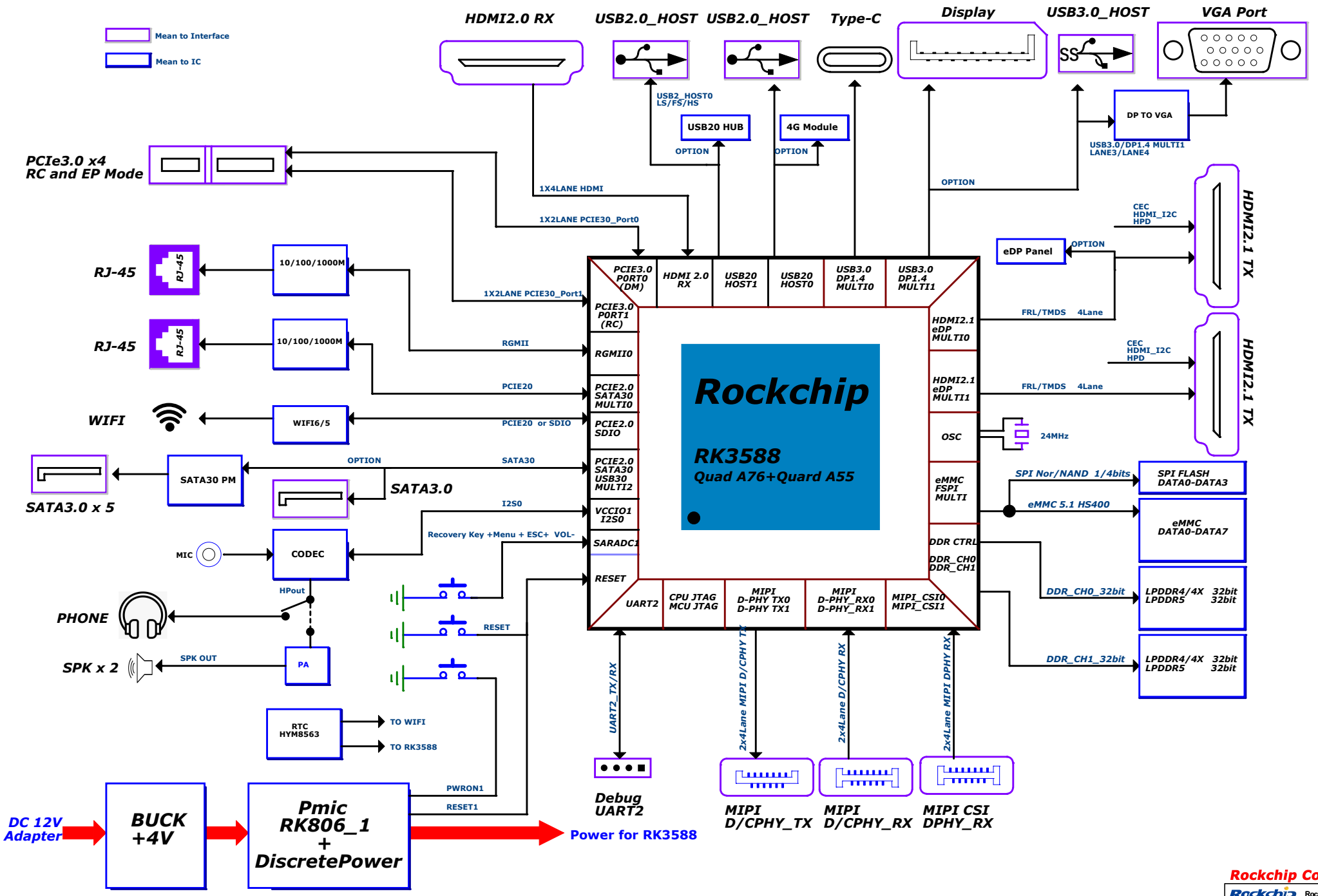
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2021-12-28	Felix.ruan	1:Revision preliminary version	Chenw



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Power Tree

12V/3A Adapter

VCC12V_DCIN

Note:
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe

DC/DC 8000mA

DC/DC 3000mA or 8000mA

Option

VCC4V0_SYS Seq:0

VCC5V0_SYS Seq:0

DC/DC 3000mA
- FAN Max:
- VCC3V3_PCIE Max:
- MOS
- VCC12V_PCIE30 Max:

Option
- FAN(Opt) Max:
- TYPEC0 Max:
- USB30_HOST Max:
- USB2.0 HOST Max:
- VCC5V_HDMI_TX0/1 Max:

Note:
For more information about RK3588'S power,please read document "RK3588 Power Consumption Test Report"

RK806-1

Power on Sequence

VCC1	BUCK1 6.5A max	Seq:5	VDD_GPU_S0 Max:6200mA	VDD_GPU / VDD_GPU_MEM
VCC2	BUCK2 5.0A max	Seq:3	VDD_CPU_LIT_S0 Max:2800mA	VDD_CPU_LIT / VDD_CPU_LIT_MEM
VCC3	BUCK3 5.0A max	Seq:2	VDD_LOGIC_S0 Max:1750mA	VDD_LOGIC
VCC4	BUCK4 5.0A max	Seq:5	VDD_VDENC_S0 Max:1800mA	VDD_VDENC / VDD_VDENC_MEM
VCC5	BUCK5 2.5A max	Seq:2	VDD_DDR_S0 Max:2300mA	VDD_DDR_S0: DDR_CH0_VDD Max:, DDR_CH0_VDD_MIF Max:, DDR_CH1_VDD Max:, DDR_CH1_VDD_MIF Max:
VCC6	BUCK6 2.5A max	Seq:4	VDD2_DDR_S3 Max:1000mA	LPDDR4 VDDQ Max:, LPDDR4/4x VDD2 Max:, LPDDR5 VDD2H Max:, DDR_CH0/1_VDDQ_CKE Max:
VCC7	BUCK7 2.5A max	Seq:1	VCC_2V0_PLDO_S3 Max:	
VCC8	BUCK8 2.5A max	Seq:6	VCC_3V3_S3	VCC_3V3_S3: MOS; VCC_3V3_S0: VGA IC Max:, LCD Max:, RGMII Max:; Typec CC IC Max:, WIFI BATT Max:, eMMC VCC Max:, VCC_RTC Max:, Hall IC Max:, Camera Input Max:, IR Receiver Max:, Debug Max:, PMUIO2 Max:, VCCIO5&VCCIO6 Max:
VCC9	BUCK9 2.5A max	Seq:6	VDDQ_DDR_S0 Max:500mA	VDDQ_DDR_S0: LPDDR4x/LPDDR5 VDDQ Max:, DDR_CH1_VDDQ_CK Max:, DDR_CH0_VDDQ_CK Max:, DDR_CH1_VDDQ Max:, DDR_CH0_VDDQ Max:
VCC10	BUCK10 2.5A max	Seq:3	VCC_1V8_S3	VCC_1V8_S3: VDD1_1V8_DDR Max:, WIFI VDDIO Max:, eMMC VCCQ Max:, EMMCIO_1V8 Max:, PMUIO1_1V8 Max:, PMUIO2_1V8 Max:
	PLDO1 500mA max	Seq:3	VCCA_1V8_S0	VCCA_1V8_S0: OSC_1V8 Max:, PLL_AVDD1V8 Max:, USB20_AVDD_1V8 Max:, SARADC_AVDD_1V8 Max:, DDR_CH0_PLL_AVDD1V8 Max:, DDR_CH1_PLL_AVDD1V8 Max:, TYPEC0_DP0_VDDH_1V8 Max:, TYPEC0_DP1_VDDH_1V8 Max:, PCIE20_SATA30_0_AVDD_1V8 Max:, PCIE20_SATA30_1_AVDD_1V8 Max:, PCIE20_SATA30_USB30_2_AVDD_1V8 Max:, PCIE30_PORT0_AVDD1V8 Max:, PCIE30_PORT1_AVDD1V8 Max:
VCC_2V0_PLDO_S3	PLDO2 300mA max	Seq:3	VCC_1V8_S0	VCC_1V8_S0: MIPI_CSI0_AVCC1V8 Max:, MIPI_CSI1_AVCC1V8 Max:, HDMI/EDP_TX0_VDD_IO_1V8 Max:, HDMI/EDP_TX0_VDD_CMN_1V8 Max:, HDMI/EDP_TX1_VDD_IO_1V8 Max:, HDMI/EDP_TX1_VDD_CMN_1V8 Max:, MIPI_D/C_PHY0_VDD_1V8 Max:, MIPI_D/C_PHY1_VDD_1V8 Max:, VCCIO1-6_VDD_1V8 Max:, AVCC_1V8_CODEC Max:, RGMII Max:
VCC11	PLDO3 300mA max	Seq:4	VDDA_1V2_S0	MIPI_D/C_PHY0_VDD_1V2 Max:, MIPI_D/C_PHY1_VDD_1V2 Max:
VCC12	PLDO4 500mA max	Seq:6	VCCA_3V3_S0	Sensor Max:, CODEC_VCCA3V3 Max:, USB20_AVDD_3V3 Max:, HDMIRX_VPH3V3 Max:, HDMIRX_DVDD3V3 Max:
	PLDO5 300mA max	Seq:6	VCCIO_SD_S0	VCCIO_SD Max:
VCCA	PLDO6 300mA max	Seq:3	VCC_1V8_S3_PLDO6	
	NLDO1 300mA max	Seq:2	VDD_0V75_S3	VDD_0V75_S3: PMU_0V75 Max:, USB20_DVDD_0V75 Max:, HDMI/EDP_TX0_VDD/AVDD_0V75 Max:, HDMI/EDP_TX1_VDD/AVDD_0V75 Max:, HDMI_RX_AVDD0V75 Max:
VCC_1V1_NLDO_S3	NLDO2 300mA max	Seq:2	VDDA_DDR_PLL_S0	DDR_CH0_PLL_DVDD Max:, DDR_CH1_PLL_DVDD Max:
	NLDO3 500mA max	Seq:2	VDDA_0V75_S0	VDDA_0V75_S0: PLL_DVDD0V75 Max:, OTP_VDDOTP_0V75 Max:, MIPI_CSI0_AVCC0V75 Max:, MIPI_CSI1_AVCC0V75 Max:, PCIE30_PORT0_AVDD0V75 Max:, PCIE30_PORT1_AVDD0V75 Max:, MIPI_D/C_PHY0_VDD Max:, MIPI_D/C_PHY1_VDD Max:
VCC_1V1_NLDO_S3	NLDO4 500mA max	Seq:2	VDDA_0V85_S0	VDDA_0V85_S0: TYPEC0_DP0_VDD_0V85 Max:, TYPEC0_DP0_VDDA_0V85 Max:, TYPEC0_DP1_VDD_0V85 Max:, TYPEC0_DP1_VDDA_0V85 Max:, PCIE20_SATA30_0_AVDD_0V85 Max:, PCIE20_SATA30_1_AVDD_0V85 Max:, PCIE20_SATA30_USB30_2_AVDD_0V8 Max:
	NLDO5 300mA max	Seq:2	VDD_0V75_S0	VDD_0V75_S0
	RK860-2 ,6A	Seq:6A	VDD_CPU_BIG0_S0 Max:3500mA	VDDCPU_BIG0 / VDDCPU_BIG0_MEM
	RK860-3 ,6A	Seq:6A	VDD_CPU_BIG1_S0 Max:3500mA	VDDCPU_BIG1 / VDDCPU_BIG1_MEM
	RK860-2 ,6A	Seq:6A	VDD_NPU_S0 Max:4000mA	VDD_NPU / VDD_NPU_MEM
	EXT DC/DC ,2A	Seq:0A	VCC_1V1_NLDO_S3 Max:	
	EXT DC/DC ,2A	Seq:0A	VDD2L_DDR_S3 Max:	LPDDR5 VDD2L Max:

VCC_3V3_S3 → LDO or BUCK / LDO / LDO → VCC_1V2_CAM Max:, VCC_1V8_CAM Max:, VCC_2V8_CAM Max:

VCC_3V3_S3 → MOS → VCC3V3_SD_S0 Max:

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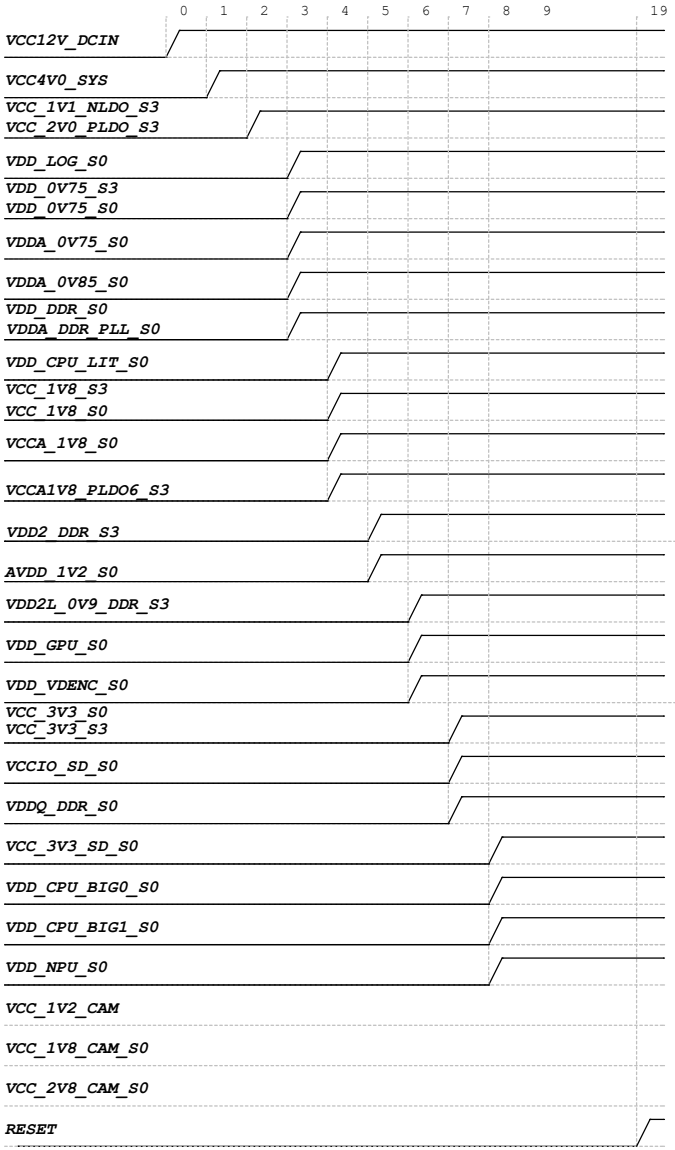
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

Rockchip	Rockchip Electronics Co., Ltd				
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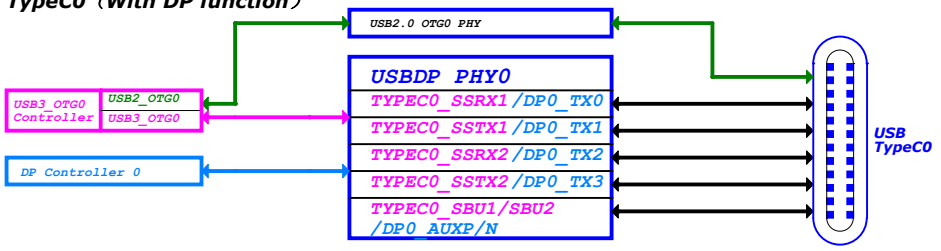
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

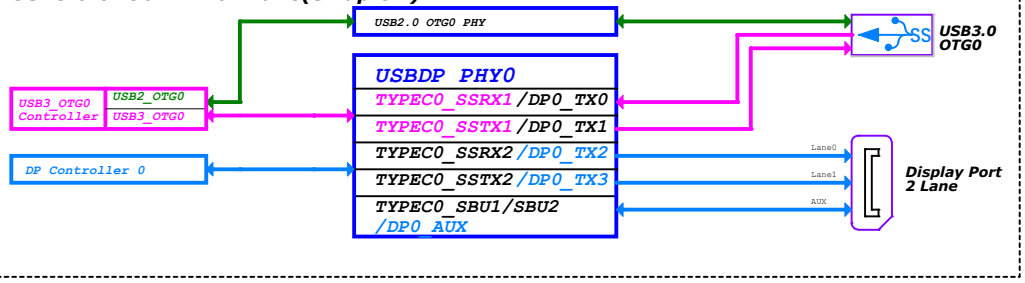
			OPTION1 USB30 HOST	OPTION2 USB30 HOST	OPTION3 USB30 HOST
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM		
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM			USB20_HOST1_DP USB20_HOST1_DM	
					TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

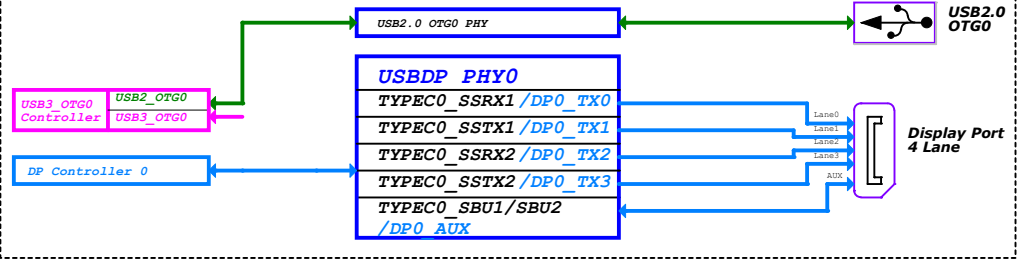
Config0:
TypeC0（With DP function）



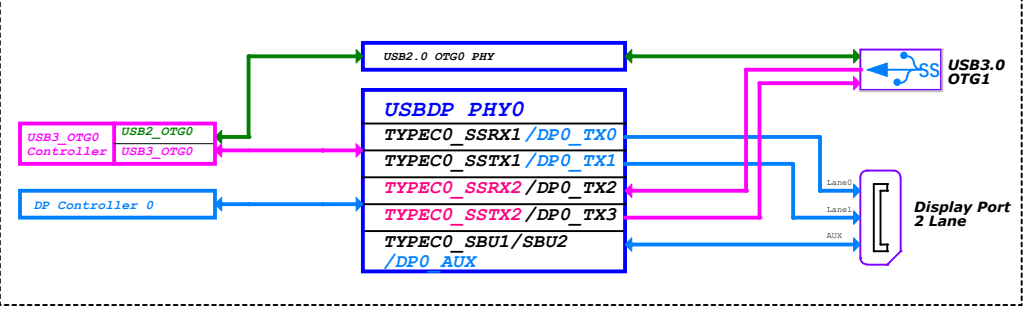
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



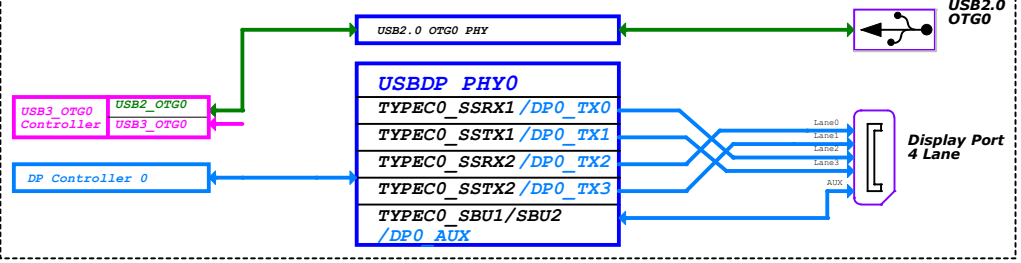
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)

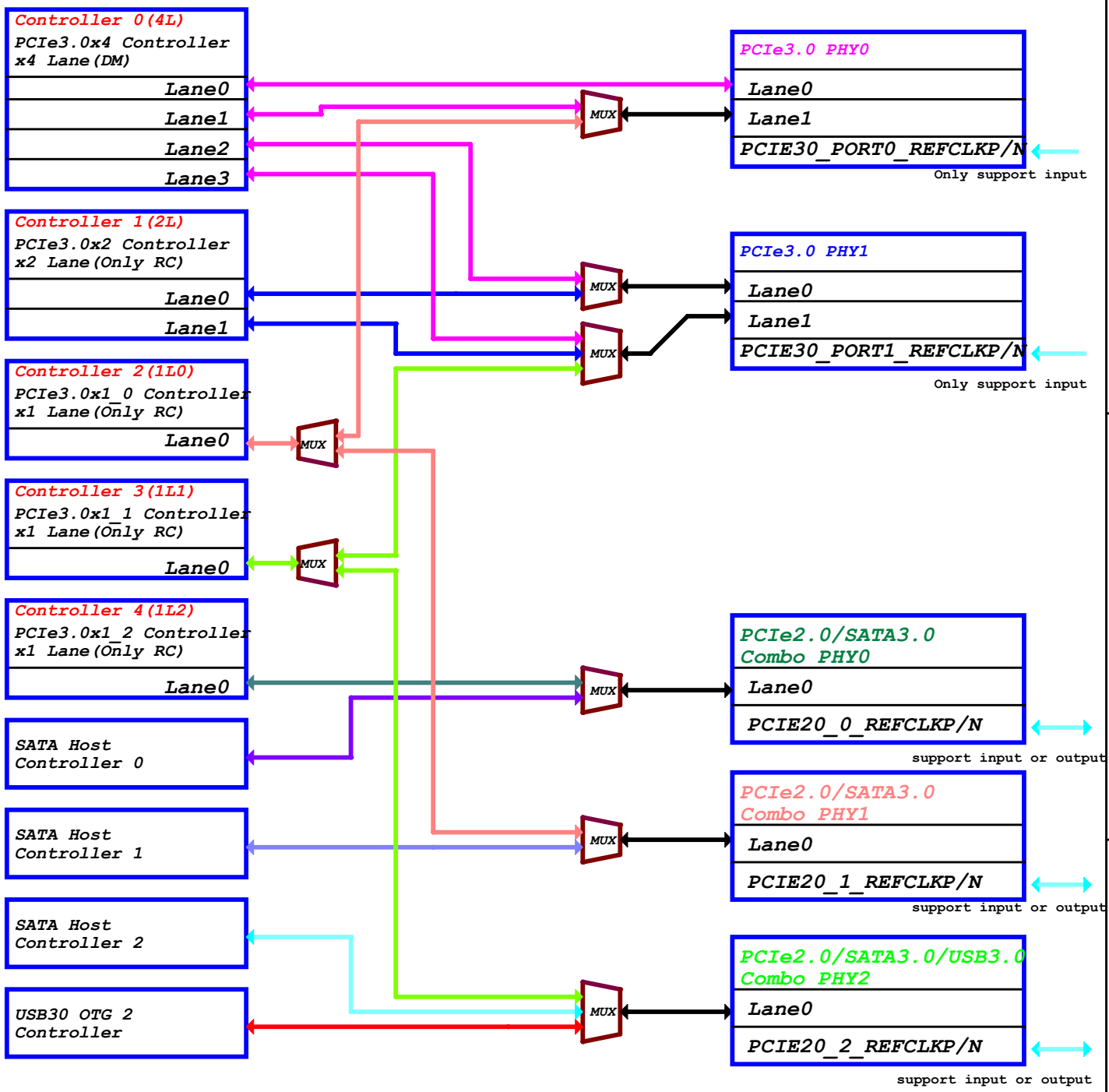


Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	07.USB Controller Configure Tab
Date:	Thursday, December 30, 2021
Designed by:	RDF
Reviewed by:	
Rev:	V1.0
Sheet:	7 of 99

PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M*
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M*
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

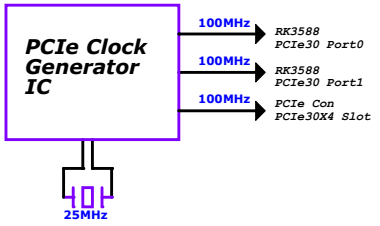
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

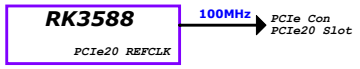
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



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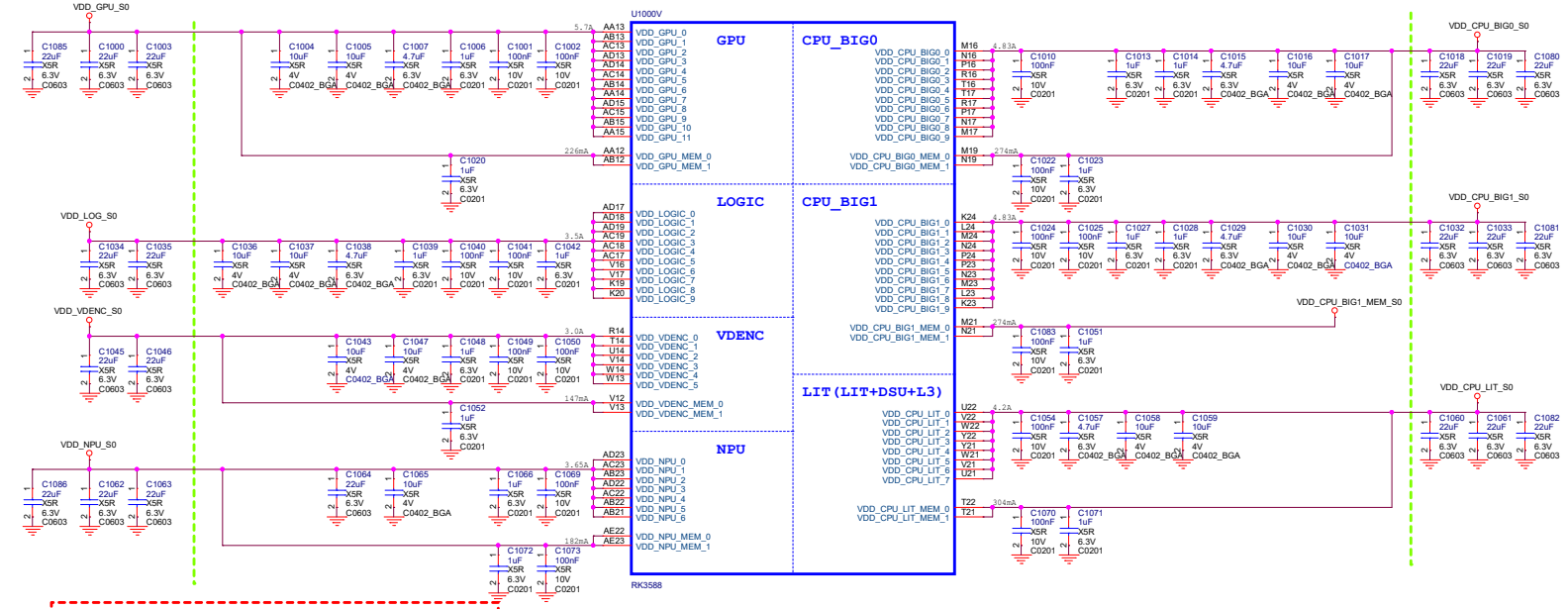
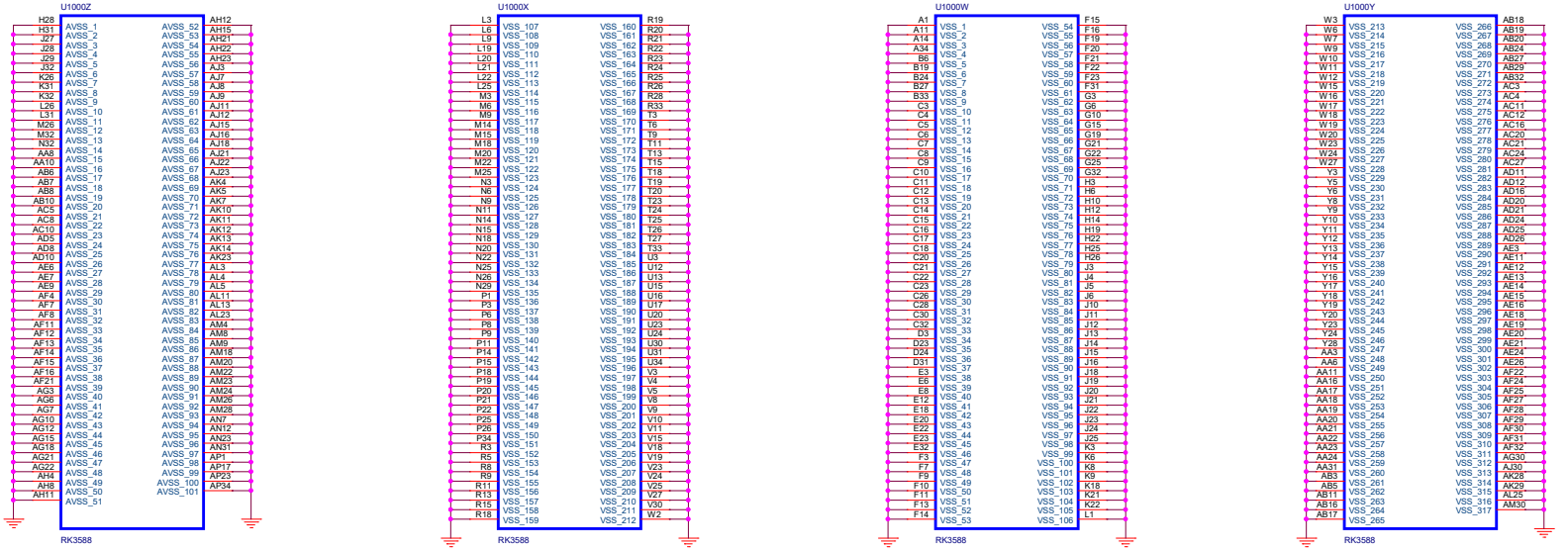
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	08.PCIE Fun Map		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by:	Sheet: 8 of 99

RK3588_V(POWER)



Note:

The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



Rockchip Confidential

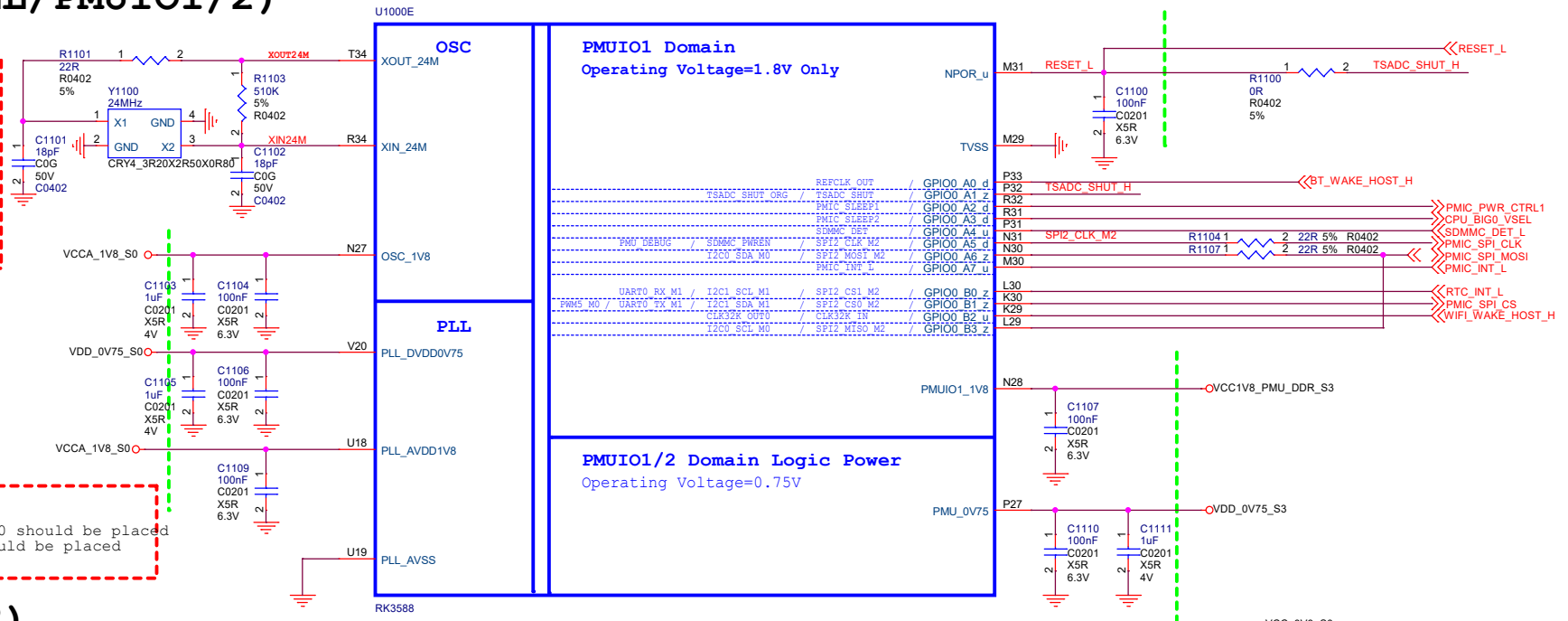
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	10.RK3588_Power/GND		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by:	Sheet: 10 of 99

RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

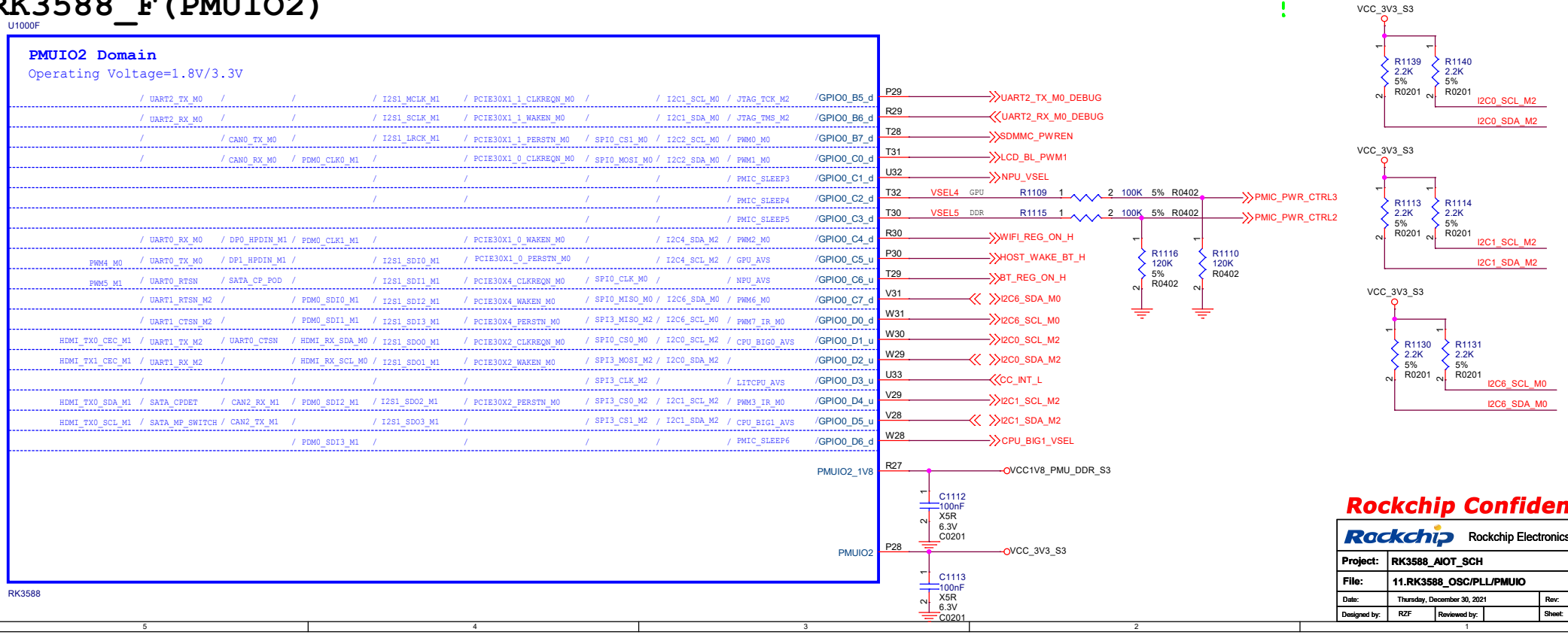
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588_F(PMUIO2)



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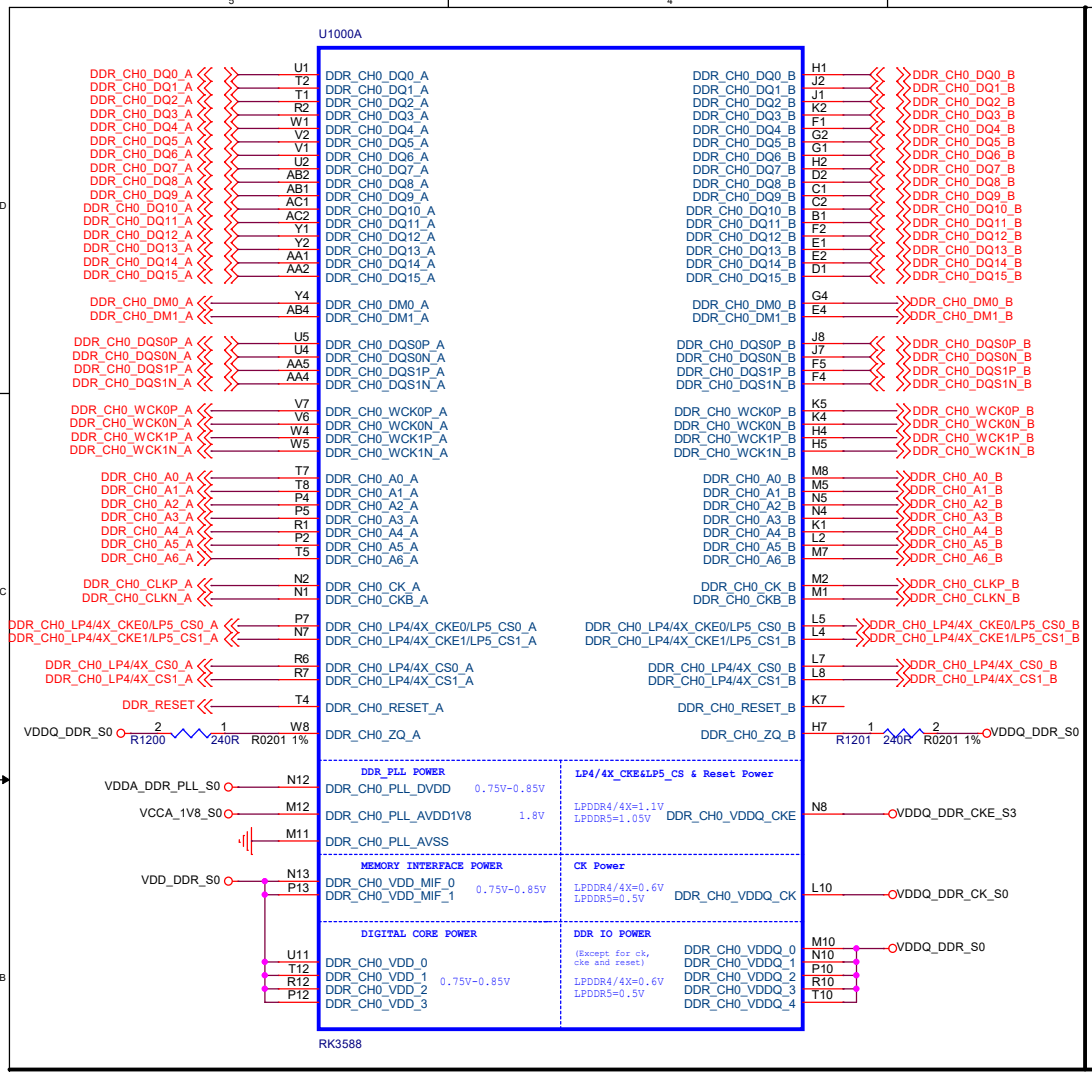
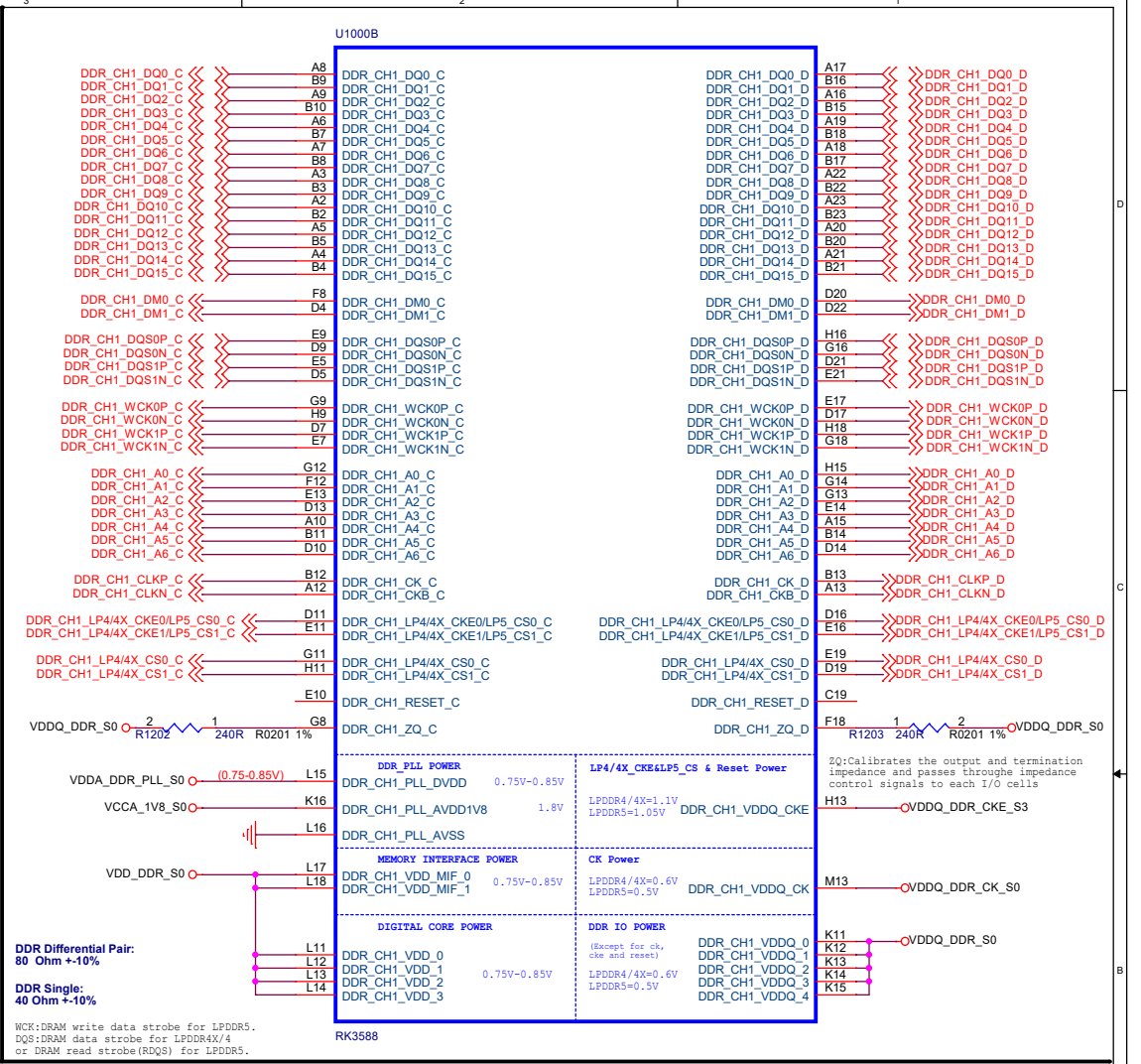
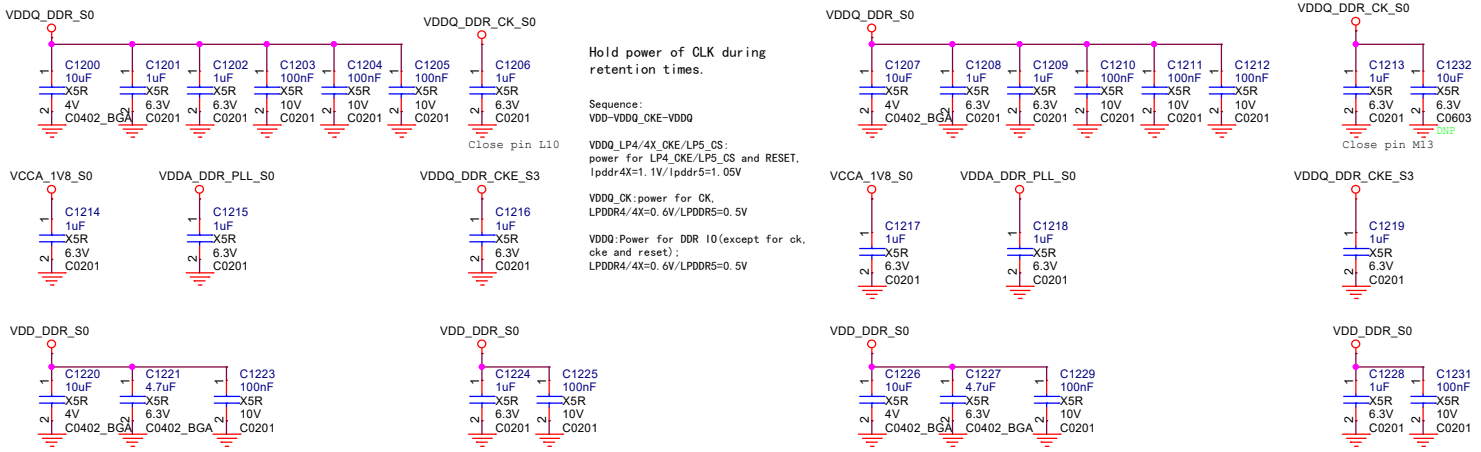
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	11.RK3588_OSC/PLL/PMUIO		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	11 of 99



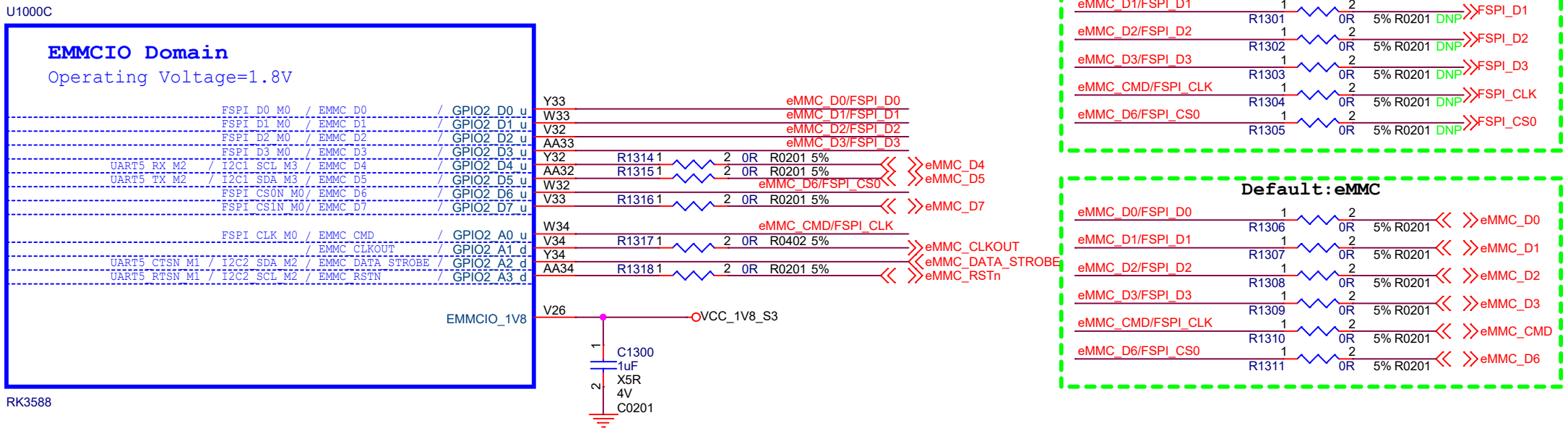


DDR FILTER

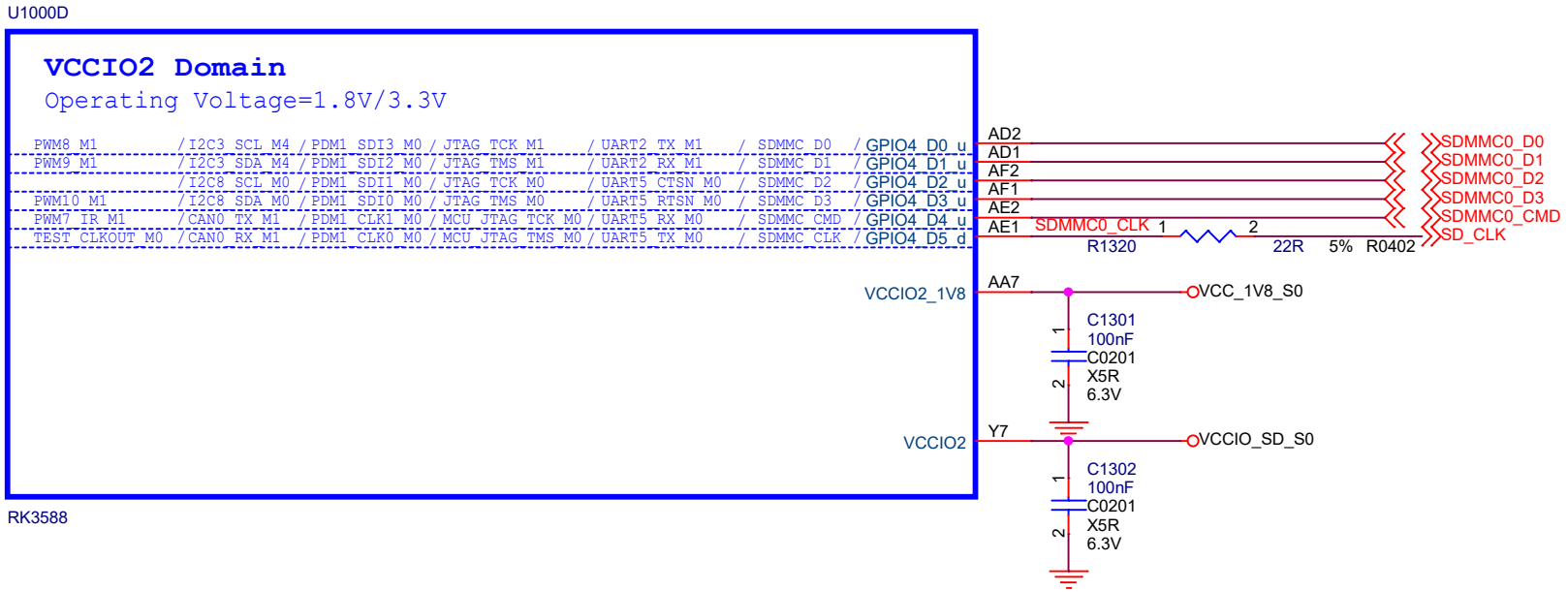


Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	12.RK3588 DDR Controler				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	12 of 99

RK3588_C(EMMCIO Domain)



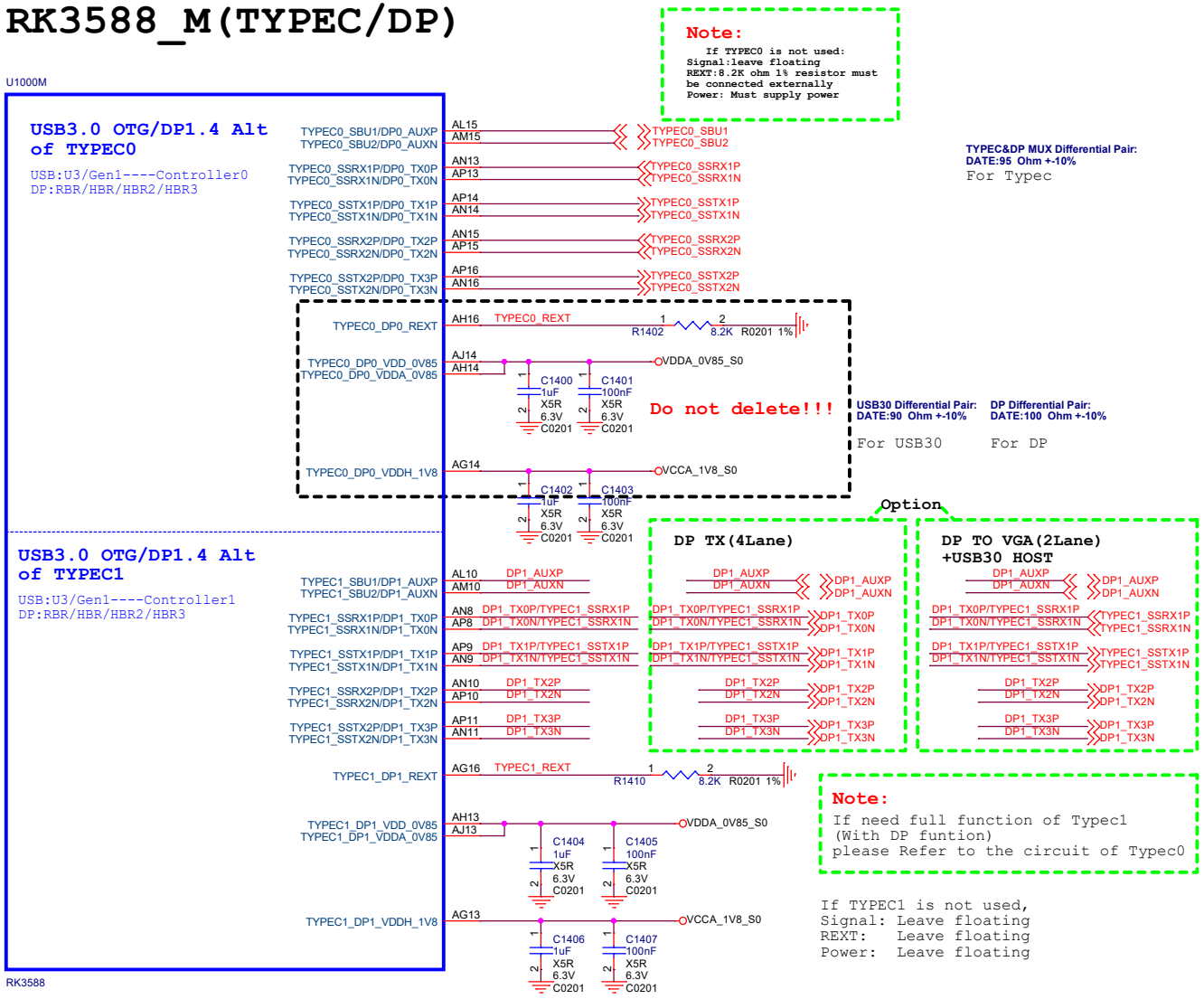
RK3588_D(VCCIO2 Domain)



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	13.RK3588_Flash/SD Controller		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	13 of 99

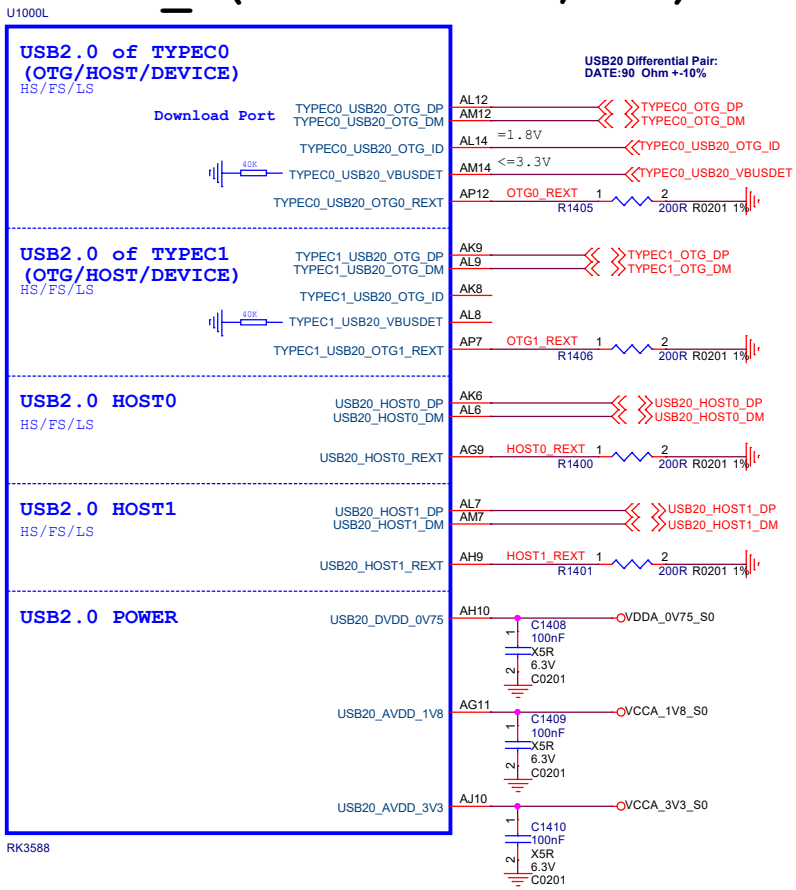
RK3588_M(TYPEC/DP)



USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:

TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:

If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating

USB20_HOST0/USB20_HOST1:

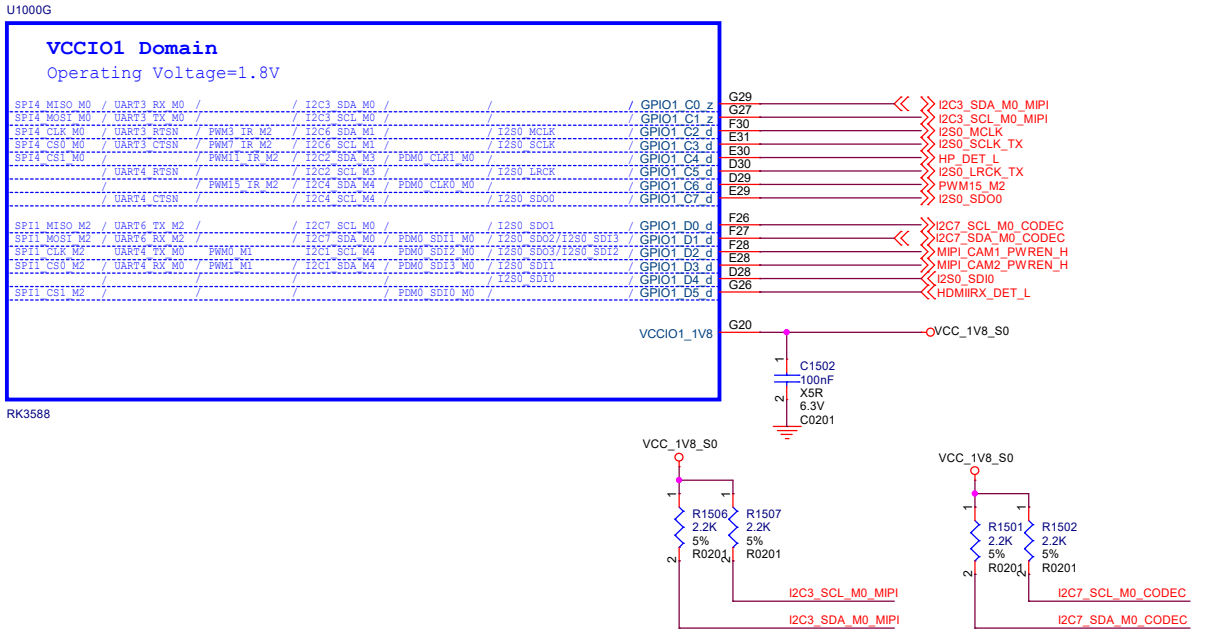
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:

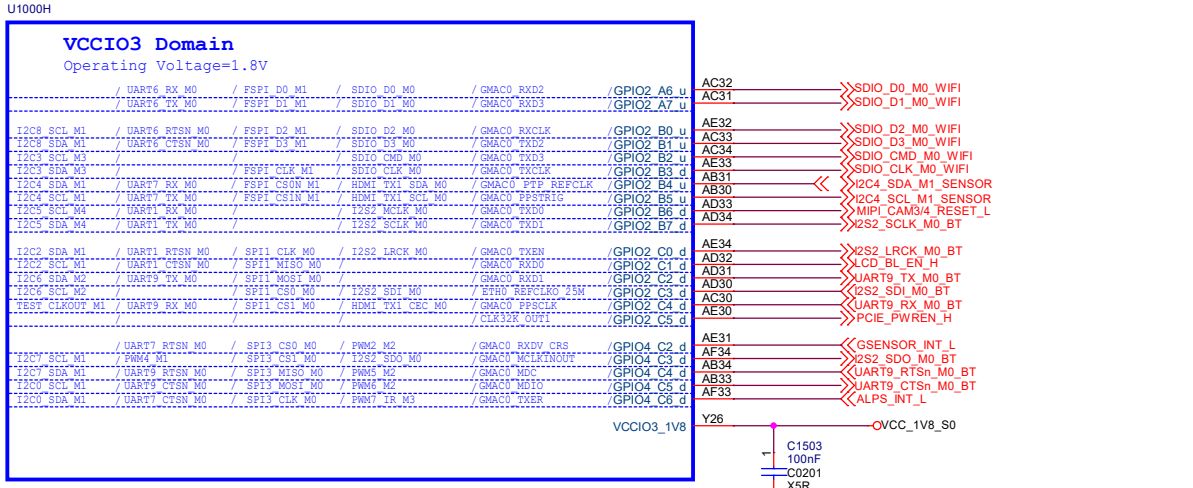
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

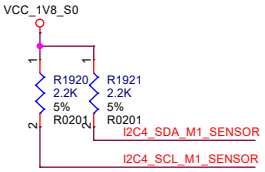
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	14.RK3588_USB30/USB20_Ctrl				
Date:	Thursday, December 30, 2021		Rev:	V1.0	
Designed by:	RZF	Reviewed by:		Sheet:	14 of 99

RK3588_G(VCCIO1 Domain)

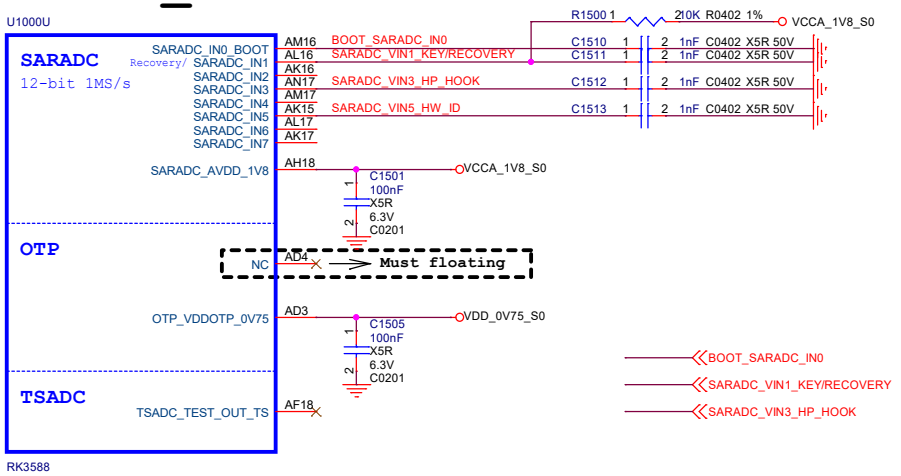


RK3588_H(VCCIO3 Domain)





RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

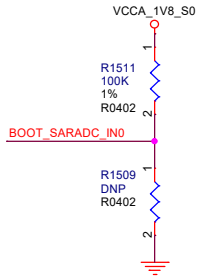


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

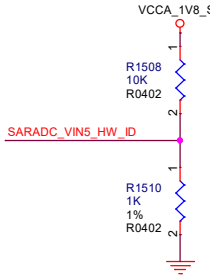


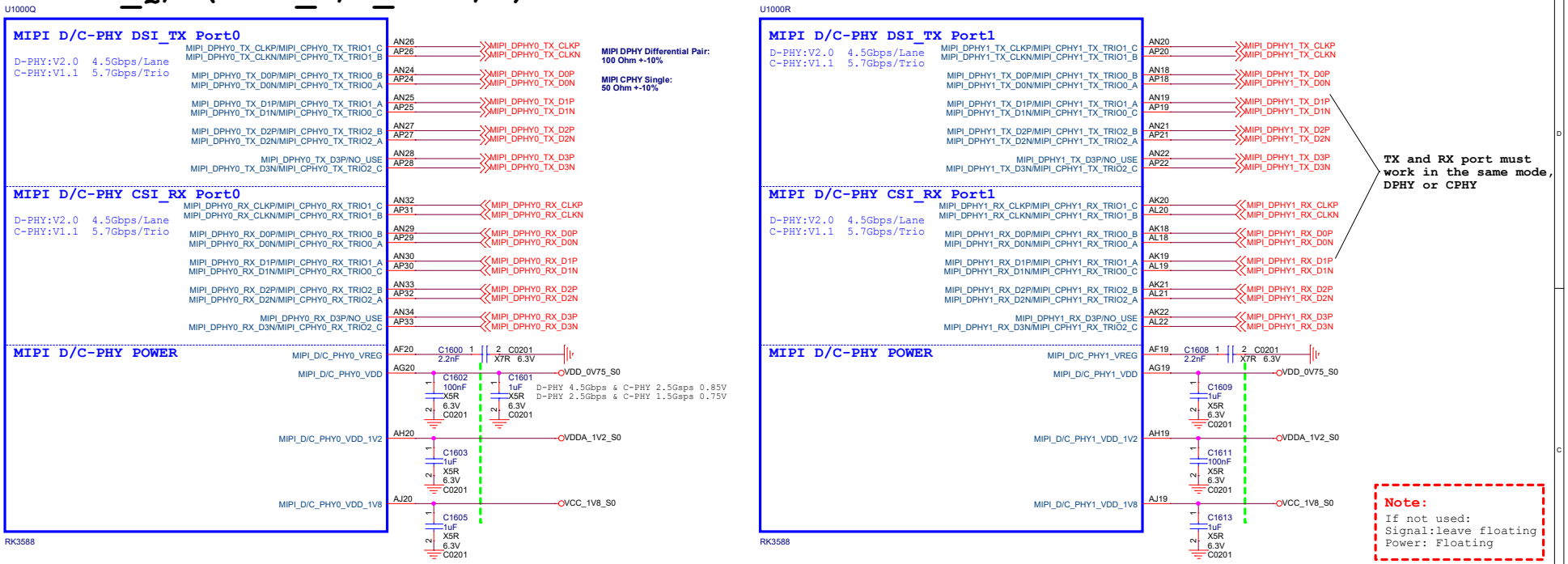
TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

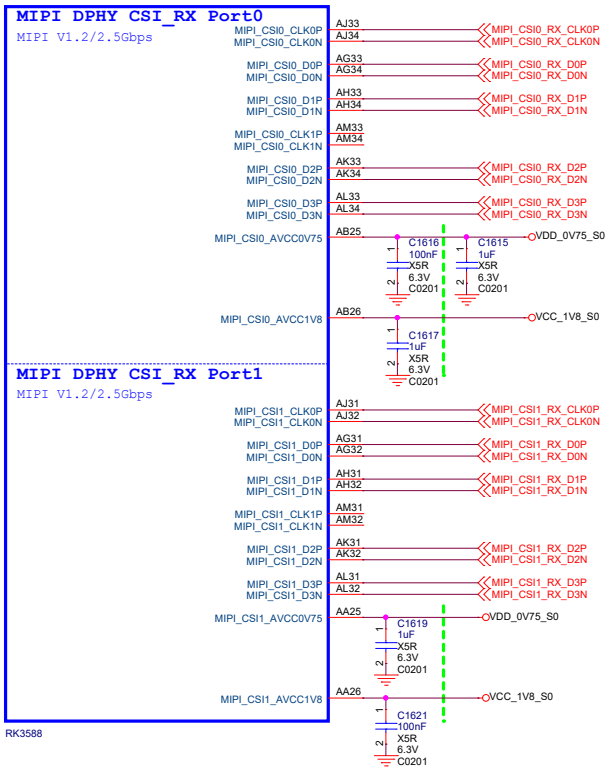
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	15.RK3588_SARADC/1.8V Only GPIO		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	15 of 99

RK3588_Q/R(MIPI_D/C_PHY0/1)



RK3588_P(MIPI_DPHY_CSI_RX_PHY)



MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

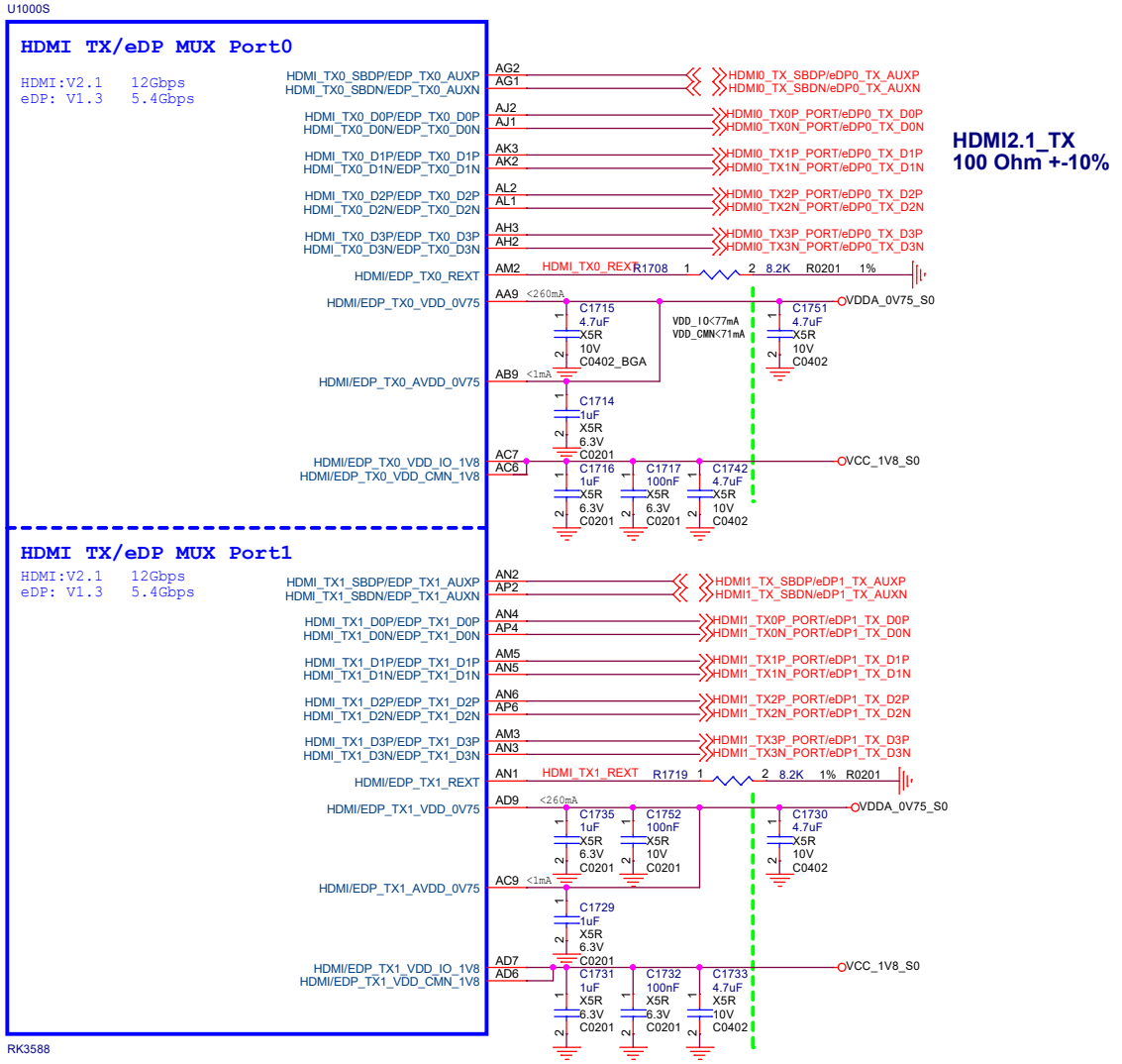
Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	16.RK3588_MIPI Interface		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	16 of 99

RK3588_S(HDMI2.1 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

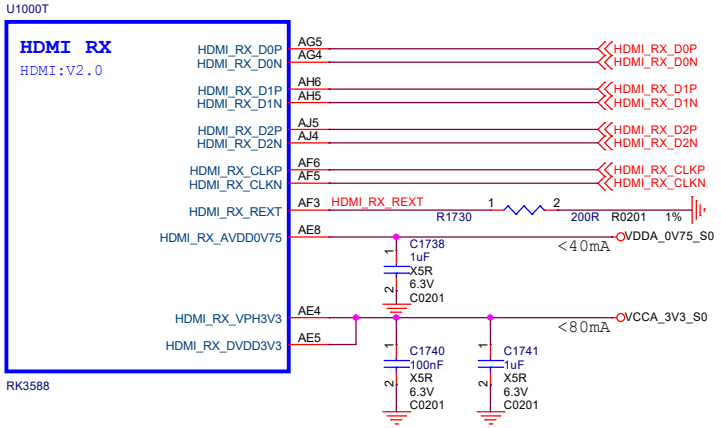


HDMI2.1_TX
100 Ohm +-10%

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



HDMI20_RX
100 Ohm +-10%

Note:
If not used:
Signal:leave floating
Power: Floating

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Project:	RK3588_AIOT_SCH				
File:	17.RK3588_HDMI/eDP Interface				
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RK3588_N(PCIE20)

U1000N

Note:
If not used:
Signal:leave floating
Power: Floating

PCIE20/SATA30 Mux0

PCIe20x1_2 1Lane(RC)--4(1L2)
SATA30 HOST Controller0
MUX
input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN — L32 / L33
PCIE20_0_TXP/SATA30_0_TXP — M34 → PCIE20_0_TXP/SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN — M33 → PCIE20_0_TXN/SATA30_0_TXN
PCIE20_0_RXP/SATA30_0_RXP — N33 → PCIE20_0_RXP/SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN — N34 → PCIE20_0_RXN/SATA30_0_RXN
PCIE20_SATA30_0_AVDD_0V85 — M28 → VDDA_0V85_S0
C1810 10uF X5R 4V C0402
PCIE20_SATA30_0_AVDD_1V8 — M27 → VCCA_1V8_S0
C1808 1uF X5R 4V C0201

CLK Differential Pair: 100 Ohm±10%
DATA Differential Pair: PCIE20: 85 Ohm ±10% SATA30: 100 Ohm ±10% USB30: 90ohm ±10%

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0 1Lane(RC)--2(1L0)
SATA30 HOST Controller1
MUX
input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN — H32 / H33 → PCIE20_1_REFCLKP / PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP — K33 → PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN — K34 → PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP — J33 → PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN — J34 → PCIE20_1_RXN/SATA30_1_RXN
PCIE20_SATA30_1_AVDD_0V85 — L28 → VDDA_0V85_S0
C1818 100nF X5R 6.3V C0201
PCIE20_SATA30_1_AVDD_1V8 — L27 → VCCA_1V8_S0
C1816 100nF X5R 6.3V C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1 1Lane(RC)--3(1L1)
SATA30 HOST Controller2
USB30 HOST Controller2
MUX
input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN — G31 / G30 → PCIE20_2_REFCLKP / PCIE20_2_REFCLKN
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP — H30 → PCIE20_2_TXP/SATA30_2_TXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN — H29 → PCIE20_2_TXN/SATA30_2_TXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP — J31 → PCIE20_2_RXP/SATA30_2_RXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN — J30 → PCIE20_2_RXN/SATA30_2_RXN
PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 → VDDA_0V85_S0
C1806 1uF X5R 4V C0201
PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 → VCCA_1V8_S0
C1804 1uF X5R 4V C0201

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4 4Lane(DM)--0(4L)
PCIe30x1_0 1Lane(RC)--2(1L0) — PCIE20/SATA30 MUX1
PCIe30x2 2Lane(RC)--1(2L)
PCIe30x1_1 1Lane(RC)--3(1L1) — PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN — E33 / E34 → PCIE30_PORT0_REFCLKP_IN / PCIE30_PORT0_REFCLKN_IN

Lane0:
PCIE30_PORT0_TX0P/N — D32 / D33 → PCIE30_PORT0_TX0P/N
PCIE30_PORT0_RX0P/N — G33 / G34 → PCIE30_PORT0_RX0P/N

Lane1:
PCIE30_PORT0_TX1P/N — C33 / C34 → PCIE30_PORT0_TX1P/N
PCIE30_PORT0_RX1P/N — F32 / F33 → PCIE30_PORT0_RX1P/N

PCIE30_PORT0_RESREF — B34 PCIE30_0_REF — R1801 1 2 200R 1% R0201
PCIE30_PORT0_AVDD0V75 — G24 → VDD_0V75_S0
C1802 1uF X5R 6.3V C0201
C1803 4.7uF X5R 10V C0402
PCIE30_PORT0_AVDD1V8 — G23 → VCCA_1V8_S0
C1800 1uF X5R 6.3V C0201
C1801 4.7uF X5R 10V C0402

CLK Differential Pair: 100 Ohm ±10%
DATA Differential Pair: PCIE30: 85 Ohm ±10%

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN — A28 / B28 → PCIE30_PORT1_REFCLKP_IN / PCIE30_PORT1_REFCLKN_IN

Lane0:
PCIE30_PORT1_TX0P/N — B30 / A30 → PCIE30_PORT1_TX2P/N
PCIE30_PORT1_RX0P/N — B32 / A32 → PCIE30_PORT1_RX2P/N

Lane1:
PCIE30_PORT1_TX1P/N — C29 / B29 → PCIE30_PORT1_TX3P/N
PCIE30_PORT1_RX1P/N — C31 / B31 → PCIE30_PORT1_RX3P/N

PCIE30_PORT1_RESREF — A33 PCIE30_1_REF — R1807 1 2 200R 1% R0201
PCIE30_PORT1_AVDD0V75 — H24 → VDD_0V75_S0
C1814 1uF X5R 6.3V C0201
C1815 4.7uF X5R C0402 10V
PCIE30_PORT1_AVDD1V8 — H23 → VCCA_1V8_S0
C1812 100nF X5R 6.3V C0201
C1813 4.7uF X5R 10V C0402

RK3588

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

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Project:	RK3588_AIOT_SCH				
File:	18.RK3588_PCIE30/PCIE20/SATA30				
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Designed by:	RZF	Reviewed by:		Sheet:	18 of 99

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d
CAN2_RX_M0	PCIE30X4_CLKREQn_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1/ HDMI_TX0_HPD_M1/	MCU_JTAG_TCK_M1		GPIO3_D4_d
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d

AA29	MAC1_TXD2	R1512 1 2 0R 5% R0402	GMAC1_TXD2	
AA30	MAC1_TXD3	R1513 1 2 0R 5% R0402	GMAC1_TXD3	
AD27			GMAC1_RXD2	
AE27			GMAC1_RXD3	
AD28	MAC1_TXCLK	R1514 1 2 0R 5% R0402	GMAC1_TXCLK	
AH30			GMAC1_RXCLK	
AH27			ETH1_REFCLKO_25M	
AG29			GMAC1_RXD0	
AG28			GMAC1_RXD1	
AH29			GMAC1_RXDV_CRS	
AE28			USB_HUB_RESET	
AC28	MAC1_TXD0	R1515 1 2 0R 5% R0402	GMAC1_TXD0	
AC29	MAC1_TXD1	R1516 1 2 0R 5% R0402	GMAC1_TXD1	
AD29	MAC1_TXEN	R1517 1 2 0R 5% R0402	GMAC1_TXEN	
AE29	MAC1_MCLKINOUT	R1519 1 2 0R 5% R0402	GMAC1_MCLKINOUT	
AA28			GMAC1_RSTn_L	
Y29			TP_INT_L	
Y27			TP_RST_L	
Y31			GMAC1_MDC	
Y30		R1520 1 0R 2 5% R0402	GMAC1_MDIO	
AH26			HDMITX1_CEC_M2	
AH25			HDMITX1_SDA_M1	
AG26			HDMITX1_SCL_M1	
AJ24			I2C5_SCL_M0_TP	
AH24			I2C5_SDA_M0_TP	
AG23			HDMI_RX_CEC	
AG25			HDMI_RX_SCL_M1	
AG24			HDMI_RX_SDA_M1	
AA27			HDMIIRX_HPDOUT_H	
AB28			DP1_HPDIN_M0	

VCCIO5_1V8

W25 C1903 100nF X5R 6.3V C0201 VCC_1V8_S0

VCCIO5

W26 C1902 100nF X5R 6.3V C0201 VCC_3V3_S0

RK3588

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1		I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1		I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1			I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
		UART0_TX_M2			PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2		PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2	I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2	I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1		I2C5_SDA_M2	I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3	I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3	I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA0_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3	I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3	I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIFP0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1		I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1		HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1	HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d
		SPI3_CLK_M1		I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u
		SPI3_CS0_M1		I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d

AK30		PCIEX1_1_CLKREQn_M1_L
AL30		PCIEX1_1_WAKEn_M1_L/GPIO4_A1
AM29		PCIEX1_1_PERSTn_M1_L
AL29		SPK_CTL_H
AL28		PHONE_CTL
AK27		VGA_HPDIN_L
AL27		TYPEC0_SBU1_DC
AM27		TYPEC0_SBU2_DC
AK26		USB_HOST_PWREN_H
AL24		HDMI0_TX_ON_H
AK25		HDMI1_TX_ON_H
AM25		PCIE30X4_PRSNT_L/GPIO4_B3
AL26		PCIE30X4_CLKREQn_M1_L
AJ26		PCIE30X4_WAKEn_M1_L/GPIO4_B5
AJ27		PCIE30X4_PERSTn_M1_L
AJ28		HDMITX0_SCL_M0
AJ25		HDMITX0_SDA_M0
AK24		HDMITX0_CEC_M0

VCCIO6_1V8

AC25 C1909 100nF X5R 6.3V C0201 VCC_1V8_S0

VCCIO6

AC26 C1908 100nF X5R 6.3V C0201 VCC_3V3_S0

RK3588

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

	SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2/	DP0_HPDIN_M2		I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d	
SATA1_ACT_LED_M1	SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2		I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d	
PWM0_M2	SPI4_CLK_M2		VOP_POST_EMPTY		I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d	
PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2		I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d	
	SPI2_MISO_M0		HDMI_TX1_SCL_M2				GPIO1_A4_d	
	SPI2_MOSI_M0		HDMI_TX0_HPD_M0				GPIO1_A5_d	
	SPI2_CLK_M0		HDMI_TX1_HPD_M0				GPIO1_A6_d	
PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2			PDM1_SDI0_M1		GPIO1_A7_u	
	SPI2_CS1_M0	PCIE30X4_CLKREQN_M3			PDM1_SDI1_M1		GPIO1_B0_u	
	SPI0_MISO_M2	PCIE30X4_WAKEN_M3			PDM1_SDI2_M1		GPIO1_B1_d	
	SPI0_MOSI_M2	PCIE30X4_PERSTN_M3			PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d	
SATA0_ACT_LED_M1	SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2			PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d	
	SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2			PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u	
	SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2/				UART7_TX_M2	GPIO1_B5_u	
HDMI_RX_HPDOUT_M2/	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0		I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u	
SATA2_ACT_LED_M1/ HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0		I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u	
HDMI_RX_SCL_M2	PWM14_M2			MIPI_CAMERA3_CLK_M0		I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u	
HDMI_RX_SDA_M2	PWM15_IR_M3		PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0		I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u	

A24		I2C2_SDA_M4_MIPI
A25		I2C2_SCL_M4_MIPI
A26		MIPI_CAM1_PDN_L
A27		MIPI_CAM1/2_RESET_L
B25		MIPI_CAM2_PDN_L
B26		HDMITX0_HPDIN_M0
C24		HDMITX1_HPDIN_M0
C25		MIPI_CAM3_PDN_L
C27		MIPI_CAM4_PDN_L
D25		MIPI_CAM4_PWREN_H
D26		MIPI_CAM3_PWREN_H
D27		PCIEx1_0_WAKEn_M1_L/GPIO1_B3
E24		PCIEx1_0_PERSTn_M1_L
E25		PCIEx1_0_CLKREQn_M1_L
E26		MIPI_CAM1_CLKOUT
E27		MIPI_CAM2_CLKOUT
F24		MIPI_CAM3_CLKOUT
F25		MIPI_CAM4_CLKOUT

VCCIO4_1V8

H20 C1907 100nF X5R 6.3V C0201 VCC_1V8_S0

VCCIO4

H21

RK3588

PCIE30X4_WAKEn_M1_L/GPIO4_B5 R1910 1 2 0R R0402 5% DNP PCIE30X4_WAKEn_M1_L

R1909 1 2 0R R0402 5% PWM12_M1_FAN

PCIEX1_1_WAKEn_M1_L/GPIO4_A1 R1906 1 2 0R R0402 5% TYPEC5V_PWREN_H

R1931 1 2 0R R0402 5% DNP PCIEX1_1_WAKEn_M1_L

R1911 1 2 0R R0402 5% DNP PCIE30X4_PRSNT_L

PCIE30X4_PRSNT_L/GPIO4_B3 R1930 1 2 0R R0402 5% HG_DISABLE_L

R9507 1 2 0R R0402 5% DNP PCIEx1_0_WAKEn_M1_L

PCIEx1_0_WAKEn_M1_L/GPIO1_B3 R9507 1 2 0R R0402 5% LCD_PWREN_H

VCC_3V3_S0

R9507 2.2K 5% R0201 1 2 R95074 2.2K 5% R0201

I2C5_SDA_M0_TP

I2C5_SCL_M0_TP

VCC_1V8_S0

R1903 2.2K 5% R0201 1 2 R1904 2.2K 5% R0201

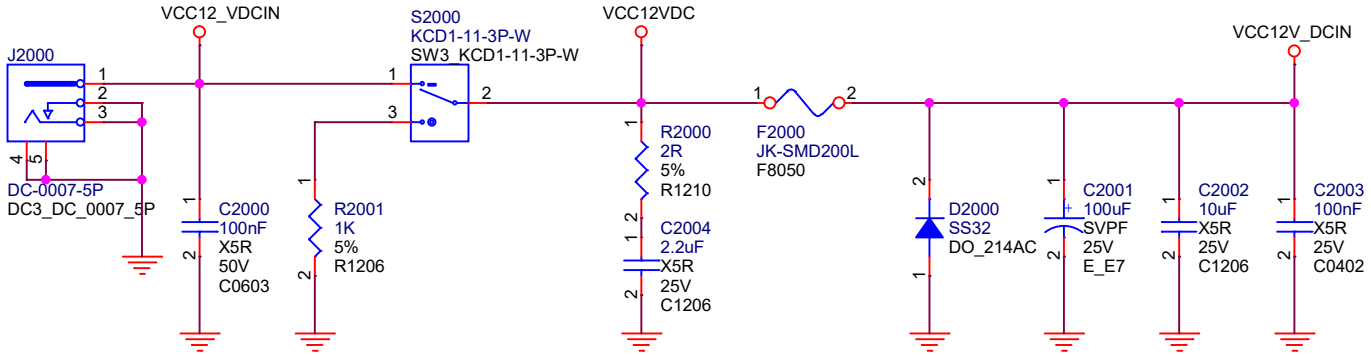
I2C2_SDA_M4_MIPI

I2C2_SCL_M4_MIPI

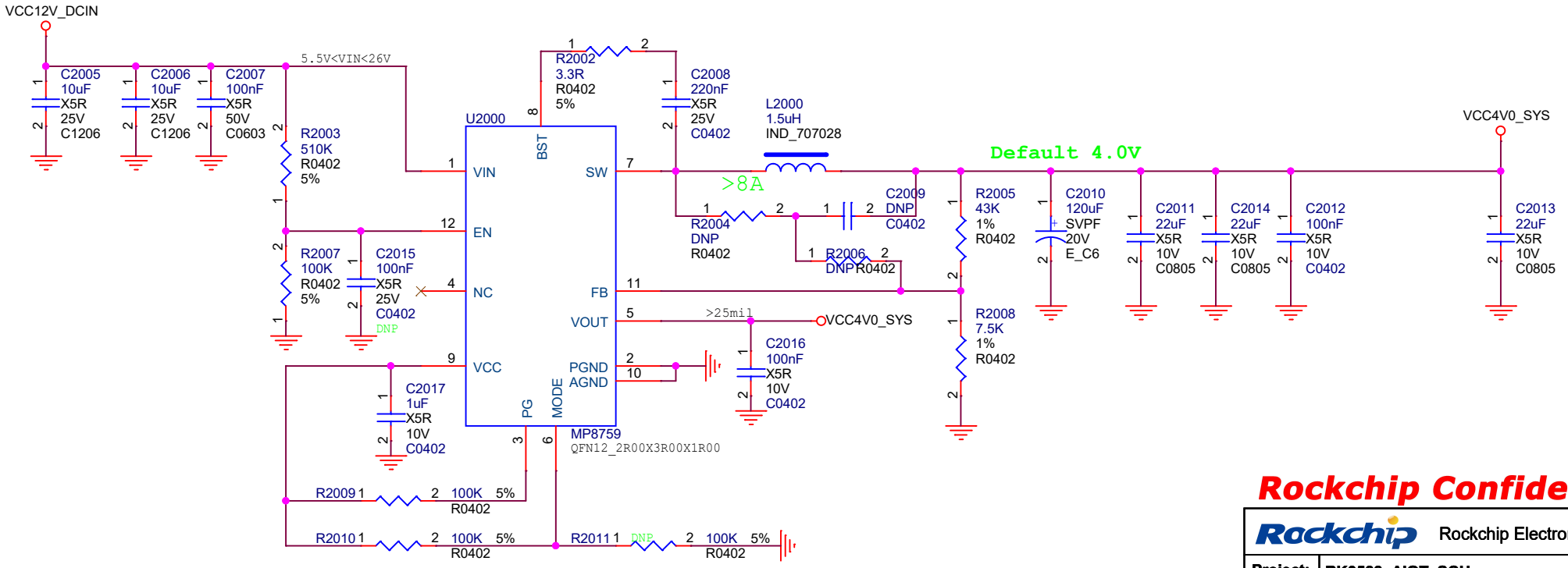
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	19.RK3588_1.8V/ 3.3V GPIO		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by:	Sheet: 19 of 99

12V DCIN



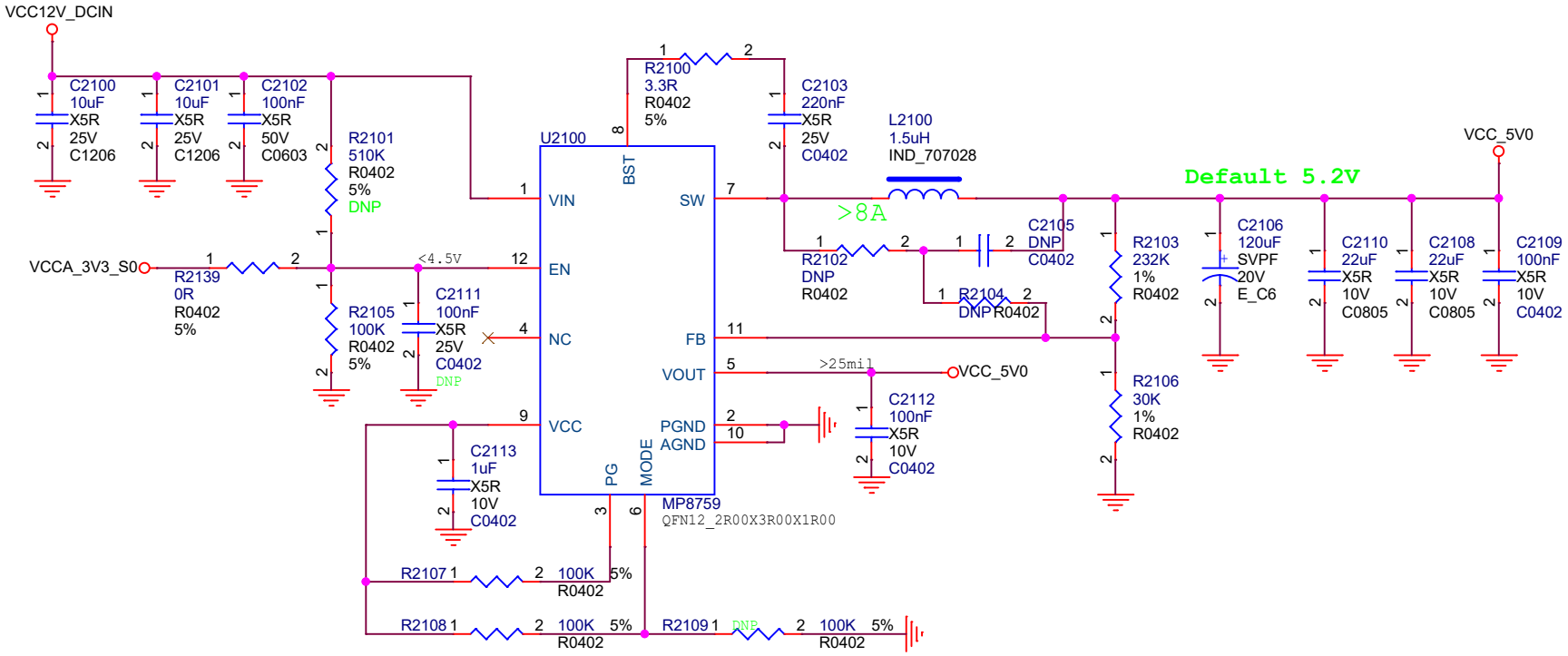
VCC4V0_SYS



Rockchip Confidential

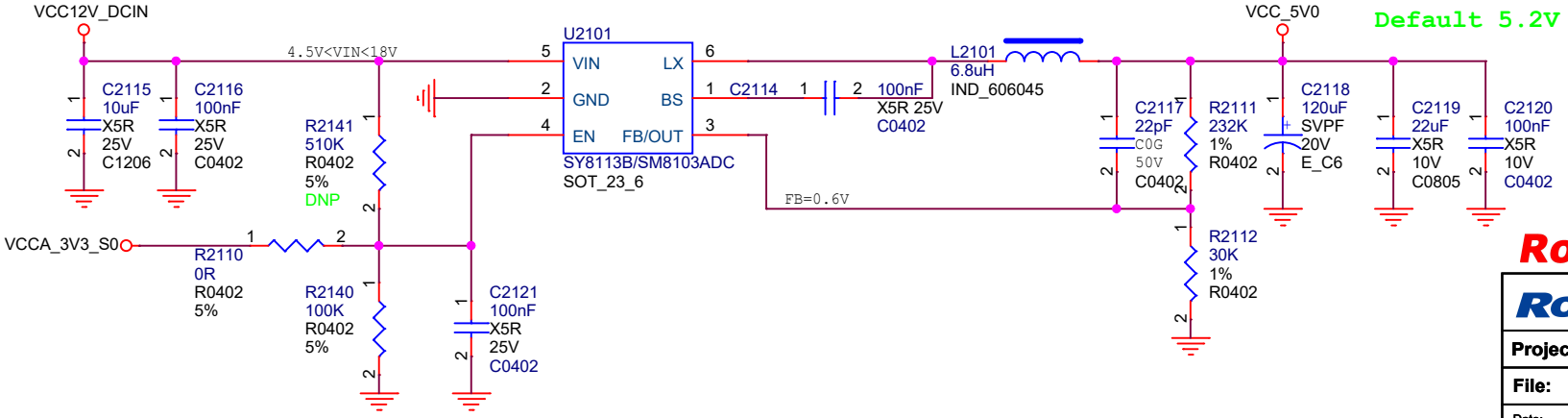
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	20.Power_DC IN/VCC4V0_SYS				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	Default	Sheet:	20 of 99

VCC5V0_SYS
OPTION1:Output Support 5V/8A



Note:
DCDC power supply is recommended if the current exceeds 3A

VCC5V0_SYS
OPTION2:Output Support 5V/3A

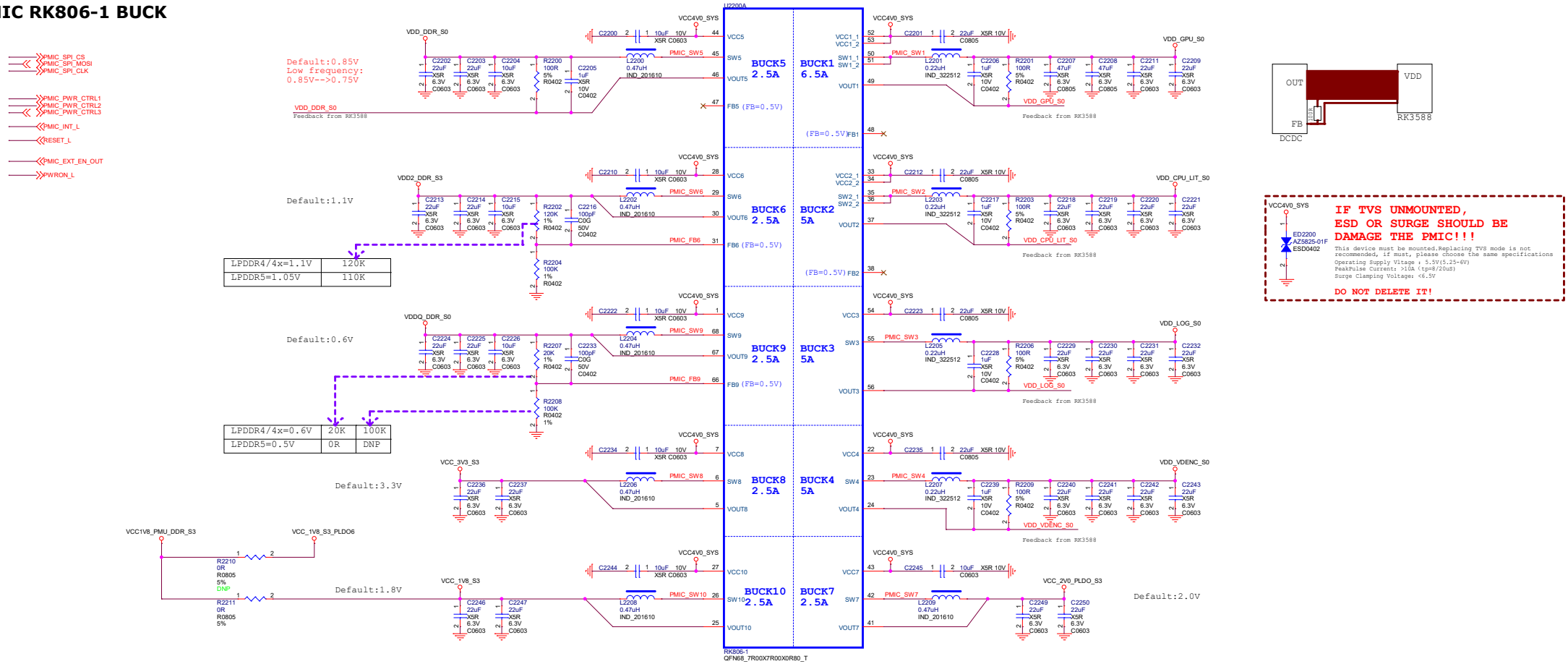


Note:
DCDC power supply is recommended if the current below 3A

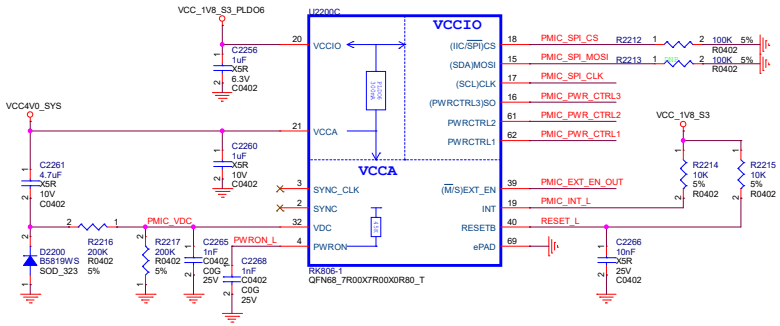
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	21.Power_Ext VCC_5V0				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	21 of 99

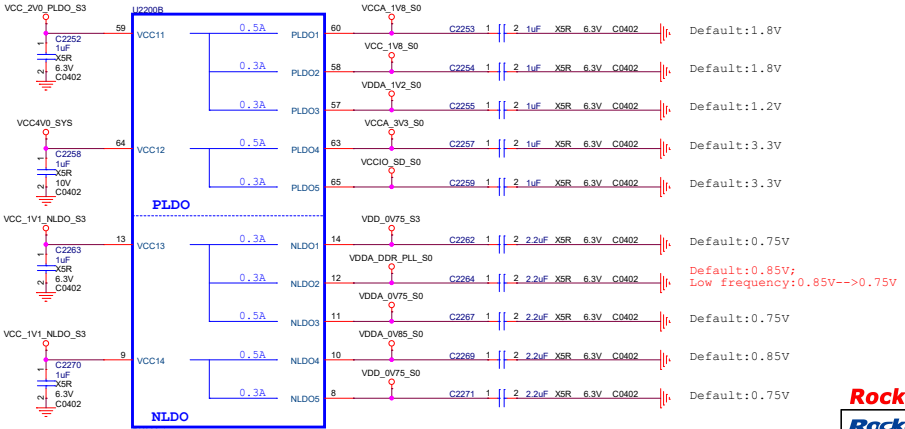
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



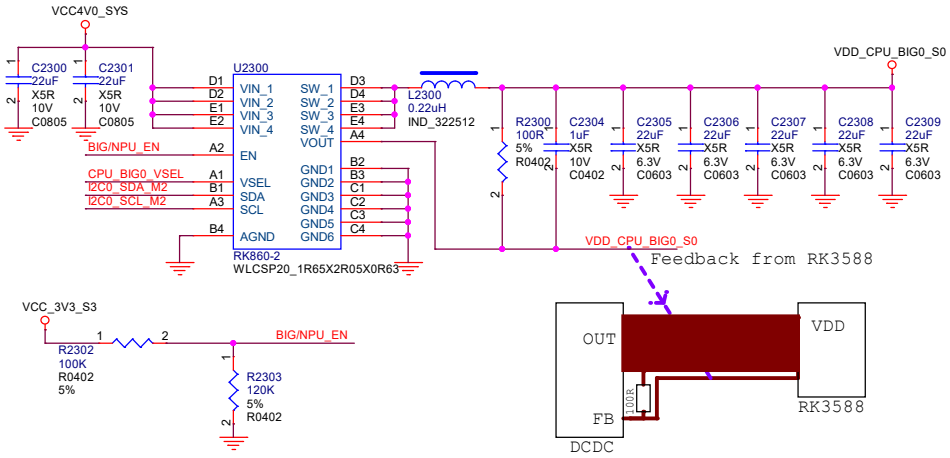
PMIC RK806-1 LDO



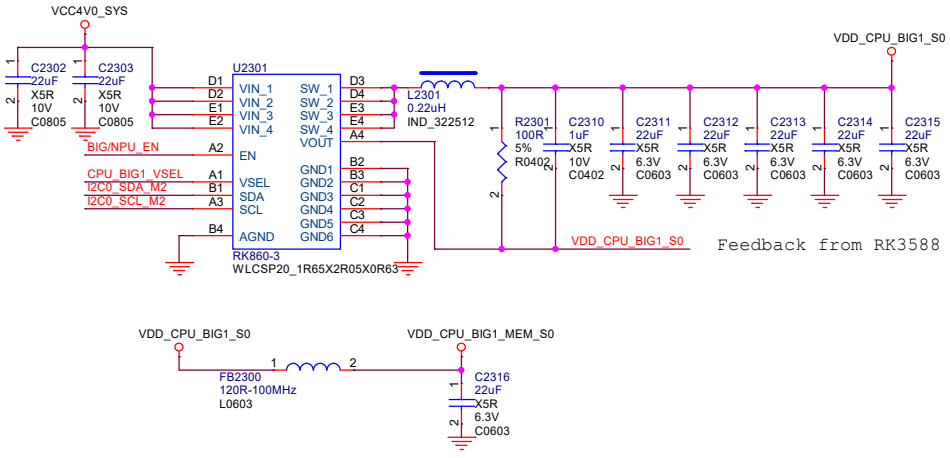
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	22.Power-PMIC_RK806-1		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by: Default	Sheet:	22 of 99

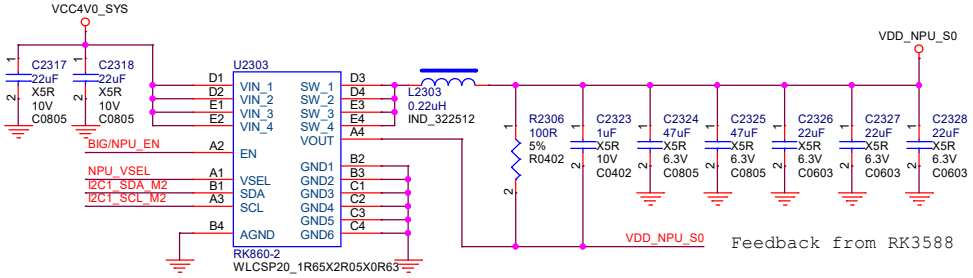
VDD_CPU_BIG0



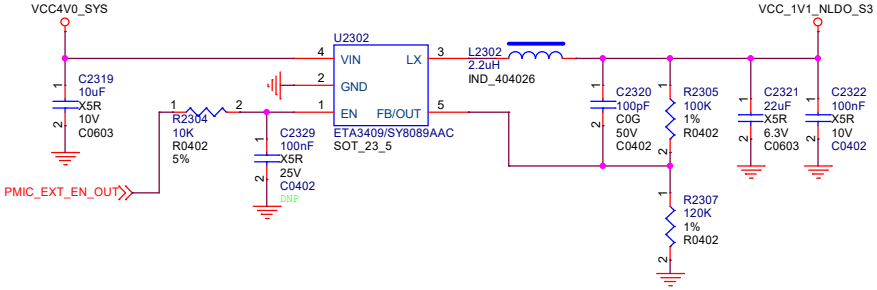
VDD_CPU_BIG1

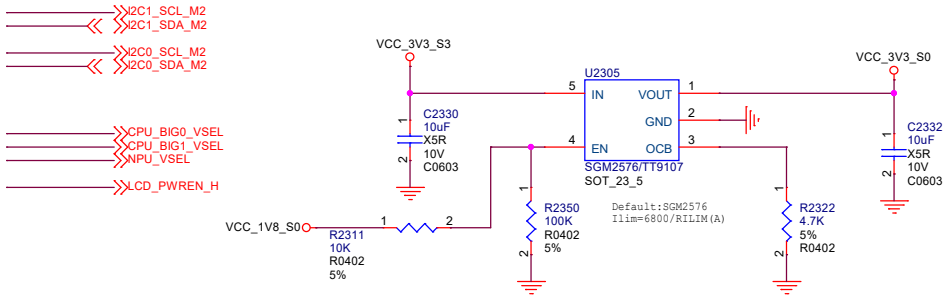


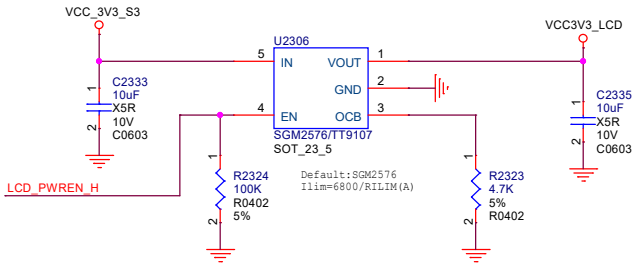
VDD_NPU



VCC_1V1_NLDO_S3



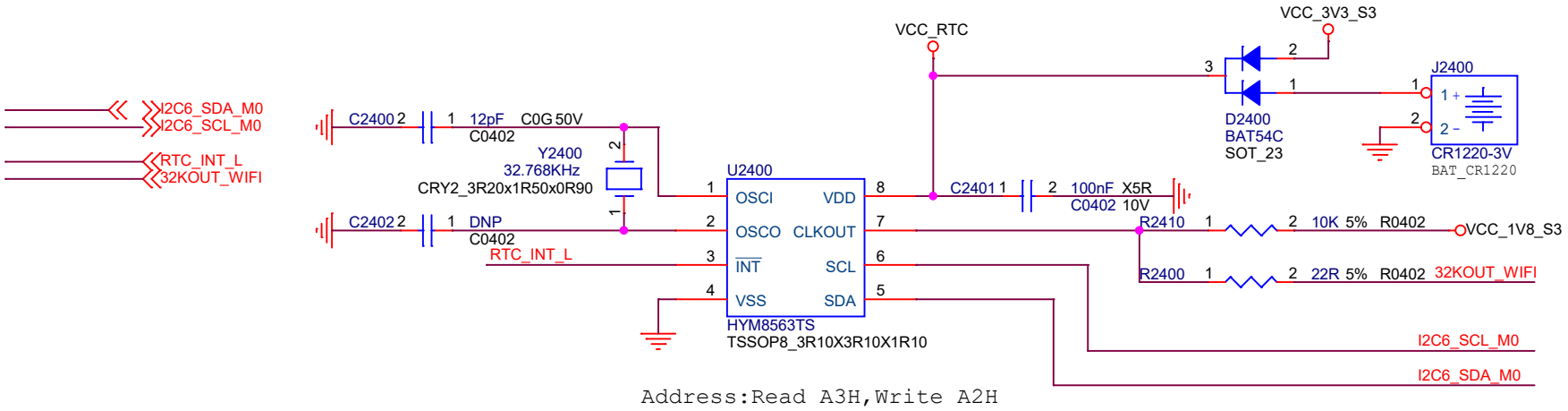




Rockchip Confidential

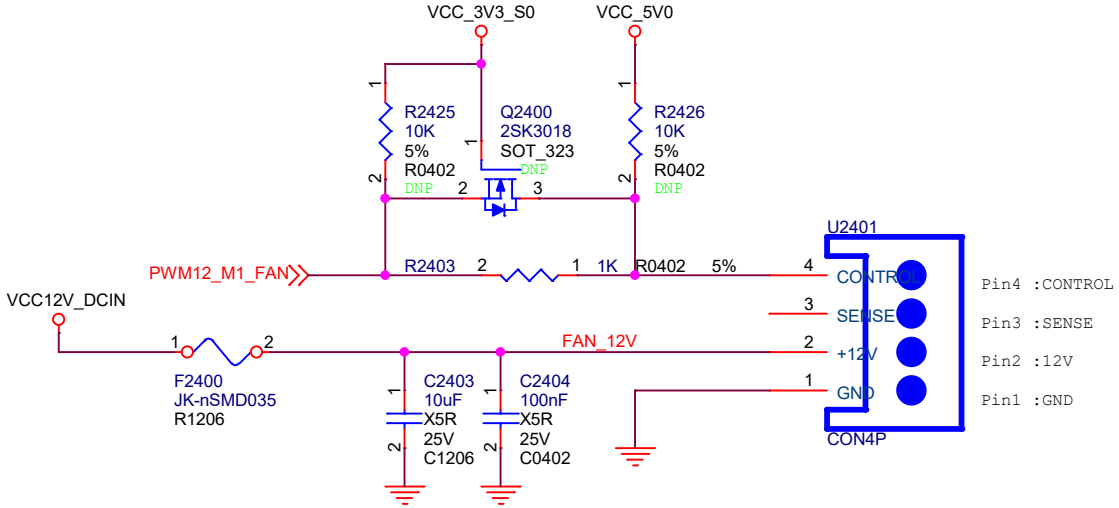
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	23.Power_Ext Discrete				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	Default	Sheet:	23 of 99

RTC IC

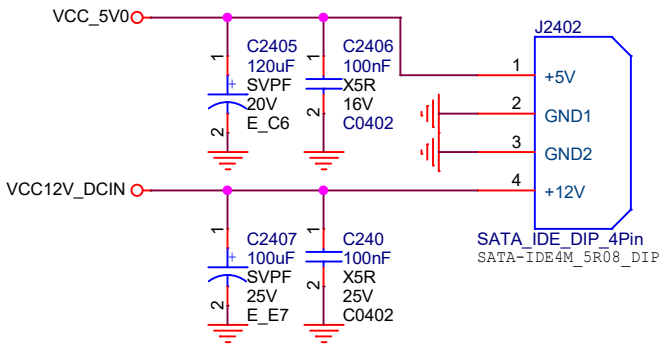


Address:Read A3H,Write A2H

FAN_POWER



SATA_POWER



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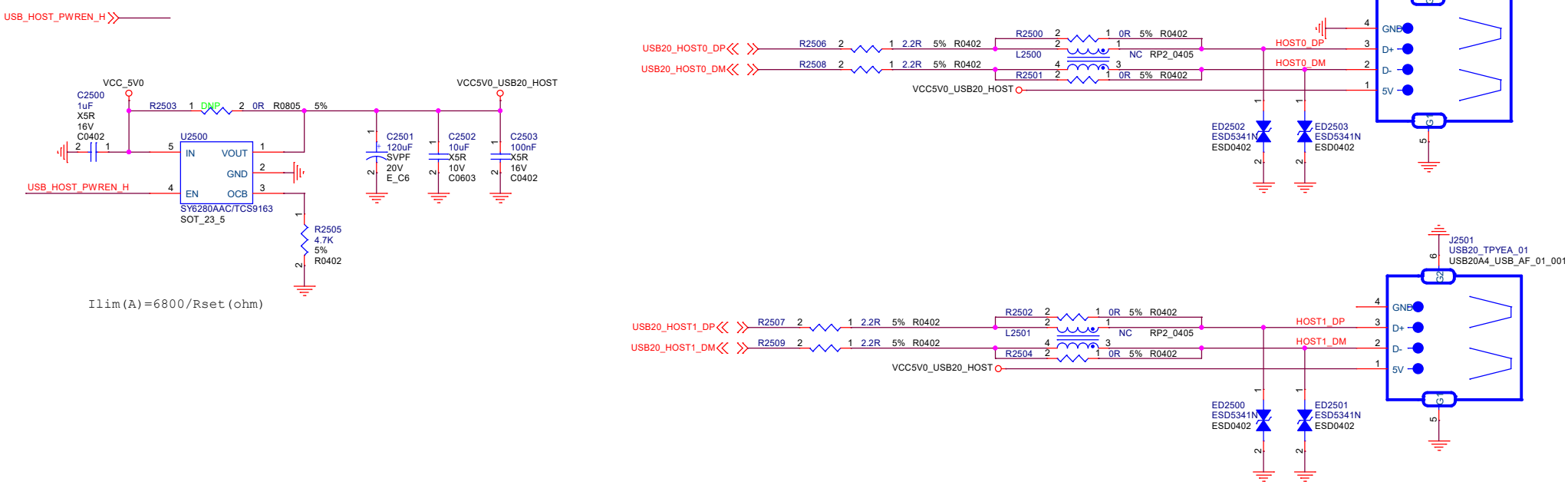
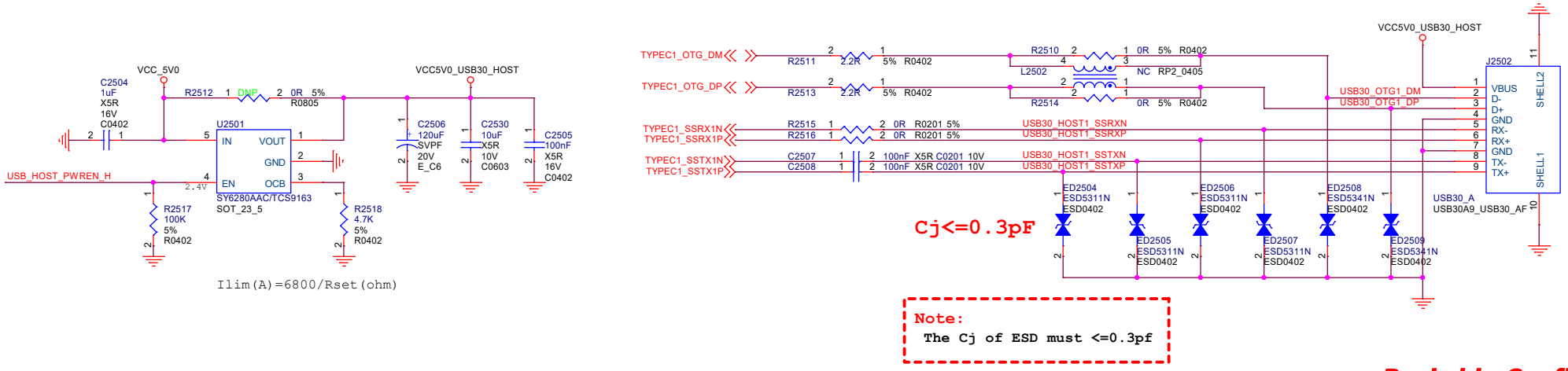
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	24.RTC/FAN/SATA POWER				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	24 of 99

USB2.0 HOST PORT



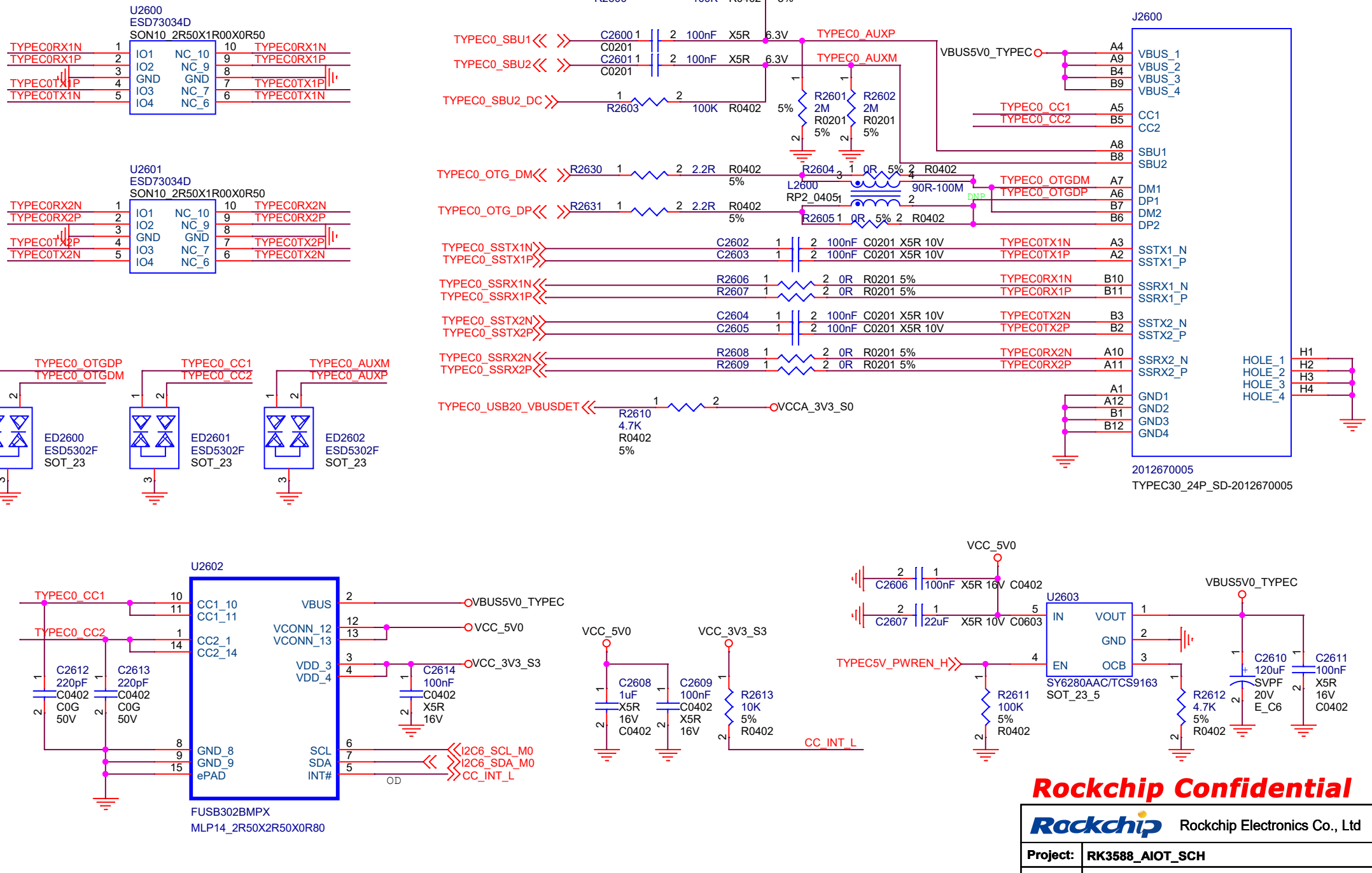
USB3.0 HOST PORT



Note:
The Cj of ESD must <=0.3pf

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	25.USB20/USB30 Port				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	25 of 99

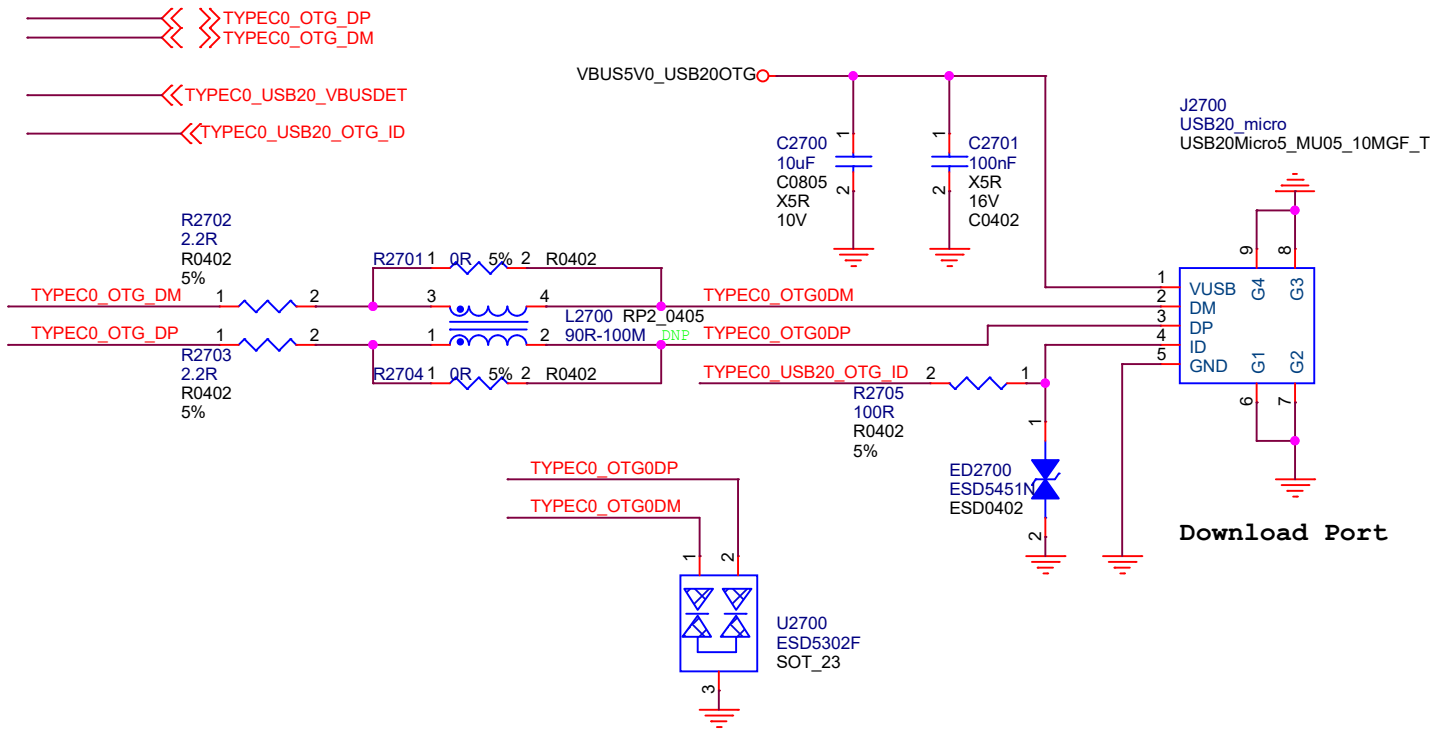
Type-C PORT



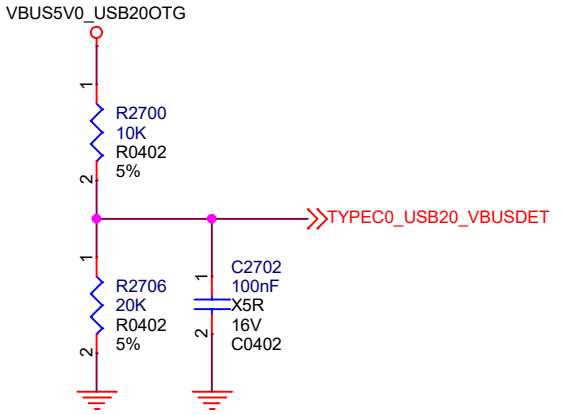
Rockchip Confidential

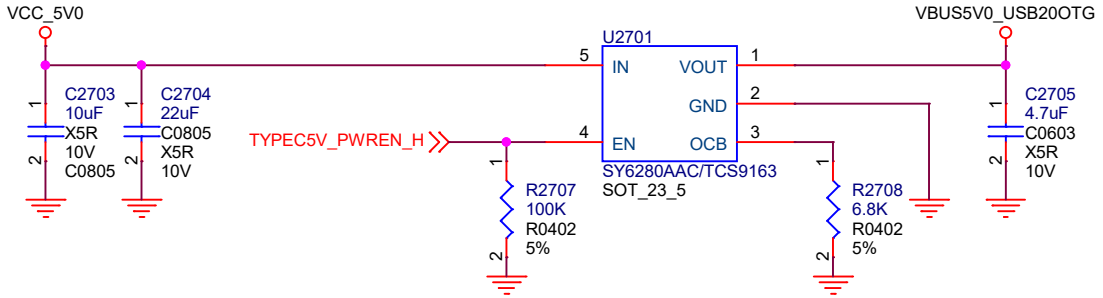
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	26.Type-C Port		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	26 of 99

USB2.0 Micro Port



USB Detection

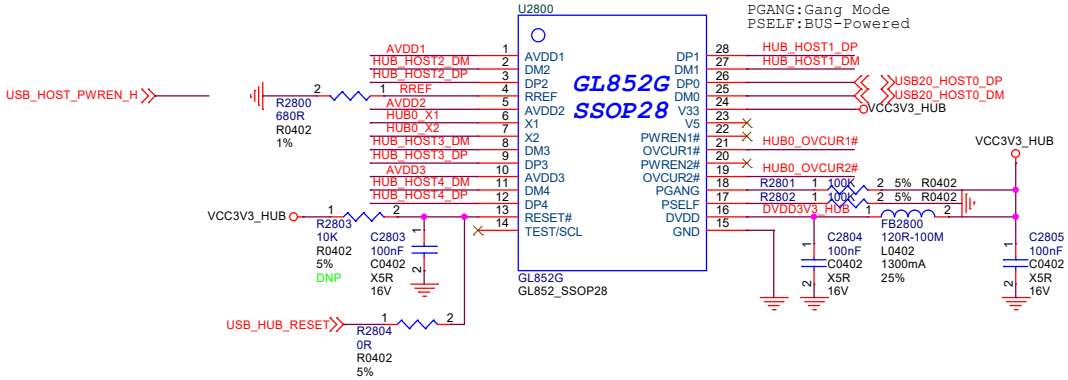




Rockchip Confidential

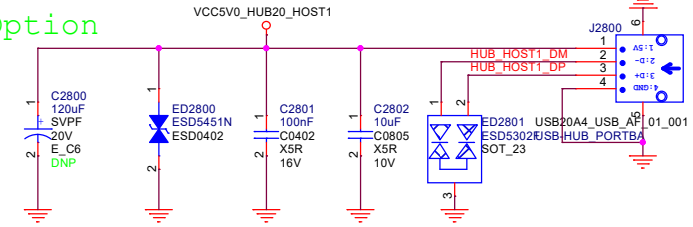
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	27.USB2.0 Micro Port(option)				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	27 of 99

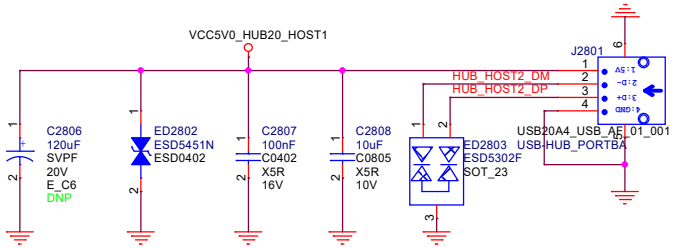
USB2.0 HUB

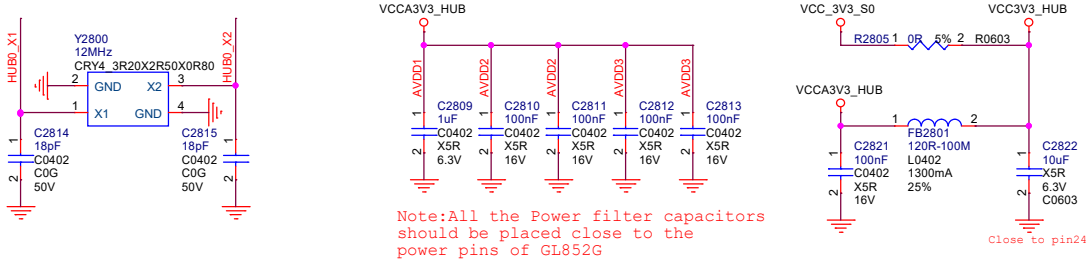


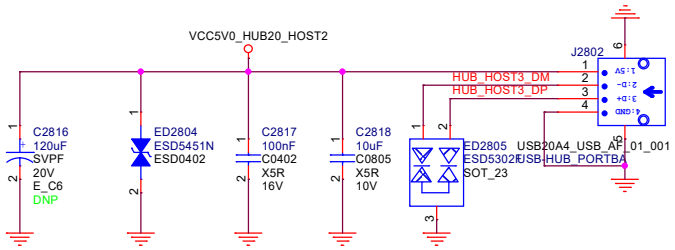
Note:
Used ECAP if want to drive mobile hard-disk and enough structure space for place.

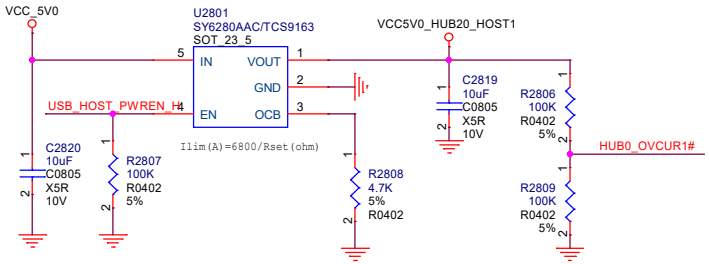
Option

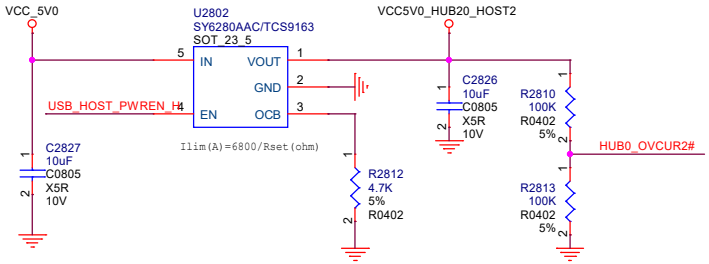


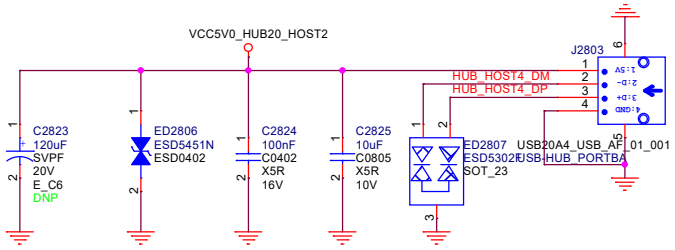






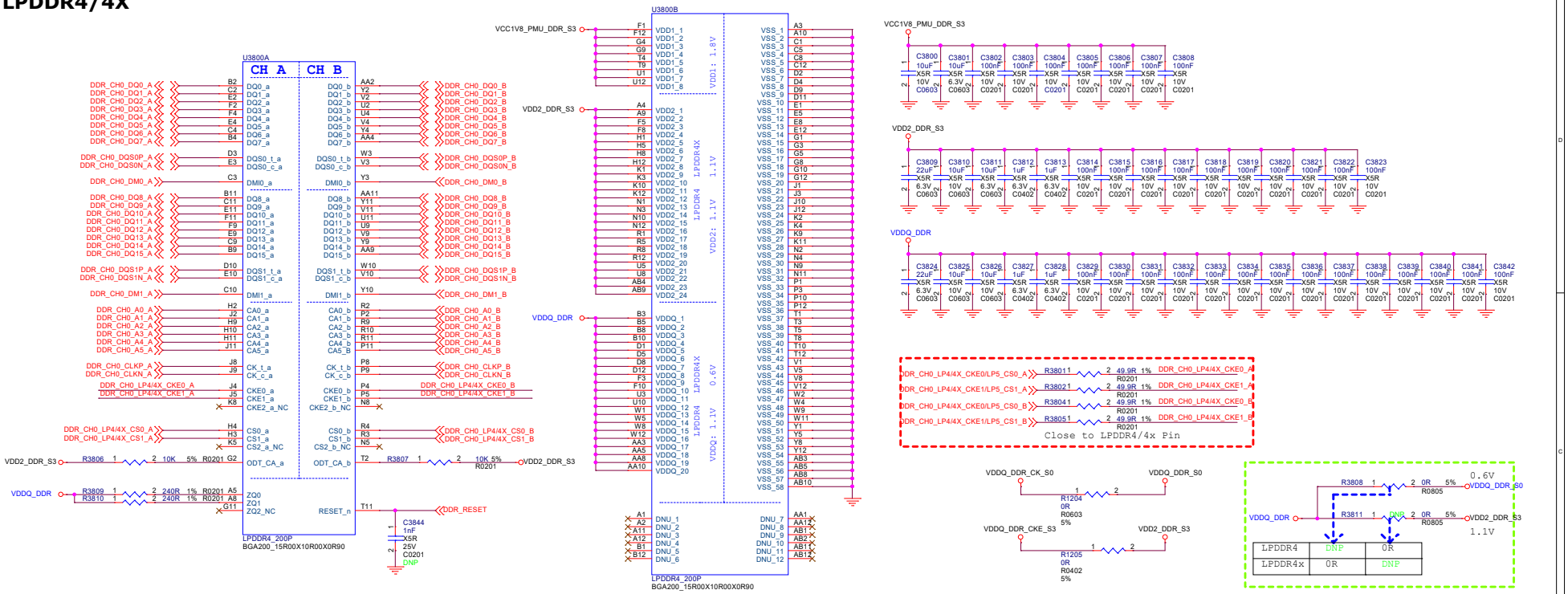


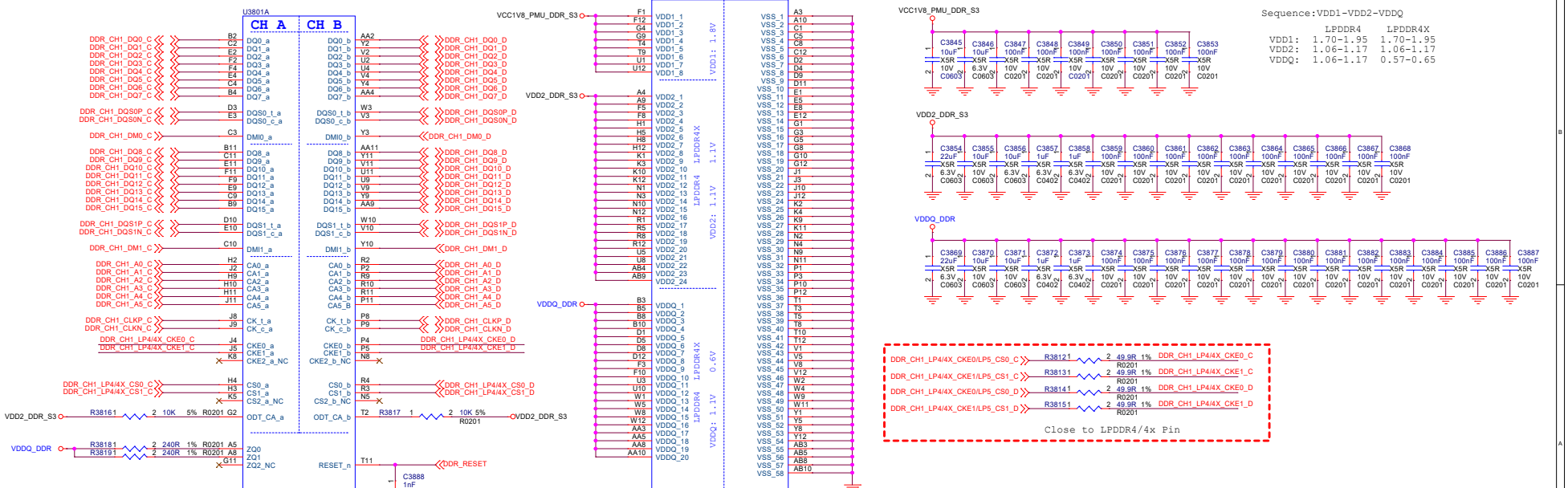




Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	28.USB HUB GL85x (option)				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	28 of 99

LPDDR4/4X





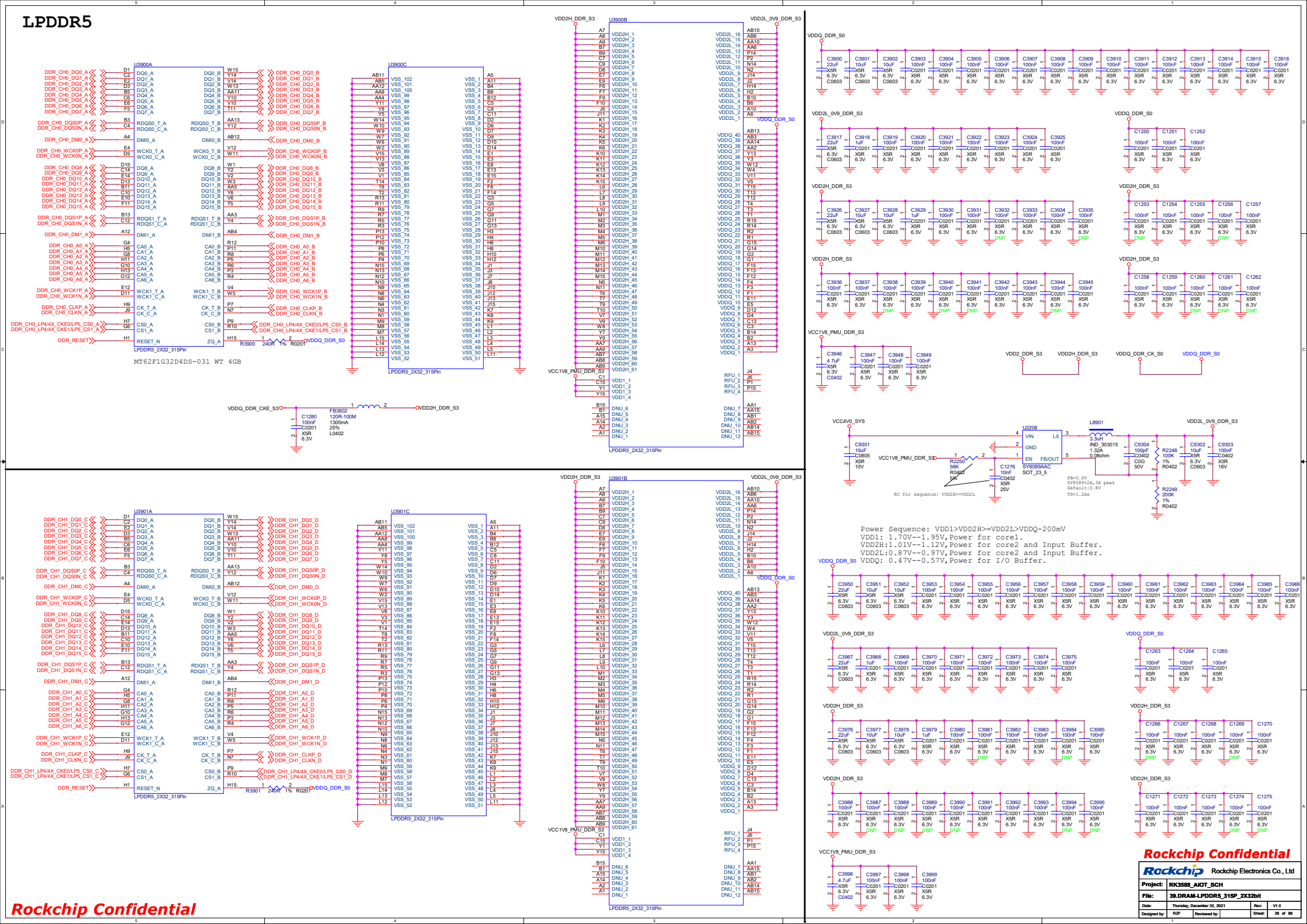
Sequence:VDD1-VDD2-VDDQ

	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	38.DRAM-LPDDR4X_200P_2X32bit		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by:	Sheet: 38 of 99

LPDDR5



Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.

Rockchip	Rockchip Electronics Co., Ltd
Project:	RK3588_AIOT_SCH
File:	39.DRAM-LPDDR5_315P_2X32bit
Date:	Thursday, December 30, 2021
Rev:	V1.0
Designed by:	RZF
Reviewed by:	
Sheet:	39 of 99

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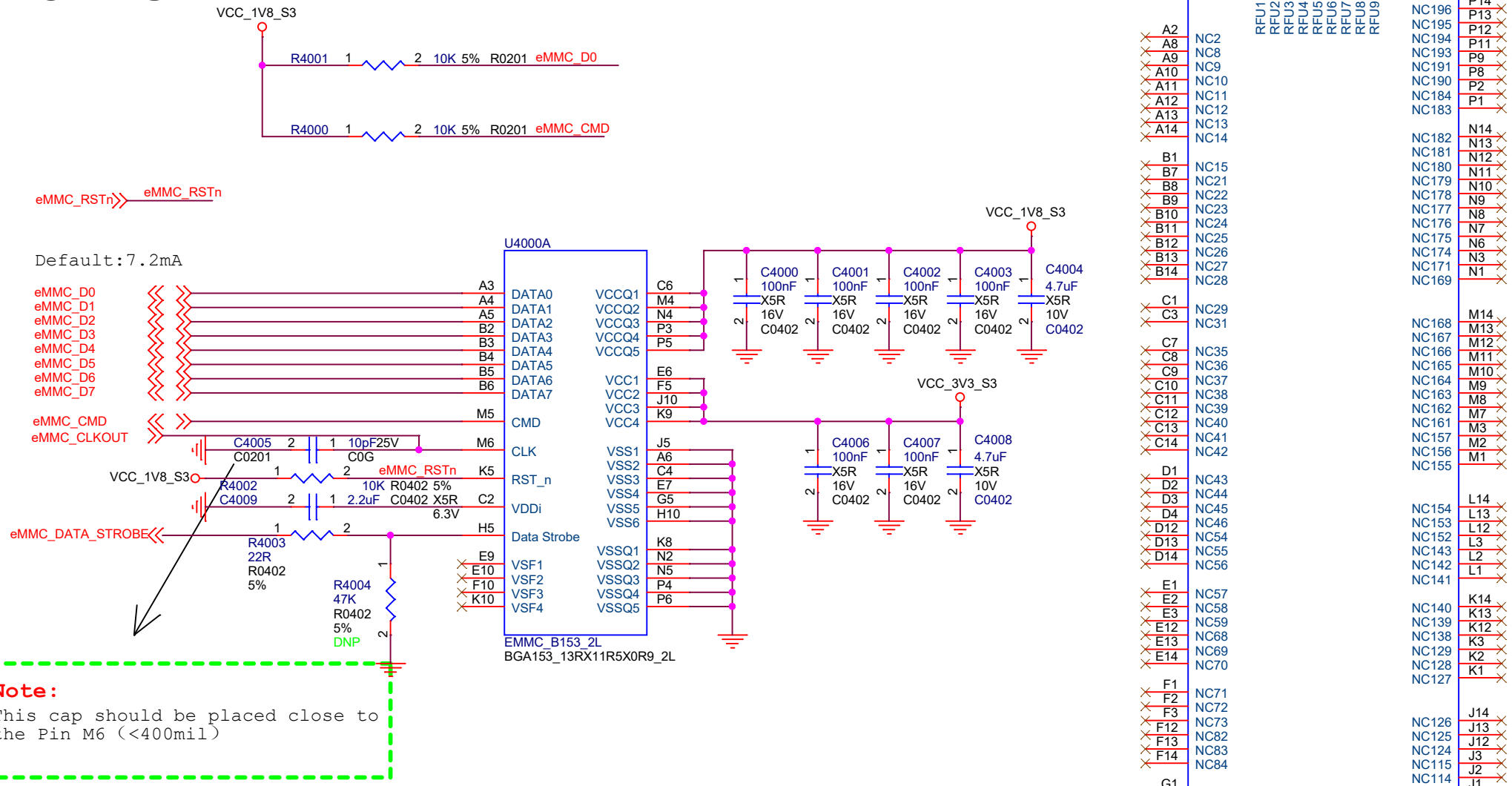
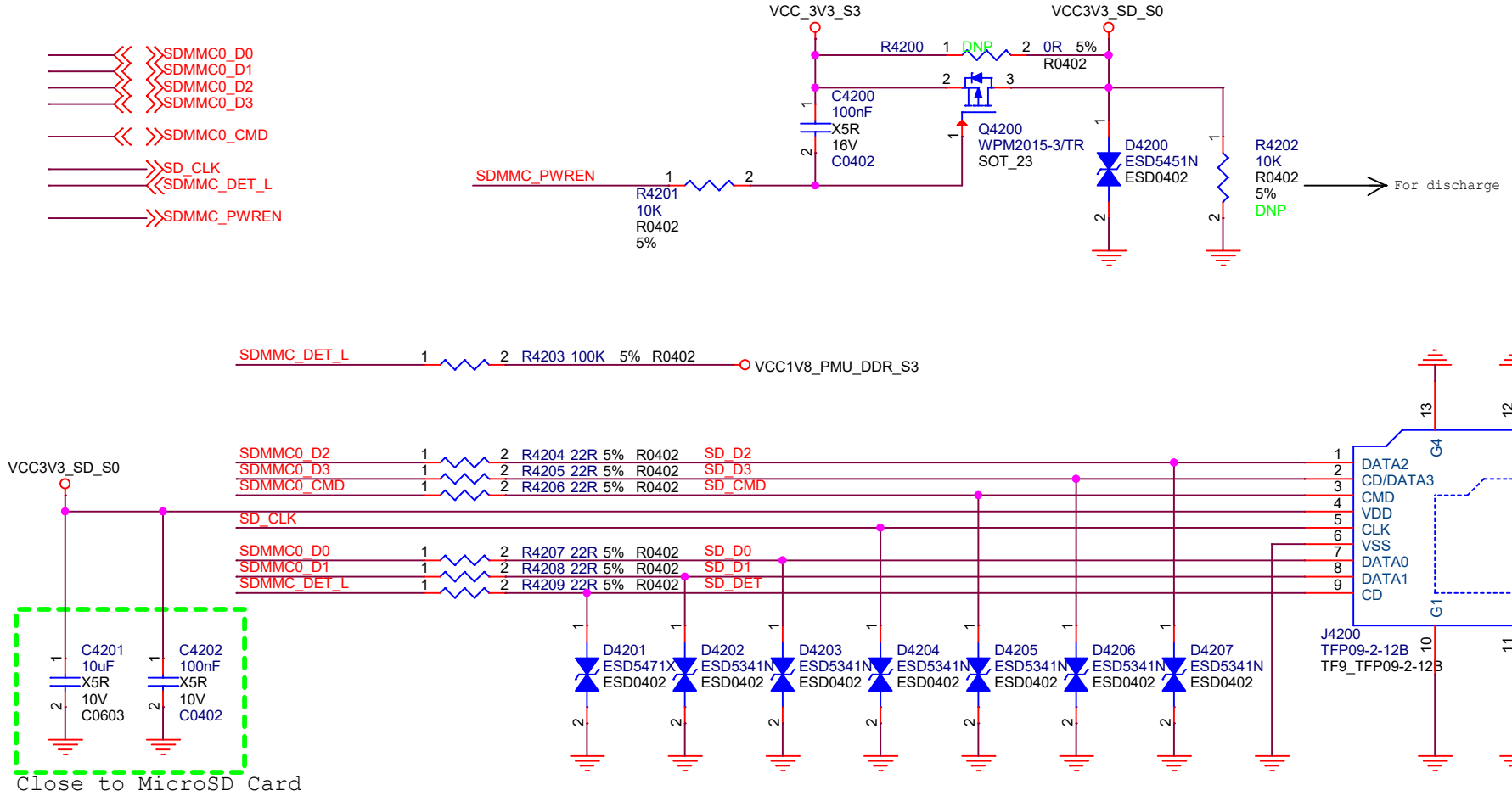
eMMC FLASH



Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	40.Flash-eMMC Flash		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	40 of 99

TF CARD



MicroSD Card

Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	42.Flash-TF Card		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	42 of 99

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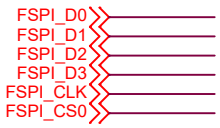
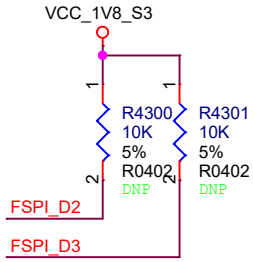
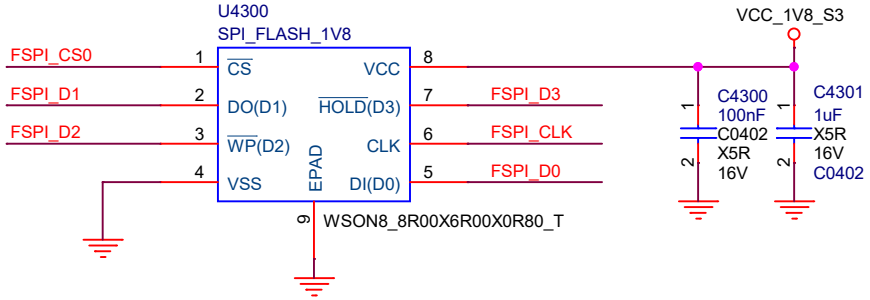
SPI NOR OR NAND Flash







SPI FLASH:1.8V

Note:
When using SPI FLASH with only 1 bit, it needs to be stuffed.

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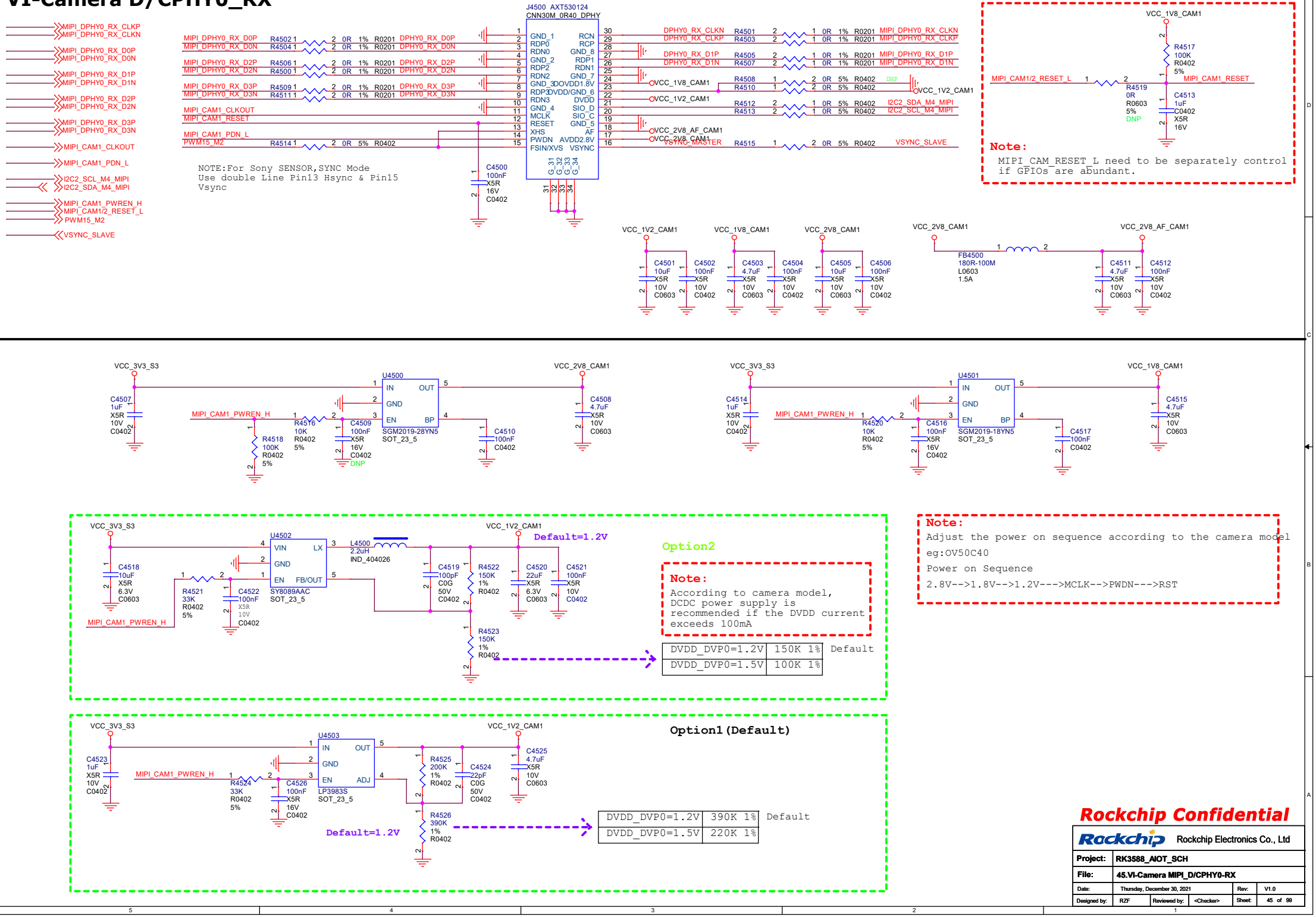
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	43.Flash-SPI FLASH(option)				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	43 of 99

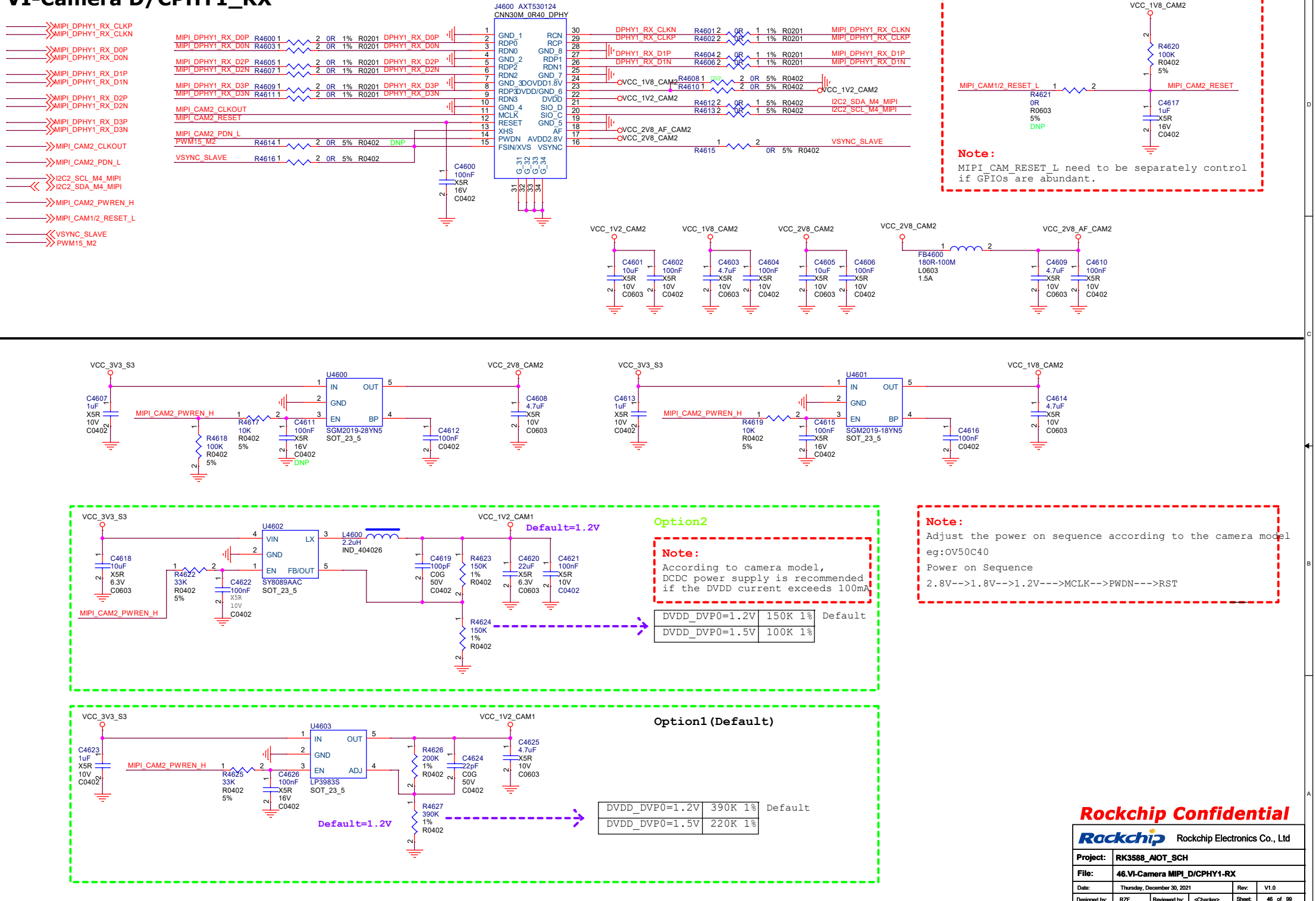
VI-Camera D/CPHY0_RX



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	45.VI-Camera MIPI_D/CPHY0-RX				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	45 of 99

VI-Camera D/CPHY1_RX



Note:

Adjust the power on sequence according to the camera model

eg:OV50C40

Power on Sequence

2.8V-->1.8V-->1.2V--->MCLK-->PWDN--->RST

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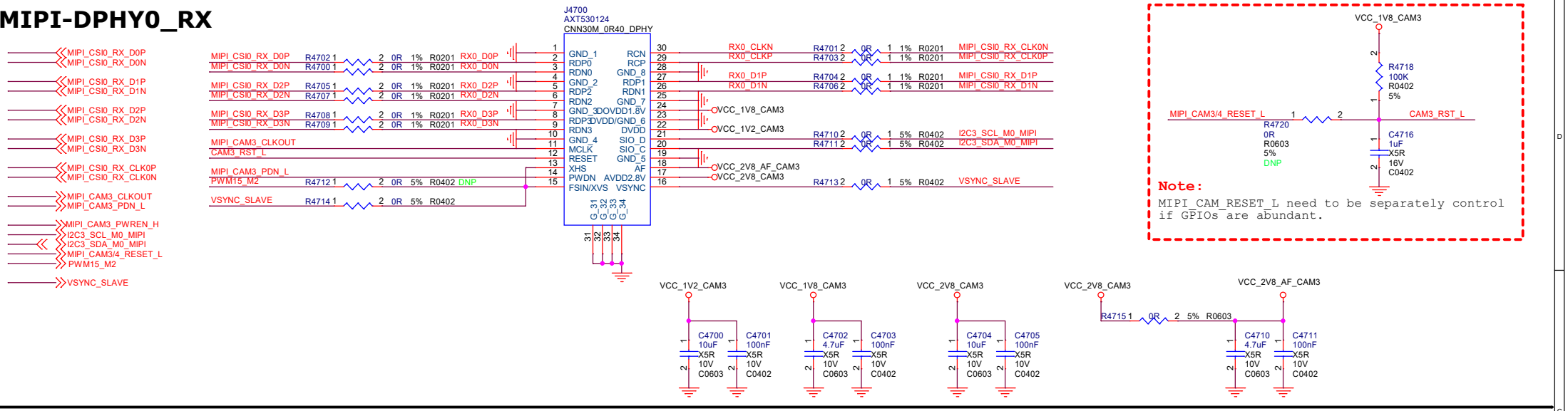
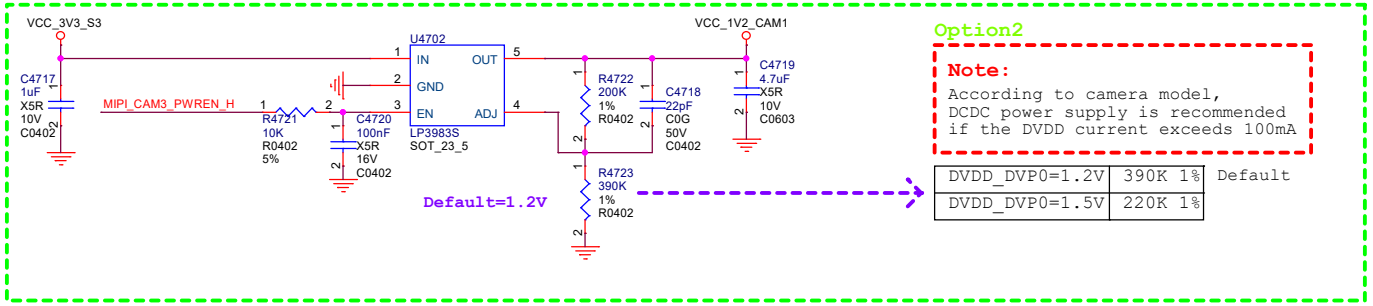
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	46.VI-Camera MIPI_D/CPHY1-RX				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	46 of 99

MIPI-DPHY0_RX





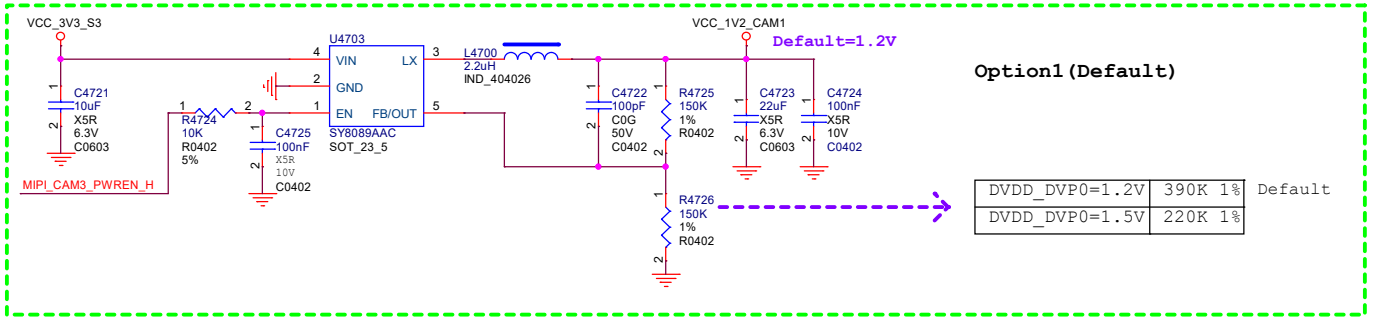
Note:

Adjust the power on sequence according to the camera model

eg:GC8034

Power on Sequence

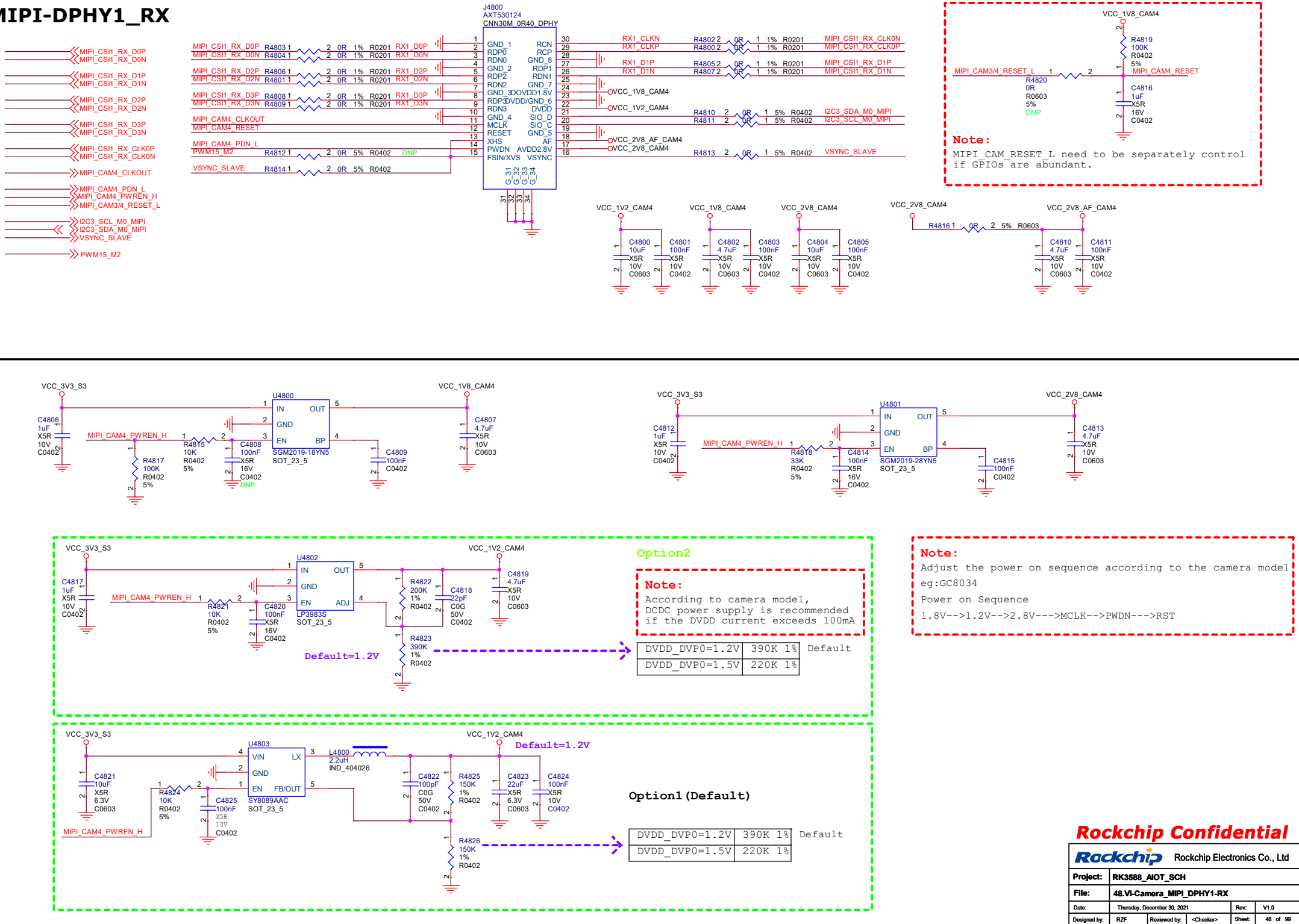
1.8V-->1.2V-->2.8V--->MCLK-->PWDN--->RST



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	47.VI-Camera_MIPI_DPHY0-RX				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	47 of 99

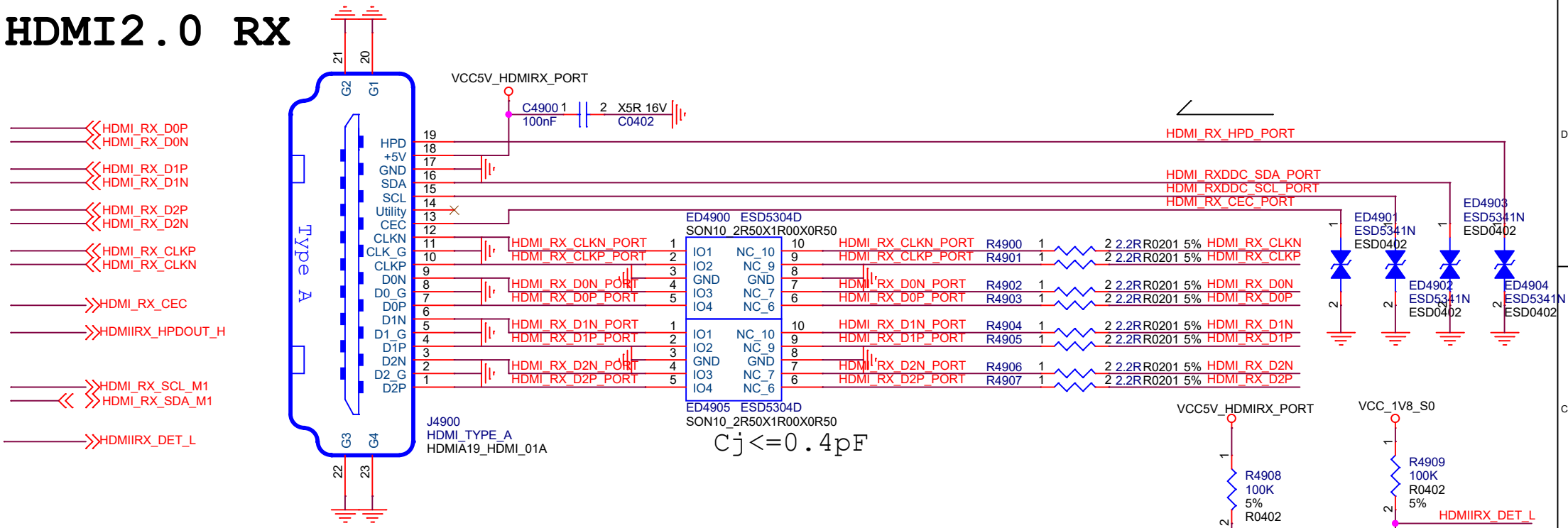
MIPI-DPHY1_RX



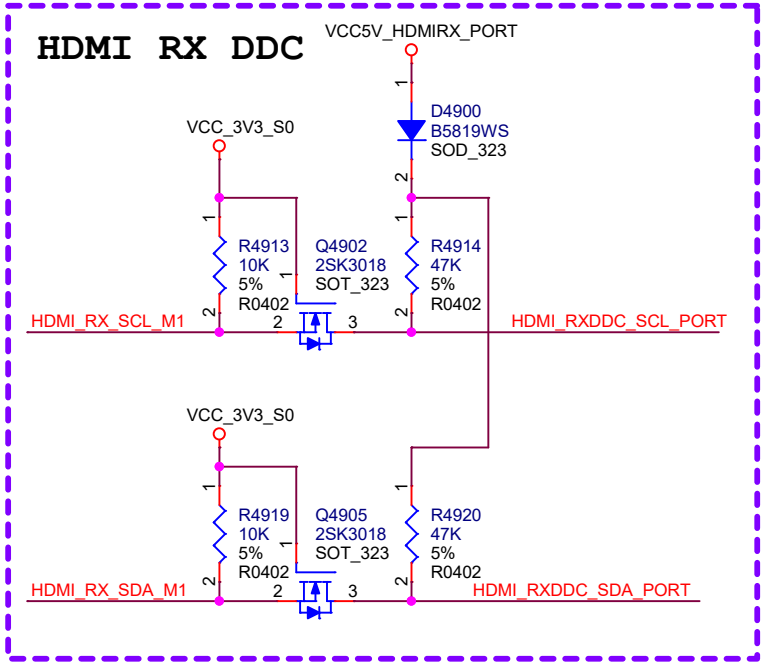
Rockchip Confidential

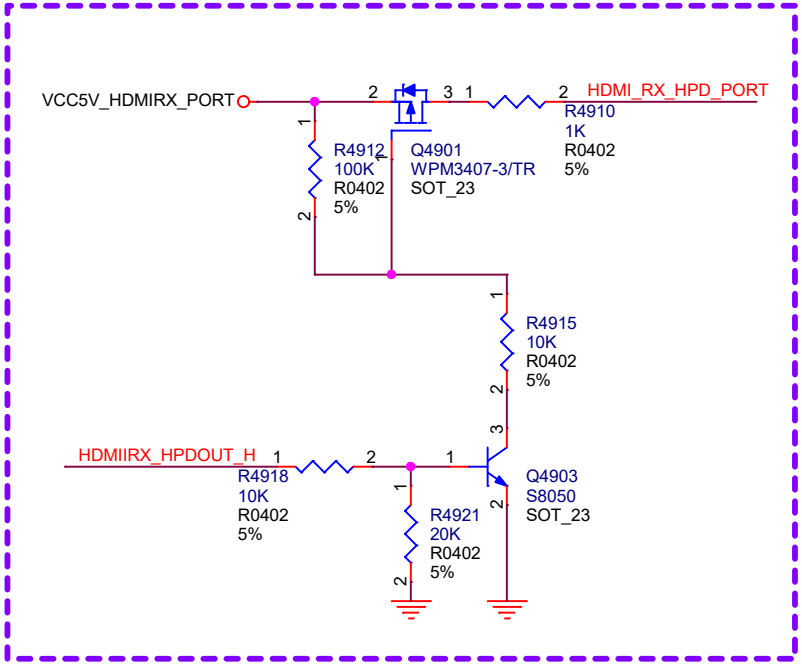
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	48.VI-Camera_MIPI_DPHY1-RX				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	<Checker>	Sheet:	48 of 99

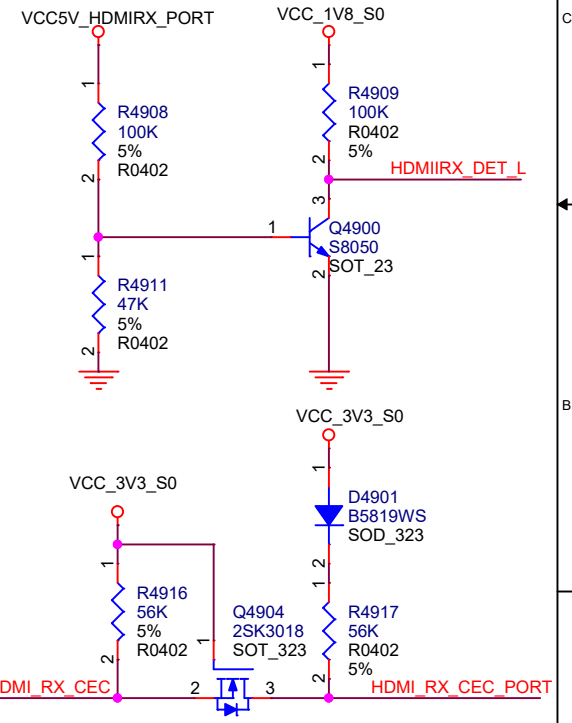
HDMI2.0 RX



HDMI RX DDC







HPD:
Sink Side: Require output, Min 2.4V; Max 5.3V
Source Side:Require input and Detection.
Min 2.0V,Max:5.3V

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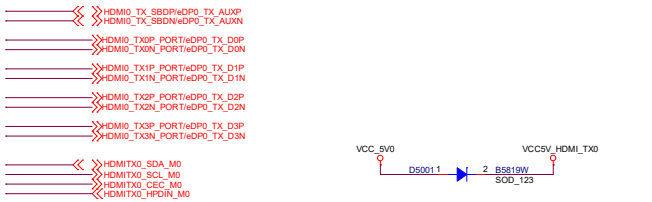
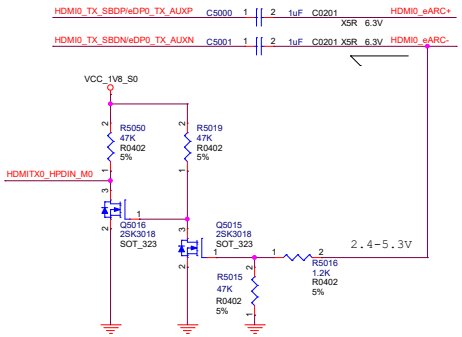
Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	49.VI-HDMI2.0 RX				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	49 of 99

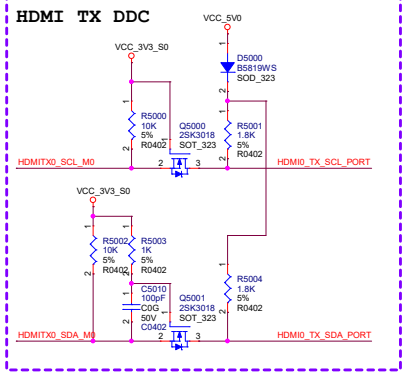
HDMI TX0



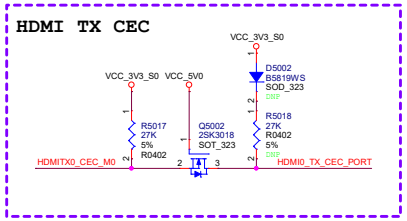
HDMI TX eARC

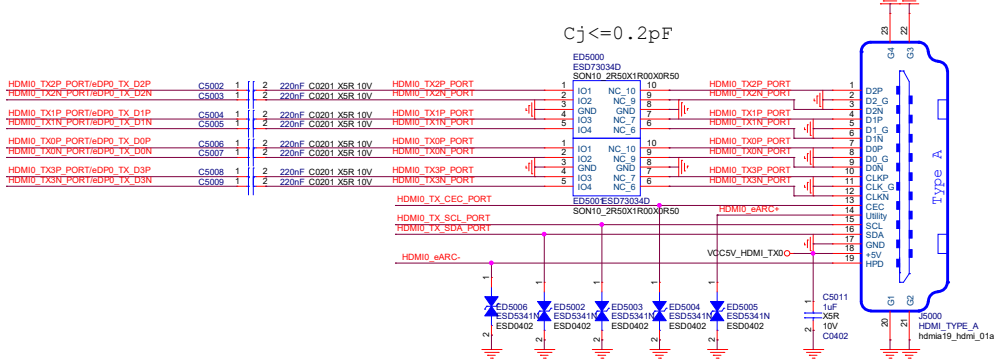


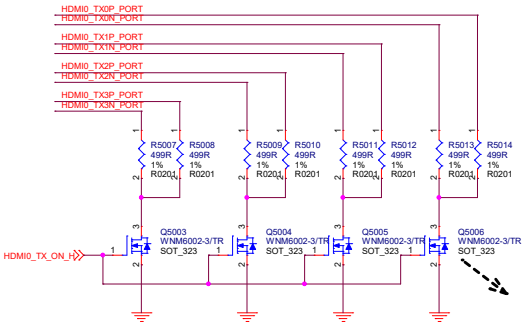
HDMI TX DDC



HDMI TX CEC





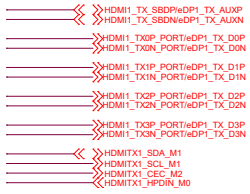


Note:

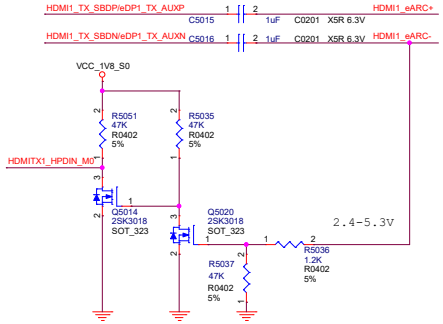
The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

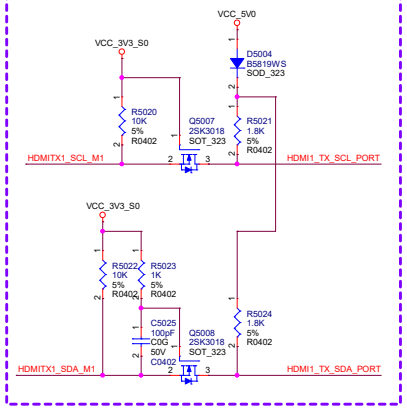
HDMI TX1



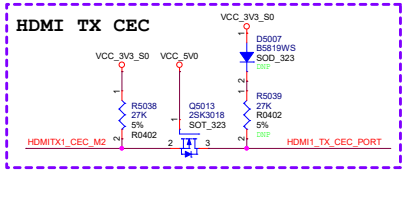
HDMI TX eARC

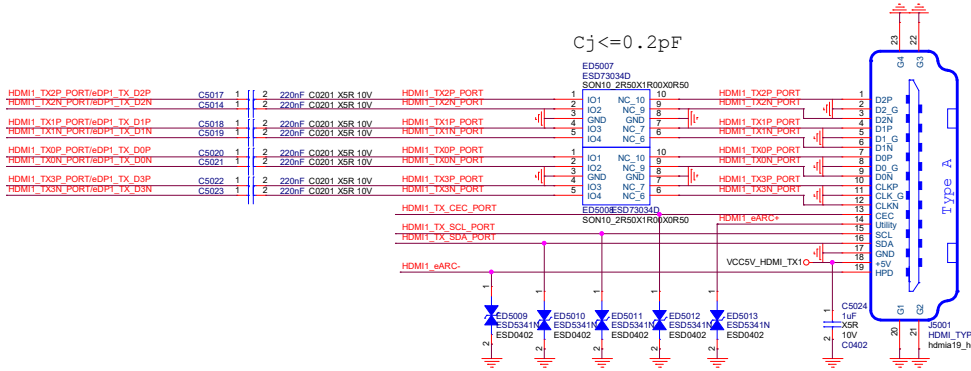


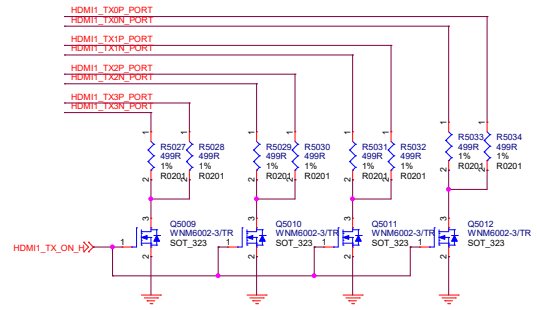
HDMI TX DDC



HDMI TX CEC







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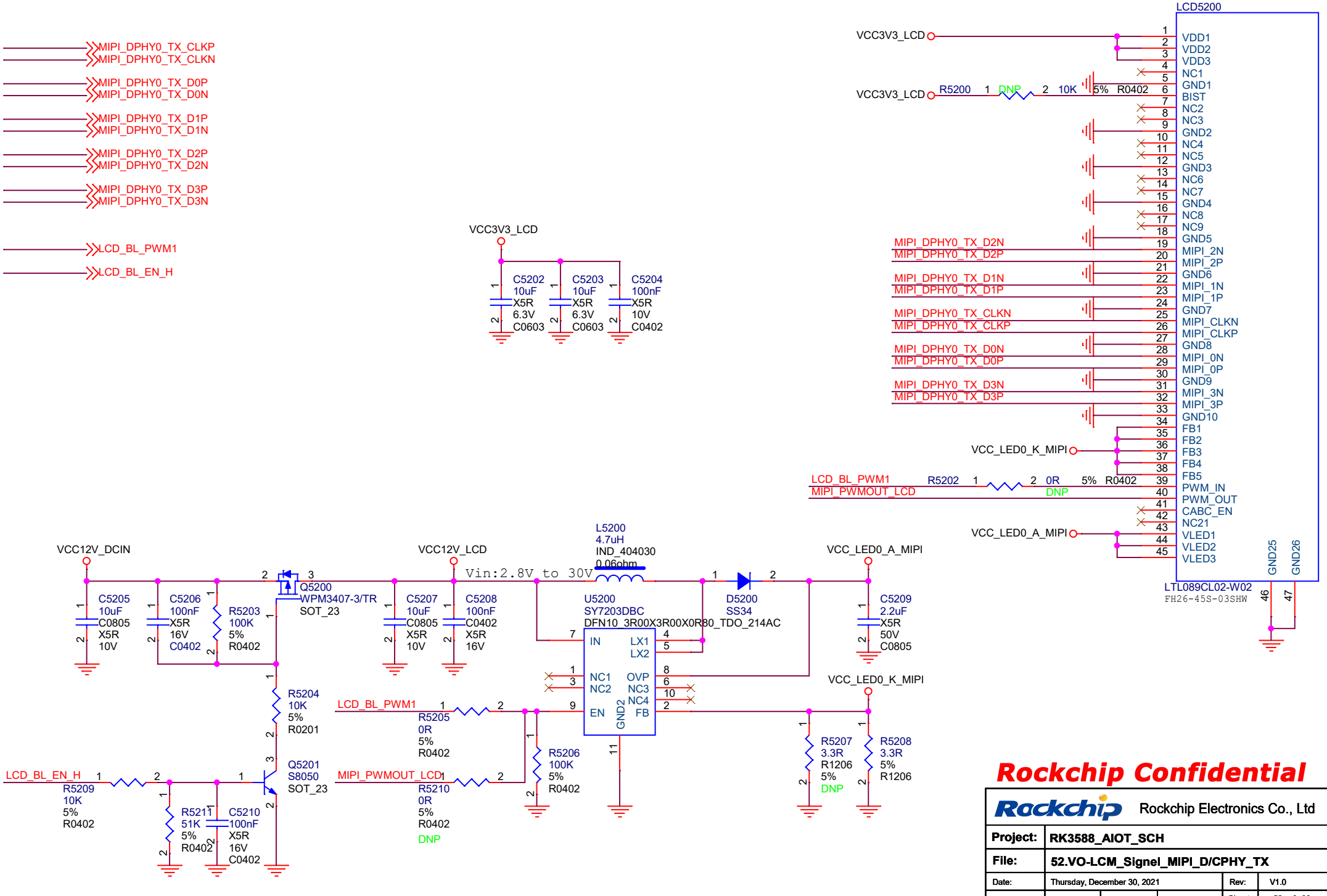
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	50.VO-HDMI2.1 TX		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by:	
		Sheet:	50 of 99

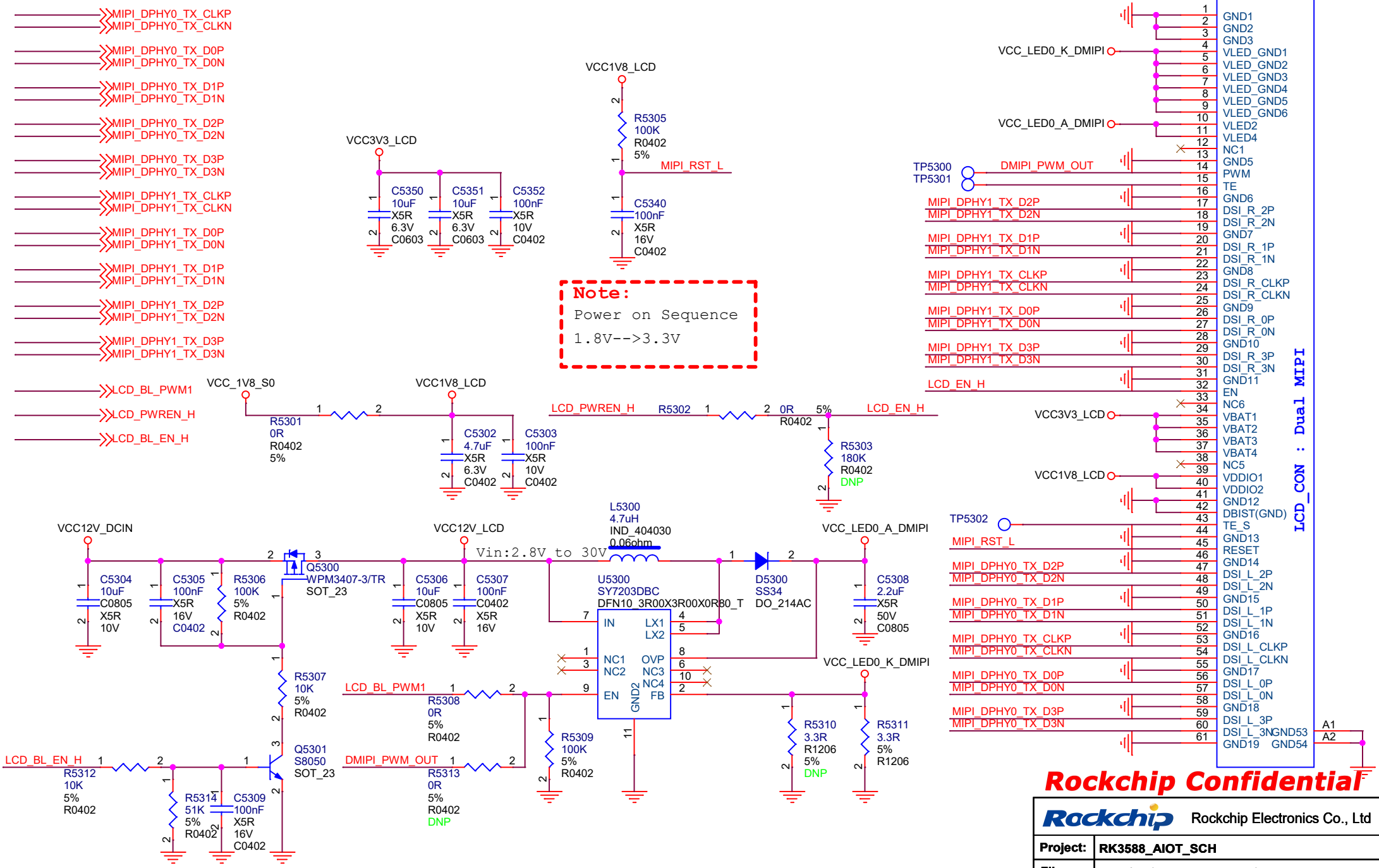
Single-MIPI0 LCM



Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	52.VO-LCM_Signel_MIPI_D/CPHY_TX				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	Default	Sheet:	52 of 99

Dual-MIPI LCM



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	53.VO-LCM_Dual MIPI_D/CPHY TX				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	Default	Sheet:	53 of 99

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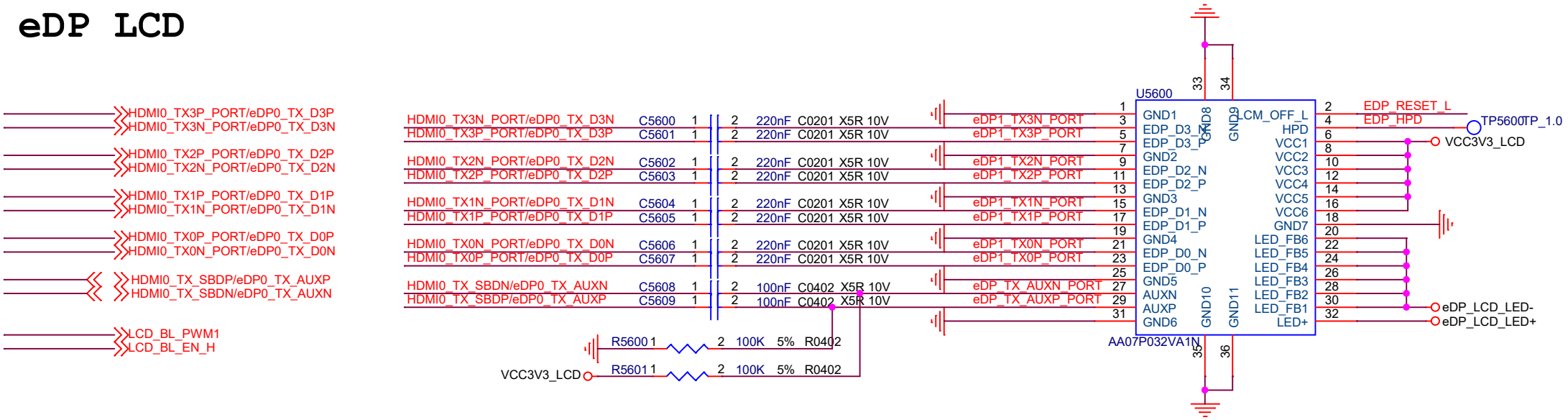
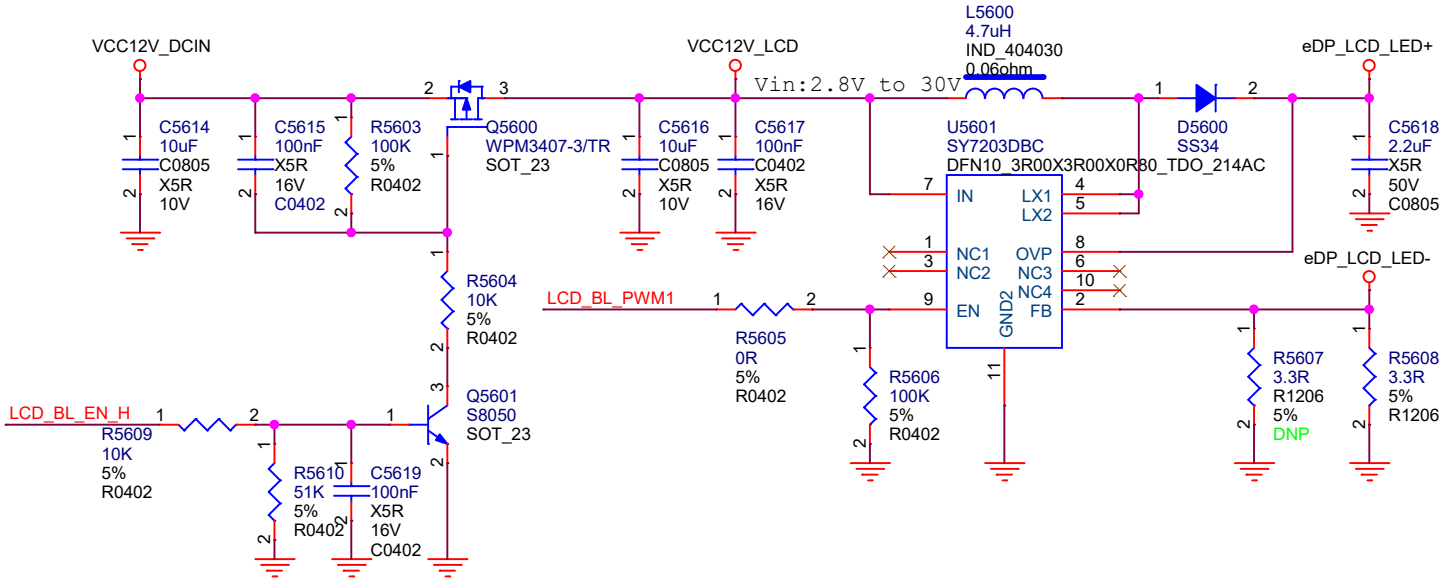
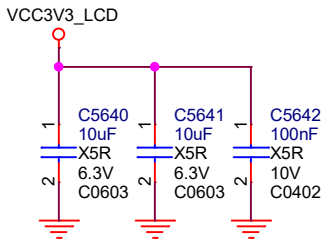
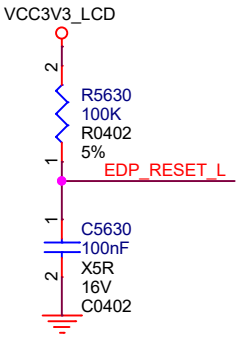
eDP LCD





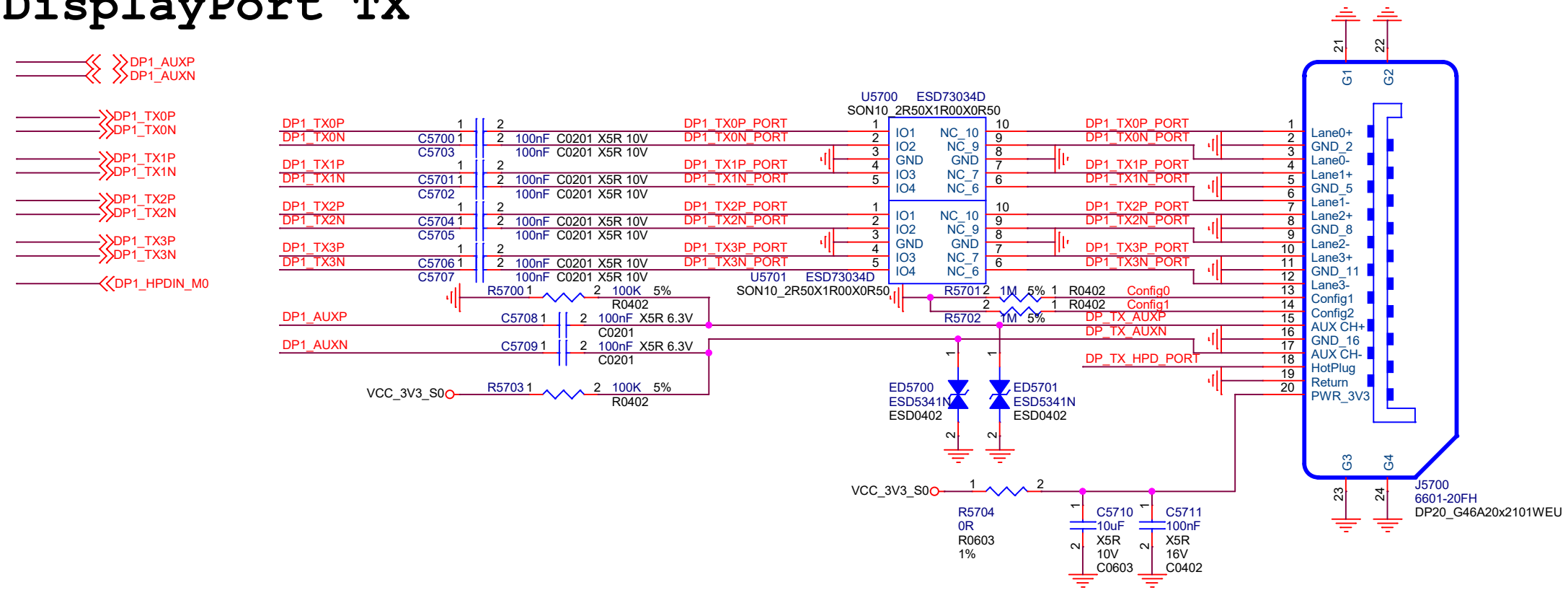




Rockchip Confidential

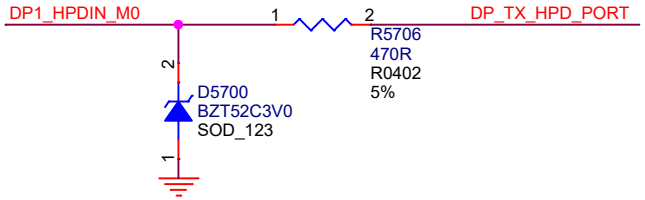
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	56.VO-LCM_eDP		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	56 of 99

DisplayPort TX



DP_TX_HPD

HPD Voltage:2.25-3.6V



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Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	57.VO-DP		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by:	Sheet: 57 of 99

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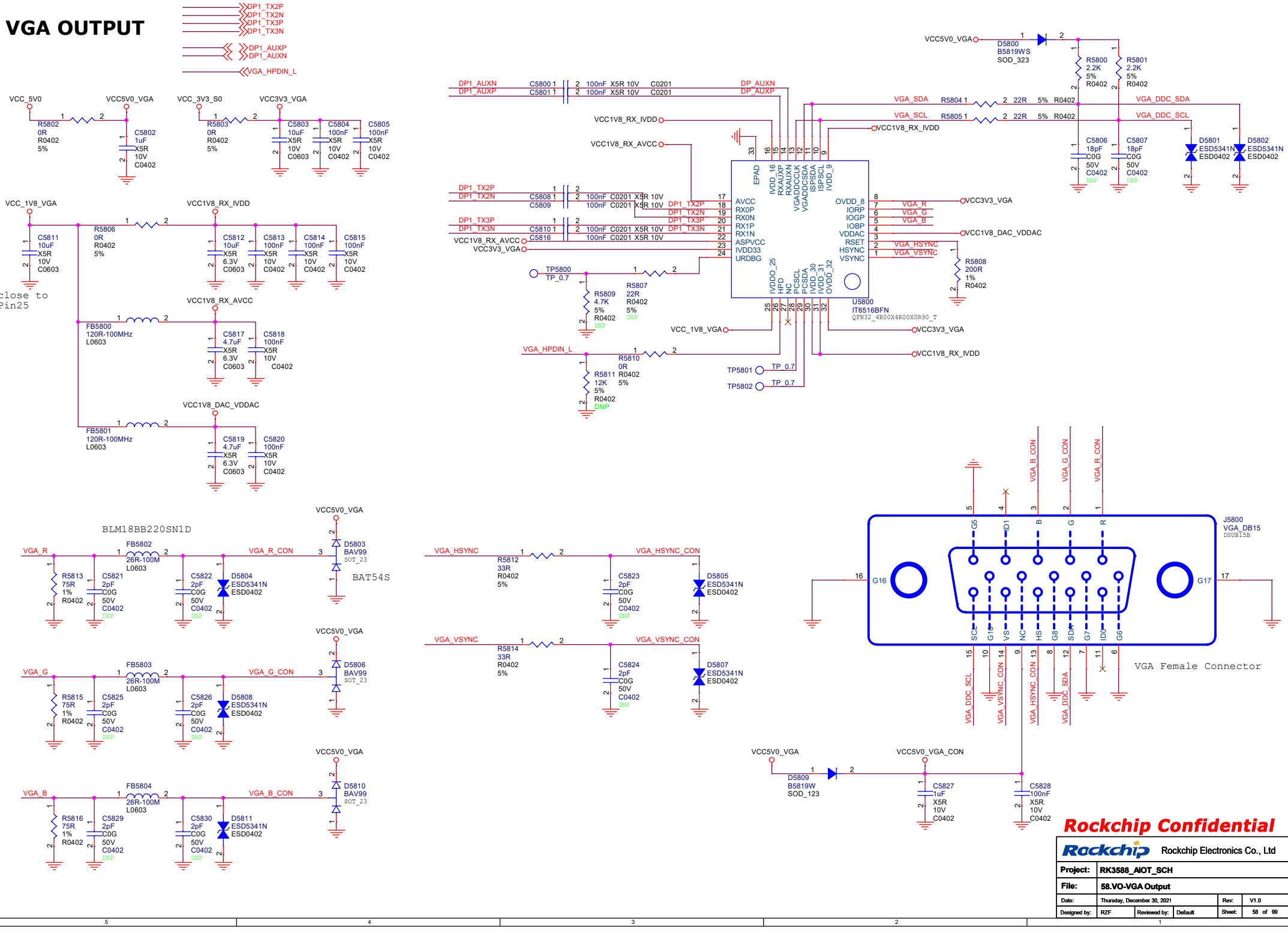
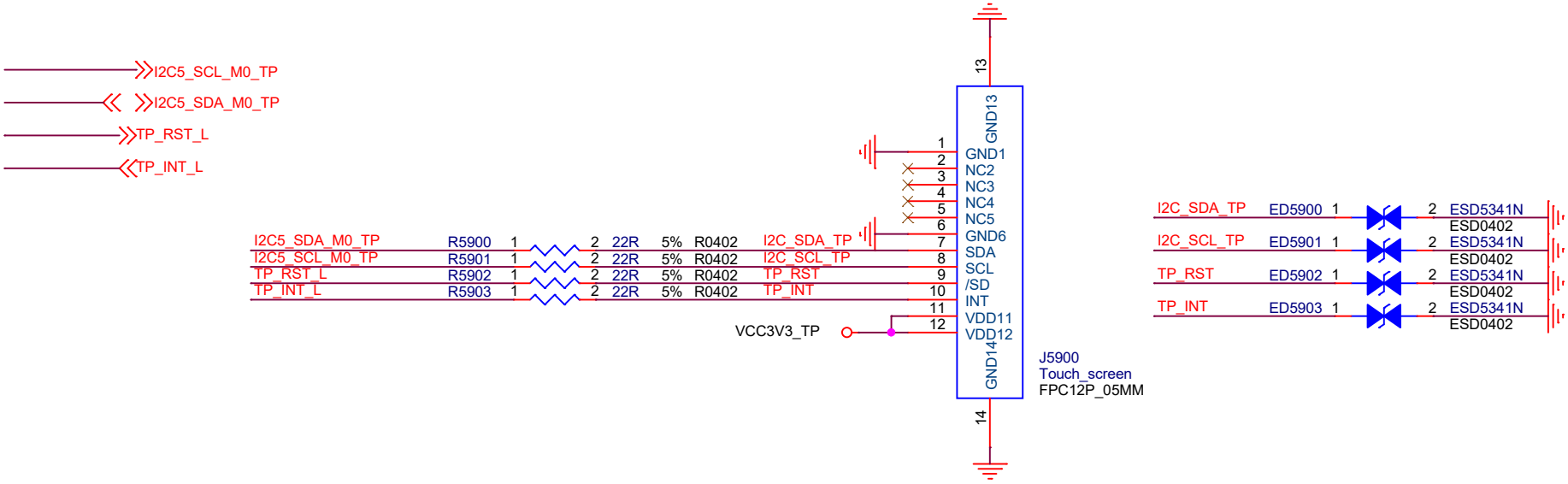
VGA OUTPUT

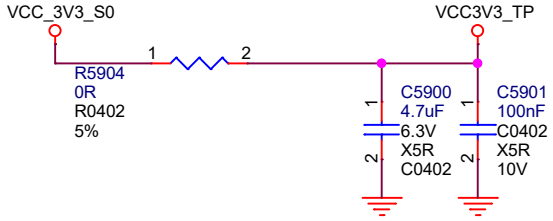


Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	58.VO-VGA Output		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by: Default	Sheet: 58 of 99

Touch Panel connector





Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	59.TP Connector_COF				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	Default	Sheet:	59 of 99

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WIFI（802.11 a/b/g/n/ac 2x2 MIMO）

UART9_TX_M0_BT
UART9_RX_M0_BT
UART9_RTSn_M0_BT
UART9_CTSn_M0_BT

WIFI_REG_ON_H
BT_REG_ON_H
BT_WAKE_HOST_H
HOST_WAKE_BT_H
WIFI_WAKE_HOST_H

Note:
Adjusted the load capacitance according to the crystal specification.

50 Ohm RF trace

J6200
G1 G2 G3 G4 ANT
SMA-J-P-H-RA-TH1
ANT5_SMA_RA_TH1
C6200 10pF C0402 C0G 50V
C6201 DNP C0402
C6202 DNP C0402

J6201
G1 G2 G3 G4 ANT
SMA-J-P-H-RA-TH1
ANT5_SMA_RA_TH1
C6203 10pF C0402 C0G 50V
C6205 DNP C0402
C6206 DNP C0402

C6204 22pF C0402 C0G 50V
R6200 22R 5% R0402
Y6200 X2 GND GND X1
37.4MHz
CRY4_3R20X2R50X0R80
C6207 22pF C0402 C0G 50V

U6200
AP6398S
MD50_AP6XXX_13RX15RX1R5

GND_9 GND_8 WL_ANT1 GND_7 GND_6 GND_5 GND_4 GND_3 GND_2 WL/BT_ANT0 GND_1

12 NC/NC/PCIE_PREST_L
13 XTAL_OUT
14 XTAL_IN
15 WL_REG_ON
16 WL_HOST_WAKE
17 SDIO_DATA_CMD
18 SDIO_DATA_CLK
19 SDIO_DATA_3
20 SDIO_DATA_2
21 SDIO_DATA_0/HUSB_DP
22 SDIO_DATA_1/HUSB_DM
23 GND_10
24 NC/SDIO_VSEL/PCIE_PME_L
25 VIN_LDO

50 BT_HOST_WAKE
49 BT_WAKE
48 GPIO8_9/NC_BT_ANT/NC
47 GPIO4/NC/PCIE_TDP
46 GPIO5/WL_UART_RX/PCIE_RDP
45 NC/WL_UART_TX/PCIE_RDN
44 UART_CTS_N
43 UART_RTS_N
42 UART_RXD
41 UART_TXD
40 GND_12
39 BT_REG_ON
38 NC/NC/PCIE_CLKREQ_L
37

VIN_LDO_OUT PCM_SYNC PCM_IN PCM_OUT PCM_CLK LPO GND_11 NC/NC/PCIE_REFCLK_N VDDIO NC/NC/PCIE_REFCLK_P VBAT

26 27 28 29 30 31 32 33 34 35 36

WIFI_REG_ON_S
WIFI_WAKE_HOST_H
SDIO_CMD_M0_WIFI R6206 0R R0402 5% WIFI_CMD
SDIO_CLK_M0_WIFI R6207 0R R0402 5% WIFI_CLK
SDIO_D3_M0_WIFI R6208 0R R0402 5% WIFI_D3
SDIO_D2_M0_WIFI R6209 0R R0402 5% WIFI_D2
SDIO_D1_M0_WIFI R6210 0R R0402 5% WIFI_D0
SDIO_D0_M0_WIFI R6211 0R R0402 5% WIFI_D1
SDIO_VSEL

VCCIO_WL R6214 10K R0402 5%
R6217 10K 5% R0402 DNP
C6211 4.7uF 10V X5R C0603
L6200 4.7uH IND_303012
1A_DCR<=80mohm

SDIO voltage select:
0: 3.3V 1:1.8V

BT_HOST_WAKE
BT_WAKE_HOST_H
HOST_WAKE_BT_S
R6204 0R 5% R0402
C6209 DNP C0402
C6208 10pF C0402 C0G 50V DNP
C6210 DNP C0402
ANT
GND1 GND2
ANT6200
ANT_JACK
ANT_JACK

UART9_RTSn_M0_BT
UART9_CTSn_M0_BT
UART9_TX_M0_BT
UART9_RX_M0_BT
BT_REG_ON_S

WIFI_REG_ON_H 3.3V R6201 100K R0402 5%
WIFI_REG_ON_S R6202 120K 5% R0402

BT_REG_ON_H 3.3V R6203 100K R0402 5%
BT_REG_ON_S R6205 120K 5% R0402

HOST_WAKE_BT_H 3.3V R6212 100K R0402 5%
HOST_WAKE_BT_S R6213 120K 5% R0402

I2S2_LRCK_M0_BT R6219 22R R0402 5% PCM_SYNC_BT
I2S2_SDO_M0_BT R6220 22R R0402 5% PCM_IN_BT
I2S2_SDI_M0_BT R6221 22R R0402 5% PCM_OUT_BT
I2S2_SCLK_M0_BT R6222 22R R0402 5% PCM_CLK_BT

32KOUT_WIFI
1.6V<V<3.3V
R6223 DNP R0402
C6213 DNP C0402

VCC3V3_WL_VBAT
VCC_3V3_S3
VCCIO_WL
R6218 0R R0805 1%
VCC_1V8_S3
R6216 0R R0603 1%

C6214 100nF X5R 10V C0402
C6215 100nF X5R 10V C0402
C6216 22uF X5R 10V C0805
C6212 1uF X5R 10V C0402

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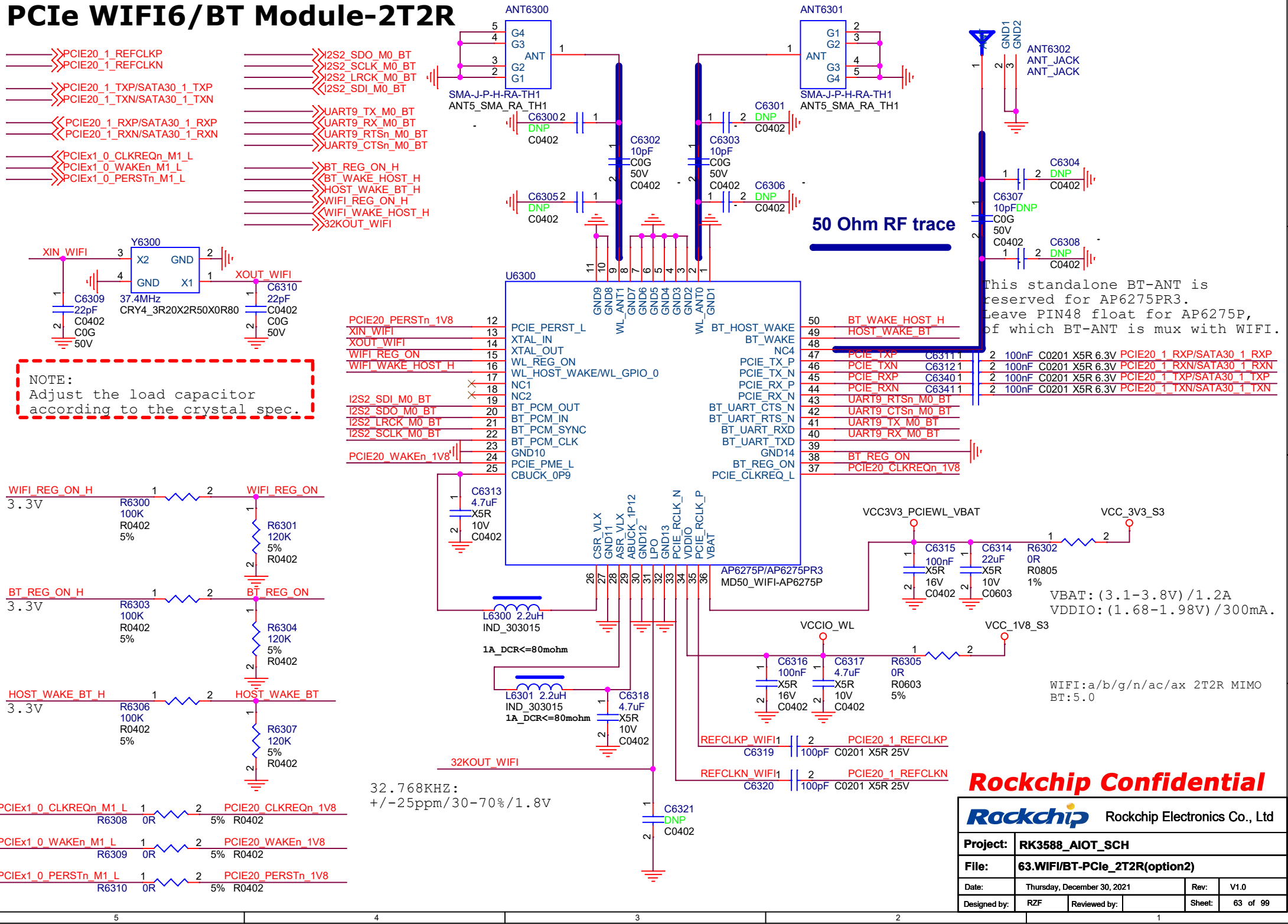
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	62.WIFI/BT-SDIO_2T2R		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	62 of 99

PCIe WIFI6/BT Module-2T2R



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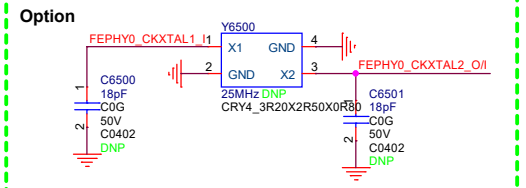
Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	63.WIFI/BT-PCIe_2T2R(option2)		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	63 of 99

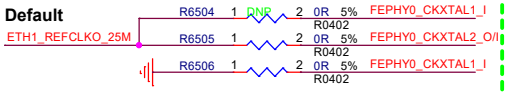
RMII

GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXEN
GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXDV_CRS
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO
ETH1_REFCLKO_25M
GMAC1_RSTn_L

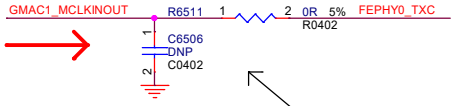
Option

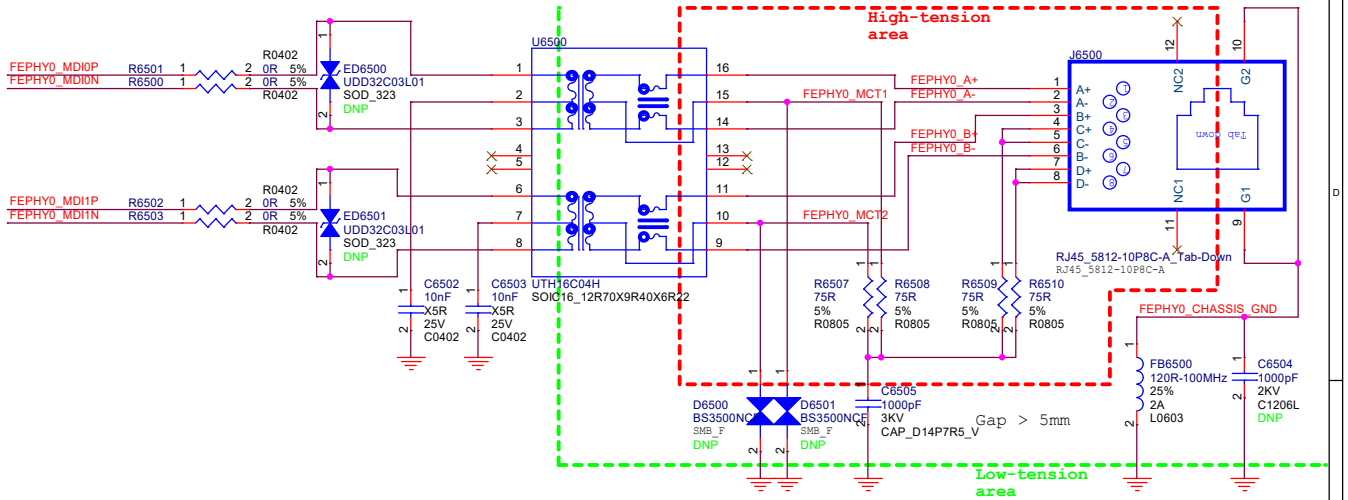


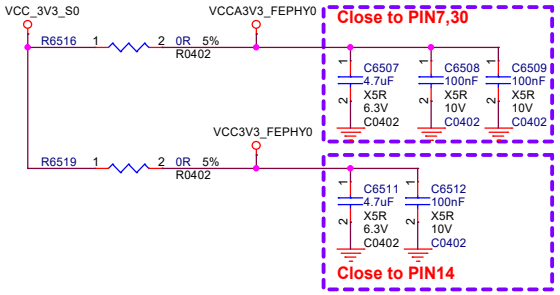
Default

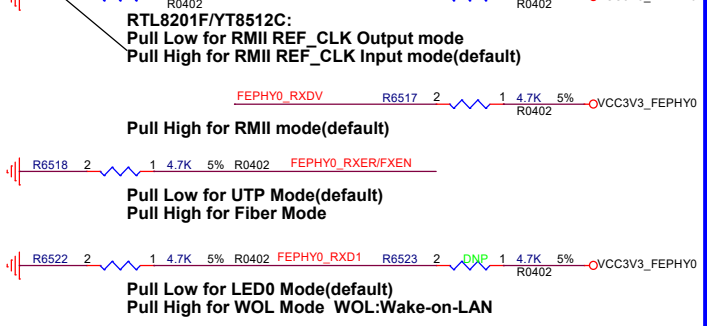


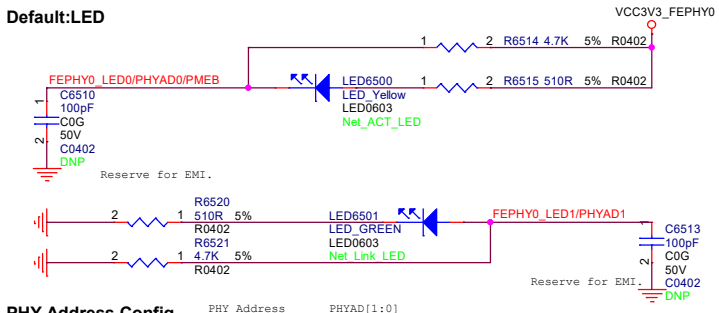
Default: Refclk:MAC output,PHY input

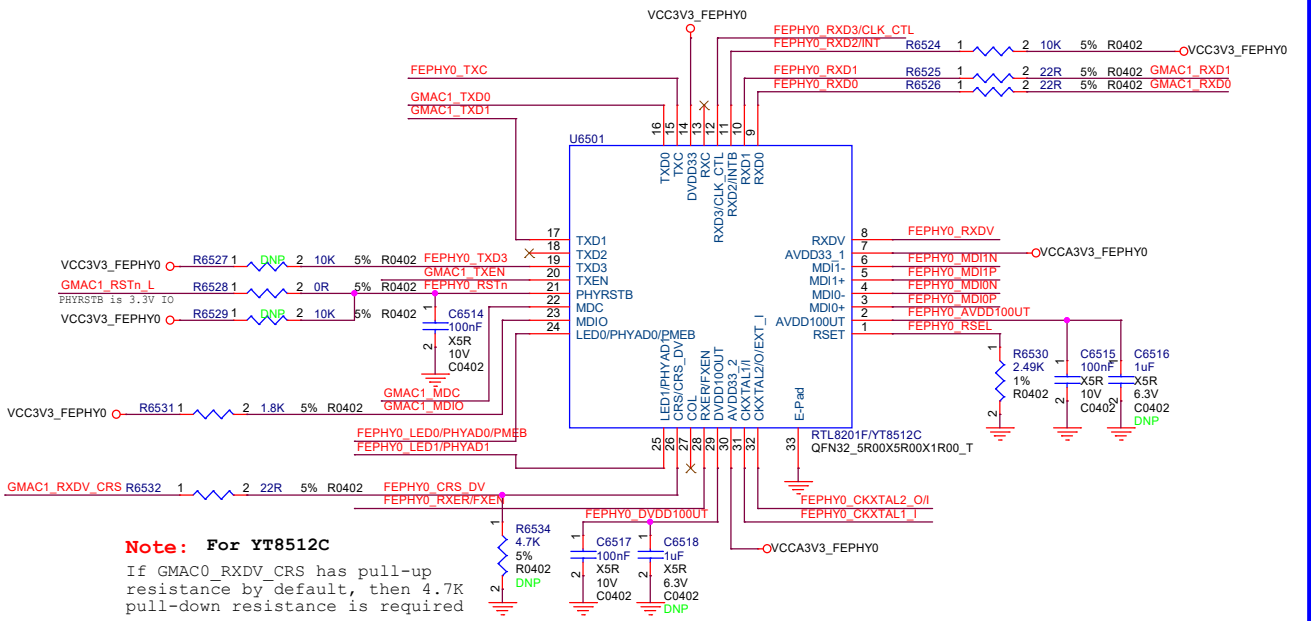






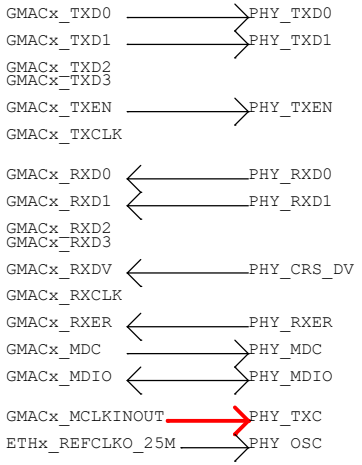




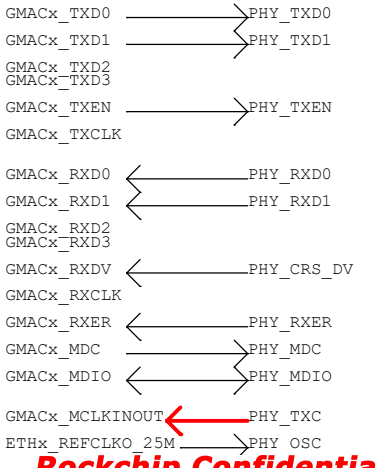


Default

Refclk:MAC output,PHY input



Refclk:MAC input,PHY output



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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	65.Ethernet-RMII(option)				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	Default	Sheet:	65 of 99

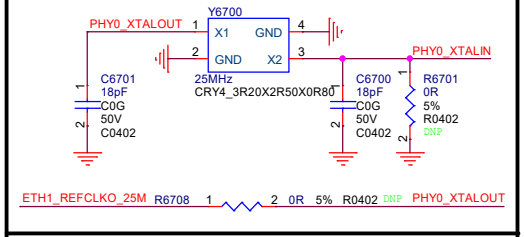
RGMII TO RJ45

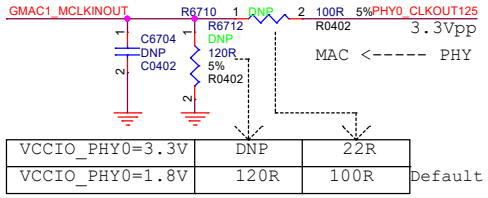
GMAC1_TXD0
GMAC1_TXD1
GMAC1_TXD2
GMAC1_TXD3
GMAC1_TXEN
GMAC1_TXCLK

GMAC1_RXD0
GMAC1_RXD1
GMAC1_RXD2
GMAC1_RXD3
GMAC1_RXDV_CRS

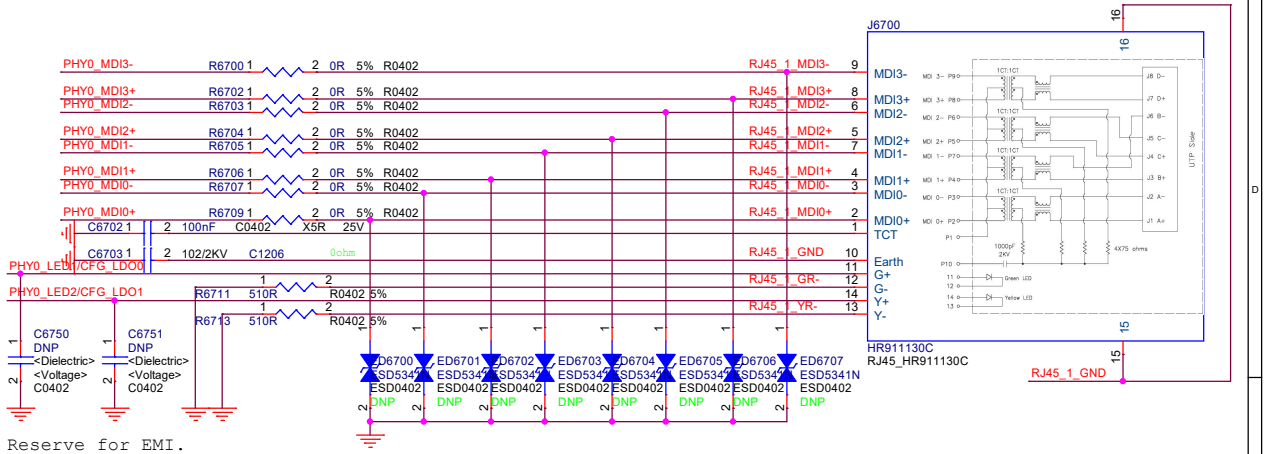
GMAC1_RXCLK
ETH1_REFCLKO_25M
GMAC1_MCLKINOUT
GMAC1_MDC
GMAC1_MDIO

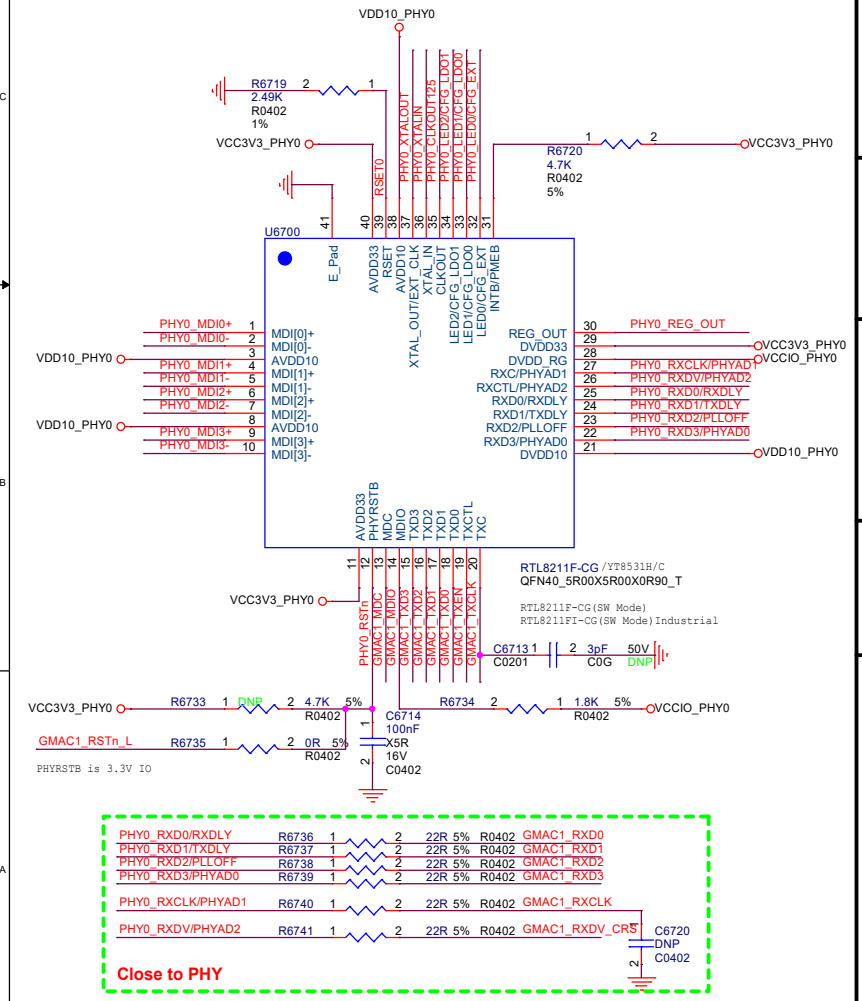
GMAC1_RSTn_L

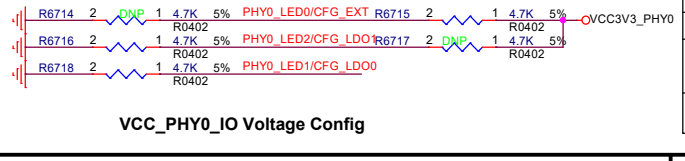




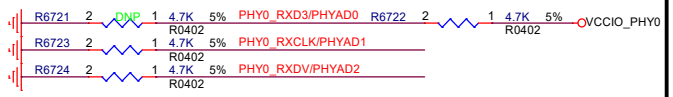
VCCIO_PHY0=3.3V	DNP	22R	
VCCIO_PHY0=1.8V	120R	100R	Default

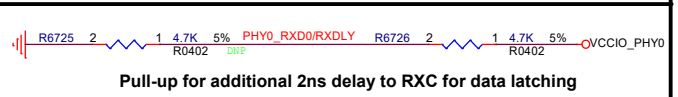


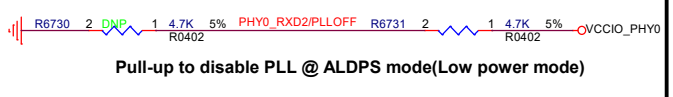


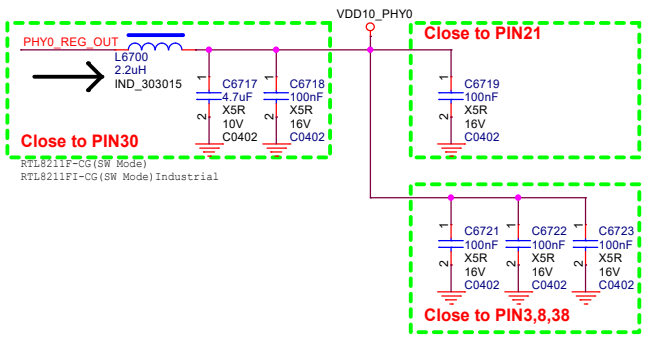


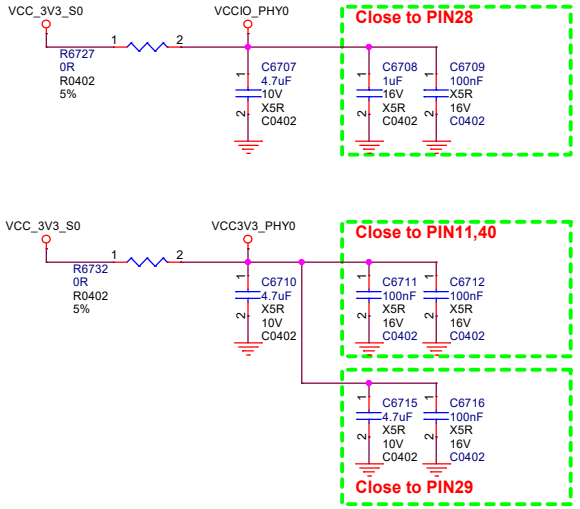
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	











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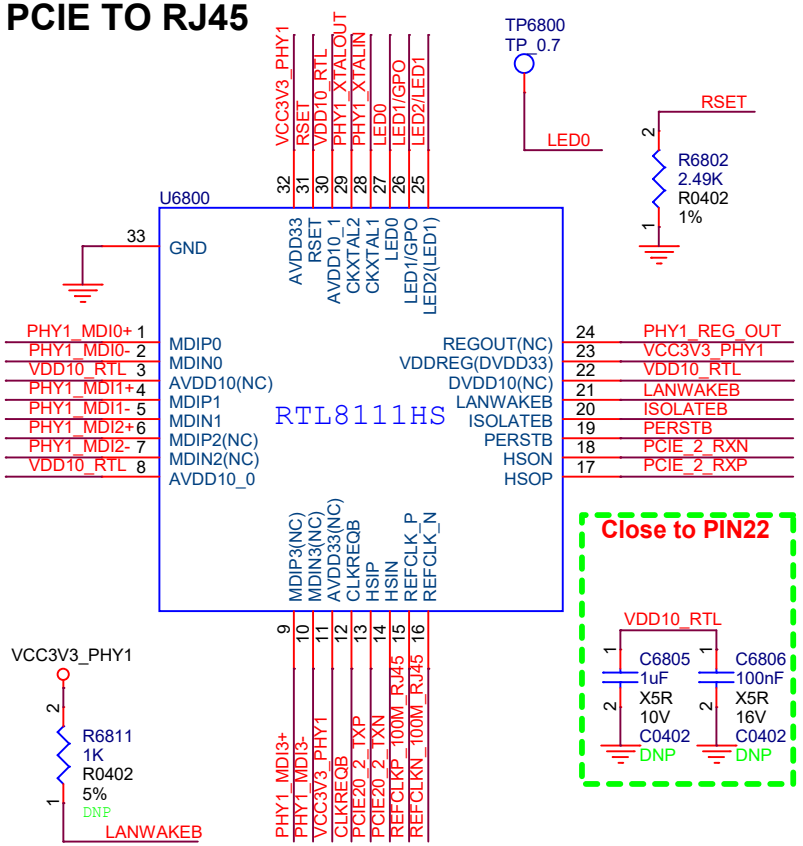
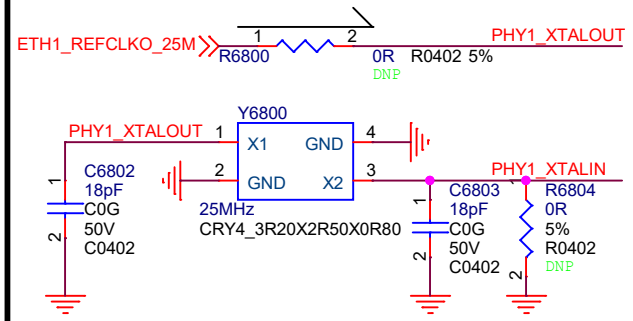
Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	67.Ethernet-GPHY_RGMII1		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by:	RZF	Reviewed by: Default	Sheet: 67 of 99

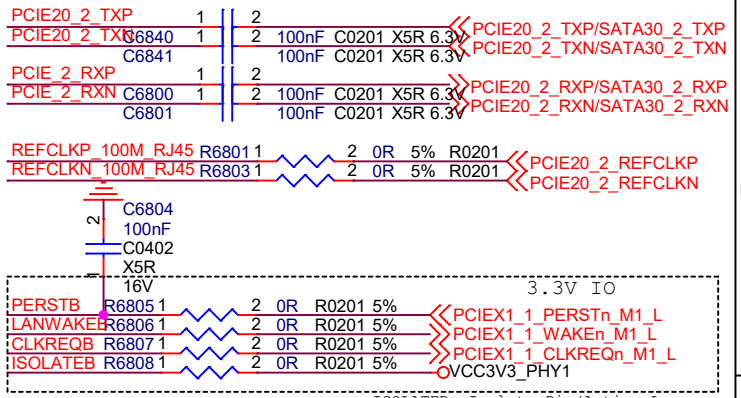
PCIE TO RJ45





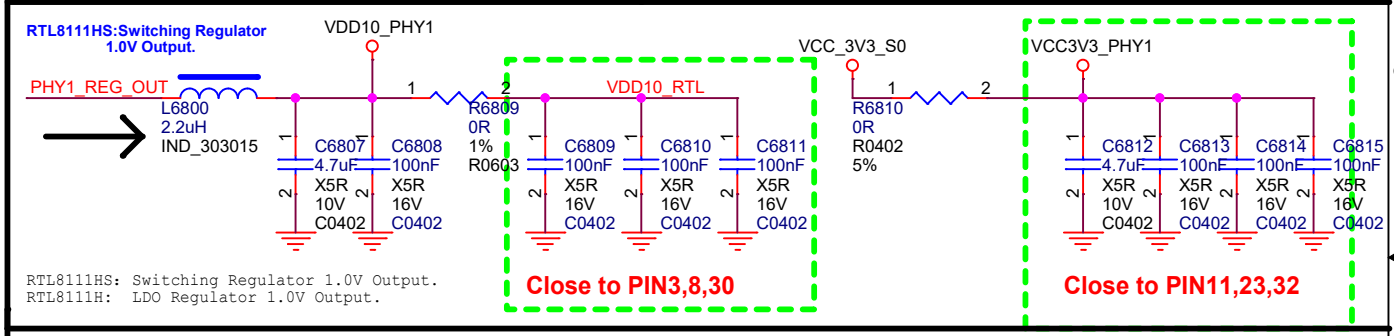
25Mhz Crystal: Stuff Y6800 C6801,No Stuff R6808,R6804
External Clock: Stuff R6804,R6808,No stuff: Y6800,C6801.

CKXTAL1(I): Input of 25Mhz Clock Reference.
CKXTAL2(IO): Input of External Clock Source
Output of 25Mhz Clock Reference.

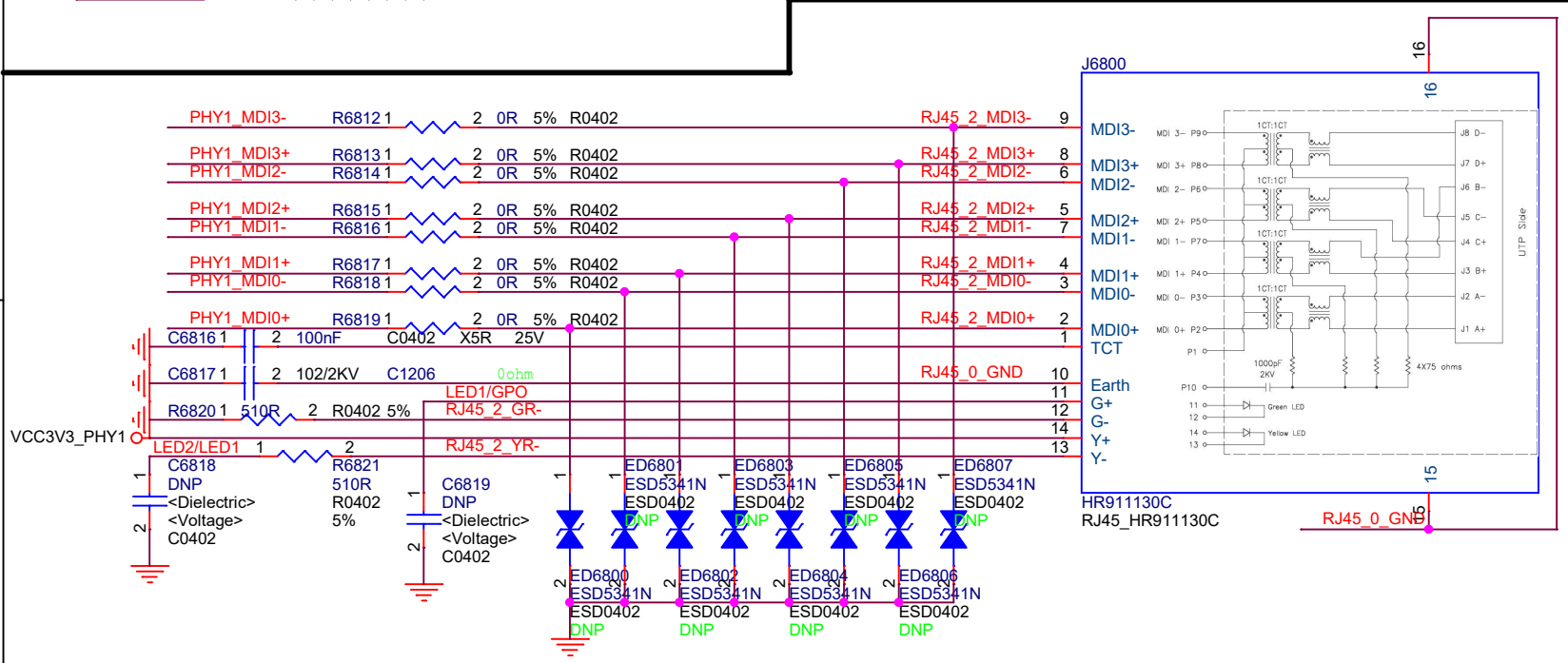


LANWAKEB:Power Management Event (Open Drain;Active Low,1.8V/3.3V compatible input/output mode with a weak external pull resistor)

ISOLATEB :Isolate Pin(Active Low, 1.8V/3,3V compatible input)Used to isolate the RTL8111HS from the PCI Express bus,The RTL8111HS will not drive its PCI Express input as long as the Isolate pin is asserted.



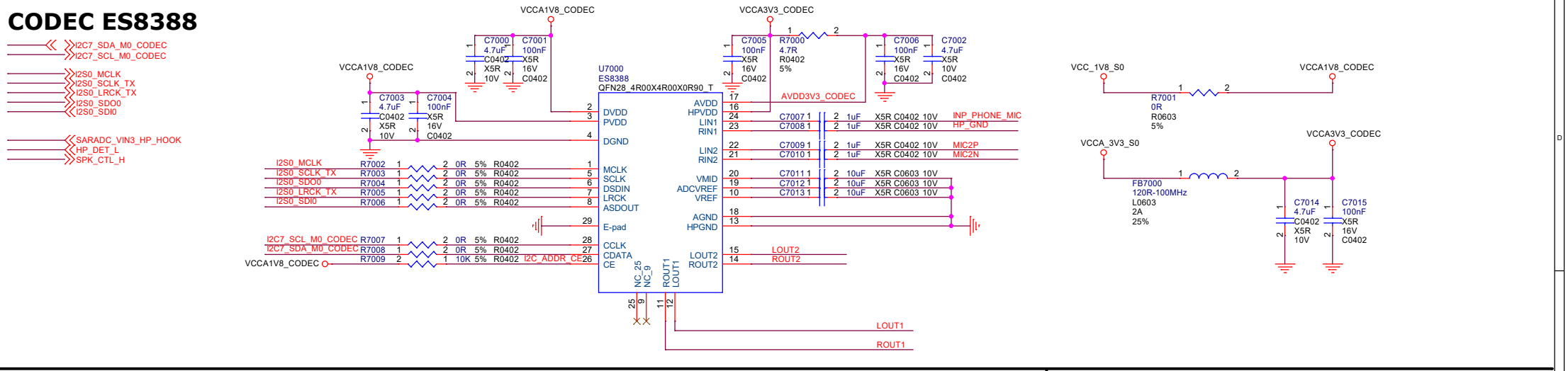
RTL8111HS: Switching Regulator 1.0V Output.
RTL8111H: LDO Regulator 1.0V Output.



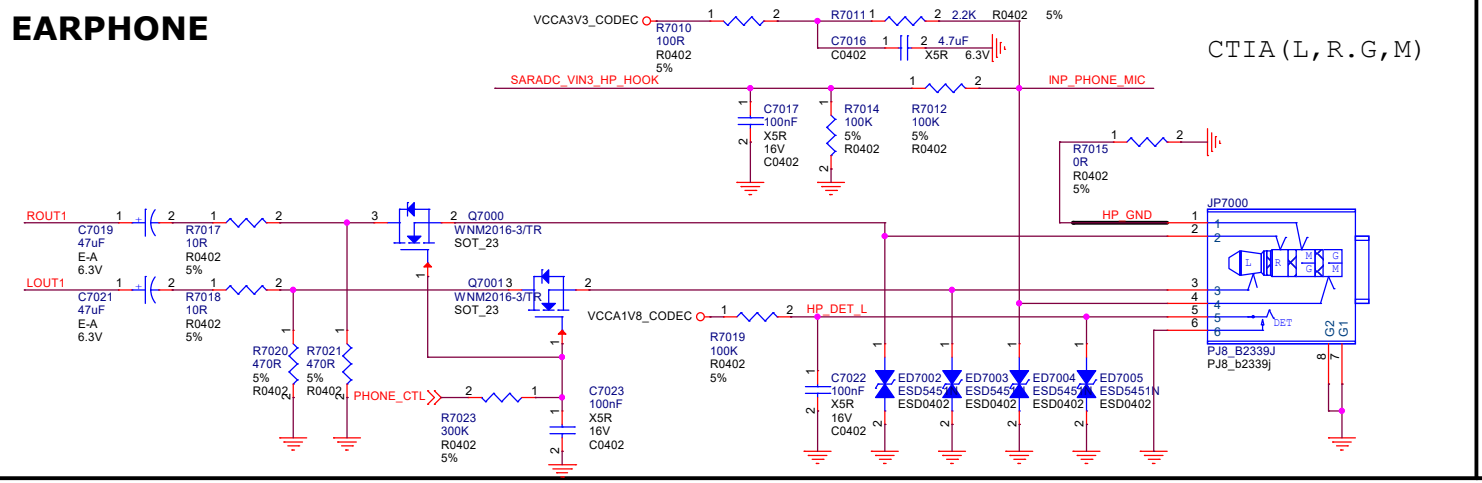
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	68.Ethernet-PCIE				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:	Default	Sheet:	68 of 99

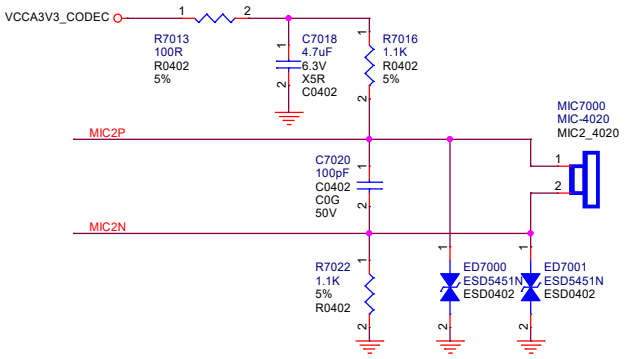
CODEC ES8388



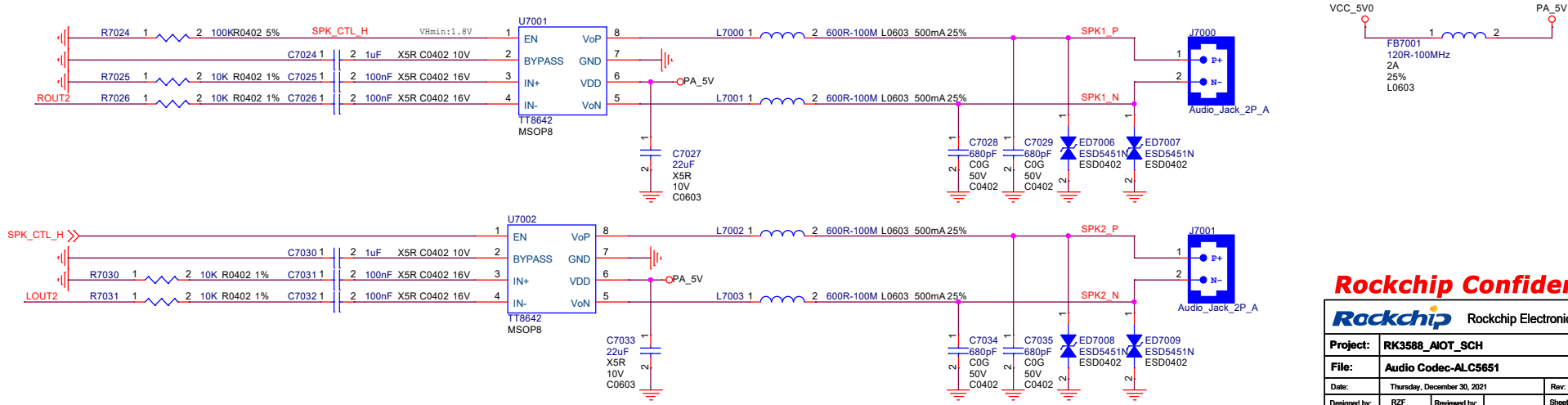
EARPHONE



Analog MIC



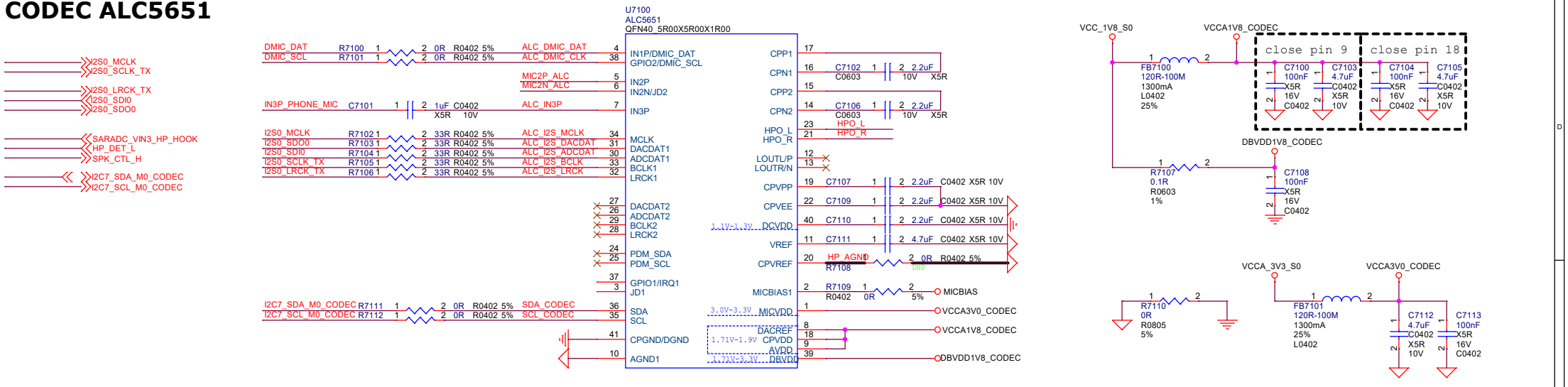
SPEAKER



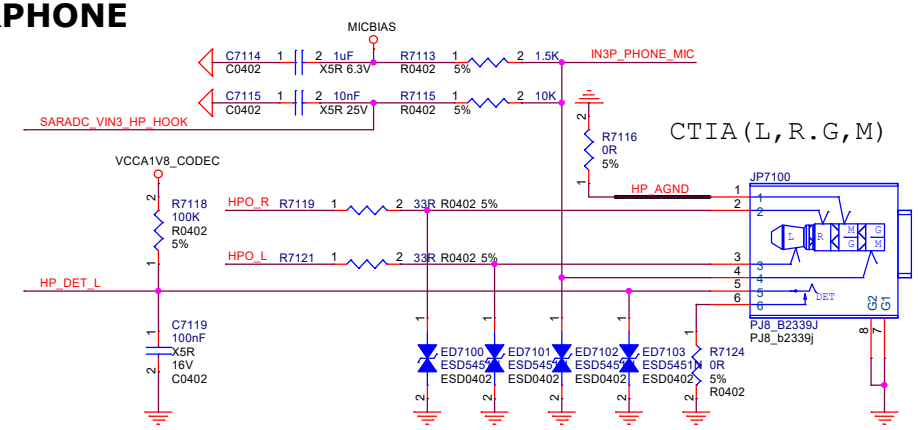
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH			
File:	Audio Codec-ALC5651			
Date:	Thursday, December 30, 2021		Rev:	V1.0
Designed by:	RZF	Reviewed by:	Sheet:	70 of 99

CODEC ALC5651



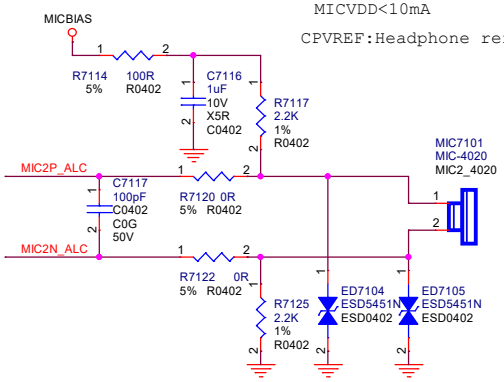
EARPHONE



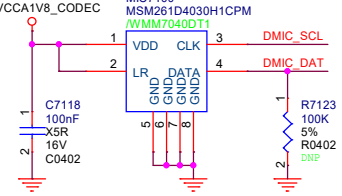
Analog MIC

Power Sequence:
DBVDD-MICVDD
DBVDD<150mA
MICVDD<10mA

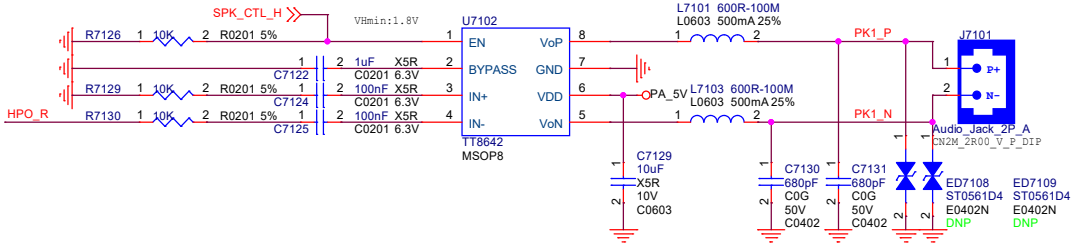
CPVREF:Headphone reference ground.

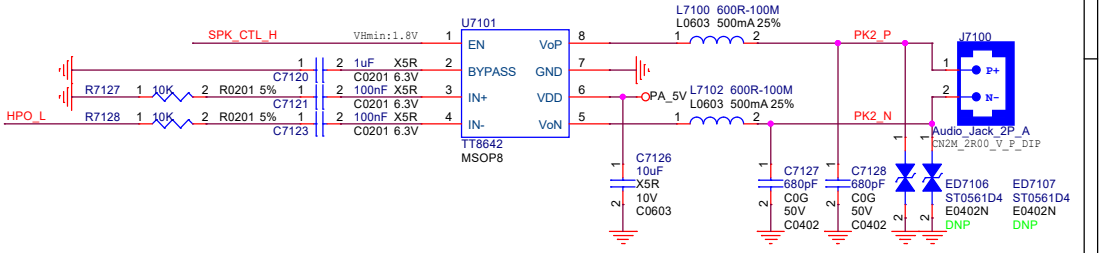


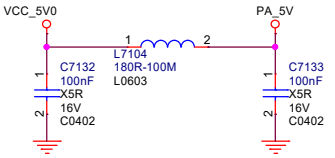
DIGITAL MIC



SPEAKER







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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	71.Audio Codec(option)				
Date:	Thursday, December 30, 2021		Rev:	V1.0	
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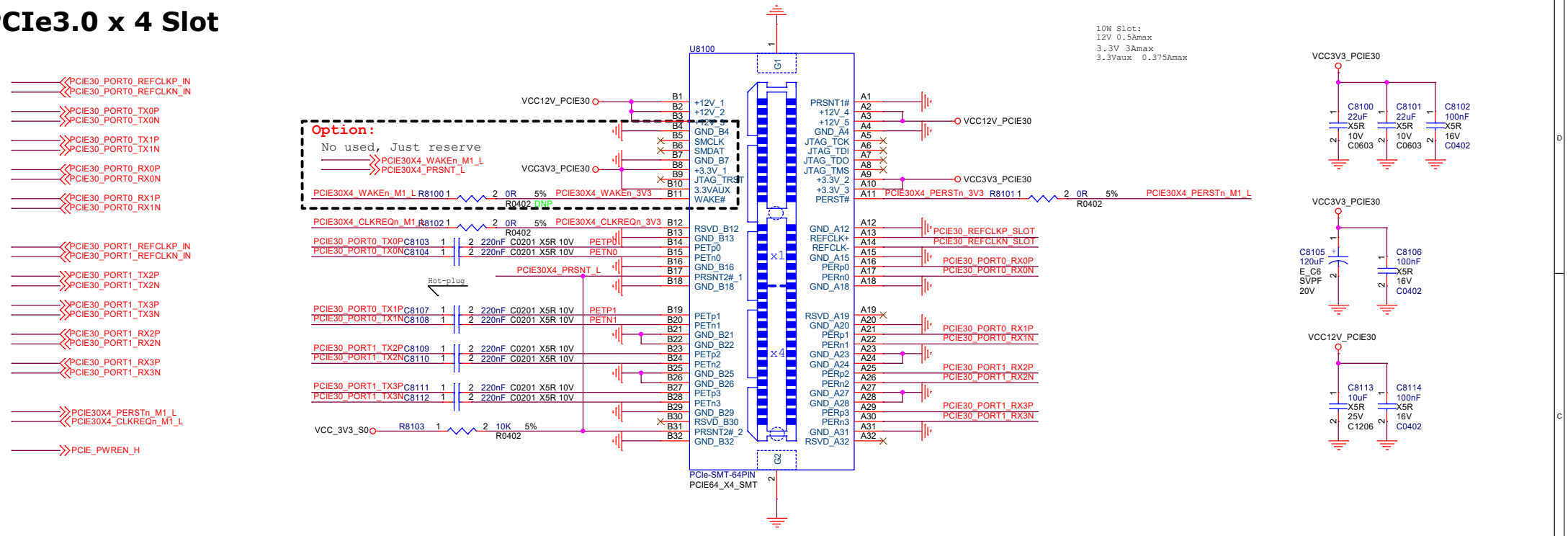
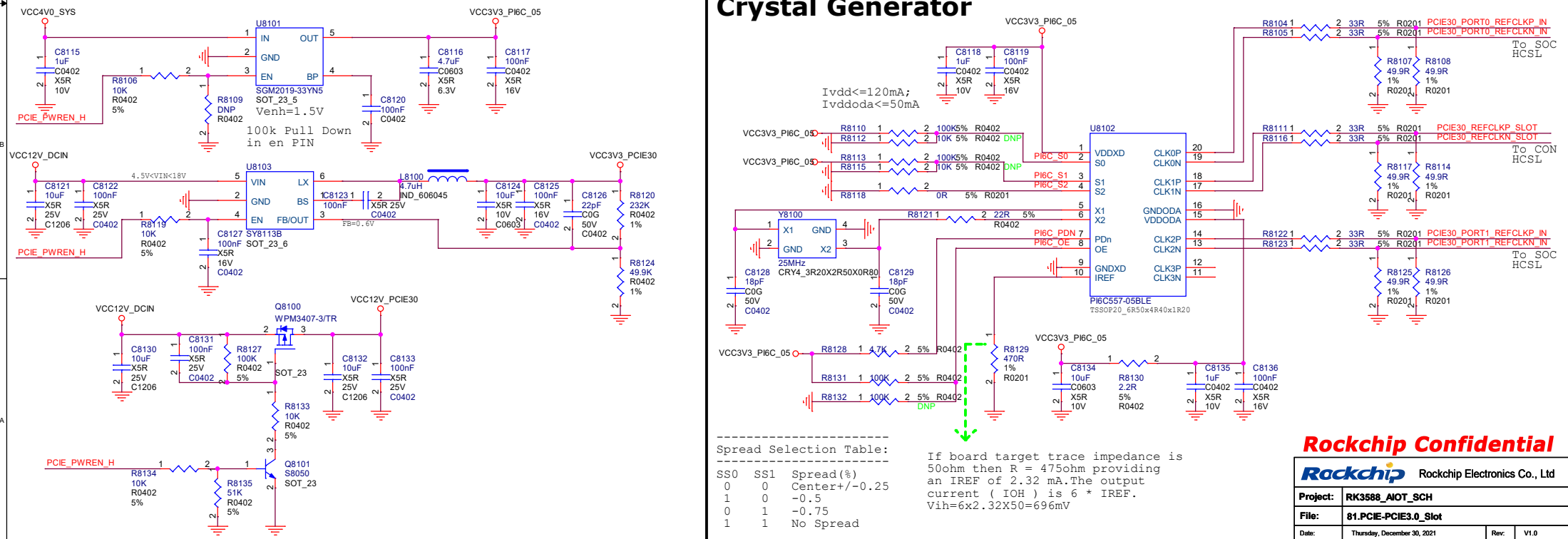
PCIe3.0 x 4 Slot

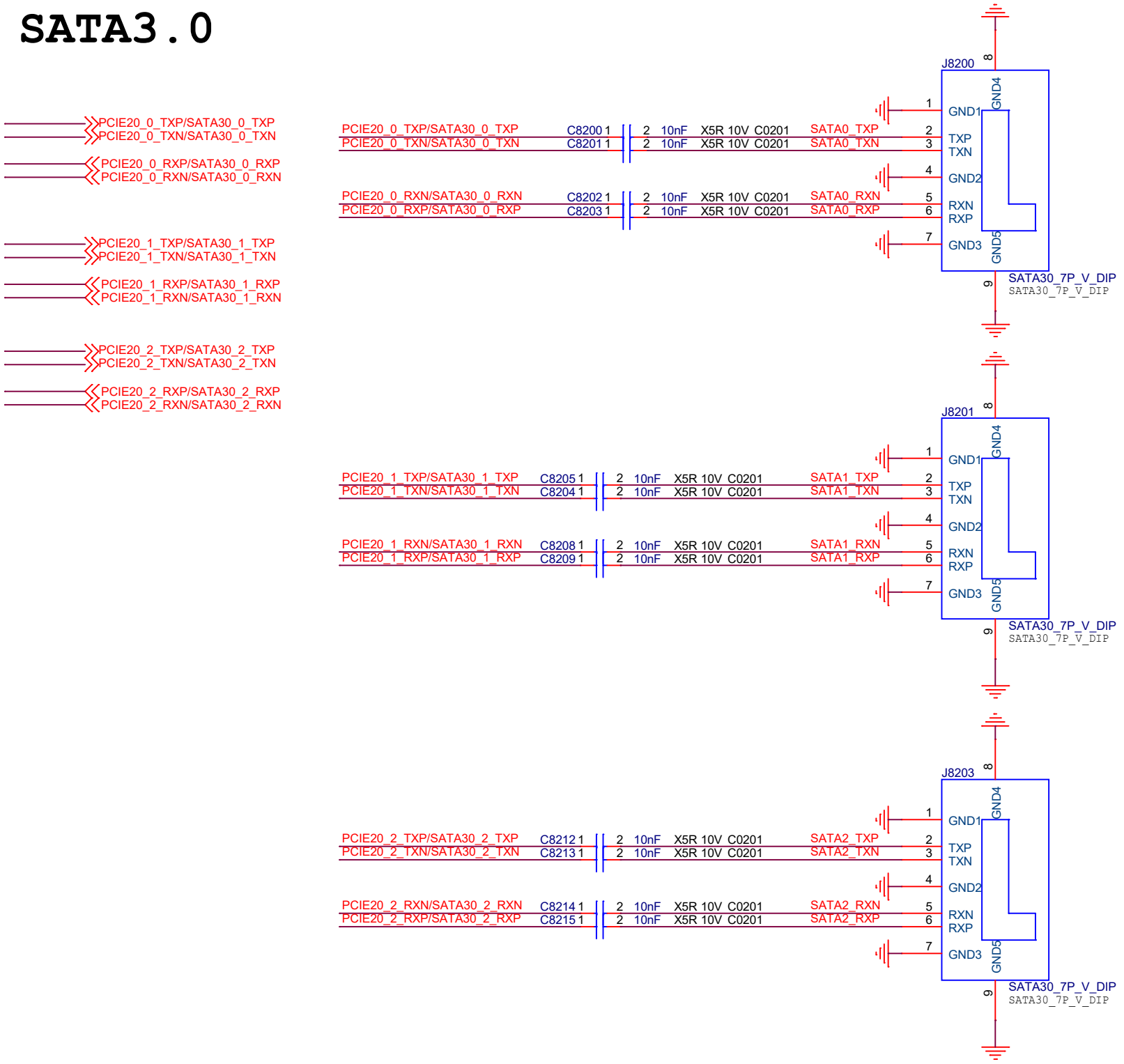


Crystal Generator



Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	81.PCIE-PCIE3.0_Slot		
Date:	Thursday, December 30, 2021	Rev:	V1.0
Designed by: RZF	Reviewed by:	Sheet:	81 of 99

SATA3.0



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Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	82.SATA-SATA3.0 Slot_7P				
Date:	Thursday, December 30, 2021			Rev:	V1.0
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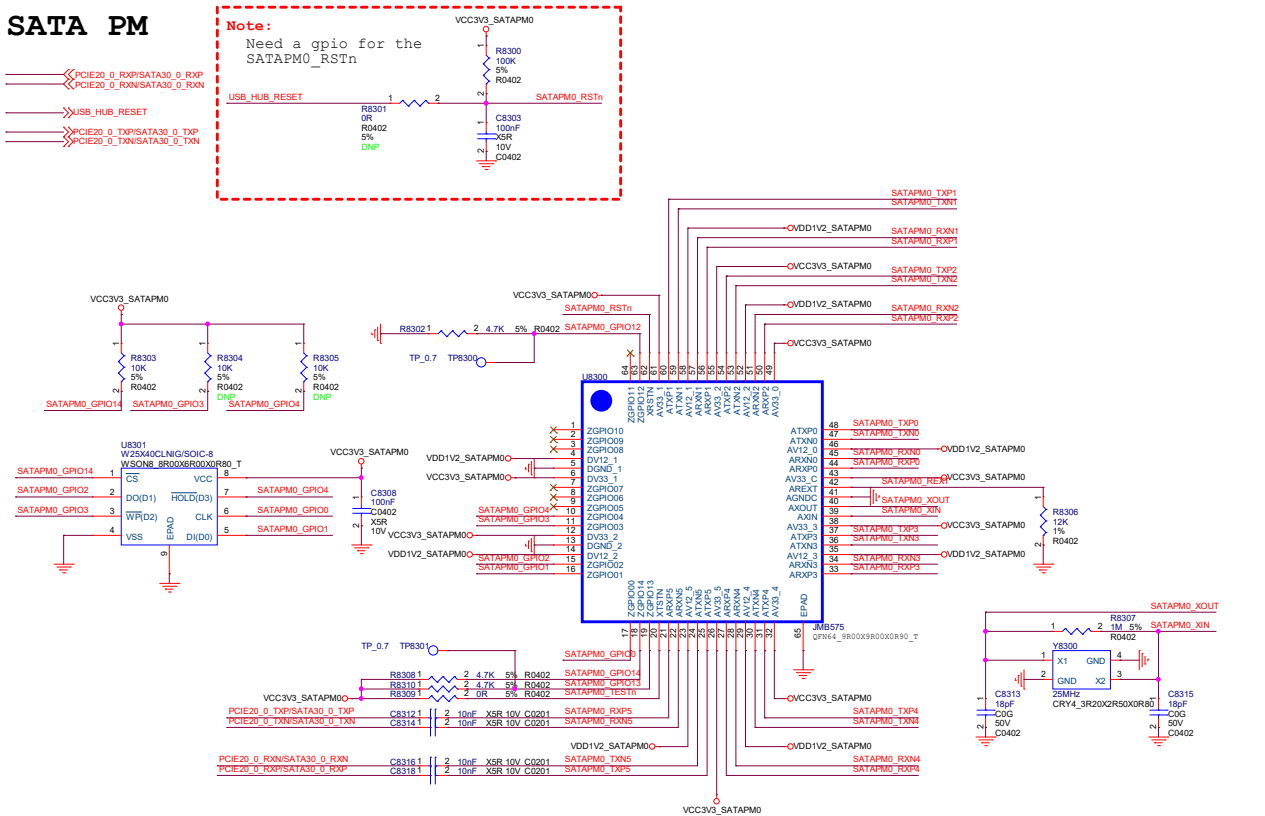
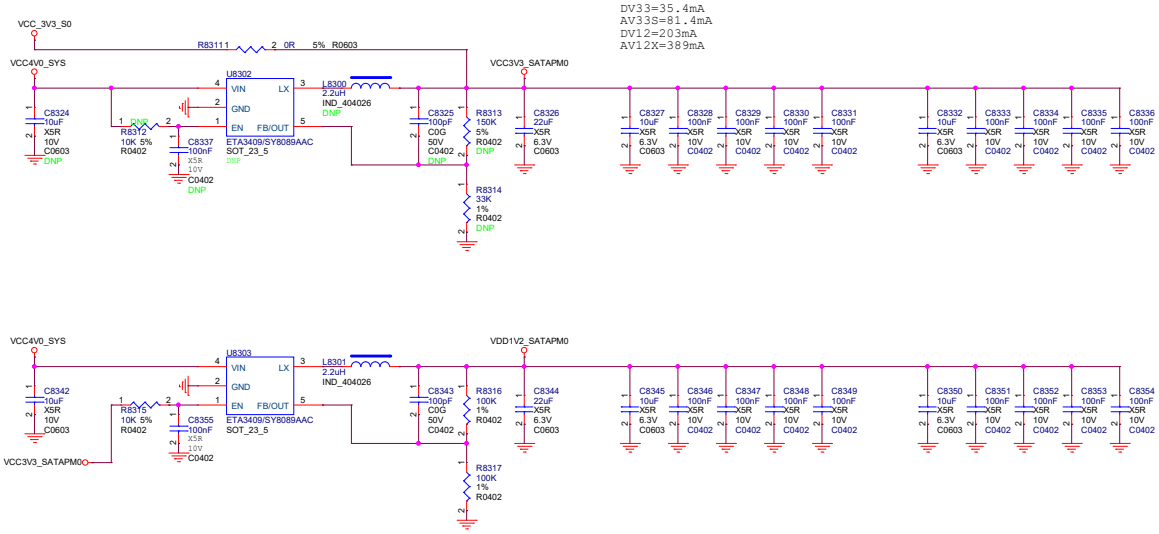
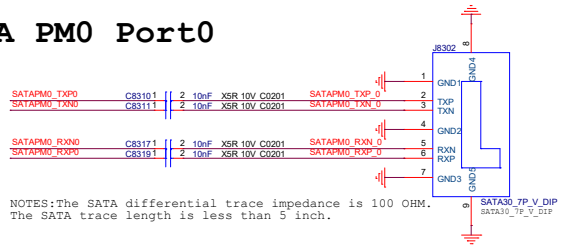
SATA PM



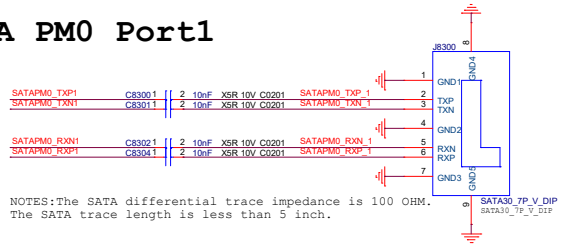


SATA PM0 Port0



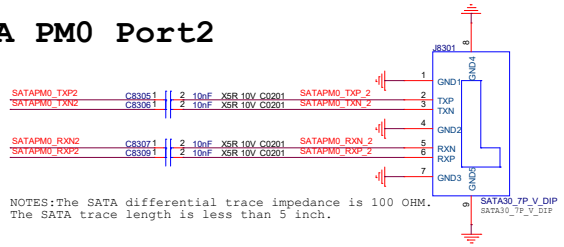
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port1



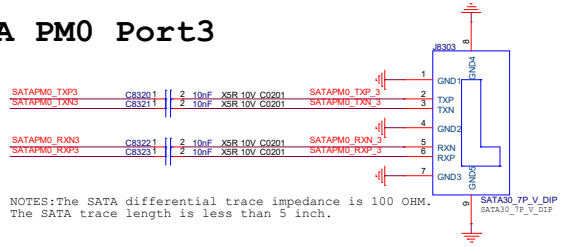
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port2



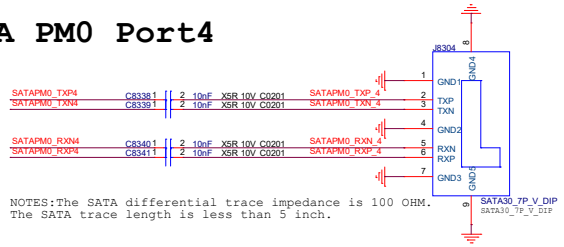
NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port3



NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

SATA PM0 Port4



NOTES:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.

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Rockchip	Rockchip Electronics Co., Ltd		
Project:	RK3588_AIOT_SCH		
File:	83.SATA-SATA PM0(option)		
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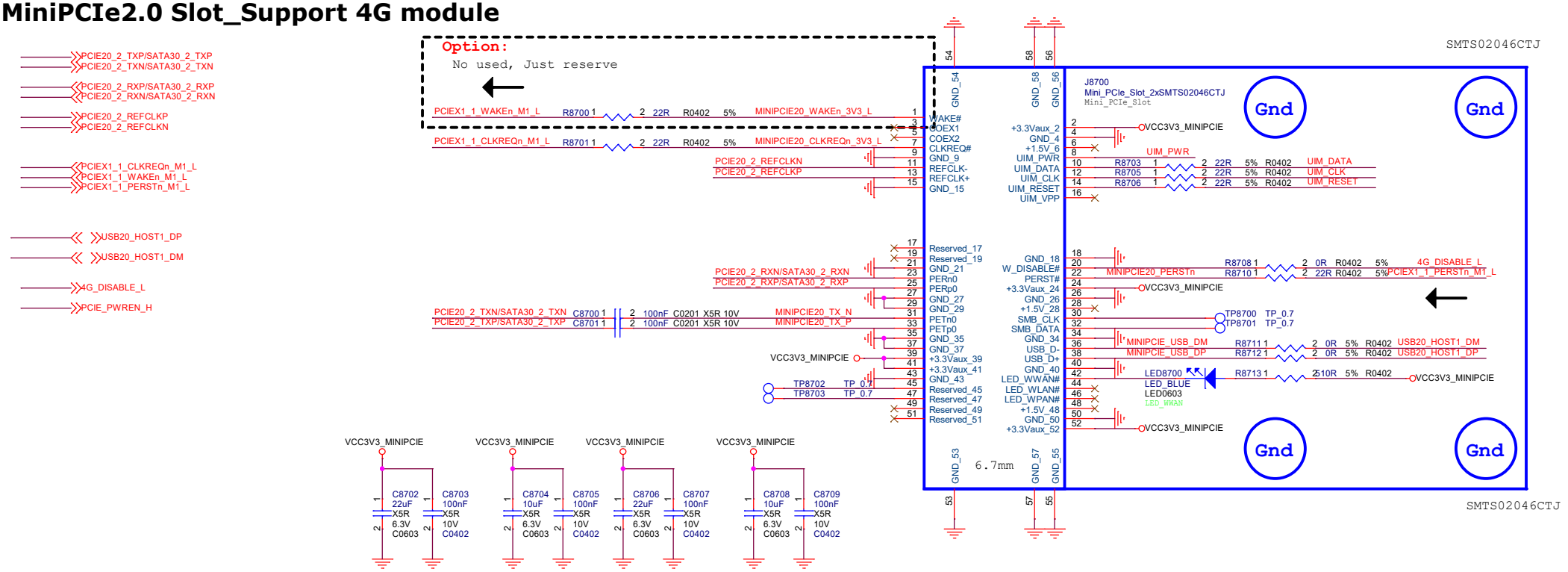
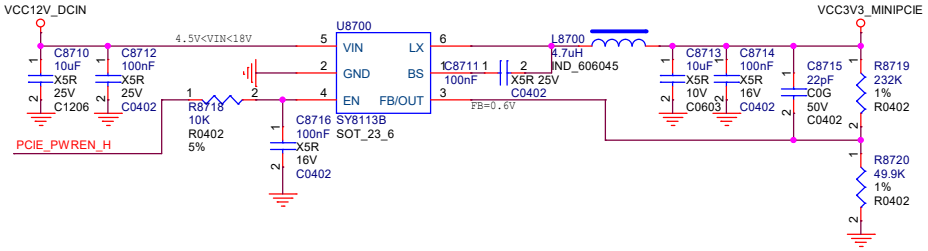
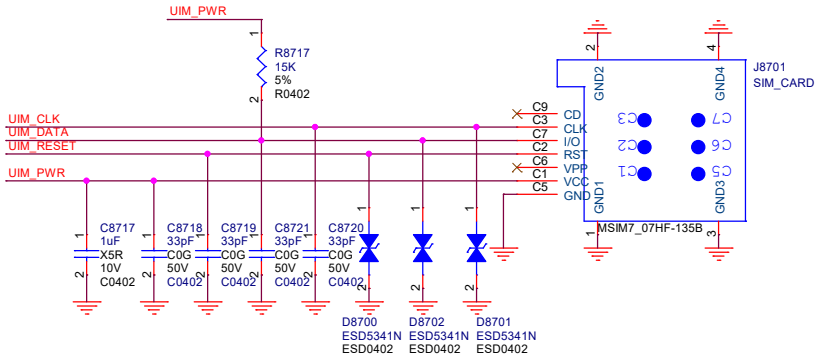
MiniPCIe2.0 Slot_Support 4G module



MiniPCIe2.0 Slot Power



Sim Card



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Rockchip	Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH			
File:	87.MiniPCIe2.0 Slot(option)			
Date:	Thursday, December 30, 2021		Rev:	V1.0
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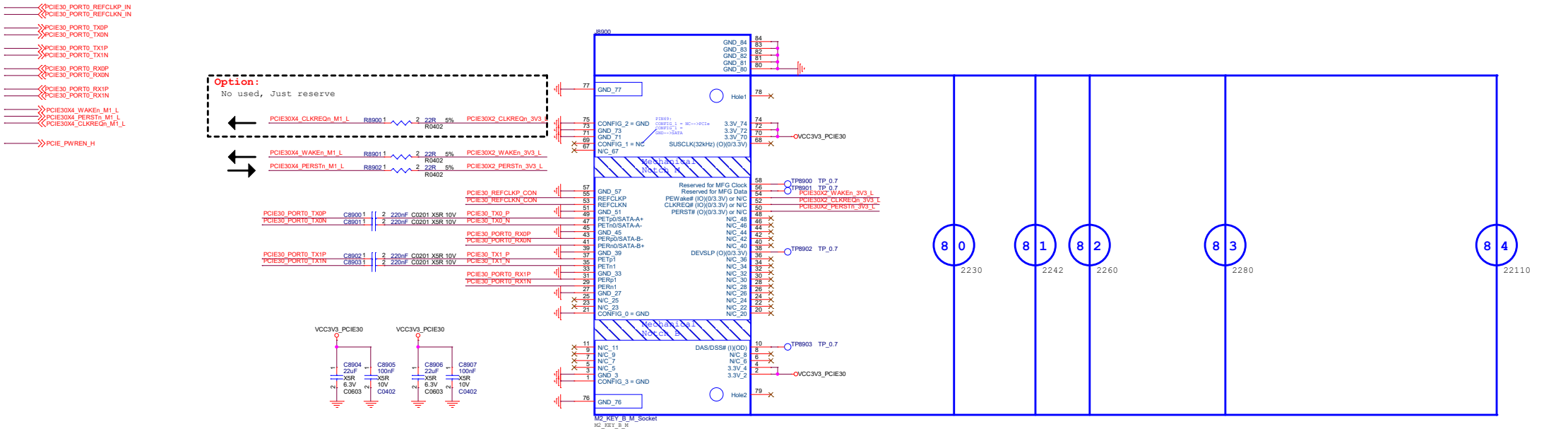
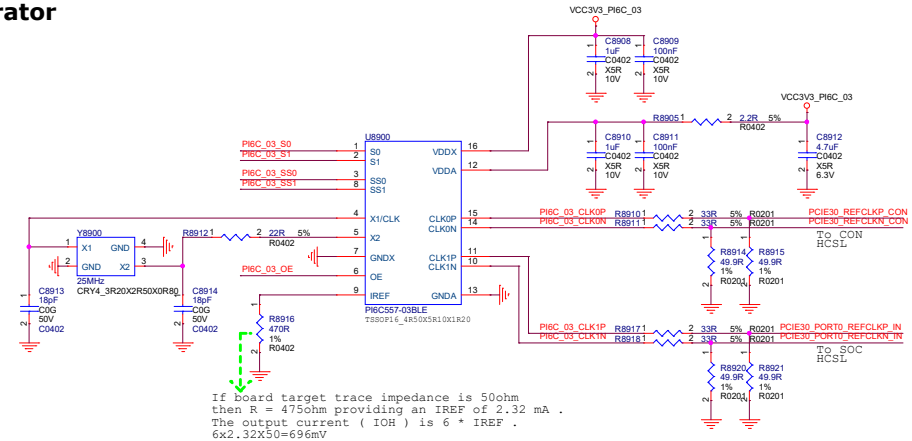
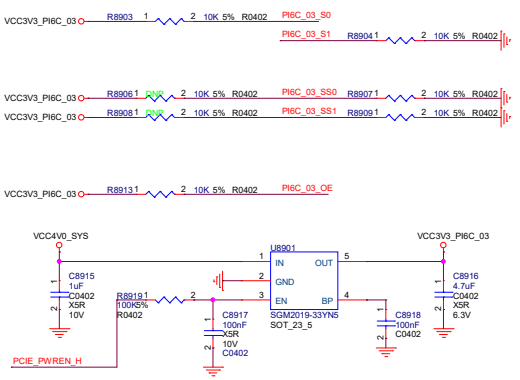
M.2_PCIe3.0 x 2Lanes



Crystal Generator

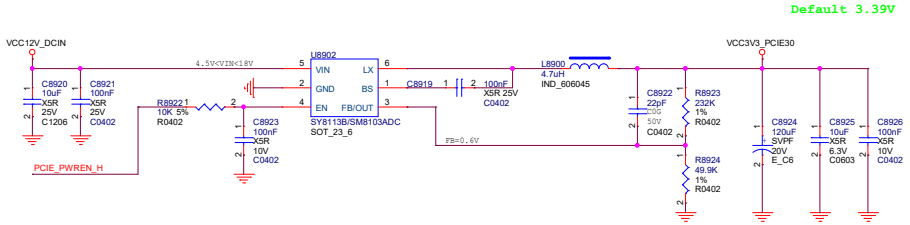




PI6C_S1	PI6C_S0	Out Freq
0	1	100MHz

PI6C_SS1	PI6C_SS0	Spread %
0	0	No Spread
0	1	-0.5
1	0	-1.0
1	1	No Spread

M.2 Power



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Rockchip Electronics Co., Ltd			
Project:	RK3588_AIOT_SCH		
File:	89.PCIE-M.2(option)		
Date:	Thursday, December 30, 2021	Rev:	V1.0
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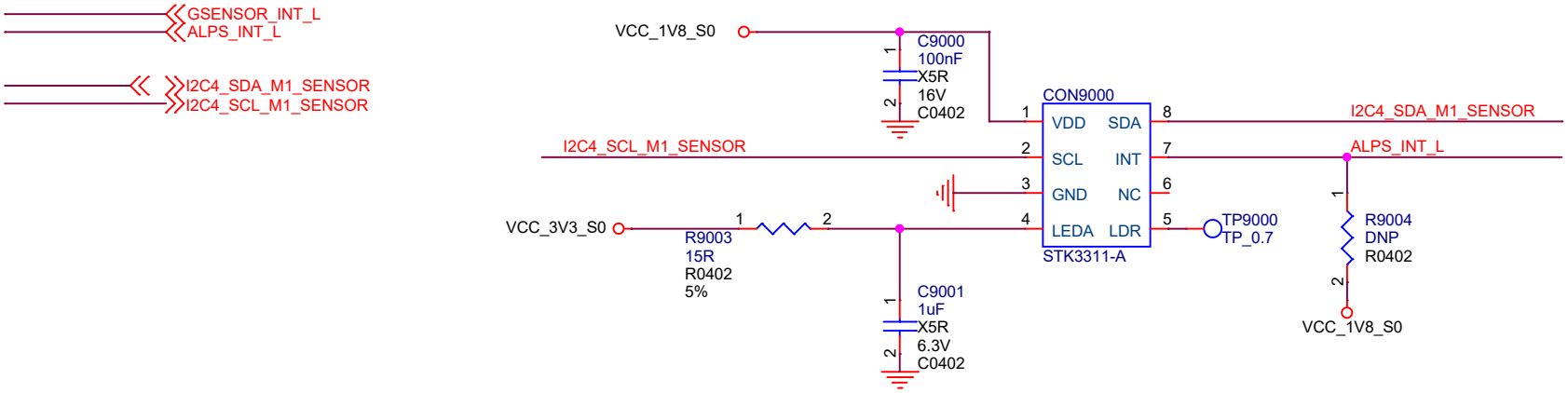
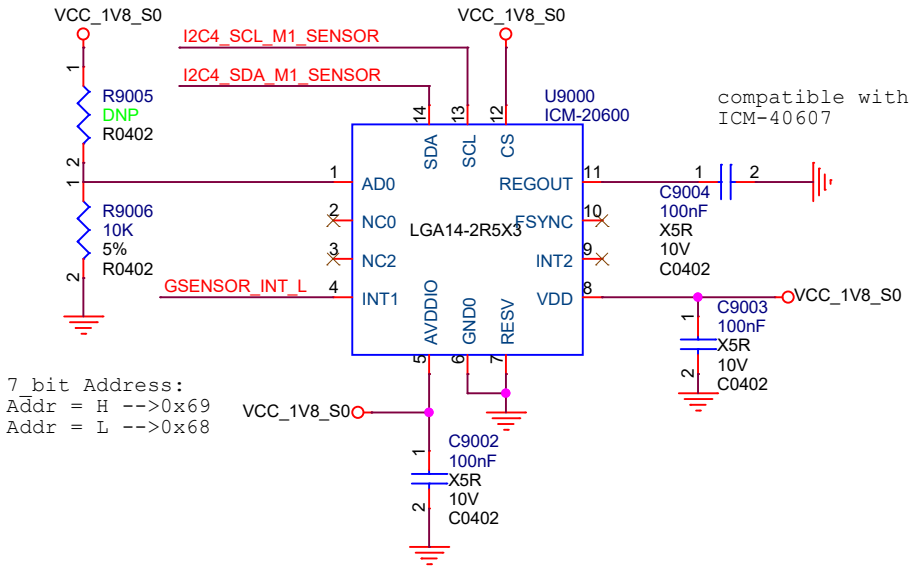
Sensor

Ambient Light+Proximity Sensor



Gyroscope+G-sensor



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Rockchip	Rockchip Electronics Co., Ltd				
Project:	RK3588_AIOT_SCH				
File:	90.SENSOR				
Date:	Thursday, December 30, 2021			Rev:	V1.0
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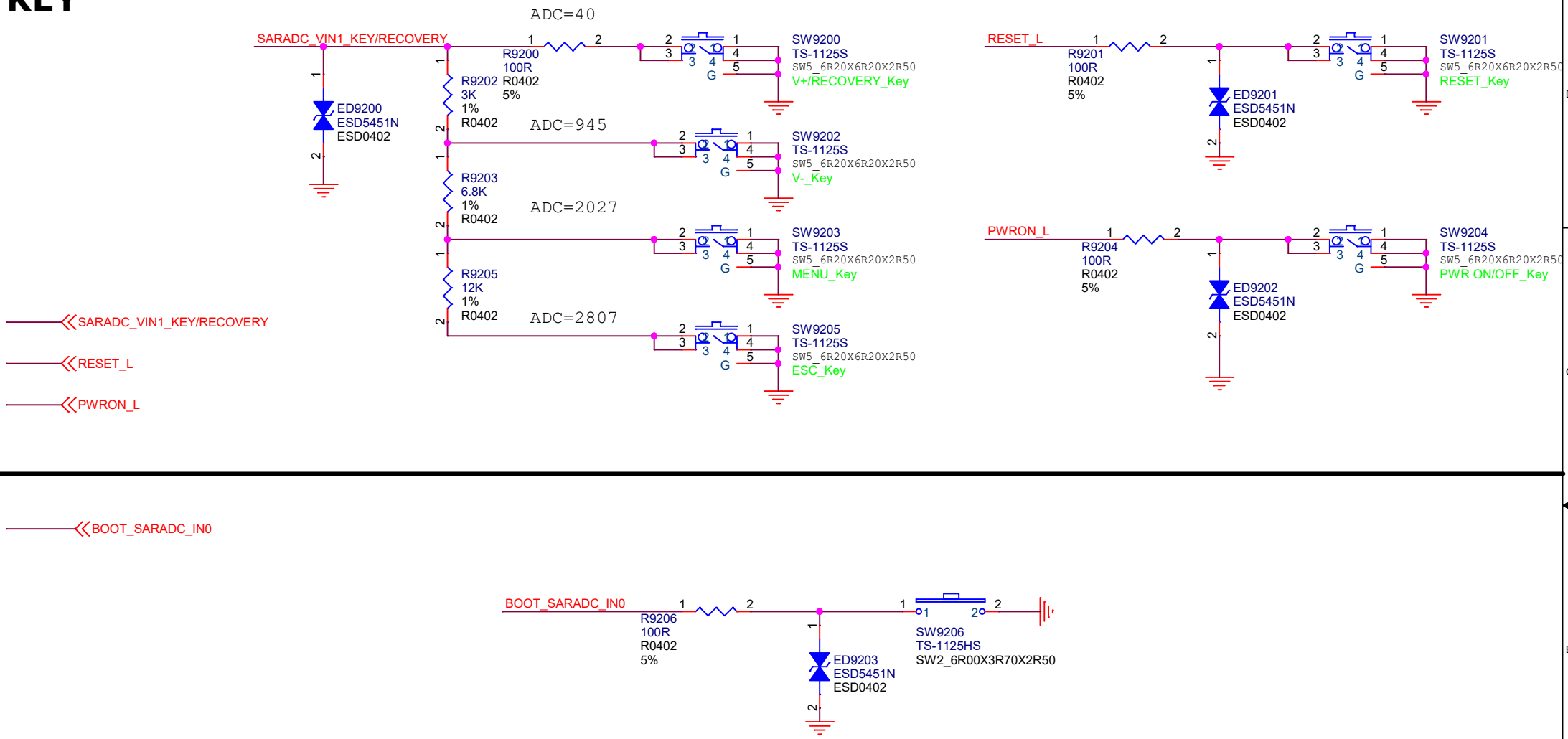
KEY



Note:

If BOOT_SARADC_IN0=0V after power-on reset, then system will enter into Maskrom mode.

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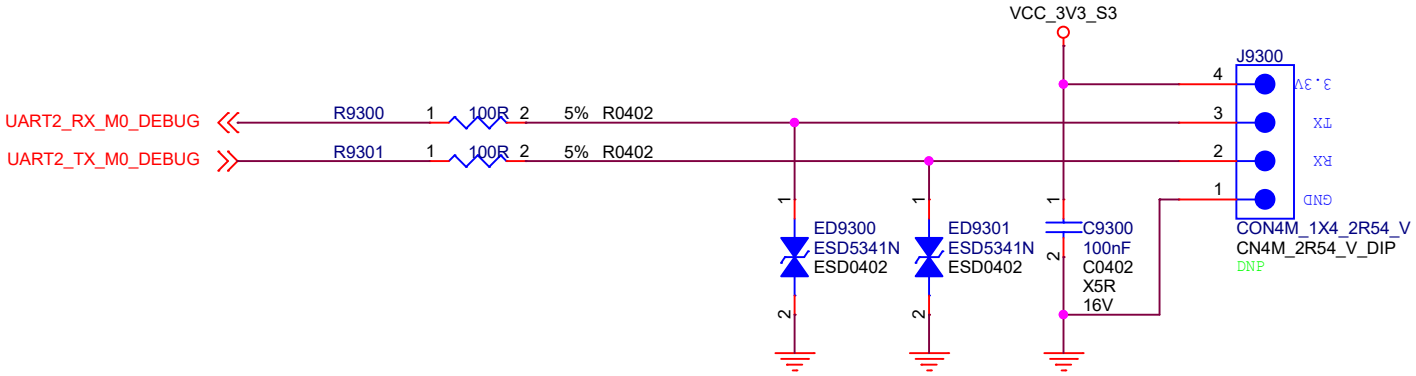
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	92.KEY Array				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	92 of 99

UART TO USB(DEBUG)



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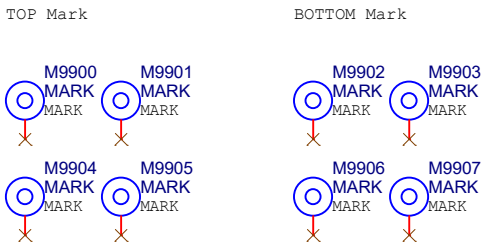
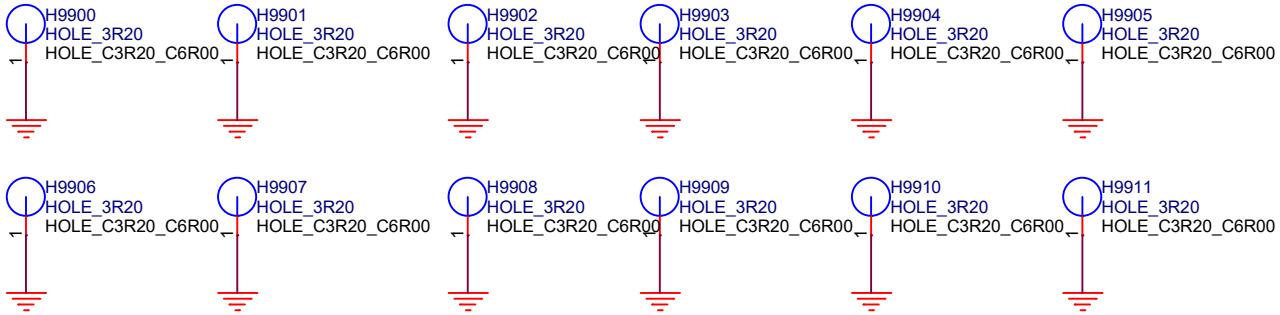
Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	93.Debug UART				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	93 of 99

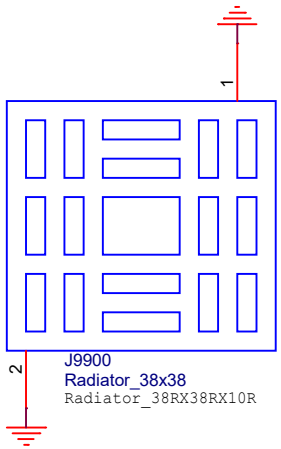
Mark



HOLE



HEATSINK



FAN:8CMX8CM

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Rockchip Electronics Co., Ltd					
Project:	RK3588_AIOT_SCH				
File:	99.Mark/Hole/Heatsink				
Date:	Thursday, December 30, 2021			Rev:	V1.0
Designed by:	RZF	Reviewed by:		Sheet:	99 of 99