ESP8089

Datasheet

Version 2.0

About This Guide

This document provides an introduction to the specifications of ESP8089.

This guide is structured as follows:

Chapter	Title	Content
Chapter 1	Introduction	Introduction to the block diagram, technology review and features of ESP8089.
Chapter 2	Schematics	Display of ESP8089 schematics.
Chapter 3	Ultra Low Power Technology	Introduction to the ESP8089's ultra low power technology and high degree of integration.
Chapter 4	ESP8089 Applications	Listing of the applications of ESP8089.
Chapter 5	Specifications	Introduction to ESP8089 's power consumption and RF specifications.
Chapter 6	CPU, Memory and Interfaces	Introduction to ESP8089's CPU, memory and interfaces.
Chapter 7	Firmware	Introduction to ESP8089's firmware.
Chapter 8	Power Management	Introduction to five power states of ESP8089.
Chapter 9	Clock Management	Introduction to ESP8089's high frequency clock and external reference requirements.
Chapter 10	Radio	Introduction to the main blocks of ESP8089 radio.
Chapter 11	Bluetooth Co-Existence	Introduction to ESP8089's bluetooth coexistence.
Appendix	QFN32 Package Information	Provision of QFN32 package Information.

Release Notes

Date	Version	Release Notes
2014.12	V1.0	First Release.
2016.08	V2.0	Updated editing.

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1. Introduction

1.1. ESP8089 Block Diagram

The ESP platform of high performance wireless SoCs provides an unsurpassed ability for mobile platform designers to embed Wi-Fi capabilities within other systems, at the lowest cost with the greatest functionality.

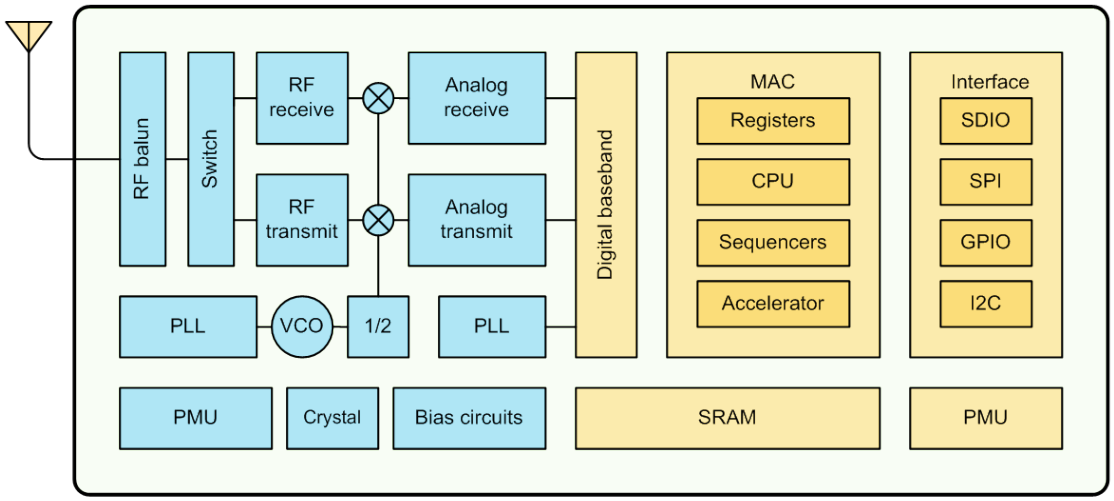


Figure 1-1. ESP8089 Block Diagram

1.2. Technology Review

The ESP8089 offers a complete and self-contained Wi-Fi networking solution, allowing it to either host the application or to off-load all Wi-Fi networking functions from another application processor.

When ESP8089 hosts the application, it is usually the only application processor in the device, with the user's applications stored in an internal/external Flash.

Alternately, serving as a Wi-Fi adapter, wireless internet access can be added to any microcontroller-based design with simple connectivity through the SPI/SDIO interface or the CPU AHB bridge interface.

ESP8089 allows direct connection to cellular baseband and application processors via SDIO/SPI or memory-mapped parallel interfaces. Its on-board processing and storage capabilities allow it to integrate with the host platform with minimal development upfront and minimal loading during runtime. With its high degree of on-chip integration, which includes the antenna switch balun and power management converters, it requires minimal external circuitry. The entire solution, including front-end module, occupies minimal PCB area.

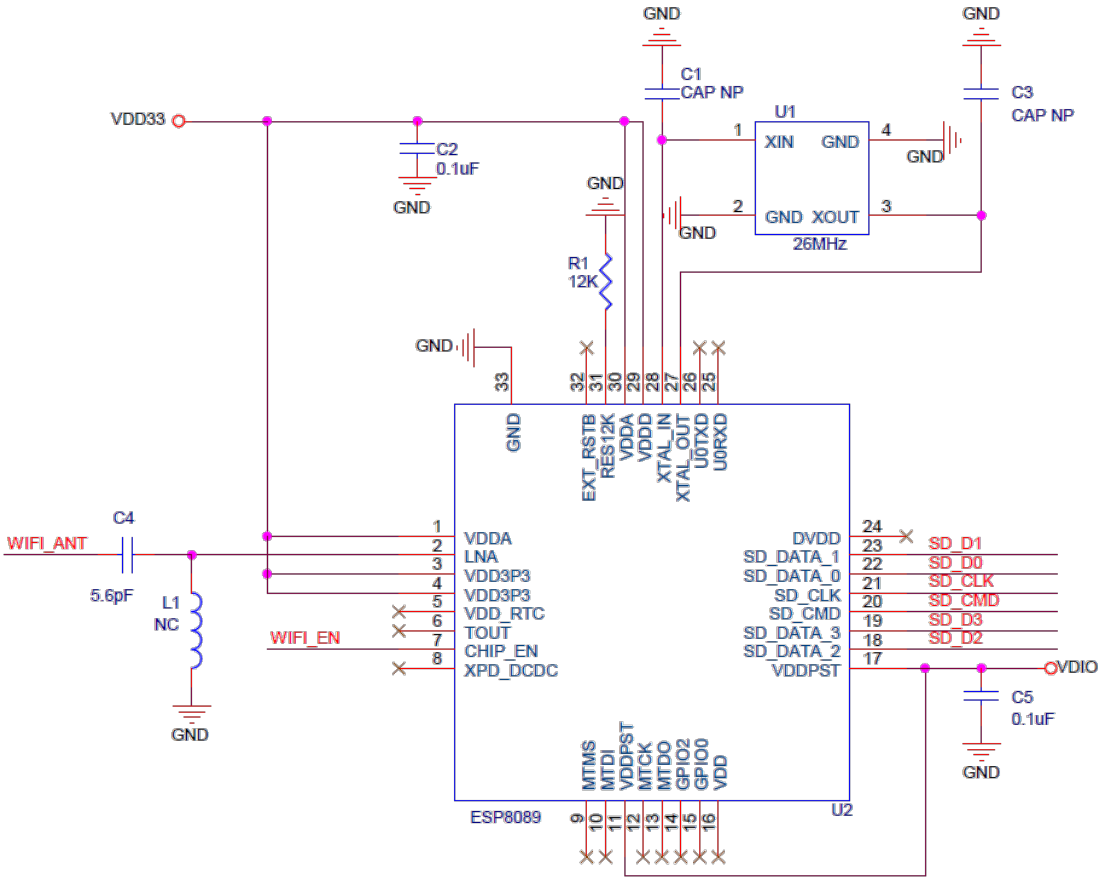
Sophisticated system-level features include:

- fast sleep/wake context switching for energy-efficient VoIP,
- adaptive radio biasing for low-power operation,
- advanced signal processing, and
- spur cancellation and radio co-existence features for cellular/Bluetooth/802.11 interference mitigation.

1.3. Features

- 802.11 b/g/n
- Wi-Fi Direct (P2P), Miracast, SoftAP
- Integrated TR switch, balun, LNA, power amplifier and matching network
- Integrated PLL, regulators, and power management units
- +19 dBm output power in 802.11 b mode
- Power down leakage current of < 10 µA
- Integrated low power 32-bit CPU could be used as application processor
- SDIO 2.0, SPI, UART
- STBC, 1×1 MIMO, 2×1 MIMO
- A-MPDU & A-MSDU aggregation & 0.4 µs guard interval
- Wake up and transmit packets in < 22 ms
- Standby power consumption of < 1.0 mW (DTIM3)

2. Schematics



3. Ultra Low Power Technology

ESP8089 is designed to achieve the lowest power consumption with a combination of several proprietary techniques. The power-saving architecture operates in two modes: active mode and sleep mode.

By using advance power management techniques and logic to power-down unrequited functions and to control switching between sleep and active modes, ESP8089 consumes less than 12 μA in sleep mode and less than 1.0 mW (DTIM=3), or less than 0.5 mW (DTIM=10) to stay connected.

In sleep mode, only the calibrated real-time clock and watchdog timer remain active. The real-time clock can be programmed to wake up ESP8089 at any required interval.

ESP8089 can be programmed to wake up when a specified condition is detected. This minimal wake-up time feature applies to mobile device SoCs, allowing them to remain in the low-power standby mode until Wi-Fi is needed.

3.1. Highest Level of Integration

By integrating the most important components such as power management unit, TR switch, RF balun, high power PA capable of delivering +23 dBm (peak), ESP8089 ensures that the BOM cost is the lowest possible, and the ease of integration into any system.

With ESP8089, the only external BOM are resistors, capacitors, and crystal. For cellphone compatibility an SAW filter may be required.

4. ESP8089 Applications

- Cellphone
- Portable Media Player (PMP) such as MP3 or MP4 players
- Mobile gaming devices
- Digital Cameras
- Camcorder
- Tablet computers

5. Specifications

5.1. Current Consumption

The following current consumption is based on 3.3V supply, and 25°C ambient temperature, using internal regulators.

1. Measurements are done at antenna port without SAW filter.
2. All the Tx measurements are based on 99% of duty cycle, in continuous Tx mode.

Table 5-1. Current Consumption

Mode	Min	Typical	Max	Unit
Transmit 802.11 b, DSSS 1 Mbps, POUT=+19.5 dBm	-	215	-	mA
Transmit 802.11 b, CCK 11 Mbps, POUT=+18.5 dBm	-	197	-	mA
Transmit 802.11 g, OFDM 54 Mbps, POUT =+16 dBm	-	145	-	mA
Transmit 802.11 n, MCS 7, POUT=+14 dBm	-	135	-	mA
Receive 802.11 b, packet length=1024 byte, -80 dBm	-	60	-	mA
Receive 802.11 g, packet length=1024 byte, -70 dBm	-	60	-	mA
Receive 802.11 n, packet length=1024 byte, -65 dBm	-	62	-	mA
Standby	-	0.9	-	mA
Deep sleep	-	10	-	µA
Power save mode DTIM 1	-	1.2	-	mA
Power save mode DTIM 3	-	0.86	-	mA
Total shutdown	-	0.5	-	µA

5.2. RF Specifications

The following data are gathered under room temperature conditions with 3.3V and 1.1V power supplies:

Table 5-2. RF Specifications

Description	Min	Typical	Max	Unit
Input frequency	2412	-	2484	MHz
Input impedance	-	50	-	Ω
Input reflection	-	-	-10	dB
Output power of PA for 72.2 Mbps	14	15	16	dBm
Output power of PA for 11b mode	17.5	18.5	19.5	dBm

Description	Min	Typical	Max	Unit
Sensitivity				
DSSS, 1 Mbps	-	-98	-	dBm
CCK, 11 Mbps	-	-91	-	dBm
6Mbps (1/2 BPSK)	-	-93	-	dBm
54Mbps (3/4 64-QAM)	-	-75	-	dBm
HT20, MCS 7 (65 Mbps, 72.2 Mbps)	-	-71	-	dBm
Adjacent channel rejection				
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS 0	-	37	-	dB
HT20, MCS 7	-	20	-	dB
Time				
Crystal power up time	-	500	-	µs
Baseband PLL power up time	-	100	-	µs
RF PLL power up time	-	200	-	µs
Rx RF power up time	-	2	-	µs
Tx RF power up time	-	2	-	µs

6. CPU, Memory and Interfaces

6.1. CPU

This chip has an ultra low power Micro 32-bit CPU embedded, with 16-bit thumb mode. This CPU can be interfaced using:

- code RAM/ROM interface (iBus) that goes to the memory controller, which can also be used to access external Flash memory,
- data RAM interface (dBus) that also goes to the memory controller,
- AHB interface, for register access, and
- JTAG interface for debugging.

6.2. Memory Controller

The memory controller contains ROM, and SRAM. The CPU can access it via the iBus, dBus and AHB interface. Any of these interfaces can request access to the ROM or RAM modules, and the memory controller arbiters serve these 3 interfaces on a first-come-first-serve basis.

6.3. AHB and AHB Blocks

The AHB blocks perform the function of an arbiter, control the AHB interfaces from the MAC, SDIO (host) and CPU. Depending on the address, the AHB data-requests can go into one of the two slaves:

- APB block, or
- Flash controller (usually for stand-alone applications).

Data requests to the memory controller are usually high-speed requests, and requests to the APB block are usually register access.

The APB block acts as a decoder. It can only access programmable registers within ESP8089's main blocks. Depending on the address, the APB request can go to the radio, SI/SPI, SDIO (host), GPIO, UART, real-time clock (RTC), MAC or digital baseband.

6.4. Interfaces

The ESP8089 contains several analog and digital interfaces described in the following sections.

6.4.1. SDIO Host Interface

The IO pins can be set in the following modes:

- 4-bit 25 MHz SDIO v1.1

- 4-bit 50 MHz SDIO v2.0

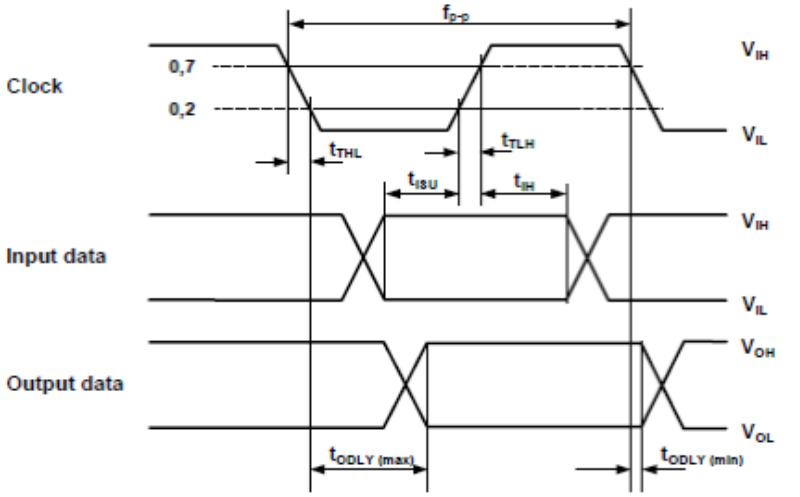


Figure 6-1. SDIO Timing Diagram

Table 6-1. SDIO Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Input setup time	t_{ISU}	6	-	ns
Input hold time	t_{IH}	2.5	-	ns
Clock fall time	t_{THL}	-	3	ns
Clock rise time	t_{TLH}	-	3	ns
Output delay time	t_{DLY}	2	12	ns
Clock frequency	f_{SDIO}	-	50	MHz

6.4.2. Master SI/SPI Control (Optional)

The master serial interface (SI) can operate in two, three or four-wire bus configurations to control the EEPROM or other I2C/SPI devices. Multiple I2C devices with different device addresses are supported by sharing the 2-wire bus.

Multiple SPI devices are supported by sharing the clock and data signals, using separate software-controlled GPIO pins as the chip selects.

The SPI can be used to control external devices such as serial Flash memories, audio CODECs, or other slave devices. It is set up as a standard master SPI device with 3 different enable pins:

- SPI_EN0
- SPI_EN1
- SPI_EN2

Both SPI master and SPI slave are supported, with the latter being used as a host interface.

In an embedded application, SPI_EN0 is used as an enable signal to an external serial Flash memory for downloading a patch code and/or MIB-data to the baseband. In a host-based application, patch code and MIB-data can alternately be downloaded via the host interface. This pin is active-low and should be left open if not used.

SPI_EN1 is usually used for a user application, e.g. to control an external audio codec or sensor ADC, in an embedded application. This pin is active-low and should be left open if not used.

SPI_EN2 usually controls an EEPROM to store individual data, such as MIB information, MAC address, and calibration data, or for general use. This pin is active-low and should be left open if not used.

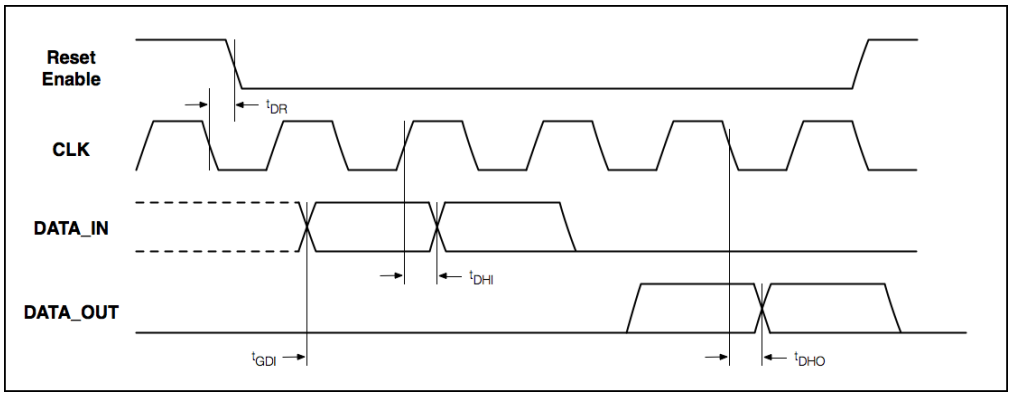


Figure 6-2. SPI Timing Characteristics

Table 6-2. SDIO Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Input setup time	t_{ISU}	11	-	ns
Input hold time	t_{IH}	0	-	ns
SPI clock frequency	f_{SPI}	-	10	MHz
Output delay time	T_{OD}	-	15	ns

6.4.3. General Purpose IO

There are up to 16 GPIO pins. They can be assigned to various functions by the firmware. Each GPIO can be configured with internal pull-up/down, input available for sampling by a software register, input triggering an edge or level CPU interrupt, input triggering a level wakeup interrupt, open-drain or push-pull output driver, or output source from a software register, or a sigma-delta PWM DAC.

These pins are multiplexed with other functions such as host interface, UART, SI, Bluetooth co-existence, etc.

6.4.4. Real Time Clock IO (EXT_LFC)

If a 32.768 kHz LFC clock is available, it can be connected to EXT_LFC. If no clock is available on this pin, the internal LFC will be used. If an EXT_LFC is available, the selection of LFC source, internal LFC or EXT_LFC can be done by a strapping pin.

6.4.5. Digital IO Pads

The digital IO pads are bidirectional, non-inverting and tri-state. It includes input and an output buffer with tri-state control inputs. Besides this, for low power operations, the IO can also be set to hold. For instance, when we power down the chip, all output enable signals can be set to hold low.

An optional hold functionality can be built into the IO if requested. When the IO is not driven by the internal or external circuitry, the hold functionality can be used to hold the state to the last used state.

The hold functionality introduces some positive feedback into the pad. Hence, the external driver that drives the pad must be stronger than the positive feedback. The required drive strength, however, is small – in the range of 5 µA.

Table 6-3. Digital IO Pads

Parameter	Symbol	Min	Max	Unit
Input low voltage	V_{IL}	-0.3	$0.25 \times V_{IO}$	V
Input high voltage	V_{IH}	$0.75 \times V_{IO}$	3.3	V
Input leakage current	I_{IL}	-	50	nA
Output low voltage	V_{OL}	-	$0.1 \times V_{IO}$	V
Output high voltage	V_{OH}	$0.8 \times V_{IO}$	-	V
Input pin capacitance	C_{pad}	-	2	pF
VDDIO	V_{IO}	1.8	3.3	V
Maximum drive capability	I_{MAX}	-	12	mA
Temperature	T_{amb}	-40	125	°C

All digital IO pins are protected from over-voltage with a snap-back circuit connected between the pad and the ground. The snap back voltage is typically about 6V, and the holding voltage is 5.8V. This provides protection from over-voltages and ESD. The output devices are also protected from reversed voltages with diodes.

7. Firmware

The firmware is executed in on-chip ROM and SRAM, which loads the instructions during wake-up, through the SDIO interface, from the host.

The firmware implements the full 802.11 b/g/n/e/i WLAN MAC protocol and Wi-Fi Direct specification. It supports not only basic service set (BSS) operations under the distributed control function (DCF) but also P2P group operation compliant with the latest Wi-Fi P2P protocol. Low level protocol functions such as

- RTS/CTS,
- acknowledgement,
- fragmentation and defragmentation,
- aggregation,
- frame encapsulation (802.11 h/RFC 1042),
- automatic beacon monitoring/scanning, and
- P2P Wi-Fi Direct

are handled by ESP8089 without host intervention.

Passive or active scanning, as well as P2P discovery procedure is performed autonomously, once initiated by a host command. Power management is handled with minimum host interaction to minimize active duty period.

7.1. Features

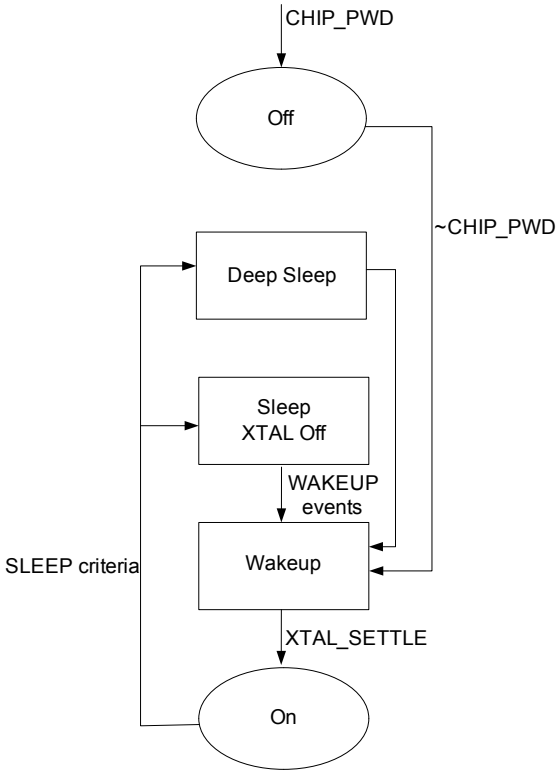
The firmware includes the following:

- 802.11 b/g/n/d/e/i/k/r support
- Wi-Fi Direct (P2P) support
  - P2P Discovery
  - P2P Group Owner Mode
  - P2P Power Management
- Infrastructure BSS Station mode/P2P mode/SoftAP mode support;
- Hardware accelerators for
  - CCMP (CBC-MAC, counter mode)
  - TKIP (MIC, RC4)
  - WAPI (SMS4)
  - WEP (RC4)
  - CRC
- Support for WPA/WPA2 PSK, and WPS;

- Additional 802.11 i security features:
  - Pre-authentication, and
  - TSN
- Open Interface for various upper layer authentication schemes over EAP such as:
  - TLS
  - PEAP
  - LEAP
  - SIM
  - AKA, or
  - Customer specific
- 802.11 n support (2.4 GHz/5 GHz);
- Supports MIMO 1×1 and 2×1, STBC, A-MPDU and A-MSDU aggregation and 0.4 μs guard interval;
- WMM power save U-APSD;
- QoS Multiple queue management to fully utilize traffic prioritization defined by 802.11 e standard;
- UMA compliant and certified;
- 802.1h/RFC1042 frame encapsulation;
- Scattered DMA for optimal CPU off-load on Zero Copy data transfer operations;
- Antenna diversity and selection (software-managed hardware);
- Clock/power-gating combined with 802.11-compliant power management, dynamically adapted to current connection condition to achieve minimal power consumption;
- Adaptive rate fallback algorithm sets the optimum transmission rate and Tx power based on actual SNR and packet loss information;
- Automatic retransmission and response on MAC to avoid packet discarding on slow host environment;
- Seamless roaming support;
- Configurable packet traffic arbitration (PTA) combined with dedicated slave processor-based design, providing flexible and exact timing BT co-existence support for a wide range of Bluetooth Chip vendors;
- Dual and single antenna BT co-existence support with optional, simultaneously-receiving Wi-Fi/BT capability.

8. Power Management

The chip can be put into the following states:



- OFF: CHIP_PD pin is low. The RTC is disabled. All registers are cleared.
- DEEP_SLEEP: Only RTC is powered on – the rest of the chip is powered off. Recovery memory of RTC can keep basic Wi-Fi connecting information.
- SLEEP: Only the RTC is operating. The crystal oscillator is disabled. Any wake-up events (MAC, host, RTC timer, external interrupts) will put the chip into the WAKE-UP state.
- WAKE-UP: In this state, the system goes from the sleep states to the PWR state. The crystal oscillator and PLLs are enabled.
- ON state: the high speed clock is operational and sent to each block enabled by the clock control register. Lower-level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction, while the system is on.

9. Clock Management

9.1. High Frequency Clock

The high frequency clock on ESP8089 is used to drive both the Tx and Rx mixers. This clock is generated from the internal crystal oscillator and an external crystal. The crystal frequency can range from 26 MHz to 52 MHz.

While internal calibration of the crystal oscillator ensures that a wide range of crystals can be used, in general, the quality of the crystal is still a factor to consider, in order to obtain reasonable phase noise and Wi-Fi sensitivity. When the crystal used is not optimal due to a frequency offset or quality problem, the maximum data processing ability and sensitivity will decrease.Please refer to the following table for measurement of frequency offset.

Table 9-1. High Frequency Clock

Parameter	Symbol	Min	Max	Unit
Frequency	F_{XO}	26	52	MHz
Loading capacitance	C_L	-	32	pF
Motional capacitance	C_M	2	5	pF
Series resistance	R_S	0	65	Ω
Frequency tolerance	ΔF_{XO}	-15	15	ppm
Frequency vs. temperature (-25°C ~ 75°C)	$\Delta F_{XO,\ Temp}$	-15	15	ppm

9.2. External Reference Requirements

For an externally-generated clock, the frequency can range from 26 MHz to 52 MHz. For good radio performance, the clock should possess the following characteristics:

Table 9-2. External Reference Requirements

Parameter	Symbol	Min	Max	Unit
Clock amplitude	V_{XO}	0.2	1	Vpp
External clock accuracy	$\Delta F_{XO,EXT}$	-15	15	ppm
Phase noise @1 kHz offset, 40 MHz clock	-	-	-120	dBc/Hz
Phase noise @10 kHz offset, 40 MHz clock	-	-	-130	dBc/Hz
Phase noise @100 kHz offset, 40 MHz clock	-	-	-138	dBc/Hz

10. Radio

The ESP8089 radio consists of the following main blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- High-speed clock generators and crystal oscillator
- Real-time clock
- Bias and regulators
- Power management

10.1. Channel Frequencies

The RF transceiver supports the following channels according to the IEEE 802.11 b/g/n standards.

Table 10-1. Channel Frequencies

Channel No.	Frequency (MHz)	Channel No.	Frequency (MHz)
1	2412	8	2447
2	2417	9	2452
3	2422	10	2457
4	2427	11	2462
5	2432	12	2467
6	2437	13	2472
7	2442	14	2484

10.2. 2.4 GHz Receiver

The 2.4 GHz receiver downconverts the RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution high-speed ADCs. To adapt to varying signal channel conditions, RF filters, automatically-gained control, DC offset cancelation circuits and baseband filters are integrated into the radio.

10.3. 2.4 GHz Transmitter

The 2.4 GHz transmitter upconverts the quadrature baseband signals to 2.4 GHz, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling a state of art performance of delivering +20.5 dBm average power for 802.11 b transmission and +16 dBm for 802.11 n transmission.

Additional calibrations are integrated, in order to cancel any imperfections of the radio such as:

- carrier leakage,
- I/Q phase matching, and
- baseband nonlinearities

This reduces the amount of time and test equipment required for production testing.

10.4. Clock Generator

The clock generator produces quadrature 2.4 GHz clock signals for the receiver and transmitter. All components of the clock generator are integrated on-chip, including:

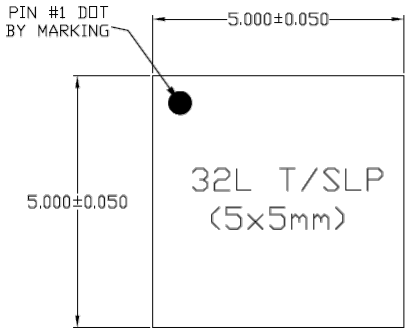
- inductor,
- varactor, and
- loop filter.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms to ensure the best receiver and transmitter performance.

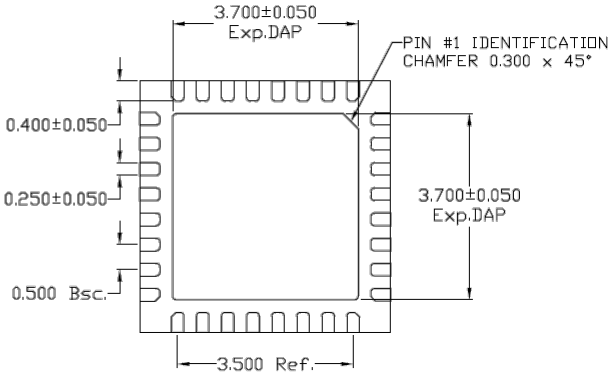
11. Bluetooth Co-Existence

ESP8089 features pre-assigned pins for BT/Wi-Fi co-existence and BT clock-request. These pins act as the interface to a BT system to facilitate traffic arbitration between the two systems. The control system is in firmware and supports various standards or proprietary co-existence protocols.

I. Appendix - QFN32 Package Information



TOP VIEW

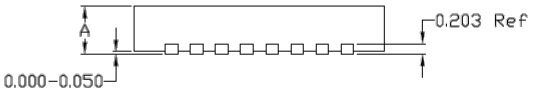


BOTTOM VIEW

NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800



SIDE VIEW

Espressif IOT Team

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